FAIRCHILD SEMICONDUCTOR™

October 1987
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MM74C901 • MM74C902
Hex Inverting TTL Buffer • Hex Non-Inverting TTL Buffer

General Description

The MM74C901 and MM74C902 hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, and high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply.

Features

- Wide supply voltage range: 3.0V to 15V
- Guaranteed noise margin: 1.0V
- High noise immunity: 0.45 V_{CC} (typ.)
- TTL compatibility: Fan out of 2 driving standard TTL

Ordering Code:

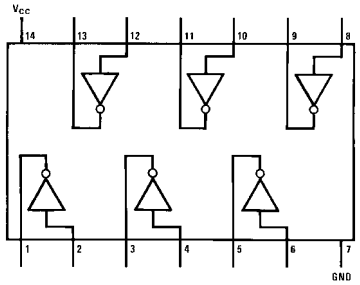
Order Number	Package Number	Package Description
MM74C901M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74C901N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.300" Wide
MM74C902M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74C902N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-011, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

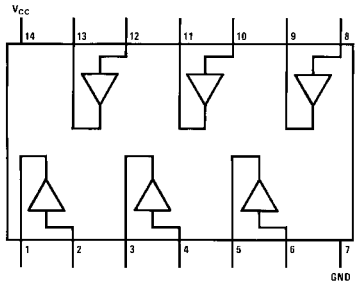
Pin Assignments for DIP and SOIC

MM74C901



Top View

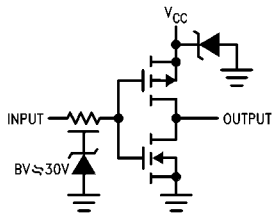
MM74C902



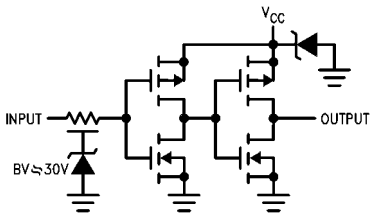
Top View

Logic Diagrams

MM74C901
CMOS to TTL Inverting Buffer



MM74C902
CMOS to TTL Buffer



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Voltage at Any Input Pin	
MM74C901	−0.3V to +15V
MM74C902	−0.3V to +15V
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating Temperature Range (T_A)	
MM74C901, MM74C902,	−40°C to +85°C
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10 µA	4.5			V
		V_{CC} = 10V, I_O = −10 µA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V			0.5	V
		V_{CC} = 10V			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	µA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		µA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	15	µA
TTL TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
CMOS TO TTL						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM74C901	V_{CC} = 4.75V	4.25			V
	MM74C902	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM74C901	V_{CC} = 4.75V			1.0	V
	MM74C902	V_{CC} = 4.75V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −800 µA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM74C901	V_{CC} = 4.75V, I_O = 2.6 mA			0.4	V
	MM74C902	V_{CC} = 4.75V, I_O = 3.2 mA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (Short Circuit Current)						
(MM74C901)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0V, V_{OUT} = 0V	−5.0			mA
	(P-Channel)	T_A = 25°C, V_{IN} = 0V				
I_{SOURCE}	Output Source Current	V_{CC} = 10V, V_{OUT} = 0V	−20			mA
	(P-Channel)	T_A = 25°C, V_{IN} = 0V				
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, V_{OUT} = V_{CC}	9.0			mA
	(N-Channel)	T_A = 25°C, V_{IN} = V_{CC}				
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, V_{OUT} = 0.4V	3.8			mA
	(N-Channel)	T_A = 25°C, V_{IN} = V_{CC}				
(MM74C902)						

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	–5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	–20			mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C, V_{IN} = 0V	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = 0.4V T_A = 25°C, V_{IN} = 0V	3.8			mA

AC Electrical Characteristics (Note 2)

T_A = 25°C, C_L = 50 pF, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM74C901						
t_{pd1}	Propagation Delay Time to a Logical "1"	V_{CC} = 5.0V		38	70	ns
		V_{CC} = 10V		22	30	ns
t_{pd0}	Propagation Delay Time to a Logical "0"	V_{CC} = 5.0V		21	35	ns
		V_{CC} = 10V		13	20	ns
C_{IN}	Input Capacitance	Any Input (Note 3)		14		pF
C_{PD}	Power Dissipation Capacity	Per Buffer (Note 4)		30		pF
MM74C902						
t_{pd1}	Propagation Delay Time to a Logical "1"	V_{CC} = 5.0V		57	90	ns
		V_{CC} = 10V		27	40	ns
t_{pd0}	Propagation Delay Time to a Logical "0"	V_{CC} = 5.0V		54	90	ns
		V_{CC} = 10V		25	40	ns
C_{IN}	Input Capacitance	Any Input (Note 3)		5.0		pF
C_{PD}	Power Dissipation Capacity	Per Buffer (Note 4)		50		pF

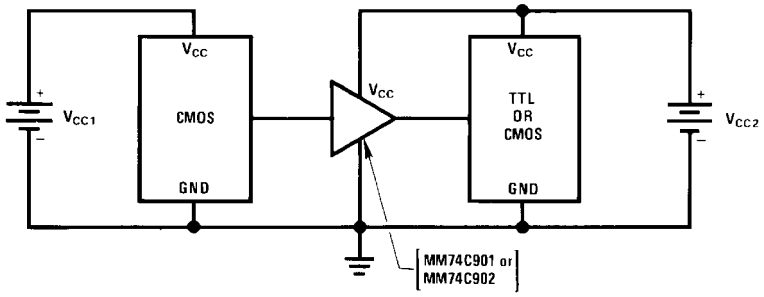
Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note AN-90.

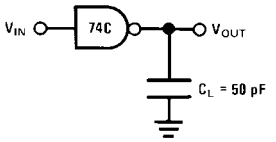
Typical Application

CMOS to TTL or CMOS at a Lower V_{CC}



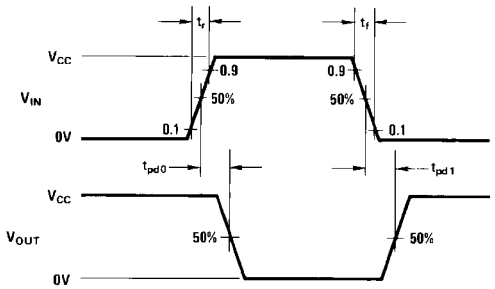
Note: V_{CC1} = V_{CC2}

AC Test Circuit and Switching Time Waveforms



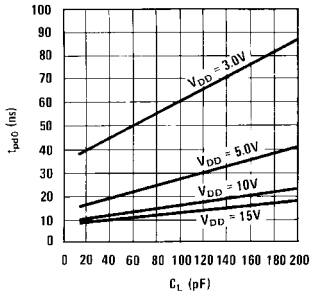
Note: Delays measured with input t_r, t_f = 20 ns.

CMOS to CMOS

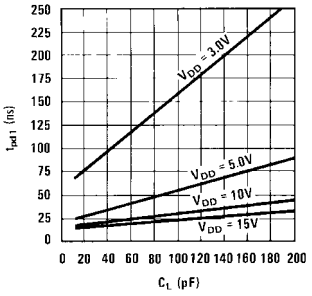


Typical Performance Characteristics

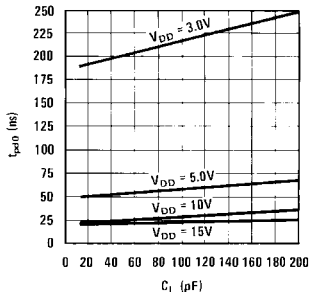
Typical Propagation Delay to a Logical "0" for the MM74C901



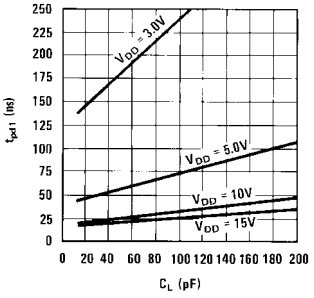
Typical Propagation Delay to a Logical "1" for the MM74C901



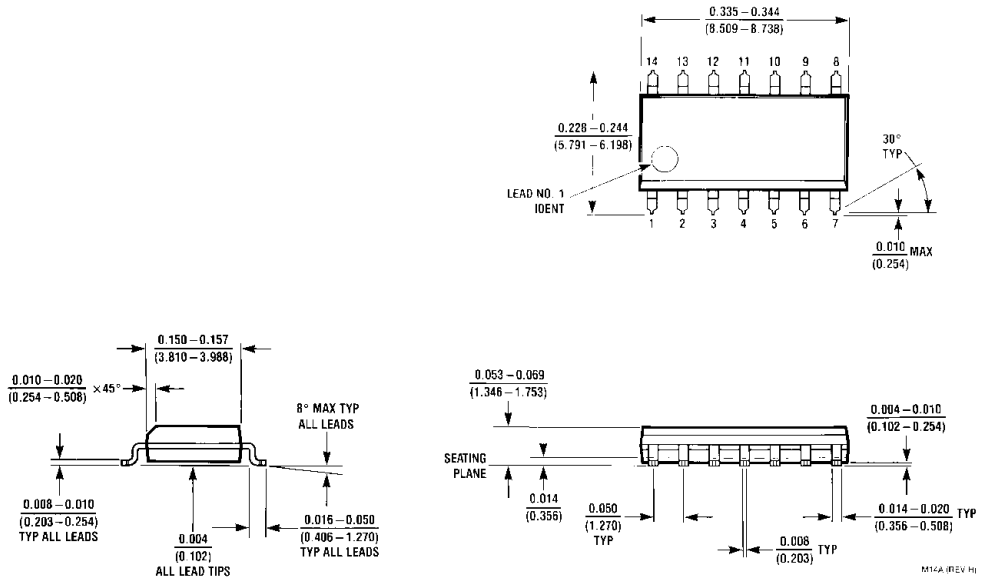
Typical Propagation Delay to a Logical "0" for the MM74C902



Typical Propagation Delay to a Logical "1" for the MM74C902

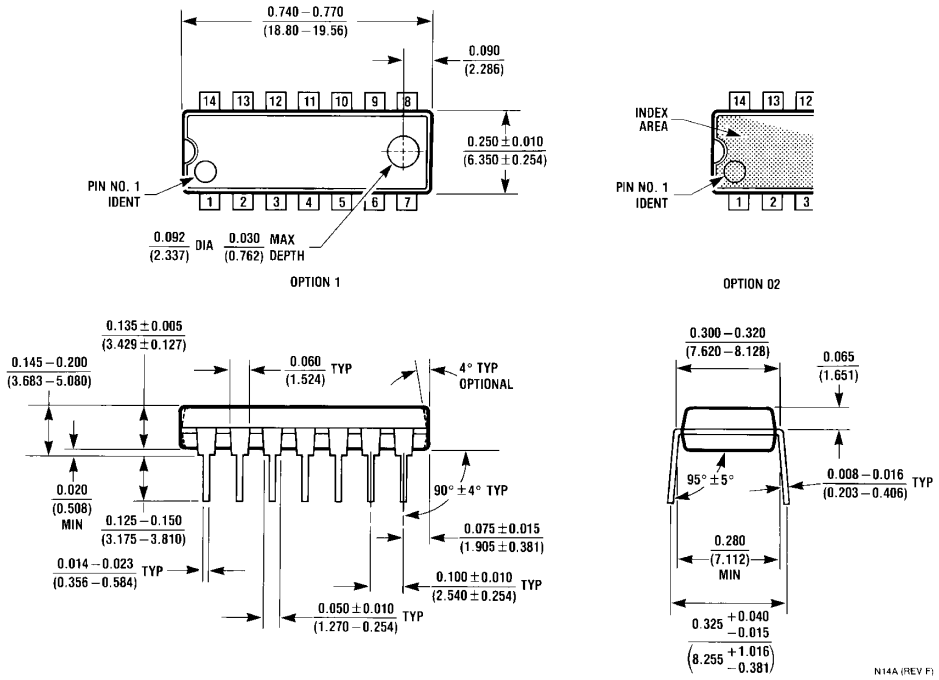


Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-120, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A

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