

# 74LVT640

3.3 V Octal transceiver with direction pin; inverting; 3-state

Rev. 4 — 23 February 2021

Product data sheet

## 1. General description

The 74LVT640 is an 8-bit inverting transceiver with 3-state outputs. The device features an output enable ( $\overline{OE}$ ) and send/receive (DIR) for direction control. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

## 2. Features and benefits

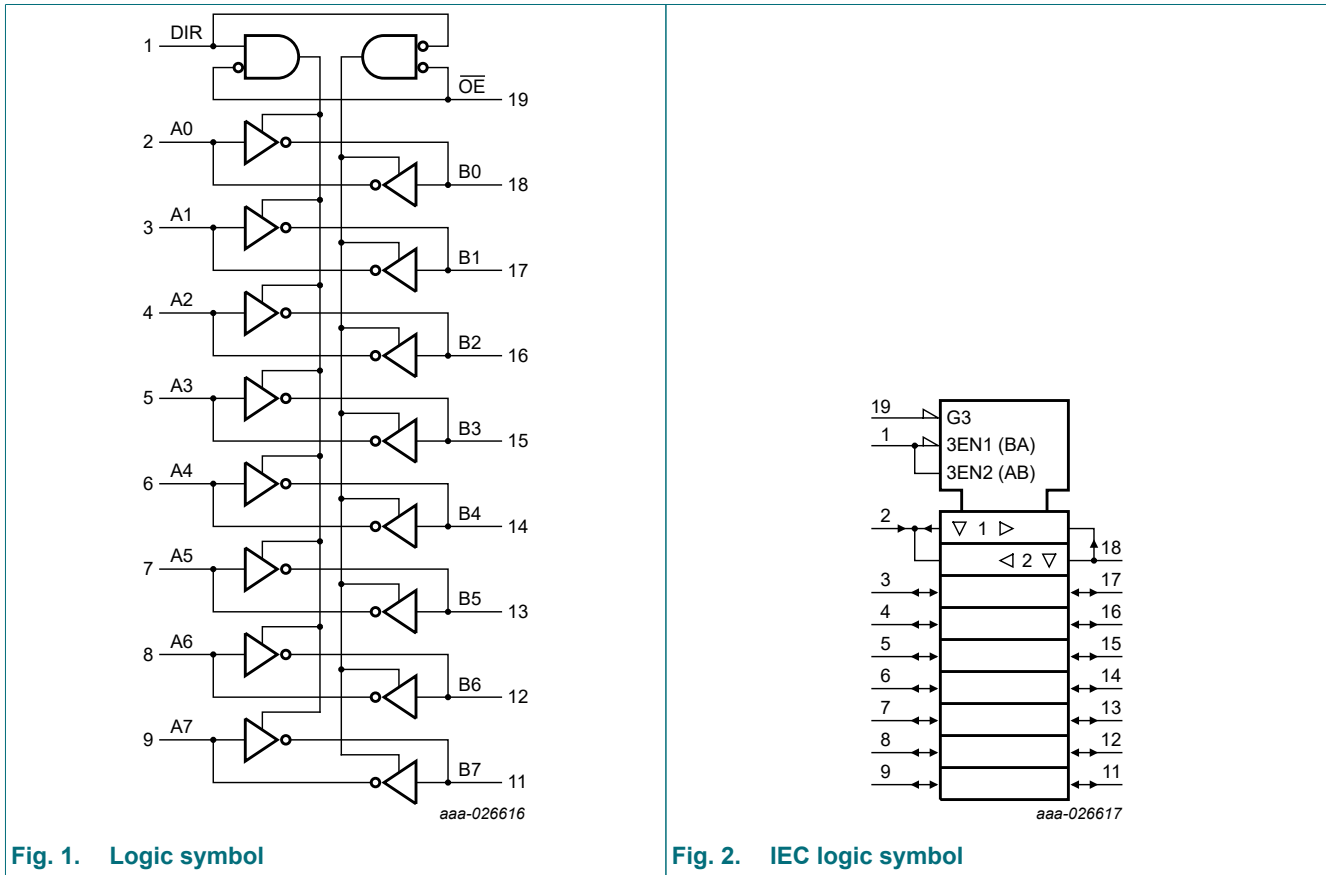
- 3-state buffers
- Wide supply voltage range from 2.7 to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Octal bidirectional bus interface
- Input and output interface capability to systems at 5 V supply
- Output capability: +64 mA and -32 mA
- Bus-hold data inputs eliminate the need for external pull-up resistors for unused inputs
- Live insertion/extraction permitted
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

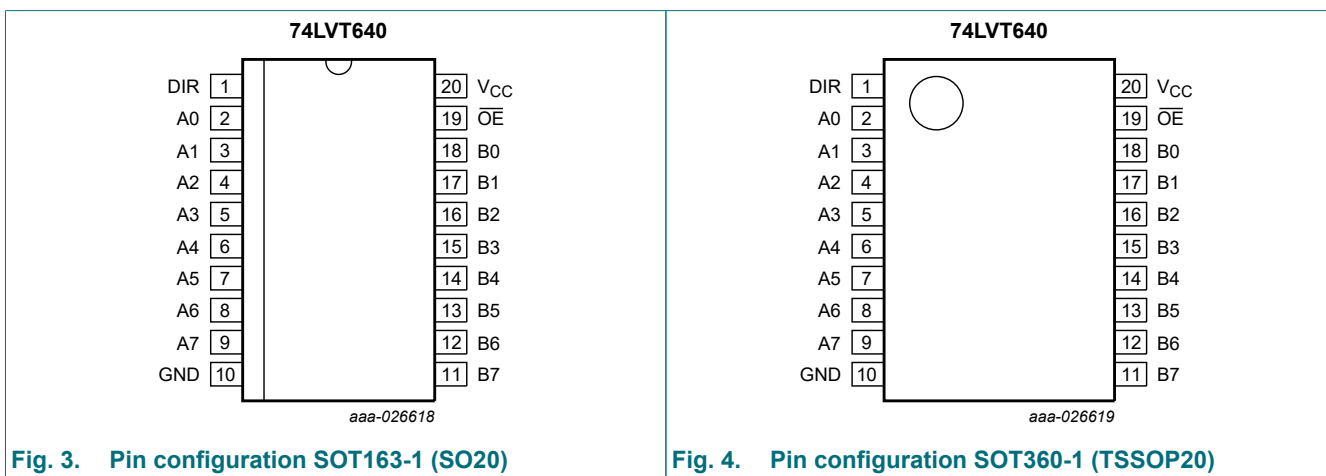
| Type number | Package           |         |   | Version  |
|-------------|-------------------|---------|---|----------|
|             | Temperature range | Name    | Description   |          |
| 74LVT640D   | -40 °C to +85 °C  | SO20    | plastic small outline package; 20 leads;<br>body width 7.5 mm             | SOT163-1 |
| 74LVT640PW  | -40 °C to +85 °C  | TSSOP20 | plastic thin shrink small outline package; 20 leads;<br>body width 4.4 mm | SOT360-1 |

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

| Symbol                         | Pin                            | Description                      |
|--------------------------------|--------------------------------|----------------------------------|
| DIR                            | 1                              | direction control input          |
| A0, A1, A2, A3, A4, A5, A6, A7 | 2, 3, 4, 5, 6, 7, 8, 9         | data inputs/outputs              |
| GND                            | 10                             | ground (0 V)                     |
| B0, B1, B2, B3, B4, B5, B6, B7 | 18, 17, 16, 15, 14, 13, 12, 11 | data inputs/outputs              |
| $\overline{OE}$                | 19                             | output enable input (active LOW) |
| $V_{CC}$                       | 20                             | supply voltage                   |

## 6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance OFF-state.

| Inputs          |     | Inputs/outputs  |        |
|-----------------|-----|-----------------|--------|
| $\overline{OE}$ | DIR | An              | Bn     |
| L               | L   | $\overline{Bn}$ | inputs |
| L               | H   | inputs          | An     |
| H               | X   | Z               | Z      |

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol    | Parameter               | Conditions                                 | Min      | Max  | Unit |
|-----------|-------------------------|--|----------|------|------|
| $V_{CC}$  | supply voltage          |  | -0.5     | +4.6 | V    |
| $V_I$     | input voltage           |  | [1] -0.5 | +7.0 | V    |
| $V_O$     | output voltage          | output in OFF or HIGH state                | [1] -0.5 | +7.0 | V    |
| $I_{IK}$  | input clamping current  | $V_I < 0$                                  | -50      | -    | mA   |
| $I_{OK}$  | output clamping current | $V_O < 0$                                  | -50      | -    | mA   |
| $I_O$     | output current          | output in LOW state                        | -        | 128  | mA   |
|           |                         | output in HIGH state                       | -64      | -    | mA   |
| $T_{stg}$ | storage temperature     |  | -65      | +150 | °C   |
| $T_j$     | junction temperature    |  | [2] -    | 150  | °C   |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40\text{ °C to }+85\text{ °C}$ | -        | 500  | mW   |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol              | Parameter                           | Conditions  | Min | Max | Unit               |
|---------------------|-------------------------------------|---|-----|-----|--------------------|
| $V_{CC}$            | supply voltage                      |   | 2.7 | 3.6 | V                  |
| $V_I$               | input voltage                       |   | 0   | 5.5 | V                  |
| $I_{OH}$            | HIGH-level output current           |   | -   | -32 | mA                 |
| $I_{OL}$            | LOW-level output current            |   | -   | 32  | mA                 |
|                     |                                     | current duty cycle $\leq 50\%$ ; $f_i \geq 1$ kHz | -   | 64  | mA                 |
| $T_{amb}$           | ambient temperature                 | in free air                                       | -40 | +85 | $^{\circ}\text{C}$ |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled                                   | -   | 10  | ns/V               |

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol         | Parameter                          | Conditions  | -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$ |                |               | Unit          |
|----------------|------------------------------------|---|--|----------------|---------------|---------------|
|                |                                    |   | Min  | Typ [1]        | Max           |               |
| $V_{IK}$       | input clamping voltage             | $V_{CC} = 2.7$ V; $I_{IK} = -18$ mA   | -1.2   | -0.9           | -             | V             |
| $V_{IH}$       | HIGH-level input voltage           |   | 2.0  | -              | -             | V             |
| $V_{IL}$       | LOW-level input voltage            |   | -  | -              | 0.8           | V             |
| $V_{OH}$       | HIGH-level output voltage          | $V_{CC} = 2.7$ V to 3.6 V; $I_{OH} = -100$ $\mu\text{A}$  | $V_{CC} - 0.2$                                   | $V_{CC} - 0.1$ | -             | V             |
|                |                                    | $V_{CC} = 2.7$ V; $I_{OH} = -8$ mA  | 2.4  | 2.5            | -             | V             |
|                |                                    | $V_{CC} = 3.0$ V; $I_{OH} = -32$ mA   | 2.0  | 2.2            | -             | V             |
| $V_{OL}$       | LOW-level output voltage           | $V_{CC} = 2.7$ V; $I_{OL} = 100$ $\mu\text{A}$  | -  | 0.1            | 0.2           | V             |
|                |                                    | $V_{CC} = 2.7$ V; $I_{OL} = 24$ mA  | -  | 0.3            | 0.5           | V             |
|                |                                    | $V_{CC} = 3.0$ V; $I_{OL} = 16$ mA  | -  | 0.25           | 0.4           | V             |
|                |                                    | $V_{CC} = 3.0$ V; $I_{OL} = 32$ mA  | -  | 0.3            | 0.5           | V             |
|                |                                    | $V_{CC} = 3.0$ V; $I_{OL} = 64$ mA  | -  | 0.4            | 0.55          | V             |
| $I_I$          | input leakage current              | control pins  |  |                |               |               |
|                |                                    | $V_{CC} = 0$ V or 3.6 V; $V_I = 5.5$ V  | -  | 1              | 10            | $\mu\text{A}$ |
|                |                                    | $V_{CC} = 3.6$ V; $V_I = V_{CC}$ or GND   | -  | $\pm 0.1$      | $\pm 1$       | $\mu\text{A}$ |
|                |                                    | I/O data pins [2]   |  |                |               |               |
|                |                                    | $V_{CC} = 3.6$ V; $V_I = 5.5$ V   | -  | 1              | 20            | $\mu\text{A}$ |
|                |                                    | $V_{CC} = 3.6$ V; $V_I = V_{CC}$  | -  | 0.1            | 1             | $\mu\text{A}$ |
|                | $V_{CC} = 3.6$ V; $V_I = 0$ V      | -5  | -1   | -              | $\mu\text{A}$ |               |
| $I_{OFF}$      | power-off leakage current          | $V_{CC} = 0$ V; $V_I$ or $V_O = 0$ V to 4.5 V   | -  | 1              | $\pm 100$     | $\mu\text{A}$ |
| $I_{CEX}$      | output high leakage current        | output in HIGH-state when $V_O > V_{CC}$ ;<br>$V_O = 5.5$ V; $V_{CC} = 3.0$ V   | -  | 60             | 125           | $\mu\text{A}$ |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} \leq 1.2$ V; $V_O = 0.5$ V to $V_{CC}$ ;<br>$V_I = \text{GND}$ or $V_{CC}$ ; $\overline{\text{OE}} = \text{don't care}$ [3] | -  | 15             | $\pm 100$     | $\mu\text{A}$ |
| $I_{BHL}$      | bus hold LOW current               | $V_{CC} = 3.0$ V; $V_I = 0.8$ V [4]   | 75   | 150            | -             | $\mu\text{A}$ |
| $I_{BHH}$      | bus hold HIGH current              | $V_{CC} = 3.0$ V; $V_I = 2.0$ V   | -75  | -150           | -             | $\mu\text{A}$ |
| $I_{BHLO}$     | bus hold LOW overdrive current     | $V_{CC} = 3.6$ V; $V_I = 0$ V to 3.6 V  | 500  | -              | -             | $\mu\text{A}$ |

## 3.3 V Octal transceiver with direction pin; inverting; 3-state

| Symbol          | Parameter                       | Conditions   | -40 °C to +85 °C |         |      | Unit          |
|-----------------|---------------------------------|--|------------------|---------|------|---------------|
|                 |                                 |  | Min              | Typ [1] | Max  |               |
| $I_{BHHO}$      | bus hold HIGH overdrive current | $V_{CC} = 3.6 \text{ V}$ ; $V_I = 0 \text{ V}$ to $3.6 \text{ V}$  | -                | -       | -500 | $\mu\text{A}$ |
| $I_{CC}$        | supply current                  | $V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$  |                  |         |      |               |
|                 |                                 | outputs HIGH   | -                | 0.13    | 0.19 | mA            |
|                 |                                 | outputs LOW  | -                | 3       | 12   | mA            |
| $\Delta I_{CC}$ | additional supply current       | per input pin; $V_{CC} = 3.0 \text{ V}$ to $3.6 \text{ V}$ ; one input = $V_{CC} - 0.6 \text{ V}$ ; other inputs = $V_{CC}$ or GND [5] | -                | 0.1     | 0.2  | mA            |
|                 |                                 | outputs disabled   | -                | 0.13    | 0.19 | mA            |
|                 |                                 |  | -                |         |      |               |
| $C_I$           | input capacitance               | DIR and $\overline{OE}$ inputs; $V_I = 0 \text{ V}$ or $3.0 \text{ V}$   | -                | 4       | -    | pF            |
| $C_{I/O}$       | input/output capacitance        | at input/output data pins, outputs disabled; $V_{I/O} = 0 \text{ V}$ or $3.0 \text{ V}$  | -                | 7       | -    | pF            |

[1] All typical values are measured at  $V_{CC} = 3.3 \text{ V}$  (unless stated otherwise) and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

[2] Unused pins at  $V_{CC}$  or GND.

[3] This parameter is valid for any  $V_{CC}$  between  $0 \text{ V}$  and  $1.2 \text{ V}$  with a transition time of up to  $10 \text{ ms}$ . From  $V_{CC} = 1.2 \text{ V}$  to  $V_{CC} = 3.0 \text{ V}$  to  $3.6 \text{ V}$  a transition time of  $100 \text{ ms}$  is permitted. This parameter is valid for  $T_{amb} = +25 \text{ }^\circ\text{C}$  only.

[4] This is the bus hold overdrive current required to force the input to the opposite logic state.

[5] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 10. Dynamic characteristics

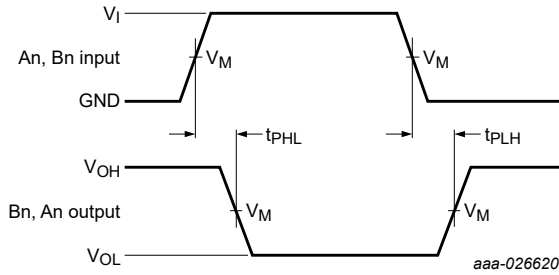
**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

| Symbol    | Parameter                           | Conditions                                 | -40 °C to +85 °C |         |     | Unit |
|-----------|-------------------------------------|--|------------------|---------|-----|------|
|           |                                     |  | Min              | Typ [1] | Max |      |
| $t_{PLH}$ | LOW to HIGH propagation delay       | An to Bn or Bn to An; see Fig. 5           |                  |         |     |      |
|           |                                     | $V_{CC} = 2.7 \text{ V}$                   | -                | -       | 4.5 | ns   |
|           |                                     | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.0              | 2.3     | 3.7 | ns   |
| $t_{PHL}$ | HIGH to LOW propagation delay       | An to Bn or Bn to An, see Fig. 5           |                  |         |     |      |
|           |                                     | $V_{CC} = 2.7 \text{ V}$                   | -                | -       | 3.1 | ns   |
|           |                                     | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.0              | 2.4     | 3.3 | ns   |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | $\overline{OE}$ to An or Bn; see Fig. 6    |                  |         |     |      |
|           |                                     | $V_{CC} = 2.7 \text{ V}$                   | -                | -       | 6.9 | ns   |
|           |                                     | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.1              | 3.5     | 5.3 | ns   |
| $t_{PZL}$ | OFF-state to LOW propagation delay  | $\overline{OE}$ to An or Bn; see Fig. 6    |                  |         |     |      |
|           |                                     | $V_{CC} = 2.7 \text{ V}$                   | -                | -       | 6.2 | ns   |
|           |                                     | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 1.5              | 3.6     | 5.3 | ns   |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | $\overline{OE}$ to An or Bn; see Fig. 6    |                  |         |     |      |
|           |                                     | $V_{CC} = 2.7 \text{ V}$                   | -                | -       | 5.6 | ns   |
|           |                                     | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 2.2              | 3.7     | 5.0 | ns   |
| $t_{PLZ}$ | LOW to OFF-state propagation delay  | $\overline{OE}$ to An or Bn; see Fig. 6    |                  |         |     |      |
|           |                                     | $V_{CC} = 2.7 \text{ V}$                   | -                | -       | 4.5 | ns   |
|           |                                     | $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | 2.0              | 3.1     | 4.5 | ns   |

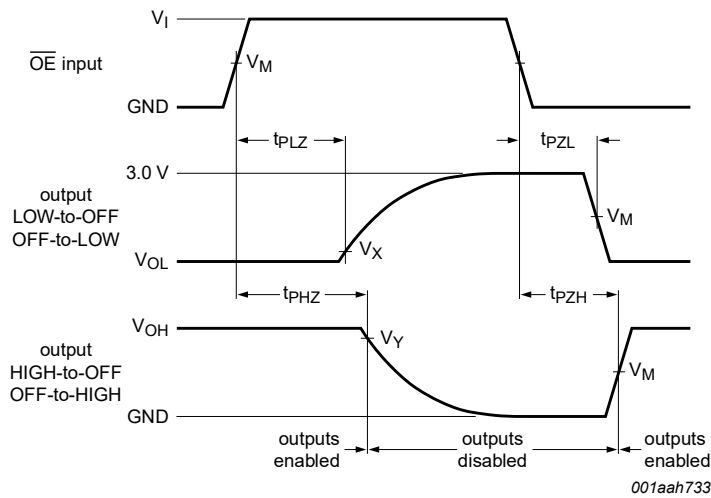
[1] Typical values are measured at  $T_{amb} = 25 \text{ }^\circ\text{C}$  and  $V_{CC} = 3.3 \text{ V}$

10.1. Waveforms and test circuit



See Table 8 for measurement points.  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 5. Input (An, Bn) to output ( $\overline{Bn}$ ,  $\overline{An}$ ) propagation delays



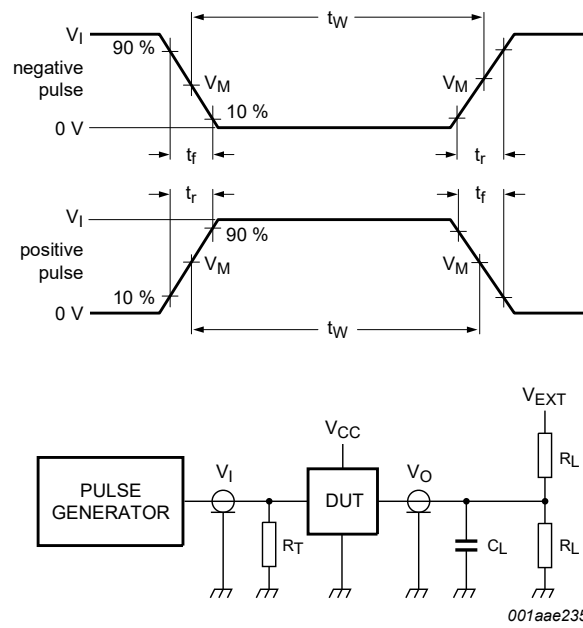
See Table 8 for measurement points.  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 6. 3-state output enable and disable times

Table 8. Measurement points

| Input        |       | Output |                  |                  |
|--------------|-------|--------|------------------|------------------|
| $V_I$        | $V_M$ | $V_M$  | $V_x$            | $V_y$            |
| GND to 2.7 V | 1.5 V | 1.5 V  | $V_{OL} + 0.3 V$ | $V_{OH} - 0.3 V$ |

3.3 V Octal transceiver with direction pin; inverting; 3-state



Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

Fig. 7. Test circuit for switching times

Table 9. Test data

| Input |               |        |               | Load         |       | $V_{EXT}$          |                    |                    |
|-------|---------------|--------|---------------|--------------|-------|--------------------|--------------------|--------------------|
| $V_I$ | $f_i$         | $t_w$  | $t_r, t_f$    | $R_L$        | $C_L$ | $t_{PHZ}, t_{PZH}$ | $t_{PLZ}, t_{PZL}$ | $t_{PLH}, t_{PHL}$ |
| 2.7 V | $\leq 10$ MHz | 500 ns | $\leq 2.5$ ns | 500 $\Omega$ | 50 pF | GND                | 6 V                | open               |

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

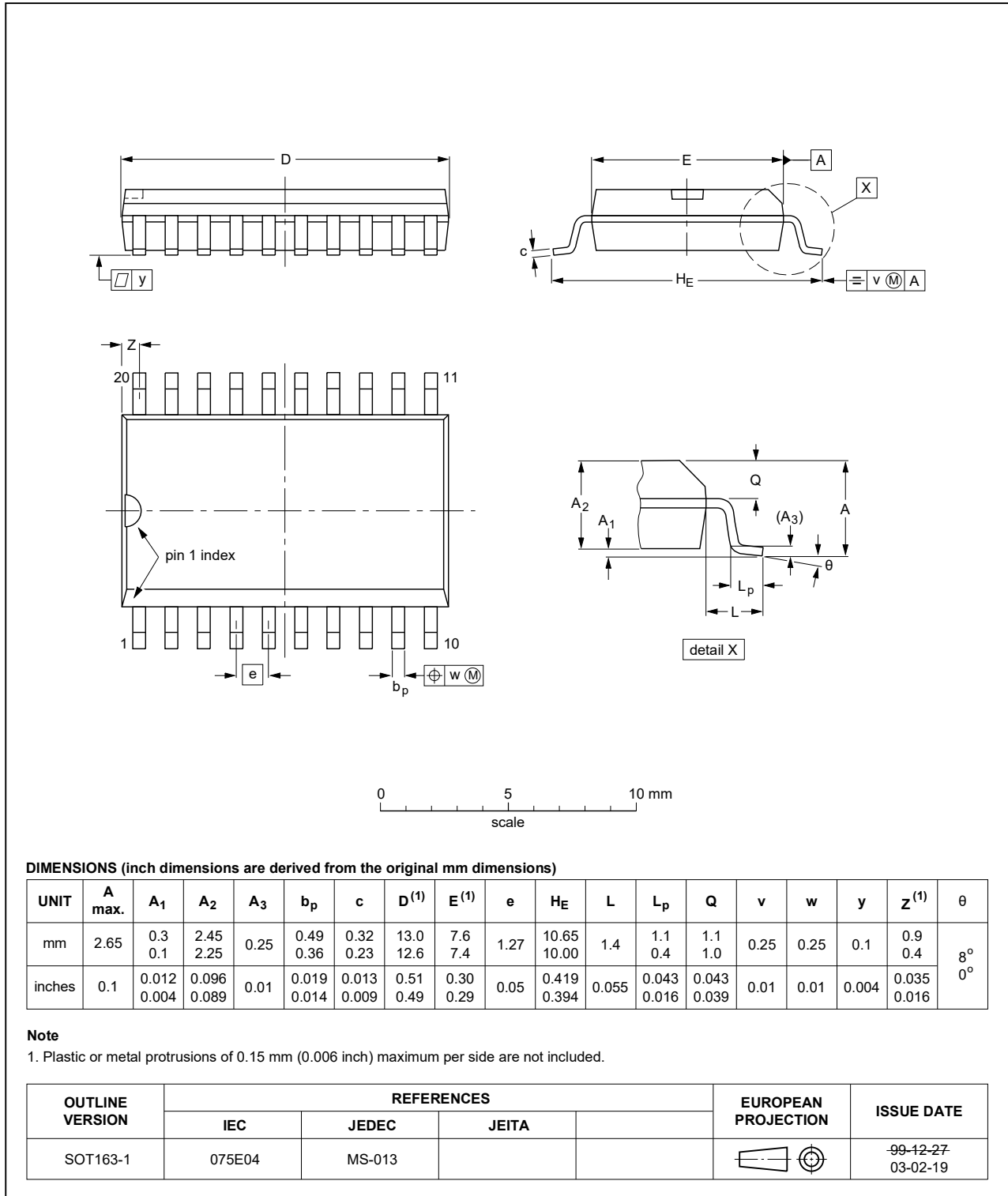


Fig. 8. Package outline SOT163-1 (SO20)



TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

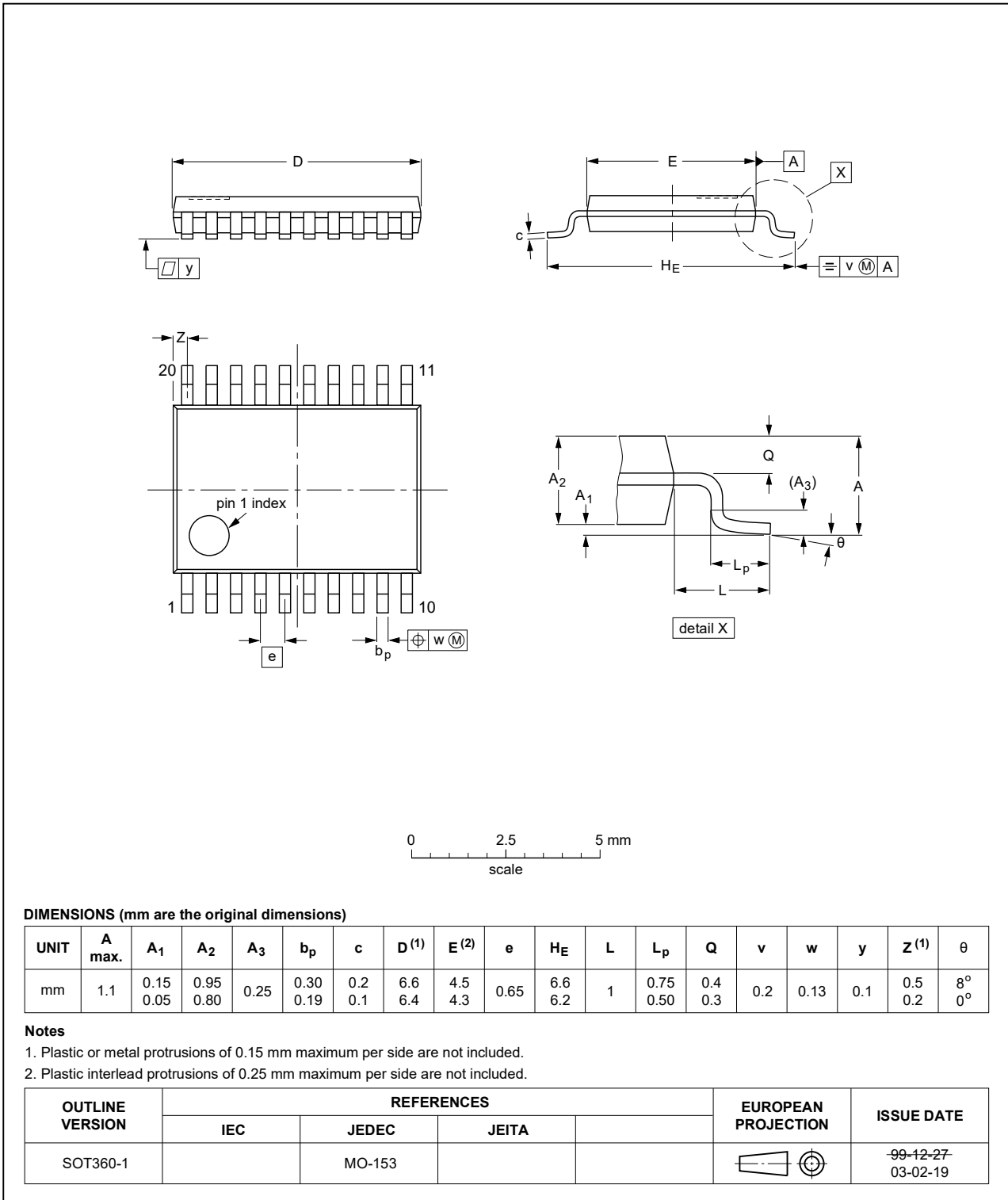


Fig. 9. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

Table 10. Abbreviations

| Acronym | Description                                     |
|---------|---|
| BiCMOS  | Bipolar Complementary Metal Oxide Semiconductor |
| DUT     | Device Under Test                               |
| ESD     | ElectroStatic Discharge                         |
| MIL     | Military  |
| MM      | Machine Model                                   |
| TTL     | Transistor-Transistor Logic                     |

## 13. Revision history

Table 11. Revision history

| Document ID    | Release date  | Data sheet status     | Change notice | Supersedes   |
|----------------|---|-----------------------|---------------|--------------|
| 74LVT640 v.4   | 20210223  | Product data sheet    | -             | 74LVT640 v.3 |
| Modifications: | <ul style="list-style-type: none"> <li>Type number 74LVT640DB (SOT339-1 / SSOP20) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>   |                       |               |              |
| 74LVT640 v.3   | 20170410  | Product data sheet    | -             | 74LVT640 v.2 |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul> |                       |               |              |
| 74LVT640 v.2   | 19980219  | Product specification | -             | 74LVT640 v.1 |
| 74LVT640 v.1   | 19961001  | Product specification | -             | -            |

## 14. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Date of release: 23 February 2021

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