SFP Controller for Dual Rx Interface

General Description

The DS1877 controls and monitors all functions for SFF, SFP, and SFP+ modules including all SFF-8472 functionality. The device supports all LOS functions for two receivers, and continually monitors for LOS of either channel. Four ADC channels monitor V_{CC}, temperature, and two differential external monitor inputs that can be used to meet all monitoring requirements. Two digital-to-analog converter (DAC) outputs with temperature-indexed lookup tables (LUTs) are available for additional monitoring and control functionality.

Applications

SFF, SFP, and SFP+ Transceiver Modules

Dual Rx Video SFPs

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS1877T+	-40°C to +95°C	28 TQFN-EP*
DS1877T+T&R	-40°C to +95°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
*EP = Exposed pad.

Features

♦ **Meets All SFF-8472 Control and Monitoring Requirements**

♦ **Four Analog Monitor Channels: Temperature, V_{CC}, RSSI1, RSSI2**
 RSSI1 and RSSI2 Support Internal and External Calibration
 Differential Input
 Common-Mode Range from GND to V_{CC}
 Scalable Dynamic Range
 Internal Direct-to-Digital Temperature Sensor
 Alarm and Warning Flags for All Monitored Channels

♦ **Two 10-Bit Delta-Sigma Outputs**
 Each Controlled by 72-Entry Temperature LUT

♦ **Digital I/O Pins: Four Inputs, Four Outputs**

♦ **Comprehensive Loss-of-Signal (LOS) Detection System**

♦ **Flexible, Two-Level Password Scheme Provides Three Levels of Security**

♦ **120 Bytes of Password-1 Protected Memory**

♦ **128 Bytes of Password-2 Protected Memory in Main Device Address**

♦ **256 Additional Bytes Located at A0h Slave Address**

♦ **Receiver 1 is Accessed at A2h Slave Address**

♦ **Receiver 2 is Accessed at B2h Slave Address**

♦ **I^2C-Compatible Interface**

♦ **+2.85V to +3.9V Operating Voltage Range**

♦ **-40°C to +95°C Operating Temperature Range**

♦ **28-Pin TQFN (5mm x 5mm x 0.75mm) Package**

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

Voltage Range on RSSI1_, RSSI2_, INX, LOS1,
and LOS2 Pins Relative to Ground...... -0.5V to (V_{CC} + 0.5V)*
Voltage Range on V_{CC}, SDA, SCL, OUTX, FAULT,
RSELOUT, and LOSOUT Pins Relative to Ground....-0.5V to +6V
Continuous Power Dissipation
28-Pin TQFN (derate 34.5mW/°C) above +70°C....2758.6mW

Operating Temperature Range .... -40°C to +95°C
Programming Temperature Range .... 0°C to +95°C
Storage Temperature Range........................... -55°C to +125°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

*Subject to not exceeding +6V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Supply Voltage	V_{CC}	(Note 1)	+2.85		+3.9	V
High-Level Input Voltage (SDA, SCL)	$V_{IH:1}$		$0.7 \times V_{CC}$		$V_{CC} + 0.3$	V
Low-Level Input Voltage (SDA, SCL)	$V_{IL:1}$		-0.3		$0.3 \times V_{CC}$	V
High-Level Input Voltage (FAULT, RSEL, INX, LOS1, LOS2)	$V_{IH:2}$		2.0		$V_{CC} + 0.3$	V
Low-Level Input Voltage (FAULT, RSEL, INX, LOS1, LOS2)	$V_{IL:2}$		-0.3		+0.8	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	(Notes 1, 2)		2.5	10	mA
Output Leakage (SDA, OUTX, RSELOUT, LOSOUT, FAULT)	I_{LO}				1	µA
Low-Level Output Voltage (SDA, OUTX, RSELOUT, LOSOUT, DAC1, DAC2, FAULT)	V_{OL}	I_{OL} = 4mA			0.4	V
		I_{OL} = 6mA			0.6	
High-Level Output Voltage (DAC1, DAC2)	V_{OH}	I_{OH} = 4mA	$V_{CC} - 0.4$			V
DAC1 and DAC2 Before LUT Recall				10	100	nA
Input Leakage Current (SCL, RSEL, INX, LOS1, LOS2)	I_{LI}				1	µA
Digital Power-On Reset	POD		1.0		2.2	V
Analog Power-On Reset	POA		2.0		2.75	V

DAC1, DAC2 ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Main Oscillator Frequency	f_{OSC}			5		MHz
Delta-Sigma Input-Clock Frequency	f_{DS}			$f_{OSC}/2$		MHz
Reference Voltage Input (REFIN)	V_{REFIN}	Minimum 0.1µF to GND	2		V_{CC}	V
Output Range			0		V_{REFIN}	V
Output Resolution		See the *Delta-Sigma Outputs* section for details			10	Bits
Output Impedance	R_{DS}			35	100	Ω

ANALOG VOLTAGE MONITORING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution				13		Bits
Input/Supply Accuracy (RSSI1_, RSSI2_, V_{CC})	ACC	At factory setting		0.25	0.5	%FS
Update Rate for Temperature, RSSI1_, RSSI2_, V_{CC}	t_{RR}			45	75	ms
Input/Supply Offset (RSSI1_, RSSI2_, V_{CC})	V_{OS}	(Note 3)		0	5	LSB
Factory Setting (Note 4)		RSSI1/RSSI2 coarse		2.5		V
		V_{CC}		6.5536		
		RSSI1/RSSI2 fine		312.5		µV

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fault Reset Time (to FAULT = 0)	t_{INITR}	From ↑ V_{CC} > VCC LO alarm (Note 5)		161		ms
LOSOUT Assert Time	t_{LOSS_ON}	LOS_ LO (Note 6)		25.6		µs
LOSOUT Deassert Time	t_{LOSS_OFF}	LOS_ HI (Note 7)		25.6		µs

ANALOG QUICK-TRIP CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RSSI Full-Scale Voltage				1.25		V
Input Resistance			35	50	65	kΩ
Resolution				8		Bits
Error		T_A = +25°C		±2		%FS
Integral Nonlinearity			-1		+1	LSB
Differential Nonlinearity			-1		+1	LSB
Temperature Drift			-2		+2	%FS
Offset			-5		+10	mV

QUICK-TRIP TIMING CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Enable Time Following POA	t_{INIT}	(Note 5)		20		ms
Sample Time per Quick-Trip Comparison	t_{REP}			12.8		µs

DIGITAL THERMOMETER CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermometer Error	T_{ERR}	-40°C to +95°C	-3		+3	°C

I2C AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, T_A = -40°C to +95°C, unless otherwise noted. Timing is referenced to $V_{IL(MAX)}$ and $V_{IH(MIN)}$.) (Figure 12)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	(Note 8)	0		400	kHz
Clock Pulse-Width Low	t_{LOW}		1.3			µs
Clock Pulse-Width High	t_{HIGH}		0.6			µs
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Hold Time	$t_{HD:STA}$		0.6			µs
START Setup Time	$t_{SU:STA}$		0.6			µs
Data Out Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data In Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals	t_R	(Note 9)	20 + 0.1C_B		300	ns
Fall Time of Both SDA and SCL Signals	t_F	(Note 9)	20 + 0.1C_B		300	ns
STOP Setup Time	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
EEPROM Write Time	t_{WR}	(Note 10)			20	ms

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NONVOLATILE MEMORY CHARACTERISTICS

(V_{CC} = +2.85V to +3.9V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Write Cycles		At +25°C	200,000			—
		At +85°C	50,000			

Note 1: All voltages are referenced to ground. Current into the IC is positive, and current out of the IC is negative.
Note 2: Inputs are at supply rail. Outputs are not loaded.
Note 3: This parameter is guaranteed by design.
Note 4: Full-scale is user programmable.
Note 5: A temperature conversion is completed and the DAC values are recalled from the LUTs and V_{CC} has been measured to be above the VCC LO alarm, if the VCC LO alarm is enabled.
Note 6: This specification is the time it takes from RSSI1_ and RSSI2_ voltage falling below the LLOS_ trip threshold to LOSOUT asserted high.
Note 7: This specification is the time it takes from RSSI1_ and RSSI2_ voltage rising above the HLOS_ trip threshold to LOSOUT asserted high.
Note 8: I2C interface timing shown is for fast-mode (400kHz) operation. This device is also backward compatible with I2C standard mode.
Note 9: C_B—Total capacitance of one bus line in pF.
Note 10: EEPROM write begins after a STOP condition occurs.

Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. SUPPLY VOLTAGE

SDA = SCL = V_{CC}
DACs AT 1FFh
+95°C
+25°C
-40°C

SUPPLY CURRENT (mA)
V_{CC} (V)

DS1877 toc01

SUPPLY CURRENT vs. TEMPERATURE

DAC POSITIONS = 1FFh
SDA = SCL = V_{CC}
V_{CC} = 3.9V
V_{CC} = 3.3V
V_{CC} = 2.85V

SUPPLY CURRENT (mA)
TEMPERATURE (°C)

DS1877 toc02

DAC1/DAC2 DNL

DAC1/DAC2 DNL (LSB)
DAC POSITION (DEC)

DS1877 toc03

DAC1/DAC2 INL

DAC1/DAC2 INL (LSB)
DAC POSITION (DEC)

DS1877 toc04

RSSI1/RSSI2 DNL

USING FACTORY-PROGRAMMED
FULL-SCALE VALUE OF 2.5V

RSSI1/RSSI2 DNL (LSB)
RSSI1/RSSI2 INPUT VOLTAGE (V)

DS1877 toc05

RSSI1/RSSI2 INL

USING FACTORY-PROGRAMMED
FULL-SCALE VALUE OF 2.5V

RSSI1/RSSI2 INL (LSB)
RSSI1/RSSI2 INPUT VOLTAGE (V)

DS1877 toc06

DS1877

SFP Controller for Dual Rx Interface

Pin Configuration

TOP VIEW

THIN QFN
(5mm × 5mm × 0.8mm)

*EXPOSED PAD.
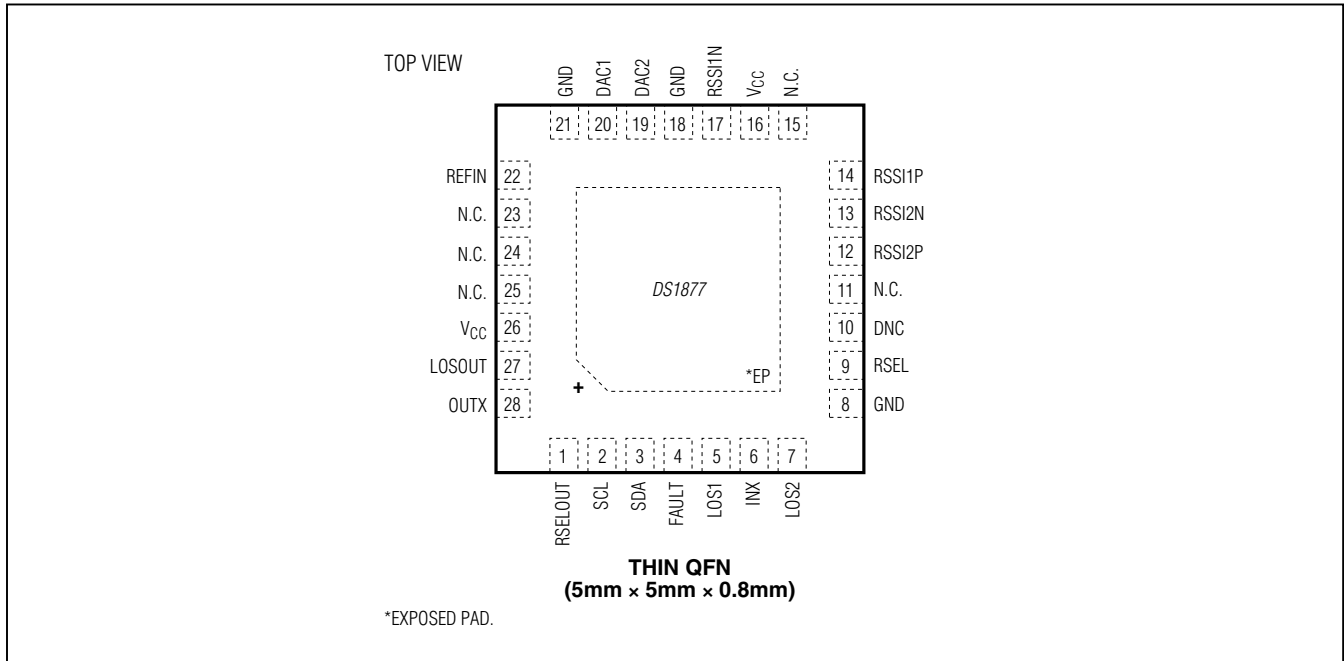
Pin Description

PIN	NAME	FUNCTION
1	RSELOUT	Rate-Select Output
2	SCL	I2C Serial-Clock Input
3	SDA	I2C Serial-Data Input/Output
4	FAULT	Transmit Fault Input and Output, Open Drain
5	LOS1	Loss-of-Signal Input 1
6	INX	Digital Input. General-purpose input, AS1 in SFF-8079, or RS1 in SFF-8431.
7	LOS2	Loss-of-Signal Input 2
8, 18, 21	GND	Ground Connection
9	RSEL	Rate-Select Input
10	DNC	Do Not Connect
11, 15, 23, 24, 25	N.C.	No Connection. Not internally connected.

PIN	NAME	FUNCTION
12, 13	RSSI2P, RSSI2N	Differential External Monitor Input 2 and LOS2 LO Quick Trip
14, 17	RSSI1P, RSSI1N	Differential External Monitor Input 1 and LOS1 LO Quick Trip
16, 26	V$_{CC}$	Power-Supply Input
19	DAC2	DAC2, Delta-Sigma Output
20	DAC1	DAC1, Delta-Sigma Output
22	REFIN	Reference Input for DAC1 and DAC2
27	LOSOUT	Receive Loss-of-Signal Output
28	OUTX	Digital Output. General-purpose output, AS1 output in SFF-8079, or RS1 output in SFF-8431.
—	EP	Exposed Pad (Connect to GND)
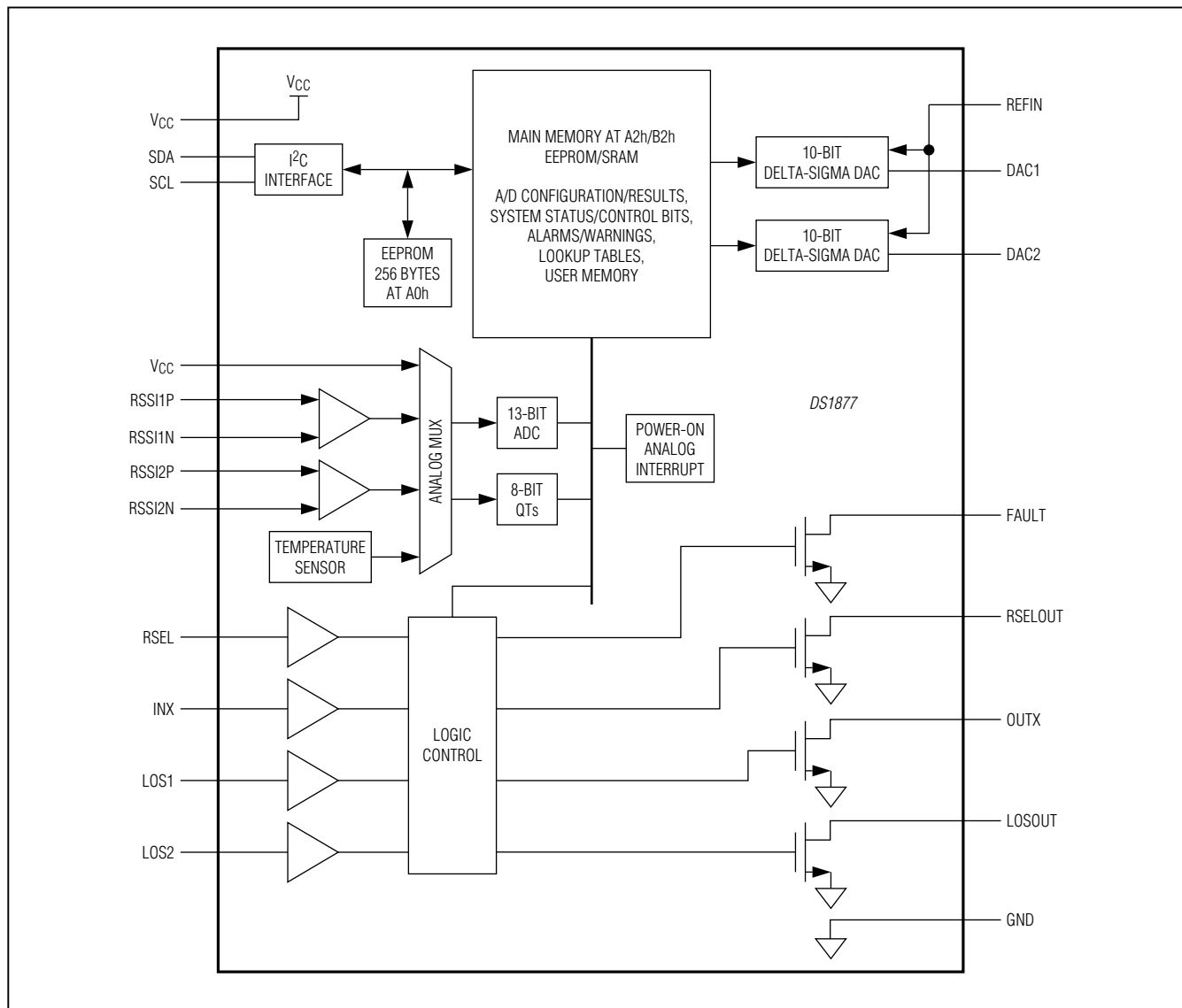
Maxim Integrated

Block Diagram

DS1877
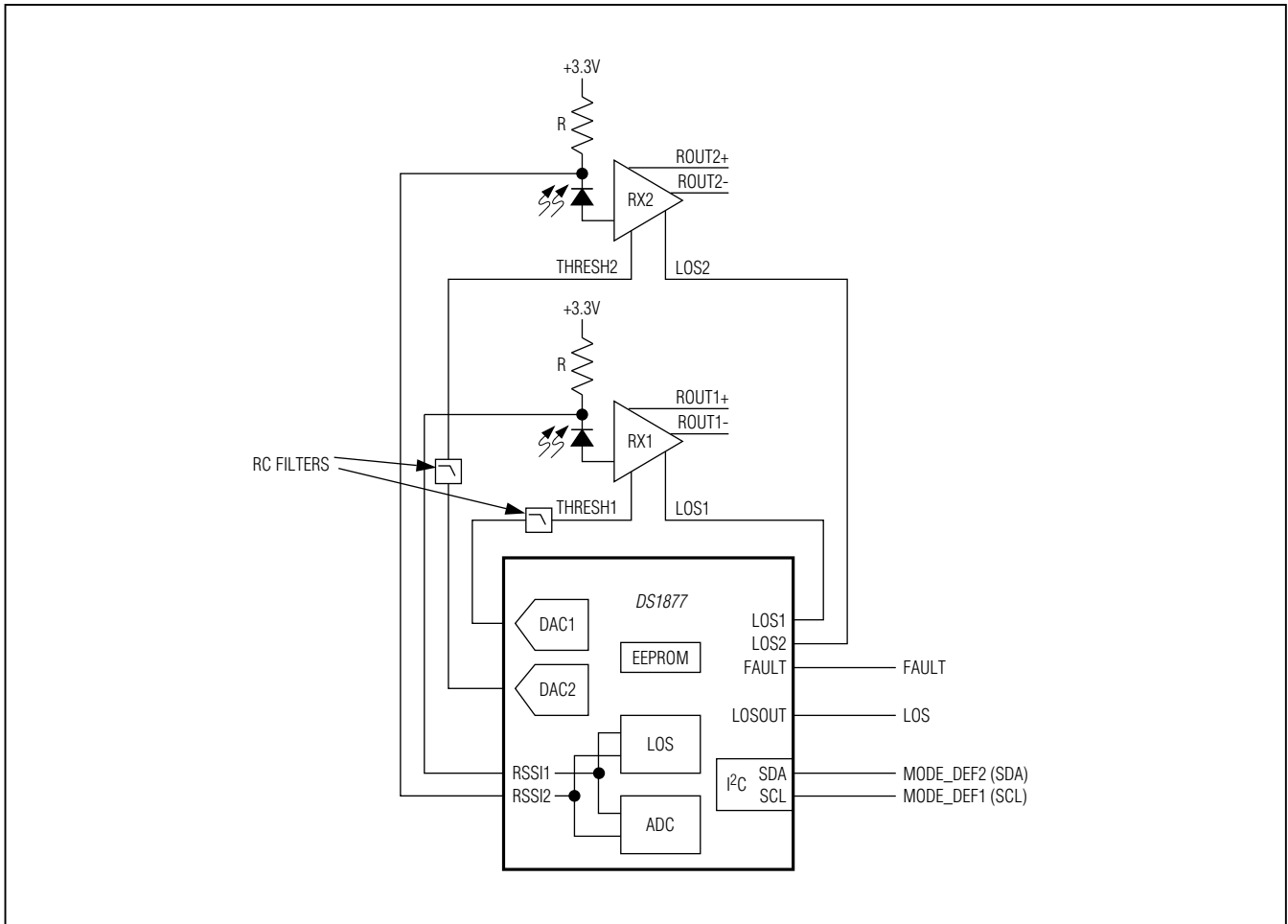
SFP Controller for Dual Rx Interface

Detailed Description

The DS1877 integrates the control and monitoring functionality required in an SFP or SFP+ system. The device is specifically designed for a dual-receiver SFP module. Key components of the device are shown in the *Block Diagram* and described in subsequent sections.

DACs During Power-Up

On power-up, the device sets the DACs to high impedance. After time t_{INIT}, the DACs are set to an initial condition set in EEPROM. After a temperature conversion is completed and if the VCC LO alarm is enabled, an additional V_{CC} conversion above the customer-defined VCC LO alarm level is required before the DACs are updated with the value determined by the temperature conversion and the DAC LUT. See Figure 1.

Quick-Trip Timing

As shown in Figure 2, the device's input comparator is shared between two LOS comparisons. The comparator polls the alarms in a multiplexed sequence. The comparator checks the LOS (RSSI1_ and RSSI2_) signals against the internal reference. Depending on the results of the comparison, the corresponding alarms and warnings are asserted or deasserted. Any QT alarm that is detected by default remains active until a subsequent comparator sample shows that the condition no longer exists.

Table 1. Acronyms

ACRONYM	DESCRIPTION
ADC	Analog-to-Digital Converter
AGC	Automatic Gain Control
APC	Automatic Power Control
APD	Avalanche Photodiode
ATB	Alarm Trap Bytes
DAC	Digital-to-Analog Converter
LOS	Loss of Signal
LUT	Lookup Table
NV	Nonvolatile
QT	Quick Trip
TIA	Transimpedance Amplifier
ROSA	Receiver Optical Subassembly
SEE	Shadowed EEPROM
SFF	Small Form Factor
SFF-8472	Document Defining Register Map of SFPs and SFFs
SFP	Small Form Factor Pluggable
SFP+	Enhanced SFP

Figure 1. Power-Up Timing

Figure 2. Quick-Trip Sample Timing

SFP Controller for Dual Rx Interface

Monitors and Fault Detection

Monitors

Monitoring functions on the device include two QT comparators and four ADC channels. This monitoring combined with the alarm enables (Table 01h/05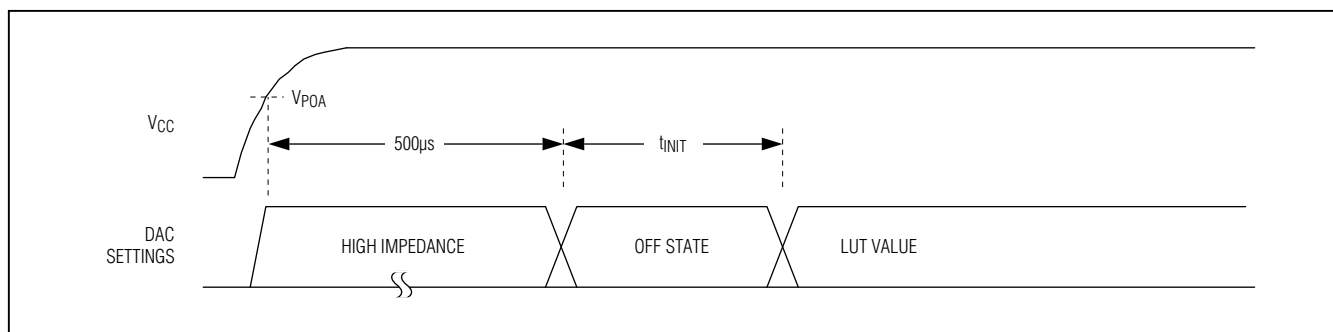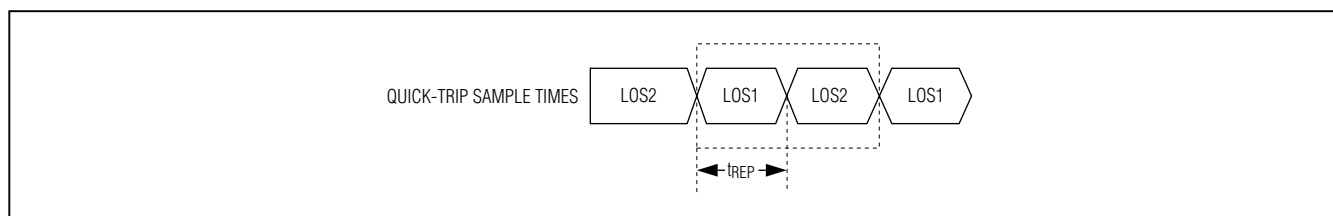h) determines when/if the device triggers the FAULT and/or LOSOUT outputs. All the monitoring levels and interrupt masks are user programmable.

Two Quick-Trip Monitors and Alarms

Two quick-trip monitors are provided that monitor the following:

1) Loss of signal 1 (LOS1 LO)

2) Loss of signal 2 (LOS2 LO)

The LOS_ LO QTs compare the RSSI_ input against its threshold setting to determine if the present received power is below the specification. The LOS_ LO QT can be used to set the LOSOUT pin.

Four ADC Monitors and Alarms

The ADC monitors 4 channels that measure temperature (internal temp sensor), V_{CC}, RSSI1, and RSSI2 using an analog multiplexer to measure them round-robin with a single ADC (see the *ADC Timing* section). The 3V channels have a customer-programmable full-scale range, and all channels have a customer-programmable offset value that is factory programmed to a default value (see Table 2). Additionally, RSSI1 and RSSI2 can right-shift results by up to 7 bits before the results are compared to alarm thresholds or read over the I2C bus. This allows customers with specified ADC ranges to calibrate the ADC full scale to a factor of $1/2^n$ of their specified range

to measure small signals. The device can then right-shift the results by n bits to maintain the bit weight of their specification (see the *Right-Shifting ADC Result* section).

The ADC results (after right-shifting, if used) are compared to the alarm and warning thresholds after each conversion, and the corresponding alarms are set that can be used to trigger the FAULT output. These ADC thresholds are user programmable, as are the masking registers that can be used to prevent the alarms from triggering the FAULT output.

ADC Timing

There are four analog channels that are digitized in a round-robin fashion in the order as shown in Figure 3. The total time required to convert all 4 channels is t_{RR} (see the *Analog Voltage Monitoring Characteristics* for details).

Right-Shifting ADC Result

If the weighting of the ADC digital reading must conform to a predetermined full-scale (PFS) value defined by a standard's specification (e.g., SFF-8472), then right-shifting can be used to adjust the PFS analog measurement range while maintaining the weighting of the ADC results. The device's range is wide enough to cover all requirements; when the maximum input value is ≤ 1/2 the FS value, right-shifting can be used to obtain greater accuracy. For instance, the maximum voltage might be 1/8 the specified PFS value, so only 1/8 of the converter's range is effective over this range. An alternative is to calibrate the ADC's full-scale range to 1/8 the readable PFS value and use a right-shift value of 3. With this implementation, the resolution of the measurement is increased by

Table 2. ADC Default Monitor Full-Scale Ranges

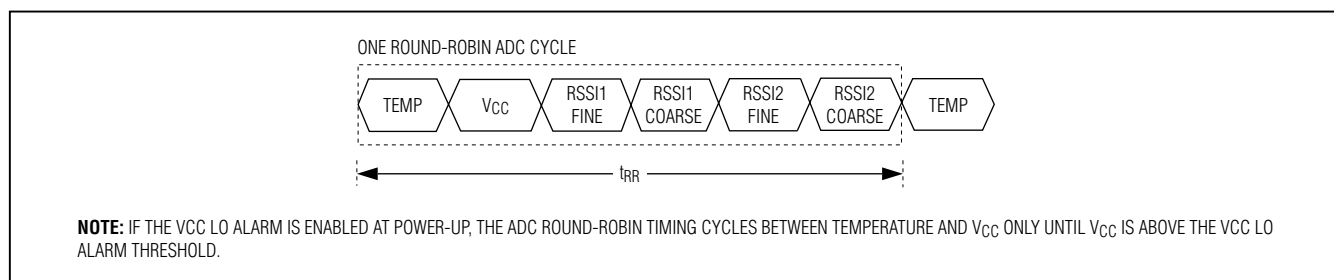| SIGNAL (UNITS)	+FS SIGNAL	+FS HEX	-FS SIGNAL	-FS HEX
Temperature (°C)	127.996	7FFF	-128	8000
V_{CC} (V)	6.5528	FFF8	0	0000
RSSI1, RSSI2 (V)	2.4997	FFF8	0	0000

Figure 3. ADC Round-Robin Timing

a factor of 8, and because the result is digitally divided by 8 by right-shifting, the bit weight of the measurement still meets the standard's specification (i.e., SFF-8472).

The right-shift operation on the ADC result is carried out based on the contents of right-shift control registers (Table 02h, Registers 8Eh–8Fh) in EEPROM. Two analog channels—RSSI1 and RSSI2—each have 3 bits allocated to set the number of right-shifts. Up to seven right-shift operations are allowed and are executed as a part of every conversion before the results are compared to the high and low alarm levels, or loaded into their corresponding measurement registers (Lower Memory, Registers 64h to 6Bh). This is true during the setup of internal calibration as well as during subsequent data conversions.

Differential RSSI1/RSSI2 Inputs

The device offers fully differential inputs for RSSI1 and RSSI2. This enables high-side monitoring of RSSI, as shown in Figure 4. It also reduces board complexity by
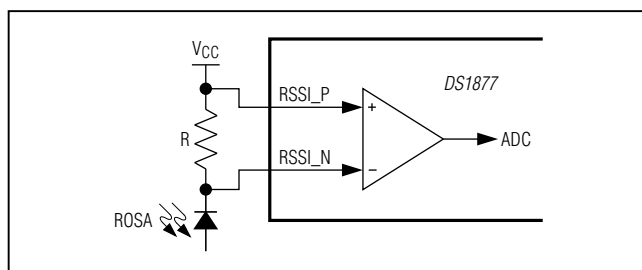
Figure 4. RSSI1/RSSI2 Differential Input for High-Side RSSI

eliminating the need for a high-side differential amplifier or a current mirror.

Enhanced RSSI Monitoring (Dual-Range Functionality)

The device offers a feature to improve the accuracy and range of RSSI1/RSSI2, which is most commonly used for monitoring RSSI. Using a traditional input, the RSSI measurement accuracy can be increased at the cost of reduced input signal swing. The device eliminates this trade-off by offering "dual-range" calibration on the RSSI1/RSSI2 channels. The dual-range calibration can operate in two modes: crossover enabled and crossover disabled. Dual-range operation is enabled by default (factory programmed in EEPROM). However, it can easily be disabled by the RSSIn_FC and RSSIn_FF bits (where n can be 1 or 2) in 8Dh, Table 02h.

Dual-range functionality consists of two ADC modes of operation: fine mode and coarse mode. Each mode is calibrated for a unique transfer function, hence the term, dual range. Table 3 highlights the registers related to RSSI1/RSSI2. Fine mode is calibrated using the gain, offset, and right-shifting registers at locations shown in Table 3, and is ideal for relatively small analog-input voltages. Coarse mode is automatically switched to when the input exceeds a threshold. Coarse mode is calibrated using different gain and offset registers from fine mode. The gain and offset registers for coarse mode are also shown in Table 3. Additional information for each of the registers can be found in the memory map (Figure 14).

Table 3. RSSI1/RSSI2 Configuration Registers

REGISTER	FINE MODE	COARSE MODE
RSSI1/RSSI2 Gain (RSSI1/2 FINE/COARSE SCALE)	9Eh–9Fh/9Ah–9Bh, Table 02h	9Ch–9Dh/98h–99h, Table 02h
RSSI1/RSSI2 Offset (RSSI1/2 FINE/COARSE OFFSET)	AEh–AFh/AAh–ABh, Table 02h	ACh–ADh/A8h–A9h, Table 02h
Right-Shift (RSHIFT$_1$, RSHIFT$_2$)	8Eh–8Fh, Table 02h	8Eh–8Fh, Table 02h
Crossover (XOVER1/XOVER2 FINE/COARSE)	A6h–A7h/96h–97h, Table 02h	A4h–A5h/94h–95Fh, Table 02h
FORCE RSSI (RSSIn_FC and RSSIn_FF Bits)	8Dh, Table 02h	
UPDATE (RSSIR Bit)	6Fh, Lower Memory	
RSSI VALUE (RSSI1/RSSI2 Measurement)	68h–69h, Lower Memory	

Dual-range operation is transparent to the end user. The results of RSSI1/RSSI2 ADCs are still stored/reported in the same memory locations (68h–69h, Lower Memory) regardless of whether the conversion was performed in fine mode or coarse mode. The RSSIR bit indicates whether a fine or coarse conversion generated the digital result.

When the device is powered up, ADCs begin in a round-robin fashion. Every RSSI1/RSSI2 time slice begins with a fine mode ADC (using fine mode's gain, offset, and right-shifting settings). If the value is too large for a fine conversion, a coarse conversion is performed and the result is reported. The coarse-mode conversion is performed using the coarse gain and offset settings. The intersection between coarse and fine depends on the crossover mode used.

The RSSIn_FC and RSSIn_FF bits are used to force fine-mode or coarse-mode conversions or to disable the dual-range functionality. Dual-range functionality is enabled by default (both RSSIn_FC and RSSIn_FF are factory programmed to 0 in EEPROM). Dual-range functionality can be disabled by setting RSSIn_FC to 0 and RSSIn_FF to 1. These bits are also useful when calibrating RSSI1/RSSI2. See the register descriptions and memory map for additional information.

Crossover Enabled

For systems with a nonlinear relationship between the ADC input and desired ADC result, the mode should be set to crossover enabled (Figure 5). The RSSI measurement of an APD receiver is one such application. Using the crossover-enabled mode allows a piecewise linear approximation of the nonlinear response of the APD's gain factor. The crossover point is the value where the fine and coarse ranges intersect. The ADC result transitions between the fine and coarse ranges as defined by the XOVER registers. Right-shifting, slope adjustment, and offset are configurable for both the fine and coarse ranges. The XOVER1/XOVER2 FINE registers determine the maximum results returned by the fine ADC conversions before right-shifting. The XOVER1/XOVER2 COARSE registers determine the minimum results returned by coarse ADC conversions before right-shifting.

Crossover Disabled

The crossover-disabled mode is intended for systems with a linear relationship between the RSSI1/RSSI2 input and the desired ADC result. The ADC result transitions between the fine and coarse ranges with hysteresis, as shown in Figure 6.

In crossover-disabled mode, the thresholds between coarse and fine mode are a function of the number of right-shifts being used. With the use of right-shifting, the fine-mode full scale is programmed to $(1/2^n)$ of the coarse-mode full scale. The device now automatically ranges to choose the range that gives the best resolution for the measurement. Table 4 shows the threshold values for each possible number of right-shifts.

Low-Voltage Operation

The device contains two power-on reset (POR) levels. The lower level is a digital POR (POD) and the higher level is an analog POR (POA). At startup, before the supply voltage rises above POA, the outputs are disabled, all SRAM locations are set to their defaults, shadowed EEPROM (SEE) locations are zero, and all analog circuitry is disabled. When V_{CC} reaches POA, the SEE is recalled, and the analog circuitry is enabled. While V_{CC} remains above POA, the device is in its normal operating state, and it responds based on its nonvolatile configuration. If during operation V_{CC} falls below POA, but is still above POD, the SRAM retains the SEE settings from the first SEE recall, but the device analog is shut down and the outputs disabled. If the supply voltage recovers back above POA, the device immediately resumes normal operation. If the supply voltage falls below POD, the device SRAM is placed in its default state and another SEE recall is required to reload the nonvolatile settings. The EEPROM recall occurs the next time V_{CC} next exceeds POA. Figure 7 shows the sequence of events as the voltage varies.

Table 4. RSSI1/RSSI2 Hysteresis Threshold Values

NO. OF RIGHT-SHIFTS	FINE MODE MAX (HEX)	COARSE MODE MIN* (HEX)
0	FFF8	F000
1	7FFC	7800
2	3FFE	3C00
3	1FFF	1E00
4	0FFF	0F00
5	07FF	0780
6	03FF	03C0
7	01FF	01E0

*This is the minimum reported coarse-mode conversion.
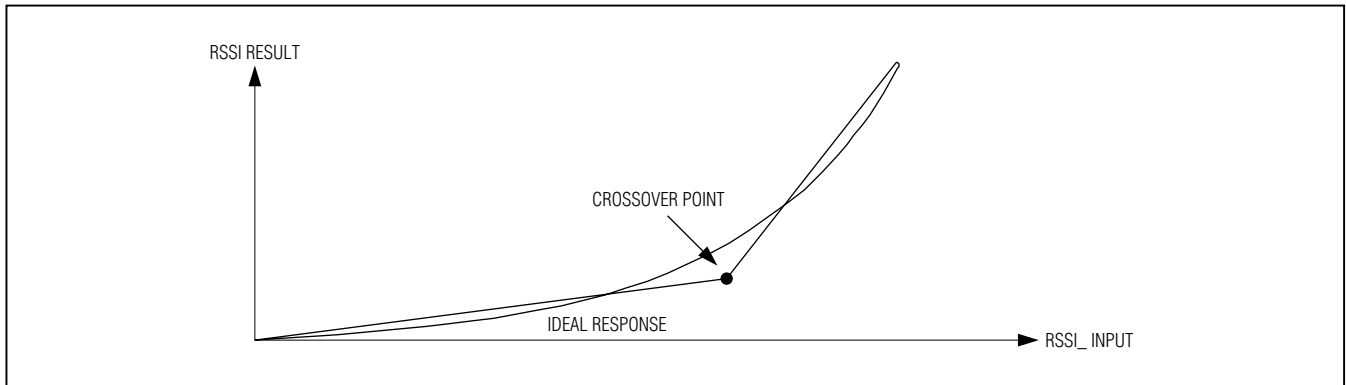
Figure 5. Crossover Enabled
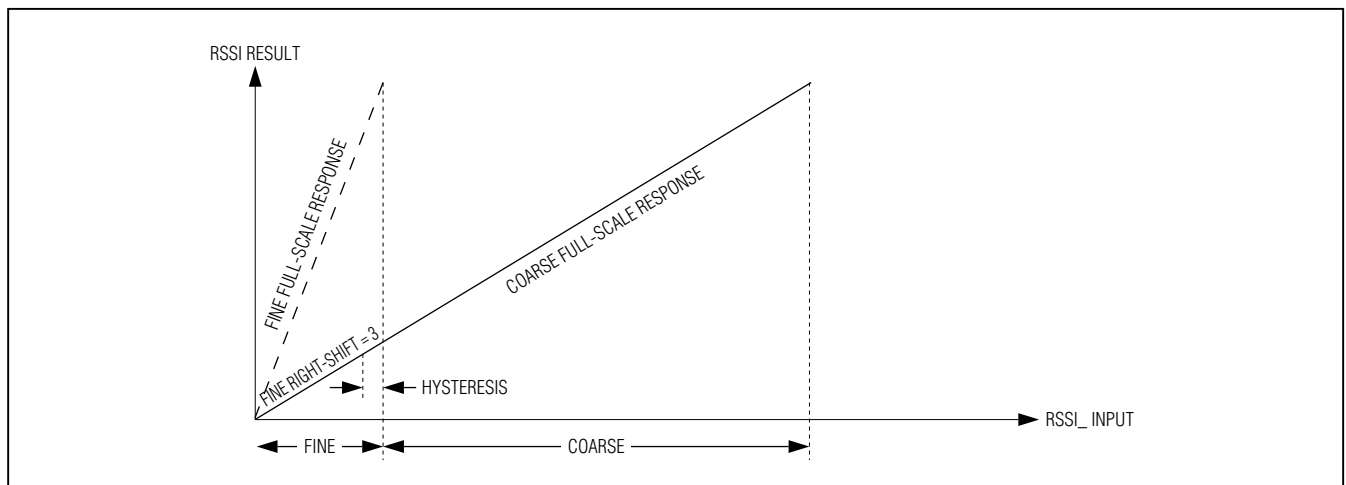
Figure 6. Crossover Disabled
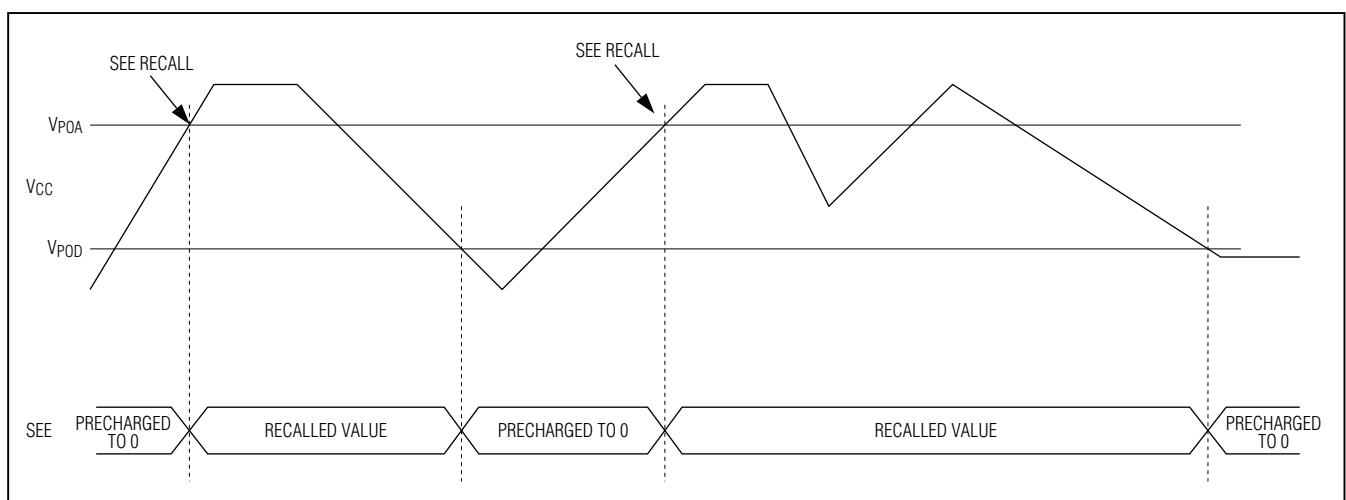
Figure 7. Low-Voltage Operation

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Any time V_{CC} is above POD, the I²C interface can be used to determine if V_{CC} is below the POA level. This is accomplished by checking the RDYB bit in the STATUS byte (Lower Memory, Register 6Eh). RDYB is set when V_{CC} is below POA; when V_{CC} rises above POA, RDYB is timed (within 500µs) to go to 0, at which point the part is fully functional.

For all device addresses sourced from EEPROM (Table 02h, Register 8Bh), the default device address is A2h until V_{CC} exceeds POA, allowing the device address to be recalled from the EEPROM.

Delta-Sigma Outputs

The device's delta-sigma outputs are 10 bits. For illustrative purposes, a 3-bit example is provided in Figure 8.
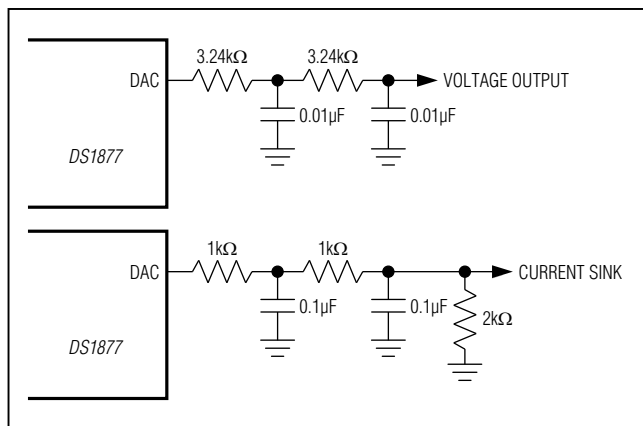
Figure 8. Recommended RC Filter for DAC Outputs

Each possible output of this 3-bit delta-sigma DAC is provided in Figure 9.

In LUT mode the DACs are each controlled by an LUT with high-temperature resolution and an OFFSET LUT with lower temperature resolution. The high-resolution LUTs each have 2°C resolutions. The OFFSET LUTs are located in the upper eight registers (F8h–FFh, Table 04h) of the table containing each high-resolution LUT. The DAC values are determined as follows:

DAC value = DAC LUT + 4 x (DAC OFFSET LUT)

An example calculation for DAC1 is as follows:

Assumptions:

1) Temperature is +43°C

2) Table 04h (DAC OFFSET LUT), Register FCh = 2Ah

3) Table 04h (DAC LUT), Register AAh = 7Bh

Because the temperature is +43°C, the DAC LUT index is AAh and the DAC1 OFFSET LUT index is FCh.

DAC1 = 7Bh + 4 x 2Ah = 123h = 291

When temperature controlled, the DACs are updated after each temperature conversion. See Figure 10.

The reference input, REFIN, is the supply voltage for the output buffer of all the DACs. The voltage connected to REFIN must be able to support the edge rate requirements of the delta-sigma outputs. In a typical application, a 0.1µF capacitor should be connected between REFIN and ground.
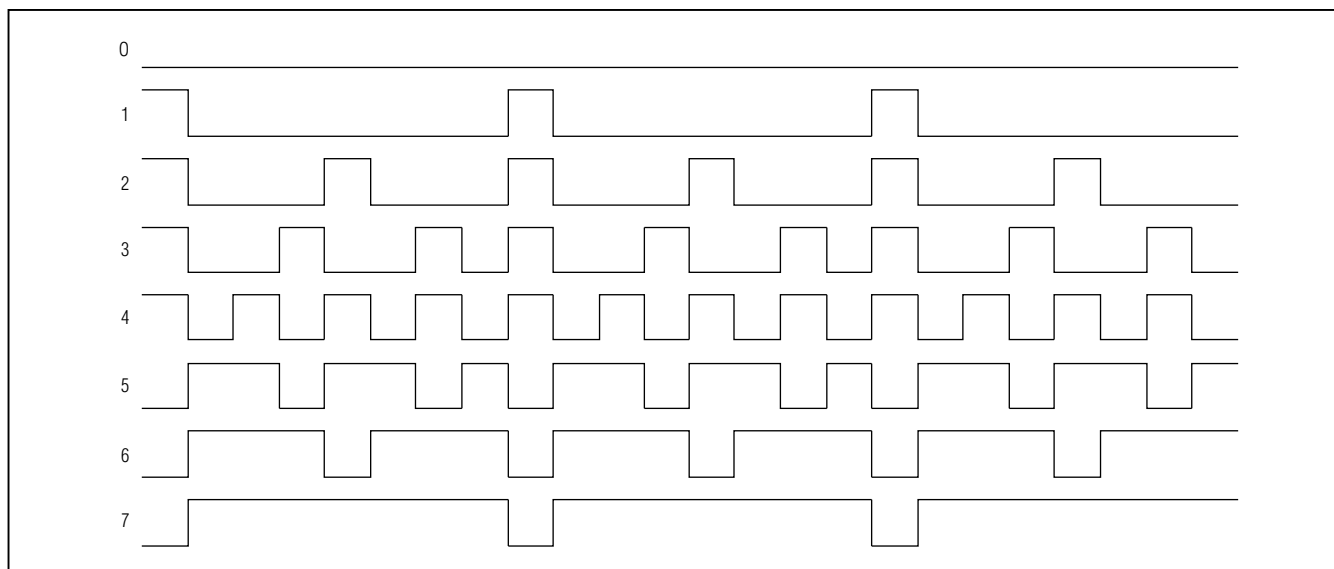
Figure 9. 3-Bit (8-Position) Delta-Sigma Example

Maxim Integrated
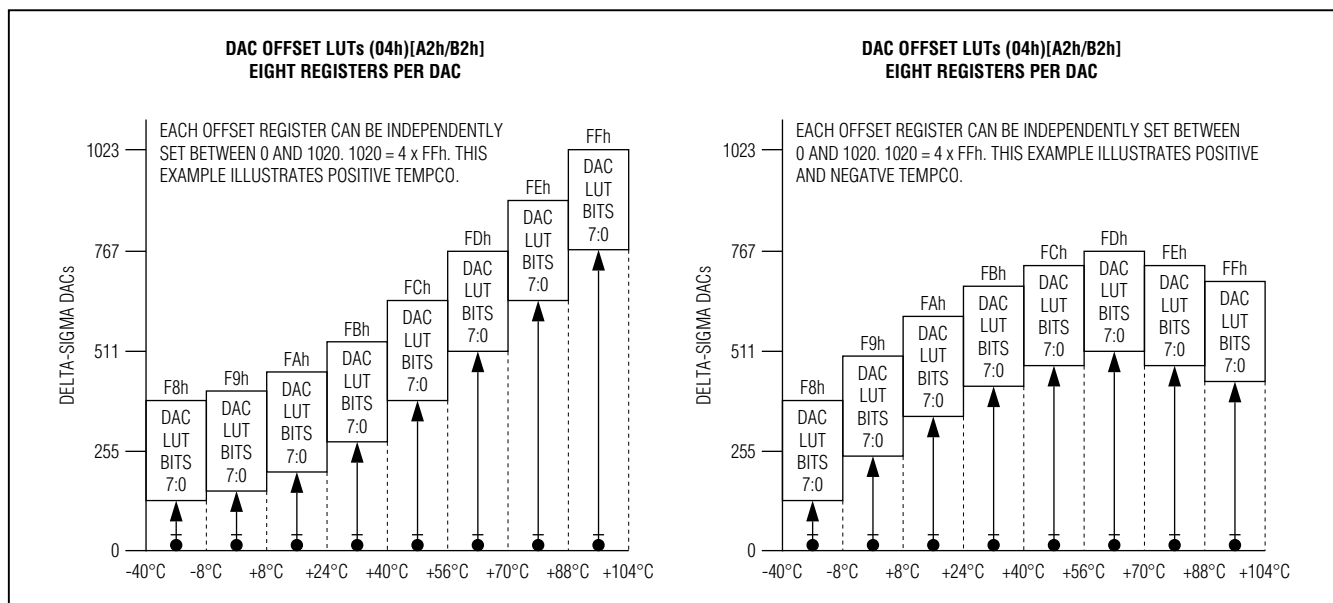
Figure 10. DAC Offset LUTs
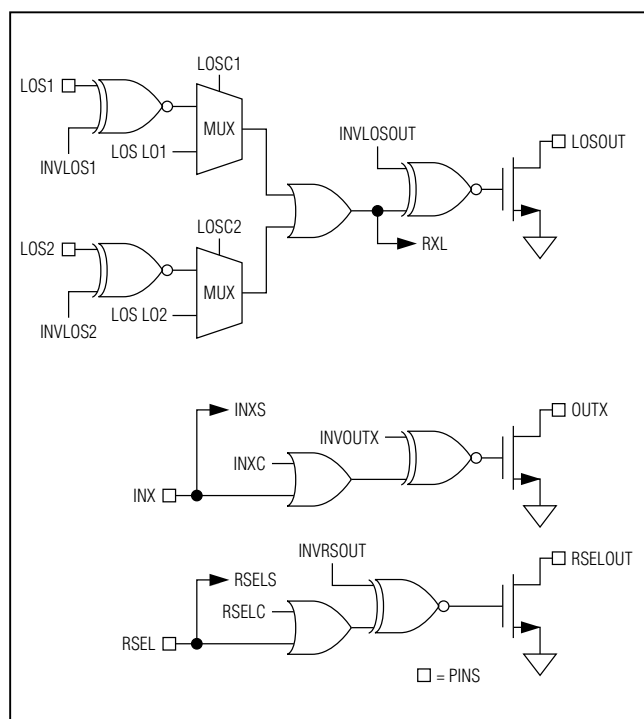
Figure 11. Logic Diagram

Digital I/O Pins
Four digital input pins and four digital output pins are provided for monitoring and control.

LOS1, LOS2, and LOSOUT
When LOSC_ = 0 (Table 02h, Register 8Ah), the LOS_ pin is used to convert a standard comparator output for LOS to an open-collector output. The output of the mux can be read in the STATUS register (Lower Memory, Register 6Eh) as the RXL bit. The RXL signal can be inverted (INVLOS_ = 1) before driving the open-drain output transistor using the XOR gate provided. Setting LOSC_ = 1 configures the mux to be controlled by the LOS LO QT alarm. The mux setting (stored in EEPROM) does not take effect until V$_{CC}$ > POA, allowing the EEPROM to recall.

INX, RSEL, OUTX, RSELOUT
Digital input pins INX and RSEL primarily serve to meet the rate-select requirements of SFP and SFP+. They can also serve as general-purpose inputs. OUTX and RSELOUT are driven by a combination of the INX, RSEL, and logic dictated by control registers in the EEPROM (see Figure 11). The levels of INX and RSEL can be read from the STATUS register (Lower Memory, Register 6Eh). The open-drain output OUTX can be controlled and/or inverted using the CNFGB register (Table 02h, Register 89h). The open-drain RSELOUT output is software controlled and/or inverted through the STATUS register and

CNFGA register (Table 02h, Register 88h). External pull-up resistors must be provided on OUTX and RSELOUT to realize high logic levels.

FAULT Output

FAULT can be triggered by all alarms, warnings, and QTs. The six ADC alarms, warnings, and LOS QTs require enabling (Table 01h/05h, Registers F8h and FCh). Latching of the alarms is controlled by the CNFGB and CNFGC registers (Table 02h, Registers 89h–8Ah).

Die Identification

The device has an ID hardcoded in its die. Two registers (Table 02h, Registers 86h–87h) are assigned for this feature. Register 86h reads 77h to identify the part as the DS1877; Register 87h reads the present device version.

I²C Communication

I²C Definitions

The following terminology is commonly used to describe I²C data transfers.

Master Device: The master device controls the slave devices on the bus. The master device generates SCL clock pulses and START and STOP conditions.

Slave Devices: Slave devices send and receive data at the master's request.

Bus Idle or Not Busy: Time between STOP and START conditions when both SDA and SCL are inactive and in their logic-high states.

START Condition: A START condition is generated by the master to initiate a new data transfer with a slave. Transitioning SDA from high to low while SCL remains high generates a START condition. See Figure 12 for applicable timing.

STOP Condition: A STOP condition is generated by the master to end a data transfer with a slave. Transitioning SDA from low to high while SCL remains high generates a STOP condition. See Figure 12 for applicable timing.

Repeated START Condition: The master can use a repeated START condition at the end of one data transfer to indicate that it will immediately initiate a new data transfer following the current one. Repeated STARTs are commonly used during read operations to identify a specific memory address to begin a data transfer. A repeated START condition is issued identically to a normal START condition. See Figure 12 for applicable timing.

Bit Write: Transitions of SDA must occur during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse

NOTE: TIMING IS REFERENCED TO $V_{IL(MAX)}$ AND $V_{IH(MIN)}$.
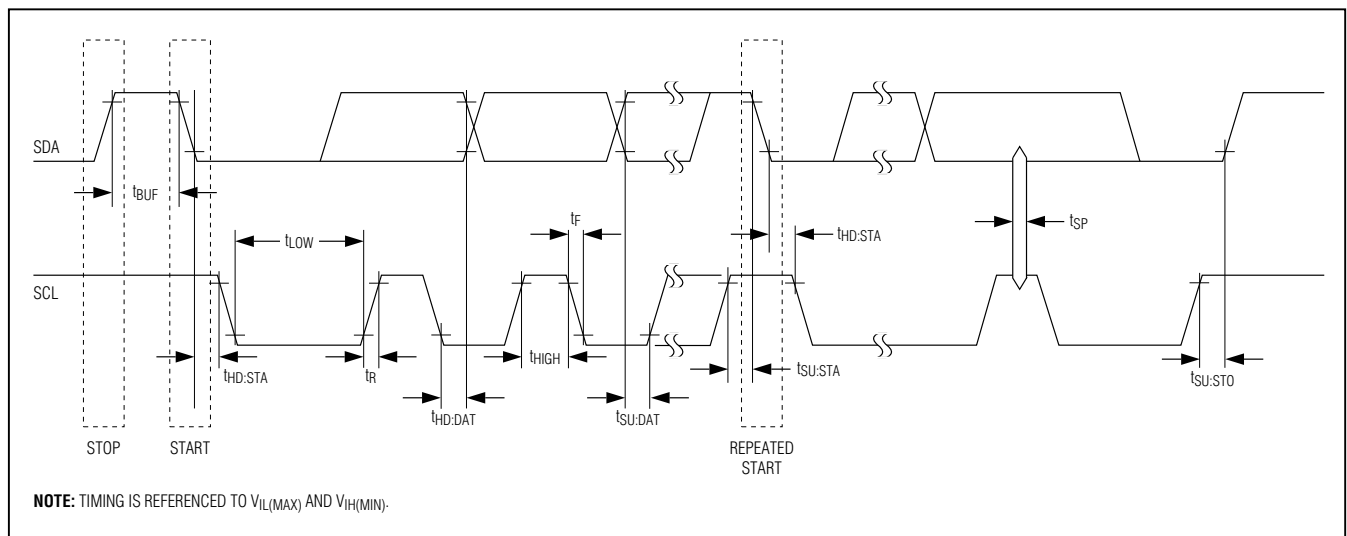
Figure 12. I²C Timing

of SCL plus the setup and hold time requirements (Figure 12). Data is shifted into the device during the rising edge of the SCL.

Bit Read: At the end of a write operation, the master must release the SDA bus line for the proper amount of setup time (Figure 12) before the next rising edge of SCL during a bit read. The device shifts out each bit of data on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. Remember that the master generates all SCL clock pulses, including when it is reading bits from the slave.

Acknowledgement (ACK and NACK): An acknowledgement (ACK) or not-acknowledge (NACK) is always the 9th bit transmitted during a byte transfer. The device receiving data (the master during a read or the slave during a write operation) performs an ACK by transmitting a zero during the 9th bit. A device performs a NACK by transmitting a one during the 9th bit. Timing (Figure 12) for the ACK and NACK is identical to all other bit writes. An ACK is the acknowledgment that the device is properly receiving data. A NACK is used to terminate a read sequence or as an indication that the device is not receiving data.

Byte Write: A byte write consists of 8 bits of information transferred from the master to the slave (most significant bit first) plus a 1-bit acknowledgement from the slave to the master. The 8 bits transmitted by the master are done according to the bit write definition and the acknowledgement is read using the bit read definition.

Byte Read: A byte read is an 8-bit information transfer from the slave to the master plus a 1-bit ACK or NACK from the master to the slave. The 8 bits of information that are transferred (most significant bit first) from the slave to the master are read by the master using the bit read definition, and the master transmits an ACK using the bit write definition to receive additional data bytes. The master must NACK the last byte read to terminate communication so the slave returns control of SDA to the master.

Slave Address Byte: Each slave on the I^{2}C bus responds to a slave address byte sent immediately following a START condition. The slave address byte contains the slave address in the most significant 7 bits and the R/$\overline{W}$ bit in the least significant bit.

The device responds to three slave addresses. The auxiliary memory always responds to a fixed I^{2}C slave address, A0h. (If the main device's slave address is programmed to be A0h/B0h, access to the auxiliary memory is disabled.) The Lower Memory and Tables 00h–05h respond to I^{2}C slave addresses whose lower 3 bits are configurable (A0h–AEh, B0h–BEh) using the DEVICE ADDRESS byte (Table 02h, Register 8Bh). The user also must set the ASEL bit (Table 02h, Register 88h) for this address to be active. By writing the correct slave address with R/$\overline{W}$ = 0, the master indicates it writes data to the slave. If R/$\overline{W}$ = 1, the master reads data from the slave. If an incorrect slave address is written, the device assumes the master is communicating with another I^{2}C device and ignores the communications until the next START condition is sent.

Memory Address: During an I^{2}C write operation to the device, the master must transmit a memory address to identify the memory location where the slave is to store the data. The memory address is always the second byte transmitted during a write operation following the slave address byte.

I^{2}C Protocol

See Figure 13 for an example of I^{2}C timing.

Writing a Single Byte to a Slave: The master must generate a START condition, write the slave address byte (R/$\overline{W}$ = 0), write the memory address, write the byte of data, and generate a STOP condition. Remember that the master must read the slave's acknowledgement during all byte write operations.

Writing Multiple Bytes to a Slave: To write multiple bytes to a slave, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address, writes up to 8 data bytes, and generates a STOP condition. The device writes 1 to 8 bytes (one page or row) with a single write transaction. This is internally controlled by an address counter that allows data to be written to consecutive addresses without transmitting a memory address before each data byte is sent. The address counter limits the write to one 8-byte page (one row of the memory map). Attempts to write to additional pages of memory without sending a STOP condition between pages result in the address counter wrapping around to the beginning of the present row.

For example: A 3-byte write starts at address 06h and writes three data bytes (11h, 22h, and 33h) to three "consecutive" addresses. The result is that addresses 06h and 07h would contain 11h and 22h, respectively, and the third data byte, 33h, would be written to address 00h.
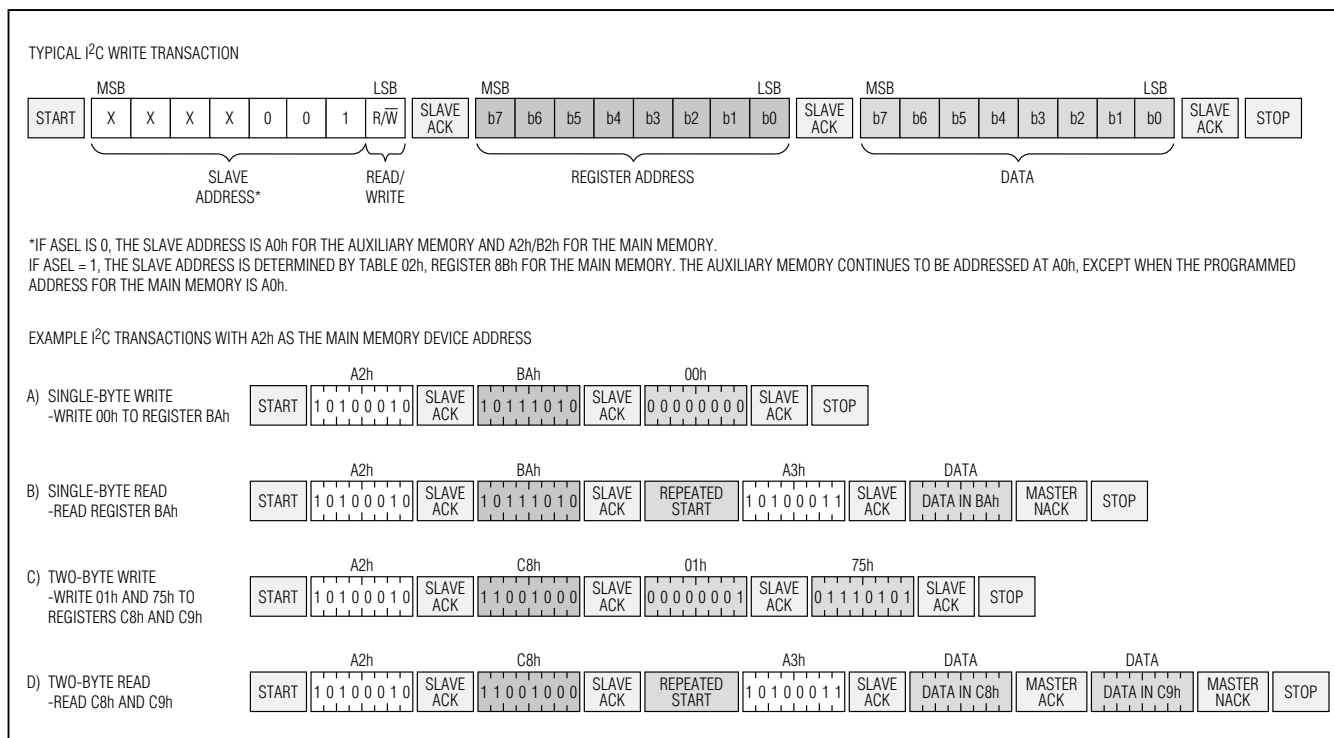
Figure 13. Example I²C Timing

To prevent address wrapping from occurring, the master must send a STOP condition at the end of the page, then wait for the bus-free or EEPROM write time to elapse. Then the master can generate a new START condition and write the slave address byte (R/$\overline{W}$ = 0) and the first memory address of the next memory row before continuing to write data.

Acknowledge Polling: Any time a EEPROM page is written, the device requires the EEPROM write time (t$_{WR}$) after the STOP condition to write the contents of the page to EEPROM. During the EEPROM write time, the device does not acknowledge its slave address because it is busy. It is possible to take advantage of that phenomenon by repeatedly addressing the device, which allows the next page to be written as soon as the device is ready to receive the data. The alternative to acknowledge polling is to wait for maximum period of t$_{WR}$ to elapse before attempting to write again to the device.

EEPROM Write Cycles: When EEPROM writes occur, the device writes the whole EEPROM memory page, even if only a single byte on the page was modified. Writes that do not modify all 8 bytes on the page are allowed and do not corrupt the remaining bytes of memory on the same page. Because the whole page is written, bytes on the page that were not modified during the transaction are still subject to a write cycle. This can result in a whole page being worn out over time by writing a single byte repeatedly. Writing a page 1 byte at a time wears the EEPROM out 8x faster than writing the entire page at once. The device's EEPROM write cycles are specified in the *Nonvolatile Memory Characteristics* table. The specification shown is at the worst-case temperature. It can handle approximately 10x that many writes at room temperature. Writing to SRAM-shadowed EEPROM memory with SEEB = 1 does not count as a EEPROM write cycle when evaluating the EEPROM's estimated lifetime.

Reading a Single Byte from a Slave: Unlike the write operation that uses the memory address byte to define where the data is to be written, the read operation occurs at the present value of the memory address counter. To read a single byte from the slave, the master generates a START condition, writes the slave address byte with R/$\overline{W}$ = 1, reads the data byte with a NACK to indicate the end of the transfer, and generates a STOP condition.

Manipulating the Address Counter for Reads: A dummy write cycle can be used to force the address pointer to a particular value. To do this, the master generates a START condition, writes the slave address byte (R/$\overline{W}$ = 0), writes the memory address where it desires to read, generates a repeated START condition, writes the slave address byte (R/$\overline{W}$ = 1), reads data with ACK or NACK as applicable, and generates a STOP condition.

Memory Organization

The device features memory tables that are internally organized into 8-byte rows. The main device located at A2h is used for overall device configuration and receiver 1 control, calibration, alarms, warnings, and monitoring.

Lower Memory, A2h is addressed from 00h–7Fh and contains alarm and warning thresholds, flags, masks, several control registers, password entry area (PWE), and the table-select byte.

Table 01h, A2h primarily contains user EEPROM (with PW1 level access) as well as alarm and warning enable bytes.

Table 02h, A2h is a multifunction space that contains configuration registers, scaling and offset values, passwords, and interrupt registers as well as other miscellaneous control bytes.

Table 04h, A2h contains a temperature-indexed LUT for control of the DAC1 voltage. The DAC1 LUT can be programmed in 2°C increments over the -40°C to +102°C range. It also contains an LUT for temperature-controlled offsets for DAC1.

Table 05h, A2h is empty by default. It can be configured to contain the alarm and warning enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 88h). In this case Table 01h is empty.

The main device located at B2h is used for receiver 2 control, calibration, alarms, warnings, and monitoring.

Lower Memory, B2h is addressed from 00h–7Fh and contains alarm and warning thresholds, flags, masks, several control registers, PWE, and the table-select byte.

Table 01h, B2h contains alarm and warning enable bytes.

Table 02h, B2h is a multifunction space that contains configuration registers, scaling and offset values, passwords, interrupt registers as well as other miscellaneous control bytes. Table 02h, B2h only contains functions related to receiver 2. All other functions are controlled by Table 02h, A2h.

Table 04h, B2h contains a temperature-indexed LUT for control of the DAC2 voltage. The DAC2 LUT can be programmed in 2°C increments over the -40°C to +102°C range. It also contains an LUT for temperature-controlled offsets for DAC2.

Table 05h, B2h is empty by default. It can be configured to contain the alarm and warning-enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 88h). In this case Table 01h is empty.

Auxiliary Memory (Device A0h) contains 256 bytes of EE memory accessible from address 00h–FFh. It is selected with the device address of A0h.

See the *Register Descriptions* section for a more complete detail of each byte's function, as well as for read/write permissions for each byte.

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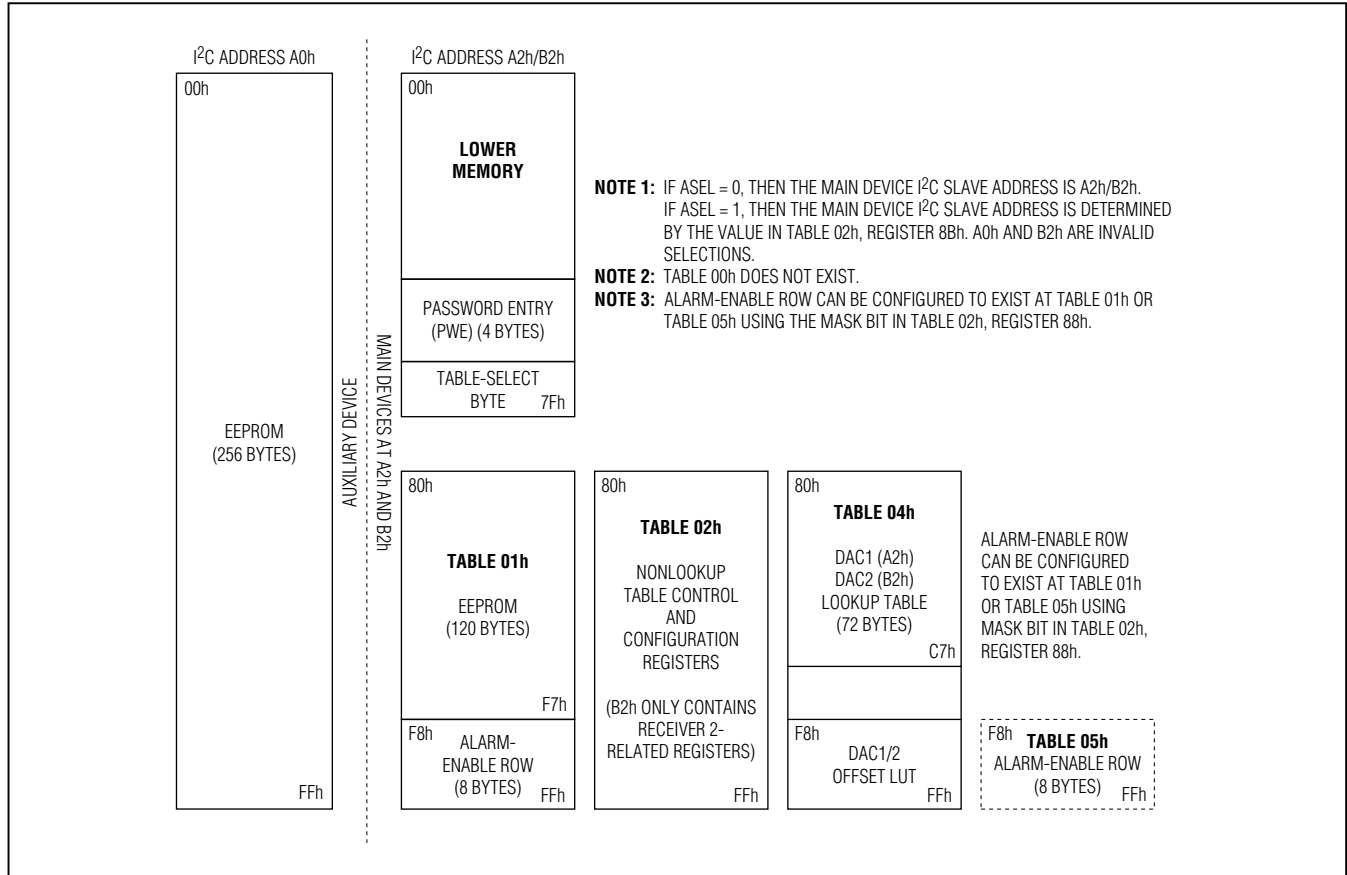
Figure 14. Memory Map

Shadowed EEPROM

Many nonvolatile memory locations (listed within the *Register Descriptions* section) are actually shadowed EEPROM and are controlled by the SEEB bit in Table 02h, Register 80h.

The device incorporates shadowed EEPROM memory locations for key memory addresses that can be written many times. By default the shadowed EEPROM bit, SEEB, is not set and these locations act as ordinary EEPROM. By setting SEEB, these locations function like SRAM cells, which allow an infinite number of write cycles without concern of wearing out the EEPROM. This also eliminates the requirement for the EEPROM write time, t_{WR}. Because changes made with SEEB enabled do not affect the EEPROM, these changes are not retained through power cycles. The power-on value is the last value written with SEEB disabled. This function can be used to limit the number of EEPROM writes during calibration or to change the monitor thresholds periodically during normal operation helping to reduce the number of times EEPROM is written. Figure 14 shows the memory map and indicates which locations are shadowed EEPROM.

Register Descriptions

The register maps show each byte/word (2 bytes) in terms of its row in the memory. The first byte in the row is located in memory at the row address (hexadecimal) in the leftmost column. Each subsequent byte on the row is one/two memory locations beyond the previous byte/word's address. A total of 8 bytes are present on each row. For more information about each of these bytes, see the corresponding register description.

Memory Map Access Codes

The following section provides the device's register definitions. Each register or row of registers has an access descriptor that determines the password level required to read or write the memory. Level 2 password is intended for the module manufacture access only. Level 1 password allows another level of protection for items the end consumer wishes to protect. Many registers are always readable, but require password access to write. There are a few registers that cannot be read without password access. The following access codes describe each mode the device uses with factory settings for the PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h) registers.

ACCESS CODE	READ ACCESS	WRITE ACCESS
<0/_>	At least 1 byte/bit in the row/byte is different than the rest of the row/byte, so look at each byte/bit separately for permissions.	
<1/_>	Read all	Write PW2
<2/_>	Read all	Write not applicable
<3/_>	Read all	Write all, but the device hardware also writes to these bytes/bits
<4/_>	Read PW2	Write PW2 + mode_bit
<5/_>	Read all	Write all
<6/_>	Read not applicable	Write all
<7/_>	Read PW1	Write PW1
<8/_>	Read PW2	Write PW2
<9/_>	Read not applicable	Write PW2
<10/_>	Read PW2	Write not applicable
<11/_>	Read all	Write PW1

Memory Addresses A0h, A2h, and B2h

There are three separate I^{2}C addresses in the device: A0h, A2h, and B2h. A2h and B2h are used to configure and monitor two receivers. Receiver 1 is accessed using A2h. Receiver 2 is accessed using B2h. Many of the registers in A2h and B2h are shared registers. These registers can be read and written from both A2h and B2h.

MEMORY CODE	A2h AND B2h REGISTERS
<C> or <_/C>	A common memory location is used for A2h and B2h device addresses. Reading or writing to these locations is identical, regardless of using A2h or B2h addresses.
<D> or <_/D>	Different memory locations are used for A2h and B2h device addresses.
<M> or <_/M>	Mixture of common and different memory locations for A2h and B2h device addresses. See the individual bytes within the row for clarification. If "M" is used on an individual byte, see the expanded bit descriptions to determine which bits are common vs. different.

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LOWER MEMORY									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
00–07	$^{<1/C>}$THRESHOLD$_0$	TEMP ALARM HI		TEMP ALARM LO		TEMP WARN HI		TEMP WARN LO	
08–0F	$^{<1/C>}$THRESHOLD$_1$	V_{CC} ALARM HI		V_{CC} ALARM LO		V_{CC} WARN HI		V_{CC} WARN LO	
10–1F	$^{<1/C>}$EEPROM	EE		EE		EE		EE	
20–27	$^{<1/D>}$THRESHOLD$_4$	RSSI ALARM HI		RSSI ALARM LO		RSSI WARN HI		RSSI WARN LO	
28–37	$^{<1/C>}$EEPROM	EE		EE		EE		EE	
38–4F	$^{<1/D>}$EEPROM	EE		EE		EE		EE	
50–5F	$^{<1/C>}$EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
60–67	$^{<2/C>}$ADC VALUES$_0$	TEMP VALUE		V_{CC} VALUE		RESERVED		RESERVED	
68–6F	$^{<0/M>}$ADC VALUES$_1$	$^{<2/D>}$RSSI VALUE		RESERVED		RESERVED		$^{<0/M>}$STATUS	$^{<3/D>}$UPDATE
70–77	$^{<2/D>}$ALARM/WARN	ALARM$_3$	ALARM$_2$	RESERVED	ALARM$_0$	WARN$_3$	RESERVED	RESERVED	RESERVED
78–7F	$^{<0/M>}$TABLE SELECT	RESERVED	RESERVED	RESERVED	$^{<6/C>}$PWE MSW		$^{<6/C>}$PWE LSW		$^{<5/D>}$TBL SEL

_<C> or <_/C> = Common, <D> or <_/D> = Different, <M> or <_/M> = Mixture of common and different._

TABLE 01h									
ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–BF	$^{<7/C>}$EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
C0–F7	$^{<8/C>}$EEPROM	EE	EE	EE	EE	EE	EE	EE	EE
F8–FF	$^{<7/M>}$ALARM ENABLE	$^{<C>}$ALARM EN$_3$	$^{<D>}$ALARM EN$_2$	RESERVED	$^{<D>}$ALARM EN$_0$	$^{<C>}$WARN EN$_3$	RESERVED	RESERVED	RESERVED

_<C> or <_/C> = Common, <D> or <_/D> = Different, <M> or <_/M> = Mixture of common and different._

Note: _The ALARM ENABLE bytes (Registers F8h–FFh) can be configured to exist in Table 05h instead of here at Table 01h with the MASK bit (Table 02h, Register 88h). If the row is configured to exist in Table 05h, these locations are empty in Table 01h._

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0/_>	<1/_>	<2/_>	<3/_>	<4/_>	<5/_>	<6/_>	<7/_>	<8/_>	<9/_>	<10/_>	<11/_>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1877 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 02h Register Map

		WORD 0		WORD 1		WORD 2		WORD 3	
ROW (HEX)	ROW NAME	BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80	$^{<0/C>}$CONFIG$_0$	$^{<8/C>}$MODE	$^{<4/C>}$TINDEX	RESERVED	RESERVED	RESERVED	RESERVED	$^{<10>}$DEVICE ID	$^{<10>}$DEVICE VER
88	$^{<8/C>}$CONFIG$_1$	CNFGA	CNFGB	CNFGC	DEVICE ADDRESS	RESERVED	FORCE RSSI	RSHIFT$_2$	RSHIFT$_1$
90	$^{<8/C>}$SCALE$_0$	RESERVED		V_{CC} SCALE		XOVER2 COARSE		XOVER2 FINE	
98	$^{<8/C>}$SCALE$_1$	RSSI2 COARSE SCALE		RSSI2 FINE SCALE		RSSI1 COARSE SCALE		RSSI1 FINE SCALE	
A0	$^{<8/C>}$OFFSET$_0$	INTERNAL TEMP OFFSET*		V_{CC} OFFSET		XOVER1 COARSE		XOVER1 FINE	
A8	$^{<8/C>}$OFFSET$_1$	RSSI2 COARSE OFFSET		RSSI2 FINE OFFSET		RSSI1 COARSE OFFSET		RSSI1 FINE OFFSET	
B0	$^{<9/C>}$PWD VALUE	PW1 MSW		PW1 LSW		PW2 MSW		PW2 LSW	
B8	$^{<8/C>}$THRESHOLD	LOS RANGING$_2$	RESERVED	HLOS2	LLOS2	LOS RANGING$_1$	RESERVED	HLOS1	LLOS1
C0	$^{<8/C>}$PWD ENABLE	PW_ENA	PW_ENB	RESERVED	RESERVED	RESERVED	RESERVED	POLARITY	TBLSELPON
C8	$^{<4/C>}$DAC VALUES	DAC2 VALUE		RESERVED		DAC1 VALUE		RESERVED	
D0–FF	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY

Table title: TABLE 02h (PW2)

<C> or <_/C> = Common, <D> or <_/D> = Different, <M> or <_/M> = Mixture of common and different.

*The final result must be XORed with BB40h before writing to this register.

Table 04h Register Map

		WORD 0		WORD 1		WORD 2		WORD 3	
ROW (HEX)	ROW NAME	BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
80–C7	$^{<8/D>}$LUT4	DAC LUT	DAC LUT	DAC LUT	DAC LUT	DAC LUT	DAC LUT	DAC LUT	DAC LUT
C8–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8–FF	$^{<8/D>}$DAC OFFSET	DAC OFFSET LUT	DAC OFFSET LUT	DAC OFFSET LUT	DAC OFFSET LUT	DAC OFFSET LUT	DAC OFFSET LUT	DAC OFFSET LUT	DAC OFFSET LUT

Table title: TABLE 04h (DAC LUT)

<C> or <_/C> = Common, <D> or <_/D> = Different, <M> or <_/M> = Mixture of common and different.

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0/_>	<1/_>	<2/_>	<3/_>	<4/_>	<5/_>	<6/_>	<7/_>	<8/_>	<9/_>	<10/_>	<11/_>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1877 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Table 05h Register Map

ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
						TABLE 05h			
80–F7	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY	EMPTY
F8–FF	$^{<7/M>}$ALARM ENABLE	$^{<D>}$ALARM EN$_3$	$^{<M>}$ALARM EN$_2$	RESERVED	$^{<D>}$ALARM EN$_0$	$^{<M>}$WARN EN$_3$	RESERVED	RESERVED	RESERVED

<C> or <_/C> = Common, <D> or <_/D> = Different, <M> or <_/M> = Mixture of common and different.

Note: Table 05h is empty by default. It can be configured to contain the alarm and warning enable bytes from Table 01h, Registers F8h–FFh with the MASK bit enabled (Table 02h, Register 88h). In this case Table 01h is empty.

Auxiliary Memory A0h Register Map

ROW (HEX)	ROW NAME	WORD 0		WORD 1		WORD 2		WORD 3	
		BYTE 0/8	BYTE 1/9	BYTE 2/A	BYTE 3/B	BYTE 4/C	BYTE 5/D	BYTE 6/E	BYTE 7/F
						AUXILIARY MEMORY (A0h)			
00–FF	$^{<5>}$AUX EE	EE	EE	EE	EE	EE	EE	EE	EE

<C> or <_/C> = Common, <D> or <_/D> = Different, <M> or <_/M> = Mixture of common and different.

The access codes represent the factory default values of PW_ENA and PW_ENB (Table 02h, Registers C0h–C1h). These registers also allow for custom permissions.

ACCESS CODE	<0/_>	<1/_>	<2/_>	<3/_>	<4/_>	<5/_>	<6/_>	<7/_>	<8/_>	<9/_>	<10/_>	<11/_>
Read Access	See each bit/byte separately	All	All	All	PW2	All	N/A	PW1	PW2	N/A	PW2	All
Write Access		PW2	N/A	All and DS1877 hardware	PW2 + mode bit	All	All	PW1	PW2	PW2	N/A	PW1

Lower Memory Register Descriptions

Lower Memory, Register 00h–01h: TEMP ALARM HI

Lower Memory, Register 04h–05h: TEMP WARN HI

FACTORY DEFAULT	7FFFh
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

00h, 04h S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
01h, 05h 2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

BIT 7   BIT 0

Temperature measurement updates above this two's complement threshold set its corresponding alarm or warning bit. Temperature measurement updates equal to or below this threshold clear its alarm or warning bit.

Lower Memory, Register 02h–03h: TEMP ALARM LO

Lower Memory, Register 06h–07h: TEMP WARN LO

FACTORY DEFAULT	8000h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

02h, 06h S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
03h, 07h 2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

BIT 7   BIT 0

Temperature measurement updates below this two's complement threshold set its corresponding alarm or warning bit. Temperature measurement updates equal to or above this threshold clear its alarm or warning bit.

Lower Memory, Register 08h–09h: V$_{CC}$ ALARM HI

Lower Memory, Register 0Ch–0Dh: V$_{CC}$ WARN HI

FACTORY DEFAULT	FFFFh
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

08h, 0Ch (top row); 09h, 0Dh (bottom row); BIT 7 (left), BIT 0 (right)

Voltage measurement updates above this unsigned threshold set its corresponding alarm or warning bit. Voltage measurements equal to or below this threshold clear its alarm or warning bit.

Lower Memory, Register 0Ah–0Bh: V$_{CC}$ ALARM LO

Lower Memory, Register 0Eh–0Fh: V$_{CC}$ WARN LO

FACTORY DEFAULT	0000h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

0Ah, 0Eh (top row); 0Bh, 0Fh (bottom row); BIT 7 (left), BIT 0 (right)

Voltage measurement updates below this unsigned threshold set its corresponding alarm or warning bit. Voltage measurements equal to or above this threshold clear its alarm or warning bit.

Lower Memory, Register 10h–1Fh: EE

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (EE)

EE	EE	EE	EE	EE	EE	EE	EE

10h–1Fh; BIT 7 (left), BIT 0 (right)

PW2 level access-controlled EEPROM.

Lower Memory, Register 20h–21h: RSSI ALARM HI

Lower Memory, Register 24h–25h: RSSI WARN HI

FACTORY DEFAULT	FFFFh
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

20h, 24h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
21h, 25h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

BIT 7   BIT 0

Voltage measurement updates above this unsigned threshold set its corresponding alarm or warning bit.
Voltage measurements equal to or below this threshold clear its alarm or warning bit.

Lower Memory, Register 22h–23h: RSSI ALARM LO

Lower Memory, Register 26h–27h: RSSI WARN LO

FACTORY DEFAULT	0000h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

22h, 26h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
23h, 27h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

BIT 7   BIT 0

Voltage measurement updates below this unsigned threshold set its corresponding alarm or warning bit. Voltage measurements equal to or above this threshold clear its alarm or warning bit.

Lower Memory, Register 28h–37h: EE

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (EE)

28h–37h	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

PW2 level access-controlled EEPROM.

Lower Memory, Register 38h–4Fh: EE

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (EE)

38h–4Fh	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

PW2 level access-controlled EEPROM.

Lower Memory, Register 50h–5Fh: EE

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WLOWER)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (EE)

50h–5Fh	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

PW2 level access-controlled EEPROM.

Lower Memory, Register 60h–61h: TEMP VALUE

POWER-ON VALUE	0000h
READ ACCESS	All
WRITE ACCESS	N/A
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Volatile

60h	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
61h	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
	BIT 7							BIT 0

Signed two's complement direct-to-temperature measurement.

Lower Memory, Register 62h–63h: V$_{CC}$ VALUE

POWER-ON VALUE	0000h
READ ACCESS	All
WRITE ACCESS	N/A
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Volatile

62h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
63h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Left-justified unsigned voltage measurement.

Lower Memory, Register 64h–67h: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

64h–67h	0	0	0	0	0	0	0	0
	BIT 7							BIT 0

These registers are reserved. The value when read is 00h.

Lower Memory, Register 68h–69h: RSSI VALUE

POWER-ON VALUE	0000h
READ ACCESS	All
WRITE ACCESS	N/A
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Volatile

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

68h (first row), 69h (second row), BIT 7 ... BIT 0

Left-justified unsigned voltage measurement.

Lower Memory, Register 6Ah–6Dh: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

0	0	0	0	0	0	0	0

6Ah–6Dh, BIT 7 ... BIT 0

These registers are reserved. The value when read is 00h.

Lower Memory, Register 6Eh: STATUS

POWER-ON VALUE	X0XX 0XXXb
READ ACCESS	All
WRITE ACCESS	See below
A2h AND B2h MEMORY	Mixture of common memory locations and different memory locations (see below)
MEMORY TYPE	Volatile

Write Access	N/A	All	N/A	All	All	N/A	N/A	N/A
6Eh	RESERVED	<5/D>TXDC	<2/C>INXS	<2/C>RSELS	<5/C>RSELC	<2/C>FLTS	<2/D>RXL	<2/C>RDYB
	BIT 7							BIT 0

BIT 7	RESERVED
BIT 6	**TXDC1 [A2h]:** TXD1 software control bit (writable by all users). 0 = (default) This bit has no effect on alarms and warnings. 1 = Setting TXDC1 inhibits the latching of low alarms and warnings LOS1 LO, LOS2 LO, RSSI1 LO, and RSSI2 LO after the condition is cleared. Once TXDC1 is set, it is internally extended by time t_{INITR} to allow for settings to stabilize. Clearing TXDC1 before t_{INITR} has no impact on the latching of these alarms and warnings. **TXDC2 [B2h]:** TXD2 software control bit (writable by all users). 0 = (default) This bit has no effect on alarms and warnings. 1 = Setting TXDC2 inhibits the latching of low alarms and warnings LOS1 LO, LOS2 LO, RSSI1 LO, and RSSI2 LO after the condition is cleared. Once TXDC2 is set, it is internally extended by time t_{INITR} to allow for settings to stabilize. Clearing TXDC2 before t_{INITR} has no impact on the latching of these alarms and warnings.
BIT 5	**INXS [A2h or B2h]:** INX status bit. Reflects the logic state of the INX pin (read-only). 0 = INX pin is logic-low. 1 = INX pin is logic-high.
BIT 4	**RSELS [A2h or B2h]:** RSEL status bit. Reflects the logic state of the RSEL pin (read-only). 0 = RSEL pin is logic-low. 1 = RSEL pin is logic-high.
BIT 3	**RSELC [A2h or B2h]:** RSEL software control bit. This bit allows for software control that is identical to the RSEL pin. Its value is wire-ORed with the logic value of the RSEL pin to create the RSELOUT pin's logic value (writable by all users). 0 = (default) 1 = Forces the device into a RSEL state regardless of the value of the RSEL pin.
BIT 2	**FLTS:** Reflects the driven state of the FAULT pin (read-only). 0 = FAULT pin is low. 1 = FAULT pin is high.
BIT 1	**RXL1 [A2h]:** Status of LOS1 pin or LOS1 LO as determined by the LOSC control bit. **RXL2 [B2h]:** Status of LOS2 pin or LOS2 LO as determined by the LOSC control bit.
BIT 0	**RDYB [A2h or B2h]:** Ready bar. 0 = V_{CC} is above POA. 1 = V_{CC} is below POA and/or too low to communicate over the I²C bus.

Lower Memory, Register 6Fh: UPDATE

POWER-ON VALUE   00h
READ ACCESS   All
WRITE ACCESS   All and device hardware
A2h AND B2h MEMORY   Different A2h and B2h memory locations
MEMORY TYPE   Volatile

6Fh	TEMP RDY	VCC RDY	RESERVED	RESERVED	RSSI RDY	RESERVED	RESERVED	RSSIR
	BIT 7							BIT 0

BITS 7, 6, 3	**TEMP RDY, VCC RDY, RSSI RDY:** Update of completed conversions. At power-on, these bits are cleared and are set as each conversion is completed. These bits can be cleared so that a completion of a new conversion is verified.
BITS 5, 4, 2, 1	RESERVED
BIT 0	**RSSIR:** RSSI range. Reports the range used for conversion update of RSSI. 0 = Fine range is the reported value. 1 = Coarse range is the reported value.

Lower Memory, Register 70h: ALARM3

POWER-ON VALUE   10h
READ ACCESS   All
WRITE ACCESS   N/A
A2h AND B2h MEMORY   Different A2h and B2h memory locations
MEMORY TYPE   Volatile

70h	TEMP HI	TEMP LO	VCC HI	VCC LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**TEMP HI:** High alarm status for temperature measurement. 0 = (default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**TEMP LO:** Low alarm status for temperature measurement. 0 = (default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**VCC HI:** High alarm status for V_{CC} measurement. 0 = (default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**VCC LO:** Low alarm status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold. 0 = Last measurement was equal to or above threshold setting. 1 = (default) Last measurement was below threshold setting.
BITS 3:0	RESERVED

Lower Memory, Register 71h: ALARM2

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
A2h AND B2h MEMORY	Mixed A2h and B2h memory locations
MEMORY TYPE	Volatile

71h	RSSI HI	RSSI LO	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FLTINT
	BIT 7							BIT 0

BIT 7	**RSSI HI:** High alarm status for RSSI measurement. A TXD event does not clear this alarm. 0 = (default) Last measurement was equal to or below the threshold setting. 1 = Last measurement was above the threshold setting.
BIT 6	**RSSI LO:** Low alarm status for RSSI measurement. A TXD event does not clear this alarm. 0 = (default) Last measurement was equal to or above the threshold setting. 1 = Last measurement was below the threshold setting.
BITS 5:1	RESERVED
BIT 0	**FLTINT:** FAULT interrupt. This bit is the wire-ORed logic of all alarms and warnings wire-ANDed with their corresponding enable bits. The enable bits are found in Table 01h/05h, Registers F8h–FFh.

Lower Memory, Register 72h: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

This register is reserved.

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Lower Memory, Register 73h: ALARM$_0$

POWER-ON VALUE	00h
READ ACCESS	All
WRITE ACCESS	N/A
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Volatile

73h	LOS HI	LOS LO	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**LOS HI:** High alarm status for RSSI; fast comparison. A TXD event does not clear this alarm. 0 = (default) Last comparison was below threshold setting. 1 = Last comparison was above threshold setting.
BIT 6	**LOS LO:** Low alarm status for RSSI; fast comparison. A TXD event does not clear this alarm. 0 = (default) Last comparison was above threshold setting. 1 = Last comparison was below threshold setting.
BITS 5:0	RESERVED

Lower Memory, Register 74h: WARN$_3$

POWER-ON VALUE	10h
READ ACCESS	All
WRITE ACCESS	N/A
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Volatile

74h	TEMP HI	TEMP LO	VCC HI	VCC LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**TEMP HI:** High warning status for temperature measurement. 0 = (default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 6	**TEMP LO:** Low warning status for temperature measurement. 0 = (default) Last measurement was equal to or above threshold setting. 1 = Last measurement was below threshold setting.
BIT 5	**VCC HI:** High warning status for V_{CC} measurement. 0 = (default) Last measurement was equal to or below threshold setting. 1 = Last measurement was above threshold setting.
BIT 4	**VCC LO:** Low warning status for V_{CC} measurement. This bit is set when the V_{CC} supply is below the POA trip-point value. It clears itself when a V_{CC} measurement is completed and the value is above the low threshold. 0 = Last measurement was equal to or above threshold setting. 1 = (default) Last measurement was below threshold setting.
BITS 3:0	RESERVED

Lower Memory, Registers 75h–7Ah: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

These registers are reserved. The value when read is 00h.

Lower Memory, Registers 7Bh–7Eh: PASSWORD ENTRY (PWE)

POWER-ON VALUE	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	All
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Volatile

	BIT 7							BIT 0
7Bh	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
7Ch	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
7Dh	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
7Eh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

There are two passwords for the device. Each password is 4 bytes long. The lower level password (PW1) has all the access of a normal user plus those made available with PW1. The higher level password (PW2) has all the access of PW1 plus those made available with PW2. The values of the passwords reside in EEPROM inside PW2 memory. At power-up, all PWE bits are set to 1. All reads at this location are 0.

Lower Memory, Register 7Fh: TABLE SELECT (TBL SEL)

POWER-ON VALUE	TBLSELPON (Table 02h, Register C7h)
READ ACCESS	All
WRITE ACCESS	All
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Volatile

	BIT 7							BIT 0
7Fh	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

The upper memory tables of the device are accessible by writing the desired table value in this register. The power-on value of this register is defined by the value written to TBLSELPON (Table 02h, Register C7h).

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Table 01h, Register 80h–F7h: EEPROM

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1A) or (PW1 and RTBL1A)
WRITE ACCESS	PW2 or (PW1 and RWTBL1A)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (EE)

80h–F7h	EE	EE	EE	EE	EE	EE	EE	EE
	BIT 7							BIT 0

EEPROM for PW1 and/or PW2 level access.

Table 01h, Register F8h: ALARM EN$_3$

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

F8h	TEMP HI	TEMP LO	VCC HI	VCC LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to ALARM$_3$ in Lower Memory, Register 70h. Enables alarms to create FLTINT (Lower Memory, Register 71h) logic. The MASK bit (Table 02h, Register 88h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**TEMP HI [A2h or B2h]:** 0 = Disables interrupt from TEMP HI alarm. 1 = Enables interrupt from TEMP HI alarm.
BIT 6	**TEMP LO [A2h or B2h]:** 0 = Disables interrupt from TEMP LO alarm. 1 = Enables interrupt from TEMP LO alarm.
BIT 5	**VCC HI [A2h or B2h]:** 0 = Disables interrupt from VCC HI alarm. 1 = Enables interrupt from VCC HI alarm.
BIT 4	**VCC LO [A2h or B2h]:** 0 = Disables interrupt from VCC LO alarm. 1 = Enables interrupt from VCC LO alarm.
BITS 3:0	RESERVED

Table 01h, Register F9h: ALARM EN$_2$

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

F9h	RSSI HI	RSSI LO	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to ALARM$_2$ in Lower Memory, Register 71h. Enables alarms to create FLTINT (Lower Memory, Register 71h). The MASK bit (Table 02h, Register 88h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**RSSI HI:** 0 = Disables interrupt from RSSI HI alarm. 1 = Enables interrupt from RSSI HI alarm.
BIT 6	**RSSI LO:** 0 = Disables interrupt from RSSI LO alarm. 1 = Enables interrupt from RSSI LO alarm.
BITS 5:0	RESERVED

Table 01h, Register FAh: RESERVED

POWER-ON VALUE	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

This register is reserved.

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Table 01h, Register FBh: ALARM EN$_0$

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

FBh	LOS HI	LOS LO	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to ALARM$_0$ in Lower Memory, Register 73h. The MASK bit (Table 02h, Register 88h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**LOS HI:** Enables alarm to create FLTINT (Lower Memory, Register 71h) logic. 0 = Disables interrupt from LOS HI alarm. 1 = Enables interrupt from LOS HI alarm.
BIT 6	**LOS LO:** Enables alarm to create FLTINT (Lower Memory, Register 71h) logic. 0 = Disables interrupt from LOS LO alarm. 1 = Enables interrupt from LOS LO alarm.
BITS 5:0	RESERVED

Table 01h, Register FCh: WARN EN$_3$

POWER-ON VALUE	00h
READ ACCESS	PW2 or (PW1 and RWTBL1C) or (PW1 and RTBL1C)
WRITE ACCESS	PW2 or (PW1 and RWTBL1C)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

FCh	TEMP HI	TEMP LO	VCC HI	VCC LO	RESERVED	RESERVED	RESERVED	RESERVED
	BIT 7							BIT 0

Layout is identical to WARN$_3$ in Lower Memory, Register 74h. Enables warnings to create FLTINT (Lower Memory, Register 71h) logic. The MASK bit (Table 02h, Register 88h) determines whether this memory exists in Table 01h or 05h.

BIT 7	**TEMP HI [A2h or B2h]:** 0 = Disables interrupt from the TEMP HI warning. 1 = Enables interrupt from the TEMP HI warning.
BIT 6	**TEMP LO [A2h or B2h]:** 0 = Disables interrupt from the TEMP LO warning. 1 = Enables interrupt from the TEMP LO warning.
BIT 5	**VCC HI [A2h or B2h]:** 0 = Disables interrupt from the VCC HI warning. 1 = Enables interrupt from the VCC HI warning.
BIT 4	**VCC LO [A2h or B2h]:** 0 = Disables interrupt from the VCC LO warning. 1 = Enables interrupt from the VCC LO warning.
BITS 3:0	RESERVED

Table 01h, Register FDh–FFh: RESERVED

POWER-ON VALUE   00h
READ ACCESS   N/A
WRITE ACCESS   N/A
A2h AND B2h MEMORY   N/A
MEMORY TYPE   N/A

These registers are reserved.

Table 02h Register Descriptions

Table 02h, Register 80h: MODE

POWER-ON VALUE   7Fh
READ ACCESS   PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS   PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY   Common A2h and B2h memory locations
MEMORY TYPE   Volatile

80h	SEEB	DAC2EN	RESERVED	RESERVED	AEN	DAC1EN	RESERVED	RESERVED
	BIT 7							BIT 0

BIT 7	**SEEB:** 0 = (default) Enables EEPROM writes to SEE bytes. 1 = Disables EEPROM writes to SEE bytes during configuration, so that the configuration of the part is not delayed by the EE cycle time. Once the values are known, write this bit to a 0 and write the SEE locations again for data to be written to the EEPROM.
BIT 6	**DAC2EN:** 0 = DAC2 VALUE is writable by the user and the LUT recalls are disabled. This allows users to interactively test their modules by writing the values for DAC2. The output is updated with the new value at the end of the write cycle. The I^{2}C STOP condition is the end of the write cycle. 1 = (default) Enables automatic control of the LUT for DAC2 VALUE.
BITS 5, 4, 1, 0	RESERVED
BIT 3	**AEN:** 0 = The temperature-calculated index value TINDEX is writable by the user and the updates of calculated indexes are disabled. This allows the user to interactively test the modules by controlling the indexing for the LUTs. The recalled values from the LUTs appear in the DAC registers after the next completion of a temperature conversion. 1 = (default) The temperature-calculated index value TINDEX is used to control the LUTs.
BIT 2	**DAC1EN:** 0 = DAC1 VALUE is writable by the user and the LUT recalls are disabled. This allows the user to interactively test their modules by writing the values for DAC1. The output is updated with the new value at the end of the write cycle. The I^{2}C STOP condition is the end of the write cycle. 1 = (default) Enables automatic control of the LUT for DAC1 VALUE.

Table 02h, Register 81h: TEMPERATURE INDEX (TINDEX)

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and AEN = 0) or (PW1 and RWTBL2 and AEN = 0)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Volatile

81h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Holds the calculated index based on the temperature measurement. This index is used for the address during lookup of Table 04h. Temperature measurements below -40°C or above +102°C are clamped to 80h and C7h, respectively. The calculation of TINDEX is as follows:

$$TINDEX = \frac{Temp\_Value + 40°C}{2°C} + 80h$$

For the temperature-indexed LUTs (2°C), the index used during the lookup function for each table is as follows:

Table 04h (DAC)	1	$TINDEX_6$	$TINDEX_5$	$TINDEX_4$	$TINDEX_3$	$TINDEX_2$	$TINDEX_1$	$TINDEX_0$

For the 8-position LUT tables, the following table shows the lookup function:

TINDEX	1000_0xxx	1001_0xxx	1001_1xxx	1010_0xxx	1010_1xxx	1011_0xxx	1011_1xxx	11xx_xxxx
BYTE	F8	F9	FA	FB	FC	FD	FE	FF
TEMP (°C)	< -8	-8 to +8	+8 to +24	+24 to +40	+40 to +56	+56 to +72	+72 to +88	≥ +88

Table 02h, Register 82h–85h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

These registers are reserved.

Table 02h, Register 86h: DEVICE ID

FACTORY DEFAULT	77h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	N/A
MEMORY TYPE	ROM

86h	0	1	1	1	0	1	1	1
	BIT 7							BIT 0

Hardwired connections to show the device ID.

Table 02h, Register 87h: DEVICE VER

FACTORY DEFAULT	DEVICE VERSION
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	N/A
MEMORY TYPE	ROM

87h	DEVICE VERSION
	BIT 7 BIT 0

Hardwired connections to show the device version.

Table 02h, Register 88h: CNFGA

FACTORY DEFAULT	C0h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

88h	RESERVED	RESERVED	RESERVED	ASEL	MASK	INVRSOUT	RESERVED	INVLOSOUT
	BIT 7							BIT 0

BITS 7:5, 1	RESERVED
BIT 4	**ASEL:** Address select. 0 = (default) Device address is A2h for receiver 1 and B2h for receiver 2. 1 = DEVICE ADDRESS byte (Table 02h, Register 8Bh) is used as the device address for receiver 1. Receiver 2 remains at B2h.
BIT 3	**MASK:** 0 = (default) Alarm-enable row exists at Table 01h, Registers F8h–FFh. Table 05h, Registers F8h–FFh are empty. 1 = Alarm-enable row exists at Table 05h, Registers F8h–FFh. Table 01h, Registers F8h–FFh are empty.
BIT 2	**INVRSOUT:** Allow for inversion of the RSELOUT pin (see Figure 11). 0 = (default) RSELOUT is not inverted. 1 = RSELOUT is inverted.
BIT 0	**INVLOSOUT:** Allow for inversion of signal driven to the LOSOUT output pin. 0 = (default) LOSOUT is not inverted. 1 = LOSOUT signal is inverted.

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Table 02h, Register 89h: CNFGB

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

89h	INXC	INVOUTX	ALATCH2	QTLATCH2	WLATCH2	ALATCH1	QTLATCH1	WLATCH1
	BIT 7							BIT 0

BIT 7	**INXC:** INX software control bit (see Figure 11). 0 = INX pin's logic controls OUTX pin. 1 = OUTX is active (bit 6 defines the polarity).
BIT 6	**INVOUTX:** Inverts the active state for OUTX (see Figure 11). 0 = Noninverted. 1 = Inverted.
BIT 5	**ALATCH2:** ADC alarm's comparison latch, Lower Memory, Registers 70h–71h. 0 = ADC alarm and flags reflect the status of the last comparison. 1 = ADC alarm flags remain set.
BIT 4	**QTLATCH2:** QT's comparison latch, Lower Memory, Register 73h. 0 = QT alarm and warning flags reflect the status of the last comparison. 1 = QT alarm and warning flags remain set.
BIT 3	**WLATCH2:** ADC warning's comparison latch, Lower Memory, Register 74h. 0 = ADC warning flags reflect the status of the last comparison. 1 = ADC warning flags remain set.
BIT 2	**ALATCH1:** ADC alarm's comparison latch, Lower Memory, Registers 70h–71h. 0 = ADC alarm and flags reflect the status of the last comparison. 1 = ADC alarm flags remain set.
BIT 1	**QTLATCH1:** QT's comparison latch, Lower Memory, Register 73h. 0 = QT alarm and warning flags reflect the status of the last comparison. 1 = QT alarm and warning flags remain set.
BIT 0	**WLATCH1:** ADC warning's comparison latch, Lower Memory, Register 74h. 0 = ADC warning flags reflect the status of the last comparison. 1 = ADC warning flags remain set.

Table 02h, Register 8Ah: CNFGC

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

8Ah	RESERVED	TXD_RST EN DAC2	LOSC2	INVLOS2	RESERVED	TXD_RST EN DAC1	LOSC1	INVLOS1
	BIT 7							BIT 0

BITS 7, 3	RESERVED
BIT 6	**TXD_RST EN DAC2:** 0 = TXDC2 has no effect on DAC2. 1 = DAC2 is reset by TXDC2.
BIT 5	**LOSC2:** See Figure 11. 0 = LOS2 LO QT drives LOSOUT logic. 1 = LOS2 input pin drives LOSOUT logic.
BIT 4	**INVLOS2:** See Figure 11. 0 = (default) LOS2 input is not inverted. 1 = LOS2 input is inverted.
BIT 2	**TXD_RST EN DAC1:** See Figure 11. 0 = TXDC1 has no effect on DAC1. 1 = DAC1 is reset by TXDC1.
BIT 1	**LOSC1:** See Figure 11. 0 = LOS1 LO QT drives LOSOUT logic. 1 = LOS1 input pin drives LOSOUT logic.
BIT 0	**INVLOS1:** See Figure 11. 0 = (default) LOS1 input is not inverted. 1 = LOS1 input is inverted.

Table 02h, Register 8Bh: DEVICE ADDRESS

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

8Bh	RESERVED	RESERVED	RESERVED	RESERVED	2^3	2^2	2^1	RESERVED
	BIT 7							BIT 0

This value becomes the I^2C slave address for the main memory when the ASEL bit (Table 02h, Register 88h) is set. If A0h/B0h is programmed to this register, the auxiliary memory is disabled. For example, writing xxxx_010x makes the main device addresses A4h and B4h.

Table 02h, Register 8Ch: RESERVED

FACTORY DEFAULT
READ ACCESS   N/A
WRITE ACCESS   N/A
A2h AND B2h MEMORY   N/A
MEMORY TYPE   N/A

This register is reserved.

Table 02h, Register 8Dh: FORCE RSSI

FACTORY DEFAULT   00h
READ ACCESS   PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS   PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY   Common A2h and B2h memory locations
MEMORY TYPE   Nonvolatile (SEE)

8Dh	RESERVED	XOVEREN2	RSSI2_FC	RSSI2_FF	RESERVED	XOVEREN1	RSSI1_FC	RSSI1_FF
	BIT 7							BIT 0

BITS 7, 3	RESERVED
BIT 6	**XOVEREN2:** Enables RSSI conversion to use the XOVER2 value during RSSI2 conversions. 0 = Uses hysteresis for linear RSSI measurements. 1 = XOVER2 value is enabled for nonlinear RSSI measurements.
BITS 5:4	**RSSI2_FC and RSSI2_FF:** RSSI2 force coarse and RSSI2 force fine. Control bits for RSSI mode of operation on the RSSI2 conversion. 00b = (default) Normal RSSI mode of operation. 01b = The fine settings of scale and offset are used for RSSI2 conversions. 10b = The coarse settings of scale and offset are used for RSSI2 conversions. 11b = Normal RSSI mode of operation.
BIT 2	**XOVEREN1:** Enables RSSI conversion to use the XOVER1 value during RSSI1 conversions. 0 = Uses hysteresis for linear RSSI measurements. 1 = XOVER1 value is enabled for nonlinear RSSI measurements.
BITS 1:0	**RSSI1_FC and RSSI1_FF:** RSSI1 force coarse and RSSI1 force fine. Control bits for RSSI mode of operation on the RSSI1 conversion. 00b = (default) Normal RSSI mode of operation. 01b = The fine settings of scale and offset are used for RSSI1 conversions. 10b = The coarse settings of scale and offset are used for RSSI1 conversions. 11b = Normal RSSI mode of operation.

Table 02h, Register 8Eh: RIGHT-SHIFT2 (RSHIFT2)

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

8Eh	RESERVED	$RSSI2C_2$	$RSSI2C_1$	$RSSI2C_0$	RESERVED	$RSSI2F_2$	$RSSI2F_1$	$RSSI2F_0$
	BIT 7							BIT 0

Allows for right-shifting the final answer of RSSI2 COARSE and RSSI2 FINE. This allows for scaling the measurement to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB.

Table 02h, Register 8Fh: RIGHT-SHIFT1 (RSHIFT1)

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

8Fh	RESERVED	$RSSI1C_2$	$RSSI1C_1$	$RSSI1C_0$	RESERVED	$RSSI1F_2$	$RSSI1F_1$	$RSSI1F_0$
	BIT 7							BIT 0

Allows for right-shifting the final answer of RSSI1 COARSE and RSSI1 FINE. This allows for scaling the measurements to the smallest full-scale voltage and then right-shifting the final result so the reading is weighted to the correct LSB.

Table 02h, Register 90h–91h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

These registers are reserved.

Table 02h, Register 92h–93h: V$_{CC}$ SCALE

Table 02h, Register 94h–95h: XOVER2 COARSE

Table 02h, Register 96h–97h: XOVER2 FINE

Table 02h, Register 98h–99h: RSSI2 COARSE SCALE

Table 02h, Register 9Ah–9Bh: RSSI2 FINE SCALE

Table 02h, Register 9Ch–9Dh: RSSI1 COARSE SCALE

Table 02h, Register 9Eh–9Fh: RSSI1 FINE SCALE

FACTORY CALIBRATED
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8
2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Rows labeled: 92h, 94h, 96h, 98h, 9Ah, 9Ch, 9Eh (top); 93h, 95h, 97h, 99h, 9Bh, 9Dh, 9Fh (bottom). BIT 7 ... BIT 0

Controls the scaling or gain of the full-scale voltage measurements. The factory-calibrated value produces an FS voltage of 6.5536V for V$_{CC}$, 2.5V for RSSI2 COARSE and RSSI1 COARSE, and 0.3125V for RSSI2 FINE and RSSI1 FINE.

Table 02h, Register A0h–A1h: INTERNAL TEMP OFFSET

FACTORY CALIBRATED
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

S	2^8	2^7	2^6	2^5	2^4	2^3	2^2
2^1	2^0	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}

Rows labeled: A0h (top); A1h (bottom). BIT 7 ... BIT 0

Allows for offset control of temperature measurement if desired. The final result must be XORed with BB40h before writing to this register. Factory calibration contains the desired value for a reading in degrees Celsius.

Table 02h, Register A2h–A3h: V$_{CC}$ OFFSET
Table 02h, Register A4h–A5h: XOVER1 COARSE
Table 02h, Register A6h–A7h: XOVER1 FINE
Table 02h, Register A8h–A9h: RSSI2 COARSE OFFSET
Table 02h, Register AAh–ABh: RSSI2 FINE OFFSET
Table 02h, Register ACh–ADh: RSSI1 COARSE OFFSET
Table 02h, Register AEh–AFh: RSSI1 FINE OFFSET

FACTORY DEFAULT	00h	
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)	
WRITE ACCESS	PW2 or (PW1 and RWTBL2)	
A2h AND B2h MEMORY	Common A2h and B2h memory locations	
MEMORY TYPE	Nonvolatile (SEE)	

S	S	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}
2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2

Rows labeled: A2h, A4h, A6h, A8h, AAh, ACh, AEh (top) and A3h, A5h, A7h, A9h, ABh, ADh, AFh (bottom). BIT 7 (left) to BIT 0 (right).

Allows for offset control of these voltage measurements if desired. This number is two's complement.

Table 02h, Register B0h–B3h: PW1

FACTORY DEFAULT	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	PW2 or (PW1 and WPW1)
MEMORY TYPE	Nonvolatile (SEE)

B0h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
B1h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B2h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
B3h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The PWE value is compared against the value written to this location to enable PW1 access. At power-on, the PWE value is set to all ones. Thus, writing these bytes to all ones grants PW1 access on power-on without writing the password entry. All reads of this register are 00h.

Table 02h, Register B4h–B7h: PW2

FACTORY DEFAULT	FFFF FFFFh
READ ACCESS	N/A
WRITE ACCESS	PW2
MEMORY TYPE	Nonvolatile (SEE)

B4h	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}
B5h	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}
B6h	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
B7h	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
	BIT 7							BIT 0

The PWE value is compared against the value written to this location to enable PW2 access. At power-on, the PWE value is set to all ones. Thus, writing these bytes to all ones grants PW2 access on power-on without writing the password entry. All reads of this register are 00h.

Table 02h, Register B8h: LOS RANGING$_2$

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory location
MEMORY TYPE	Nonvolatile (SEE)

B8h	RESERVED	HLOS2$_2$	HLOS2$_1$	HLOS2$_0$	RESERVED	LLOS2$_2$	LLOS2$_1$	LLOS2$_0$
	BIT 7							BIT 0

This register controls the full-scale range of the QT monitoring for the RSSI2 differential inputs.

BITS 7, 3	RESERVED (default = 0)		
BITS 6:4	**HLOS2[2:0]:** HLOS2 full-scale ranging: 3-bit value to select the full-scale comparison voltage for high LOS found on RSSI2. Default is 000b and creates a full scale of 1.25V.		
	HLOS2[2:0]	**% OF 1.25V**	**FS VOLTAGE (V)**
	000b	100.00	1.250
	001b	80.02	1.0003
	010b	66.69	0.8336
	011b	50.05	0.6256
	100b	40.05	0.5006
	101b	33.38	0.4172
	110b	28.62	0.3578
	111b	25.04	0.313
BITS 2:0	**LLOS2[2:0]:** LLOS2 full-scale ranging: 3-bit value to select the full-scale comparison voltage for low LOS found on RSSI2. Default is 000b and creates a full scale of 1.25V.		
	LLOS2[2:0]	**% OF 1.25V**	**FS VOLTAGE (V)**
	000b	100.00	1.250
	001b	80.02	1.0003
	010b	66.69	0.8336
	011b	50.05	0.6256
	100b	40.05	0.5006
	101b	33.38	0.4172
	110b	28.62	0.3578
	111b	25.04	0.313

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Table 02h, Register B9h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

This register is reserved.

Table 02h, Register BAh: HLOS2

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and QT2EN = 0) or (PW1 and RWTBL2 and QT2EN = 0)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

BAh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Fast comparison DAC threshold adjust for high LOS2. The combination of HLOS2 and LLOS2 creates a hysteresis comparator. As RSSI2 falls below the LLOS2 threshold, the LOS2 LO alarm bit is set to 1. The LOS2 LO alarm remains set until the RSSI2 input is found above the HLOS2 threshold setting, which clears the LOS2 LO alarm bit and sets the LOS2 HI alarm bit.

Table 02h, Register BBh: LLOS2

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and QT2EN = 0) or (PW1 and RWTBL2 and QT2EN = 0)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

BBh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Fast comparison DAC threshold adjust for low LOS2. See HLOS2 (Table 02h, Register BAh) for the functional description.

Table 02h, Register BCh: LOS RANGING$_1$

FACTORY DEFAULT   00h
READ ACCESS   PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS   PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY   Common A2h and B2h memory locations
MEMORY TYPE   Nonvolatile (SEE)

BCh	RESERVED	HLOS1$_2$	HLOS1$_1$	HLOS1$_0$	RESERVED	LLOS1$_2$	LLOS1$_1$	LLOS1$_0$
	BIT 7							BIT 0

This register controls the full-scale range of the QT monitoring for the RSSI1 differential inputs.

BITS 7, 3	RESERVED (default = 0)		
BITS 6:4	**HLOS1[2:0]:** HLOS1 full-scale ranging: 3-bit value to select the full-scale comparison voltage for high LOS found on RSSI1. Default is 000b and creates a full scale of 1.25V.		
	HLOS1[2:0]	**% OF 1.25V**	**FS VOLTAGE (V)**
	000b	100.00	1.250
	001b	80.02	1.0003
	010b	66.69	0.8336
	011b	50.05	0.6256
	100b	40.05	0.5006
	101b	33.38	0.4172
	110b	28.62	0.3578
	111b	25.04	0.313
BITS 2:0	**LLOS1[2:0]:** LLOS1 full-scale ranging: 3-bit value to select the full-scale comparison voltage for low LOS found on RSSI1. Default is 000b and creates a full scale of 1.25V.		
	LLOS1[2:0]	**% OF 1.25V**	**FS VOLTAGE (V)**
	000b	100.00	1.250
	001b	80.02	1.0003
	010b	66.69	0.8336
	011b	50.05	0.6256
	100b	40.05	0.5006
	101b	33.38	0.4172
	110b	28.62	0.3578
	111b	25.04	0.313

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Table 02h, Register BDh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

This register is reserved.

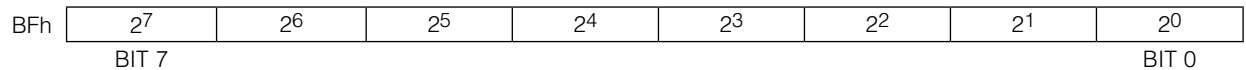**Table 02h, Register BEh: HLOS1**

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and QT2EN = 0) or (PW1 and RWTBL2 and QT2EN = 0)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

BEh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0
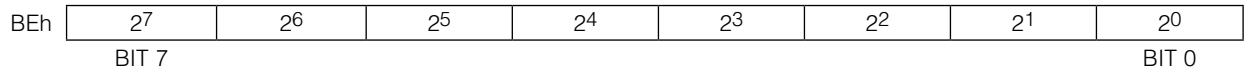
Fast comparison DAC threshold adjust for high LOS1. The combination of HLOS1 and LLOS1 creates a hysteresis comparator. As RSSI1 falls below the LLOS1 threshold, the LOS1 LO alarm bit is set to 1. The LOS1 LO alarm remains set until the RSSI1 input is found above the HLOS1 threshold setting, which clears the LOS1 LO alarm bit and sets the LOS1 HI alarm bit.

Table 02h, Register BFh: LLOS1

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and QT2EN = 0) or (PW1 and RWTBL2 and QT2EN = 0)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

BFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Fast comparison DAC threshold adjust for low LOS1. See HLOS1 (Table 02h, Register BEh) for the functional description.

Table 02h, Register C0h: PW_ENA

FACTORY DEFAULT	10h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

C0h	RESERVED	RWTBL1C	RWTBL2	RWTBL1A	RWTBL1B	WLOWER	WAUXA	WAUXB
	BIT 7							BIT 0

BIT 7	RESERVED
BIT 6	**RWTBL1C:** Table 01h or 05h bytes F8h–FFh. Table address is dependent on MASK bit (Table 02h, Register 88h). 0 = (default) Read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 5	**RWTBL2:** Table 02h. Writing a nonvolatile value to this bit requires PW2 access. 0 = (default) Read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 4	**RWTBL1A:** Table 01h, Registers 80h–BFh. 0 = Read and write access for PW2 only. 1 = (default) Read and write access for both PW1 and PW2.
BIT 3	**RWTBL1B:** Table 01h, Registers C0h–F7h. 0 = (default) Read and write access for PW2 only. 1 = Read and write access for both PW1 and PW2.
BIT 2	**WLOWER:** Bytes 00h–5Fh in main memory. All users can read this area. 0 = (default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.
BIT 1	**WAUXA:** Auxiliary memory, Registers 00h–7Fh. All users can read this area. 0 = (default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.
BIT 0	**WAUXB:** Auxiliary memory, Registers 80h–FFh. All users can read this area. 0 = (default) Write access for PW2 only. 1 = Write access for both PW1 and PW2.

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Table 02h, Register C1h: PW_ENB

FACTORY DEFAULT	03h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

C1h	RWTBL46	RTBL1C	RTBL2	RTBL1A	RTBL1B	WPW1	WAUXAU	WAUXBU
	BIT 7							BIT 0

BIT 7	**RWTBL46:** Table 04h. 0 = (default) Read and write access for PW2 only. 1 = Read and write access for PW1 and PW2.
BIT 6	**RTBL1C:** Table 01h or Table 05h, Registers F8h–FFh. Table address is dependent on MASK bit (Table 02h, Register 88h). 0 = (default) Read access for PW2 only. 1 = Read access for PW1 and PW2.
BIT 5	**RTBL2:** Table 02h. 0 = (default) Read access for PW2 only. 1 = Read access for PW1 and PW2.
BIT 4	**RTBL1A:** Table 01h, Registers 80h–BFh. 0 = (default) Read access for PW2 only. 1 = Read access for PW1 and PW2.
BIT 3	**RTBL1B:** Table 01h, Registers C0h–F7h. 0 = (default) Read access for PW2 only. 1 = Read access for PW1 and PW2.
BIT 2	**WPW1:** Register PW1 (Table 02h, Registers B0h–B3h). 0 = (default) Write access for PW2 only. 1 = Write access for PW1 and PW2.
BIT 1	**WAUXAU:** Auxiliary memory, Registers 00h–7Fh. All users can read this area. 0 = Write access for PW2 only. 1 = (default) Write access for user, PW1, and PW2.
BIT 0	**WAUXBU:** Auxiliary memory, Registers 80h–FFh. All users can read this area. 0 = Write access for PW2 only. 1 = (default) Write access for user, PW1, and PW2.

Table 02h, Register C2h–C5h: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

These registers are reserved.

Table 02h, Register C6h: POLARITY

FACTORY DEFAULT	0Ah
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

C6h	RESERVED	RESERVED	RESERVED	RESERVED	DAC2P	RESERVED	DAC1P	RESERVED
	BIT 7							BIT 0

BITS 7:4, 2, 0	RESERVED
BIT 3	**DAC2P:** DAC2 VALUE polarity. The DAC2 VALUE (Table 02h, Registers C8h–C9h) range is 000h–3FFh. A setting of 000h creates a pulse-density of zero and 3FFh creates a pulse-density of 1023/1024. This polarity bit allows the user to use GND or V_{REFIN} as the reference. The power-on of DAC2 VALUE is 000h; thus an application that needs V_{REFIN} to be the off state should use the inverted polarity. 0 = Normal polarity. A setting of 000h results in a pulse-density output of zero held at GND, and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at V_{REFIN}. 1 = Inverted polarity. A setting of 000h results in a pulse-density output of zero held at V_{REFIN}, and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at GND.
BIT 1	**DAC1P:** DAC1 VALUE polarity. The DAC1 VALUE (Table 02h, Registers CCh–CDh) range is 000h–3FFh. A setting of 000h creates a pulse-density of zero and 3FFh creates a pulse-density of 1023/1024. This polarity bit allows the user to use GND or V_{REFIN} as the reference. The power-on of DAC1 VALUE is 000h; thus an application that needs V_{REFIN} to be the off state should use the inverted polarity. 0 = Normal polarity. A setting of 000h results in a pulse-density output of zero held at GND, and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at V_{REFIN}. 1 = Inverted polarity. A setting of 000h results in a pulse-density output of zero held at V_{REFIN}, and a setting of 3FFh results in a pulsed-density output of 1023/1024 held mostly at GND.

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Table 02h, Register C7h: TBLSELPON

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	PW2 or (PW1 and RWTBL2)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (SEE)

C7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Chooses the initial value for the TBL SEL byte (Lower Memory, Register 7Fh) at power-on.

Table 02h, Register C8h–C9h: DAC2 VALUE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and DAC2EN = 0) or (PW1 and RWTBL2 and DAC2EN = 0)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Volatile

C8h	0	0	0	0	0	0	2^9	2^8
C9h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for DAC2 VALUE. It is the result of LUT4 plus DAC2 OFFSET times 4 recalled from Address B0h, Table 04h (Registers F8h–FFh) at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

$$DAC2\ VALUE = LUT4 + DAC2\ OFFSET \times 4$$

$$V_{DAC2} = \frac{V_{REFIN}}{1024} \times DAC2\ VALUE_d\ \text{(if POLARITY = 0)}$$

$$V_{DAC2} = V_{REFIN} - \frac{V_{REFIN}}{1024} \times DAC\ VALUE_d\ \text{(if POLARITY = 1)}$$

Table 02h, Register CAh–CBh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	None

These registers do not exist.

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Table 02h, Register CCh–CDh: DAC1 VALUE

FACTORY DEFAULT	0000h
READ ACCESS	PW2 or (PW1 and RWTBL2) or (PW1 and RTBL2)
WRITE ACCESS	(PW2 and DAC1EN = 0) or (PW1 and RWTBL2 and DAC1EN = 0)
A2h AND B2h MEMORY	Common A2h and B2h memory locations
MEMORY TYPE	Volatile

CCh	0	0	0	0	0	0	2^9	2^8
CDh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

The digital value used for DAC1 VALUE. It is the result of LUT4 plus DAC1 OFFSET times 4 recalled from Address A0h, Table 04h (Registers F8h–FFh) at the adjusted memory address found in TINDEX. This register is updated at the end of the temperature conversion.

$$DAC1\ VALUE = LUT4 + DAC1\ OFFSET \times 4$$

$$V_{DAC1} = \frac{V_{REFIN}}{1024} \times DAC1\ VALUE_d \ \text{(if POLARITY = 0)}$$

$$V_{DAC1} = V_{REFIN} - \frac{V_{REFIN}}{1024} \times DAC1\ VALUE_d \ \text{(if POLARITY = 1)}$$

Table 02h, Register CEh–CFh: RESERVED

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	N/A

These registers do not exist.

Table 02h, Register D0h–FFh: EMPTY

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	None

These registers do not exist.

Table 04h, Register 80h–C7h: DAC LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL46)
WRITE ACCESS	PW2 or (PW1 and RWTBL46)
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (EE)

80h–C7h	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Digital value for the DAC1 VALUE (A2h address) and DAC2 VALUE (B2h address) outputs. The DAC LUT is a set of registers assigned to hold the temperature profile for the DAC1 and DAC2 values. The temperature measurement is used to index the LUT (TINDEX, Table 02h, Register 81h) in 2°C increments from -40°C to +102°C, starting at 80h. Register 80h defines the -40°C to -38°C DAC output, Register 81h defines -38°C to -36°C DAC output, and so on. Values recalled from this EEPROM memory table are written into the DAC1 and DAC2 value (Table 02h, Registers C8h–C9h, CCh–CDh) locations that hold the values until the next temperature conversion. The device can be placed into a manual mode (DAC1EN and DAC2EN bits, Table 02h, Register 80h), where DAC1 and DAC2 values are directly controlled for calibration. If the temperature compensation functionality is not required, program the entire table to the desired modulation setting.

Table 02h, Register C8h–F7h: EMPTY

FACTORY DEFAULT	00h
READ ACCESS	N/A
WRITE ACCESS	N/A
A2h AND B2h MEMORY	N/A
MEMORY TYPE	None

These registers do not exist.

Table 04h, Register F8h–FFh: DAC OFFSET LUT

FACTORY DEFAULT	00h
READ ACCESS	PW2 or (PW1 and RWTBL46)
WRITE ACCESS	PW2 or (PW1 and RWTBL46)
A2h AND B2h MEMORY	Different A2h and B2h memory locations
MEMORY TYPE	Nonvolatile (EE)

F8h–FFh	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2
	BIT 7							BIT 0

The digital value for the temperature offset of the DAC1 and DAC2 VALUE outputs.

F8h	Less than or equal to -8°C
F9h	Greater than -8°C up to +8°C
FAh	Greater than +8°C up to +24°C
FBh	Greater than +24°C up to +40°C
FCh	Greater than +40°C up to +56°C
FDh	Greater than +56°C up to +72°C
FEh	Greater than +72°C up to +88°C
FFh	Greater than +88°C

The DAC VALUE is a 10-bit value. The DAC LUT is an 8-bit LUT. The DAC OFFSET LUT times 4 plus the DAC LUT makes use of the entire 10-bit range.

Auxiliary Memory A0h Register Descriptions

Auxiliary Memory A0h, Register 00h–7Fh: EEPROM

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WAUXA) or WAUXAU
MEMORY TYPE	Nonvolatile (EE)

00h–7Fh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Accessible with the slave address A0h.

Auxiliary Memory A0h, Register 80h–FFh: EEPROM

FACTORY DEFAULT	00h
READ ACCESS	All
WRITE ACCESS	PW2 or (PW1 and WAUXB) or WAUXBU
MEMORY TYPE	Nonvolatile (EE)

80h–FFh	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	BIT 7							BIT 0

Accessible with the slave address A0h.

Applications Information

Power-Supply Decoupling

To achieve best results, it is recommended that the power supply is decoupled with a 0.01µF or a 0.1µF capacitor. Use high-quality, ceramic, surface-mount capacitors, and mount the capacitors as close as possible to the V_{CC} and GND pins to minimize lead inductance.

SDA and SCL Pullup Resistors

SDA is an open-collector output on the device that requires a pullup resistor to realize high logic levels. A master using either an open-collector output with a pullup resistor or a push-pull output driver can be used for SCL. Pullup resistor values should be chosen to ensure that the rise and fall times listed in the *I2C AC Electrical Characteristics* table are within specification.

Package Information

For the latest package outline information and land patterns, go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
28 TQFN-EP	T2855+6	**21-0140**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/10	Initial release	—
1	4/10	Updated Figure 11 labels for LOS1/2 and INVLOSOUT, and corrected errors in the CNFGC, HLOS2, and HLOS1 bit tables.	19, 47, 54, 56

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