TOSHIBA Field Effect Transistor Silicon N Channel MOS Type (U-MOSⅢ)

SSM4K27CT

Switching Applications

Small package

Low on-resistance: $R_{DS(ON)} = 205 \text{ m}\Omega \text{ (max) (@V_{GS} = 4.0 V)}$

 $R_{DS(ON)} = 260 \text{ m}\Omega \text{ (max) (@V_{GS} = 2.5 V)}$

 $RDS(ON) = 390 \text{ m}\Omega \text{ (max) (@VGS} = 1.8 \text{ V)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-Source voltage		V_{DSS}	20	V	
Gate-Source voltage		V_{GSS}	±12	(\sqrt{y})	
Drain current	DC	ΙD	0.5	A	
	Pulse	I _{DP}	1.0		
Power dissipation		P _D (Note 1)	400	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Unit: mm Side view CST4 JEDEC JEITA **TOSHIBA** 2-1M1A

Weight: 1.1 mg (typ.)

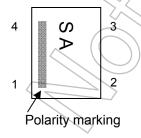
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

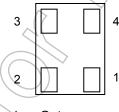
Note 1: Mounted on FR4 board.

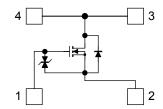
 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 645 \text{ mm}^2)$

Marking (top view)

Electrode Layout (bottom view) Equivalent Circuit (top view)







- Gate
- 2 Source
- 3 Drain
- Drain

Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

> Start of commercial production 2005-02

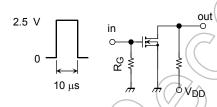
Electrical Characteristics (Ta=25°C)

Chara	acteristics	Symbol	Test Condition	Min.	Тур.	Max.	Unit
Gate leakage current		I _{GSS}	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0$	-	-	±1	μΑ
Drain-Source breakdown voltage	V (BR) DSS	$I_D = 1 \text{ mA}, V_{GS} = 0$	20	_	_	V	
	V (BR) DSX	$I_D = 1 \text{ mA}, V_{GS} = -12 \text{ V}$	10	-	-		
Drain cut-off curre	ent	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0		_	10	μА
Gate threshold vo	ltage	V _{th}	$V_{DS} = 3 \text{ V}, I_D = 1 \text{ mA}$	0.5)	1.1	V
Forward transfer	admittance	Y _{fs}	$V_{DS} = 3 \text{ V}, I_D = 0.25 \text{ A}$ (Note2)	0.8	1.6	-	S
Drain-Source on-resistance		R _{DS} (ON)	$I_D = 0.25 \text{ A}, V_{GS} = 4 \text{ V}$ (Note2)	$\bigcirc)$	175	205	mΩ
			$I_D = 0.25 \text{ A}, V_{GS} = 2.5 \text{ V}$ (Note2)		200	260	
			$I_D = 0.10 \text{ A}, V_{GS} = 1.8 \text{ V}$ (Note2)	_	250	390	
Input capacitance		C _{iss}	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz	-	174	_	pF
Reverse transfer	capacitance	C _{rss}	$V_{DS} = 10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	- /	25	\searrow	pF
Output capacitano	ce	Coss	V _{DS} = 10 V, V _{GS} = 0, f = 1 MHz	-6	31	> -	pF
Switching time	Turn-on time	t _{on}	V _{DD} = 10 V, I _D = 0.25 A,	\(C	10) -	ns
	Turn-off time	t _{off}	$V_{GS} = 0$ to 2.5 V, $R_G = 4.7 \Omega$		12/	_	

Note2: Pulse test

Switching Time Test Circuit

(a) Test Circuit



 $V_{DD}=10\;V$

 $R_G = 4.7 \Omega$

Duty ≤ 1%

 V_{IN} : t_r , $t_f < 5$ ns

Common Source

Ta = 25°C

Precaution

 $V_{th} \ can be expressed as the voltage between the gate and source when the low operating current value is ID = 1 mA for this product. For normal switching operation, VGS (on) requires a higher voltage than Vth and VGS (off) requires a lower voltage than Vth. (The relationship can be established as follows: VGS (off) < Vth < VGS (on).)$

(b) V_{IN}

(c) Vout

2,5 V

 V_{DD}

VDS (ON)

90%

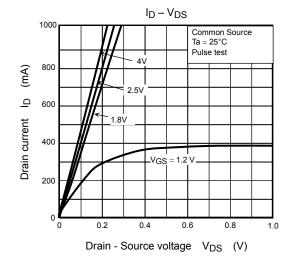
10%

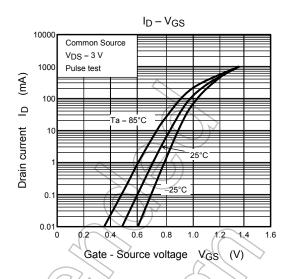
90%

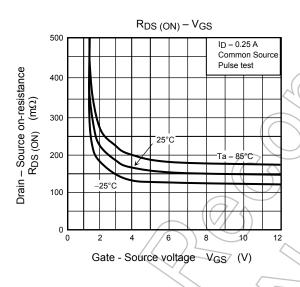
10%

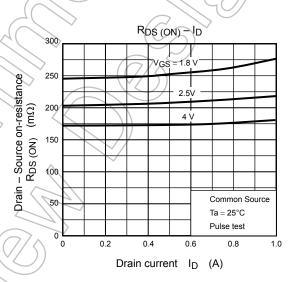
Be sure to take this into consideration when using the device.

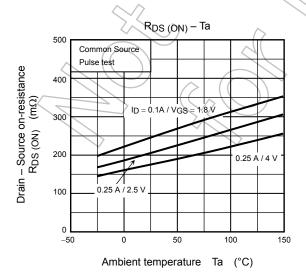
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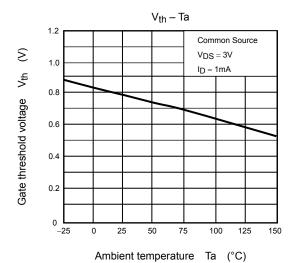






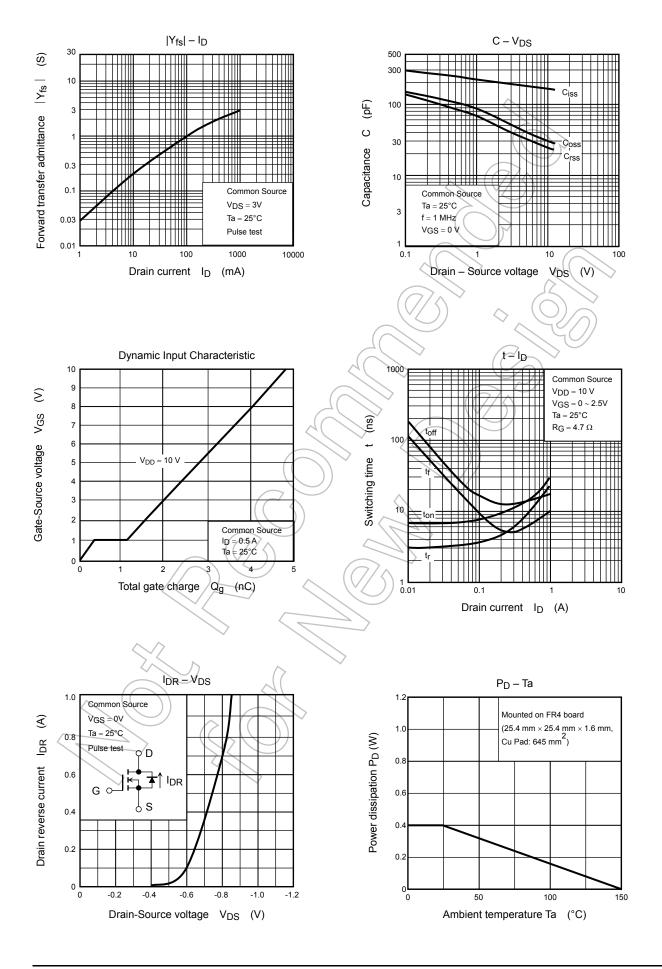






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