19-4604; Rev 3; 3/12

16-Bit Microcontroller with Infrared Module

MAXQ61H

General Description

The MAXQ61H is a low-power, 16-bit MAXQ® microcontroller designed for low-power applications including universal remote controls, consumer electronics, and white goods. The MAXQ61H combines a powerful 16-bit RISC microcontroller and integrated peripherals including an IR module with carrier frequency generation and flexible port I/O capable of multiplexed keypad control.

The MAXQ61H includes 36KB of ROM memory and 1.28KB of data SRAM.

For the ultimate in low-power battery-operated performance, the MAXQ61H includes an ultra-low-power stop mode (0.2µA, typ). In this mode, the minimum amount of circuitry is powered. Wake-up sources include external interrupts, the power-fail interrupt, and a timer interrupt. The microcontroller runs from a wide 1.70V to 3.6V operating voltage.

Applications

Remote Controls

Battery-Powered Portable Equipment

Consumer Electronics

Home Appliances

White Goods

Pin Configuration appears at end of data sheet.

Features

- **High-Performance, Low-Power 16-Bit RISC Core**
- **DC to 12MHz Operation Across Entire Operating Range**
- **1.70V to 3.6V Operating Voltage Range**
- **33 Total Instructions for Simplified Programming**
- **Three Independent Data Pointers Accelerate Data Movement with Automatic Increment/Decrement**
- **Dedicated Pointer for Direct Read from Code Space**
- **16-Bit Instruction Word, 16-Bit Data Bus**
- **16 x 16-Bit General-Purpose Working Registers**
- **Memory Features**
  - 36KB ROM
  - 1.28KB Data SRAM
- **Additional Peripherals**
  - Power-Fail Warning
  - Power-On Reset/Brownout Reset
  - Automatic IR Carrier Frequency Generation and Modulation
  - Two 16-Bit, Programmable Timers/Counters with Prescaler and Capture/Compare
  - Programmable Watchdog Timer
  - 8kHz Nanopower Ring Oscillator Wake-Up Timer
  - Up to 24 (MAXQ61HA) General-Purpose I/Os
- **Low Power Consumption**
  - 0.2µA (typ), 2.0µA (max) in Stop Mode
    T_A = +25°C, Power-Fail Monitor Disabled
  - 2.0mA (typ) at 12MHz in Active Mode

Ordering Information/Selector Guide

PART	TEMP RANGE	OPERATING VOLTAGE (V)	PROGRAM MEMORY (KB)	DATA MEMORY (KB)	PIN-PACKAGE
MAXQ61HA-0000+	0°C to +70°C	1.70 to 3.6	36 ROM	1.28	32 TQFN-EP**
MAXQ61HX-0000+*	0°C to +70°C	1.70 to 3.6	36 ROM	1.28	Bare die

Note: *Contact factory for information about masked ROM devices.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**Contact factory for availability.*
***EP = Exposed pad.*

MAXQ is a registered trademark of Maxim Integrated Products, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* ***www.maxim-ic.com/errata****.*

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Voltage Range on Any Lead with Respect to GND except V_{DD} .....-0.3V to (V_{DD} + 0.5V)
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}			V_{RST}		3.6	V
1.8V Internal Regulator	V_{REG18}			1.62	1.8	1.98	V
Power-Fail Warning Voltage for Supply (Note 2)	V_{PFW}	Monitors V_{DD}		1.75	1.8	1.85	V
Power-Fail Reset Voltage (Note 3)	V_{RST}	Monitors V_{DD}		1.64	1.67	1.70	V
Power-On Reset Voltage	V_{POR}	Monitors V_{DD}		1.0		1.45	V
RAM Data-Retention Voltage	V_{DRV}	(Note 4)		1.0			V
Active Current (Note 5)	I_{DD_1}	SysClk = 12MHz			2.5	3.75	mA
Stop-Mode Current	I_{S1}	Power-Fail Off	T_A = +25°C		0.15	2.0	µA
			T_A = 0°C to +70°C		0.15	8	
	I_{S2}	Power-Fail On	T_A = +25°C		22	31	
			T_A = 0°C to +70°C		27.6	38	
Current Consumption During Power-Fail	I_{PFR}	(Notes 4, 6)		[(3 x I_{S2}) + ((PCI - 3) x (I_{S1} + I_{NANO}))]/PCI			µA
Power Consumption During Power-On Reset	I_{POR}	(Note 7)		100			nA
Stop-Mode Resume Time	t_{ON}			375 + 8192t_{HFXIN}			µs
Power-Fail Monitor Startup Time	t_{PRM_ON}	(Note 4)				150	µs
Power-Fail Warning Detection Time	t_{PFW}	(Notes 4, 8)		10			µs
Input Low Voltage for IRTX, IRRX, $\overline{RESET}$, and All Port Pins	V_{IL}			V_{GND}		0.3 x V_{DD}	V
Input High Voltage for IRTX, IRRX, $\overline{RESET}$, and All Port Pins	V_{IH}			0.7 x V_{DD}		V_{DD}	V
Input Hysteresis (Schmitt)	V_{IHYS}				300		mV
Input Low Voltage for HFXIN	V_{IL_HFXIN}			V_{GND}		0.3 x V_{DD}	V

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage for HFXIN	V_{IH_HFXIN}		0.7 x V_{DD}		V_{DD}	V
IRRX Input Filter Pulse-Width Reject	t_{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t_{IRRX_A}		300			ns
Output Low Voltage for IRTX	V_{OL_IRTX}	V_{DD} = 3.6V, I_{OL} = 25mA (Note 4)			1.0	V
		V_{DD} = 2.35V, I_{OL} = 10mA (Note 4)			1.0	
		V_{DD} = 1.85V, I_{OL} = 4.5mA			1.0	
Output Low Voltage for $\overline{RESET}$ and All Port Pins (Note 9)	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA (Note 4)		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 8mA (Note 4)		0.4	0.5	
		V_{DD} = 1.85V, I_{OL} = 4.5mA		0.4	0.5	
Output High Voltage for IRTX and All Port Pins	V_{OH}	I_{OH} = -2mA	V_{DD} - 0.5		V_{DD}	V
Input/Output Pin Capacitance for All Port Pins	C_{IO}	(Note 4)			15	pF
Input Leakage Current	I_L	Internal pullup disabled	-100		+100	nA
Input Pullup Resistor for $\overline{RESET}$, IRTX, IRRX, and All Port Pins	R_{PU}	V_{DD} = 3.0V, V_{OL} = 0.4V (Note 4)	16	28	39	kΩ
		V_{DD} = 2.0V, V_{OL} = 0.4V	17	30	41	
EXTERNAL CRYSTAL/RESONATOR						
Crystal/Resonator	f_{HFXIN}		DC		12	MHz
Crystal/Resonator Period	t_{HFXIN}		$1/f_{HFXIN}$			ns
Crystal/Resonator Warmup Time	t_{XTAL_RDY}	From initial oscillation	8192 x t_{HFXIN}			ms
Oscillator Feedback Resistor	R_{OSCF}	(Note 4)	0.5	1.0	1.5	MΩ
EXTERNAL CLOCK INPUT						
External Clock Frequency	f_{XCLK}		DC		12	MHz
External Clock Period	t_{XCLK}		$1/f_{XCLK}$			ns
External Clock Duty Cycle	t_{XCLK_DUTY}		45		55	%
System Clock Frequency	f_{CK}		f_{HFIN}			MHz
		HFXOUT = GND	f_{XCLK}			
System Clock Period	t_{CK}		$1/f_{CK}$			MHz
NANOPOWER RING OSCILLATOR						
Nanopower Ring Oscillator Frequency	f_{NANO}	T_A = +25°C	3.0	8.0	20.0	kHz
		T_A = +25°C, V_{DD} = POR voltage (Note 4)	1.7	2.4		
Nanopower Ring Oscillator Duty Cycle	t_{NANO}	(Note 4)	40		60	%
Nanopower Ring Oscillator Current	I_{NANO}	Typical at V_{DD} = 1.64V, T_A = +25°C (Note 4)		40	400	nA

RECOMMENDED DC OPERATING CONDITIONS (continued)

(V_{DD} = V_{RST} to 3.6V, T_A = 0°C to +70°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WAKE-UP TIMER						
Wake-Up Timer Interval	t_{WAKEUP}		$1/f_{NANO}$		$65,535/f_{NANO}$	s
IR						
Carrier Frequency	f_{IR}	(Note 4)			$f_{CK}/2$	Hz

Note 1: Specifications to 0°C are guaranteed by design and are not production tested.

Note 2: The power-fail warning monitor and the power-fail reset monitor track each other with a minimum delta between the two of 0.11V.

Note 3: The power-fail reset and power-on-reset (POR) detectors operate in tandem to ensure that one or both signals are active at all times when $V_{DD} < V_{RST}$. Doing so ensures the device maintains the reset state until the minimum operating voltage is achieved.

Note 4: Guaranteed by design and not production tested.

Note 5: Measured on the V_{DD} pin and the part not in reset. All inputs are connected to GND or V_{DD}. Outputs do not source/sink any current.

Note 6: The power-check interval (PCI) can be set to always on, 1024, 2048, or 4096 nanopower ring oscillator clock cycles.

Note 7: Current consumption during POR when powering up while $V_{DD} < V_{POR}$.

Note 8: The minimum amount of time that V_{DD} must be below V_{PFW} before a power-fail event is detected.

Note 9: The maximum total current, I_{OH} (max) and I_{OL} (max), for all listed outputs combined should not exceed 32mA to satisfy the maximum specified voltage drop. This does not include the IRTX output.

Pin Description

PIN	NAME	FUNCTION
		POWER PINS
15, 29	V_{DD}	**Supply Voltage**
14	REGOUT	**Regulator Capacitor.** This pin must be connected to ground through a 1.0µF external ceramic-chip capacitor. The capacitor must be placed as close to this pin as possible. No other external devices other than the capacitor should be connected to this pin.
13, 22, 30	GND	**Ground**
—	EP (GND)	**Exposed Pad/Ground.** The GND contact is through the exposed paddle located on the underside of the package. It must be directly connected to the ground plane.
		RESET PINS
28	$\overline{RESET}$	**Digital, Active-Low, Reset Input/Output.** The CPU is held in reset when this pin is low and begins executing from the reset vector when released. The pin includes pullup current source and should be driven by an open-drain, external source capable of sinking in excess of 4mA. This pin is driven low as an output when an internal reset condition occurs.
		CLOCK PINS
18	HFXIN	**High-Frequency Crystal Input.** Connect an external crystal or resonator between HFXIN and HFXOUT as the high-frequency system clock. Alternatively, HFXIN is the input for an external, high-frequency clock source when HFXOUT is unconnected.
19	HFXOUT	
		IR FUNCTION PINS
31	IRTX	**IR Transmit Output.** IR transmit pin capable of sinking 25mA. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.
32	IRRX	**IR Receive Input.** IR receive pin. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.
		GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS
1–8	P0.0–P0.7; IRTXM; TBA0, TBA1; TBB0, TBB1; INT8–INT15	**General-Purpose, Digital, I/O, Type-D Port.** These port pins function as bidirectional I/O pins. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance input condition. All alternate functions must be enabled from software. Port 0 can optionally be defined with INT8–INT15.

PIN	PORT	SPECIAL FUNCTION
1	P0.0	IRTXM/INT8
2	P0.1	INT9
3	P0.2	INT10
4	P0.3	INT11
5	P0.4	INT12
6	P0.5	TBA0/TBA1/INT13
7	P0.6	TBB0/INT14
8	P0.7	TBB1/INT15

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Pin Description (continued)

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td rowspan="10">9–12, 16, 17, 20, 21</td><td rowspan="10">P1.0–P1.7; INT0–INT7</td><td colspan="3">General-Purpose, Digital, I/O, Type-D Port; External Edge-Selectable Interrupt. These port pins function as bidirectional I/O pins or as interrupts. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance input condition. All interrupt functions must be enabled from software.</td></tr>
<tr><td>PIN</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>9</td><td>P1.0</td><td>INT0</td></tr>
<tr><td>10</td><td>P1.1</td><td>INT1</td></tr>
<tr><td>11</td><td>P1.2</td><td>INT2</td></tr>
<tr><td>12</td><td>P1.3</td><td>INT3</td></tr>
<tr><td>16</td><td>P1.4</td><td>INT4</td></tr>
<tr><td>17</td><td>P1.5</td><td>INT5</td></tr>
<tr><td>20</td><td>P1.6</td><td>INT6</td></tr>
<tr><td>21</td><td>P1.7</td><td>INT7</td></tr>
<tr><td rowspan="6">24–27</td><td rowspan="6">P2.4–P2.7; TCK, TDI, TMS, TDO</td><td colspan="3">General-Purpose, Digital, I/O, Type-C Port. These port pins function as bidirectional I/O pins. Software must configure these pins after release from reset to remove the high-impedance input condition. All alternate functions must be enabled from software. Enabling the pin’s special function disables the general-purpose I/O on the pin.

The JTAG pins (P2.4–P2.7) default to their JTAG function with weak pullups enabled after a reset. The JTAG function can be disabled using the TAP bit in the SC register.
P2.7 functions as the JTAG test-data output on reset and defaults to an input with a weak pullup. The output function of the test data is only enabled during the TAP’s Shift_IR or Shift_DR states.</td></tr>
<tr><td>PIN</td><td>PORT</td><td>SPECIAL FUNCTION</td></tr>
<tr><td>24</td><td>P2.4</td><td>TCK</td></tr>
<tr><td>25</td><td>P2.5</td><td>TDI</td></tr>
<tr><td>26</td><td>P2.6</td><td>TMS</td></tr>
<tr><td>27</td><td>P2.7</td><td>TDO</td></tr>
<tr><td colspan="3">NO CONNECTION PINS</td></tr>
<tr><td>23</td><td>N.C.</td><td>No Connection</td></tr>
</table>

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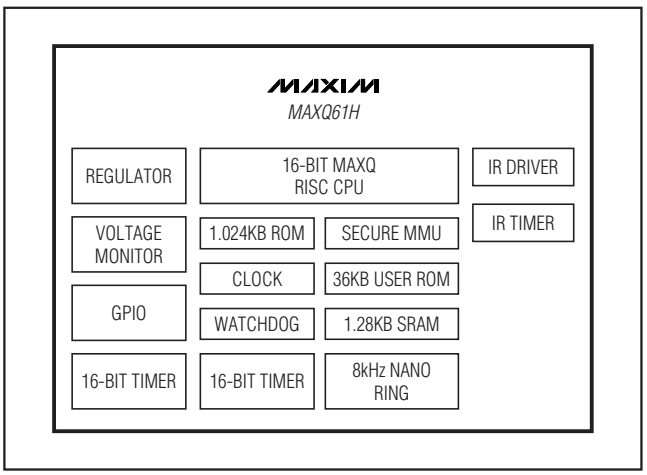
Block Diagram



Detailed Description

The MAXQ61H microcontroller provides integrated, low-cost solutions that simplify the design of IR communications equipment such as universal remote controls. Standard features include the highly optimized, single-cycle, MAXQ 16-bit RISC core, 36KB of user ROM memory, 1.28KB data RAM, a soft stack, 16 general-purpose registers, and three data pointers. The MAXQ core offers the industry's best MIPS/mA rating, allowing developers to achieve the same performance as competing microcontrollers at substantially lower clock rates. Combining reduced active-mode current with the MAXQ61H stop-mode current (0.2µA, typical) results in increased battery life. Application-specific peripherals include flexible timers for generating IR carrier frequencies and modulation, a high-current IR drive pin capable of sinking up to 25mA current, and output pins capable of sinking up to 5mA ideal for IR applications, general-purpose I/O pins ideal for keypad matrix input, and a power-fail-detection circuit to notify the application when the supply voltage is nearing the minimum operating voltage of the microcontroller.

At the heart of the MAXQ61H is the MAXQ 16-bit RISC core. The MAXQ61H operates from DC to 12MHz and almost all instructions execute in a single clock cycle (83.3ns at 12MHz), enabling nearly 12MIPS true code operation. When active device operation is not required, an ultra-low-power stop mode can be invoked from software, resulting in quiescent current consumption of less than 0.2µA (typ) and 2.0µA (max). The combination of high-performance instructions and ultra-low stop-mode current increases battery life over competing microcontrollers. An integrated POR circuit with brownout support resets the device to a known condition following a power-up cycle or brownout condition. Additionally, a power-fail warning flag is set and a power-fail interrupt can be generated when the system voltage falls below the power-fail warning voltage, V_{PFW}. The power-fail warning feature allows the application to notify the user that the system supply is low and appropriate action should be taken.

Microprocessor

The MAXQ61H is based on Maxim's low-power, 16-bit MAXQ family of RISC cores. The core supports the Harvard memory architecture with separate 16-bit program and data address buses. A fixed 16-bit instruction word is standard, but data can be arranged in 8 or 16 bits. The MAXQ core in the MAXQ61H family is implemented as a pipelined processor with performance approaching 1MIPS/MHz. The 16-bit data path is implemented around register modules, and each register module contributes specific functions to the core. The accumulator module consists of sixteen 16-bit registers and is tightly coupled with the arithmetic logic unit (ALU). A configurable soft stack supports program flow.

Execution of instructions is triggered by data transfer between functional register modules or between a functional register module and memory. Because data movement involves only source and destination modules, circuit-switching activities are limited to active modules only. For power-conscious applications, this approach localizes power dissipation and minimizes switching noise. The modular architecture also provides a maximum of flexibility and reusability that is important for a microprocessor used in embedded applications.

The MAXQ instruction set is highly orthogonal. All arithmetical and logical operations can use any register in conjunction with the accumulator. Data movement is supported from any register to any other register. Memory is accessed through specific data-pointer registers with automatic increment/decrement support.

Memory

The MAXQ61H incorporates several memory types that include the following:

- 36KB user ROM
- 1.28KB SRAM data memory
- 1.024KB utility ROM
- Soft stack

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Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and can also be used as general-purpose data storage. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and when an interrupt is serviced. An application can also store values in the stack explicitly by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (BF0h). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Utility ROM

The utility ROM is a 1.024KB block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software. These include the following:

- Test routines (internal memory tests, memory loader, etc.)
- User-callable routines for fast table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of system code, or to one of the special routines mentioned. Routines within the utility ROM are user accessible and can be called as subroutines by the application software. More information on the utility ROM functions is contained in the *MAXQ610 User's Guide*.

Watchdog Timer

An internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or ESD upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog-timer timeout and the watchdog-timer reset. The timeout period can be programmed in a range of 2^{15} to 2^{24} system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog-timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See Table 1.

IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed IR communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

The IR timer is composed of two separate timing entities: a carrier generator and a carrier modulator. The

Table 1. Watchdog Interrupt Timeout (Sysclk = 12MHz, CD[1:0] = 00)

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (µs)
00	Sysclk/2^{15}	2.7ms	42.7
01	Sysclk/2^{18}	21.9ms	42.7
10	Sysclk/2^{21}	174.7ms	42.7
11	Sysclk/2^{24}	1.4s	42.7

carrier generation module uses the 16-bit IR Carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR Modulator Time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

The IR timer is enabled when the IR enable bit (IREN) is set to 1. The IR Value register (IRV) defines the beginning value for the carrier modulator. During transmission, the IRV register is initially loaded with the IRMT value and begins down counting towards 0000h, whereas in receive mode it counts upward from the initial IRV register value. During the receive operation, the IRV register can be configured to reload with 0000h when capture occurs on detection of selected edges or can be allowed to continue free-running throughout the receive operation. An overflow occurs when the IR timer value rolls over from 0FFFFh to 0000h. The IR overflow flag (IROV) is set to 1 and an interrupt is generated if enabled (IRIE = 1).

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

$$\text{IR Input Clock } (f_{IRCLK}) = f_{SYS}/2^{IRDIV[2:0]}$$

$$\text{Carrier Frequency } (f_{CARRIER}) = f_{IRCLK}/(IRCAH + IRCAL + 2)$$

$$\text{Carrier High Time} = IRCAH + 1$$

$$\text{Carrier Low Time} = IRCAL + 1$$

$$\text{Carrier Duty Cycle} = (IRCAH + 1)/(IRCAH + IRCAL + 2)$$

During transmission, the IRCA register is latched for each IRV downcount interval and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV downcount interval so that duty-cycle variation and frequency shifting is possible from one interval to the next, which is illustrated in Figure 1.

Figure 2 illustrates the basic carrier generation and its path to the IRTX output pin. The IR transmit polarity bit (IRTXPOL) defines the starting/idle state and the carrier polarity of the IRTX pin when the IR timer is enabled.

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV downcounter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When IRCFME = 1, the IRV downcounter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If IRTXPOL = 1, the IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a downcounter in transmit mode. An IR transmission starts when 1) the IREN bit is set to 1 when IRMODE = 1, 2) the IRMODE bit is set to 1 when IREN = 1, or 3) when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR timer value reloads its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

1) Reloads IRV with IRMT.
2) Samples IRCA, IRDATA, and IRTXPOL.
3) Generates IRTX accordingly.
4) Sets IRIF to 1.
5) Generates an interrupt to the CPU if enabled (IRIE = 1).

To terminate the current transmission, the user can switch to receive mode (IRMODE = 0) or clear IREN to 0.

$$\text{Carrier Modulation Time} = IRMT + 1 \text{ carrier cycles}$$

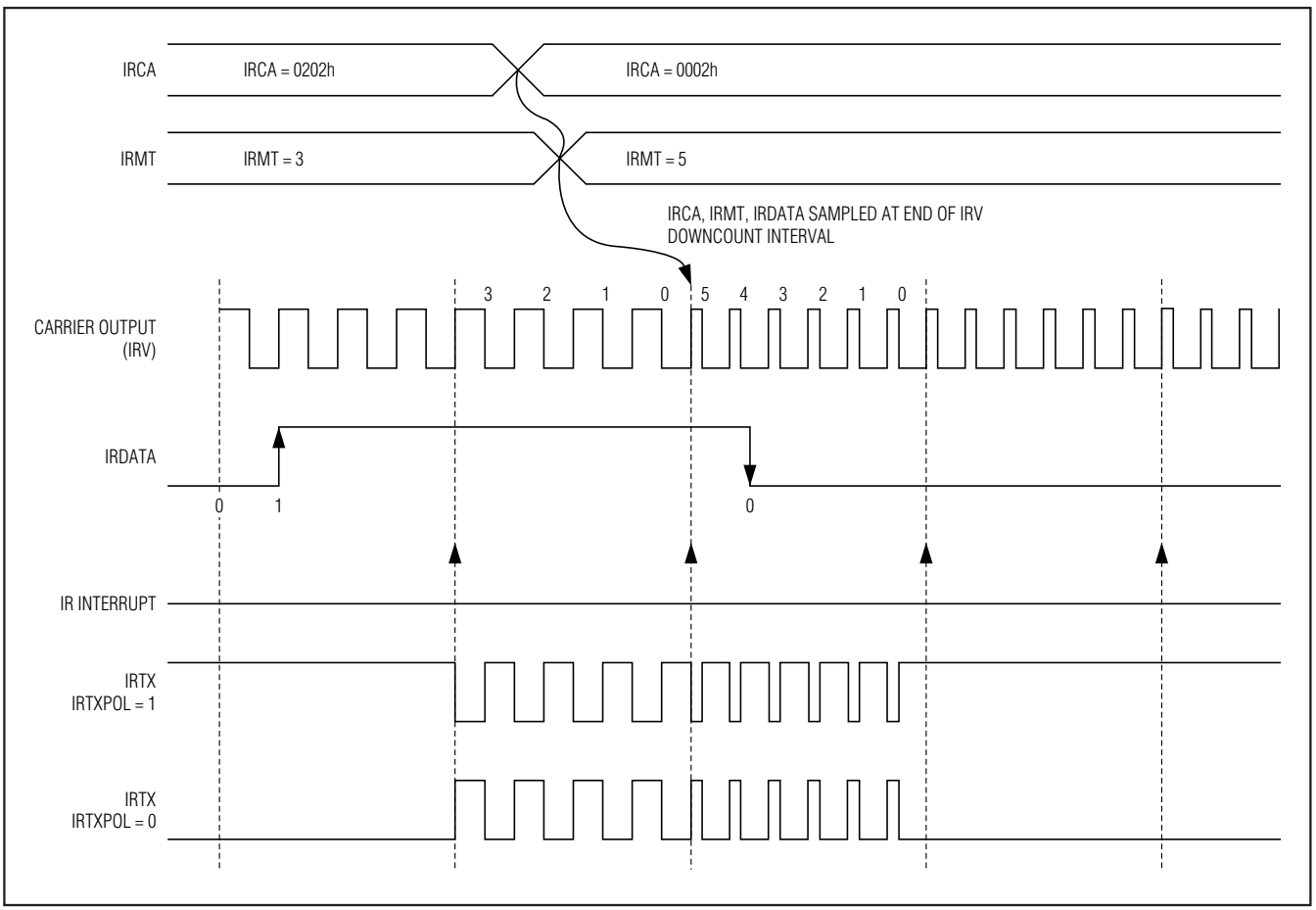


Figure 1. IR Transmit Frequency Shifting Example (IRCFME = 0)

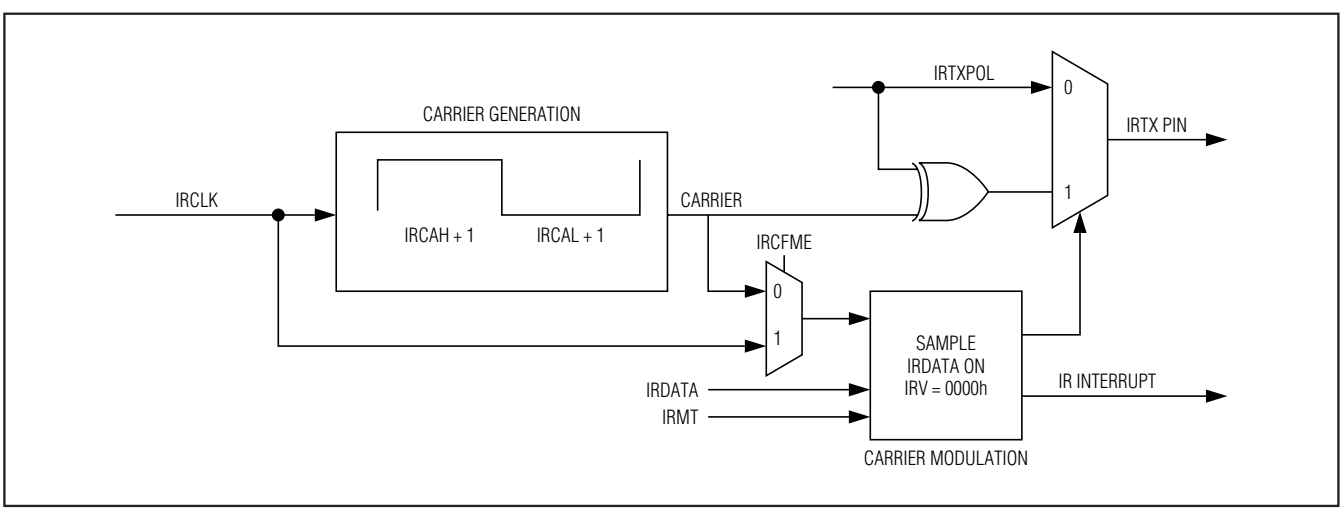


Figure 2. IR Transmit Carrier Generation and Carrier Modulator Control

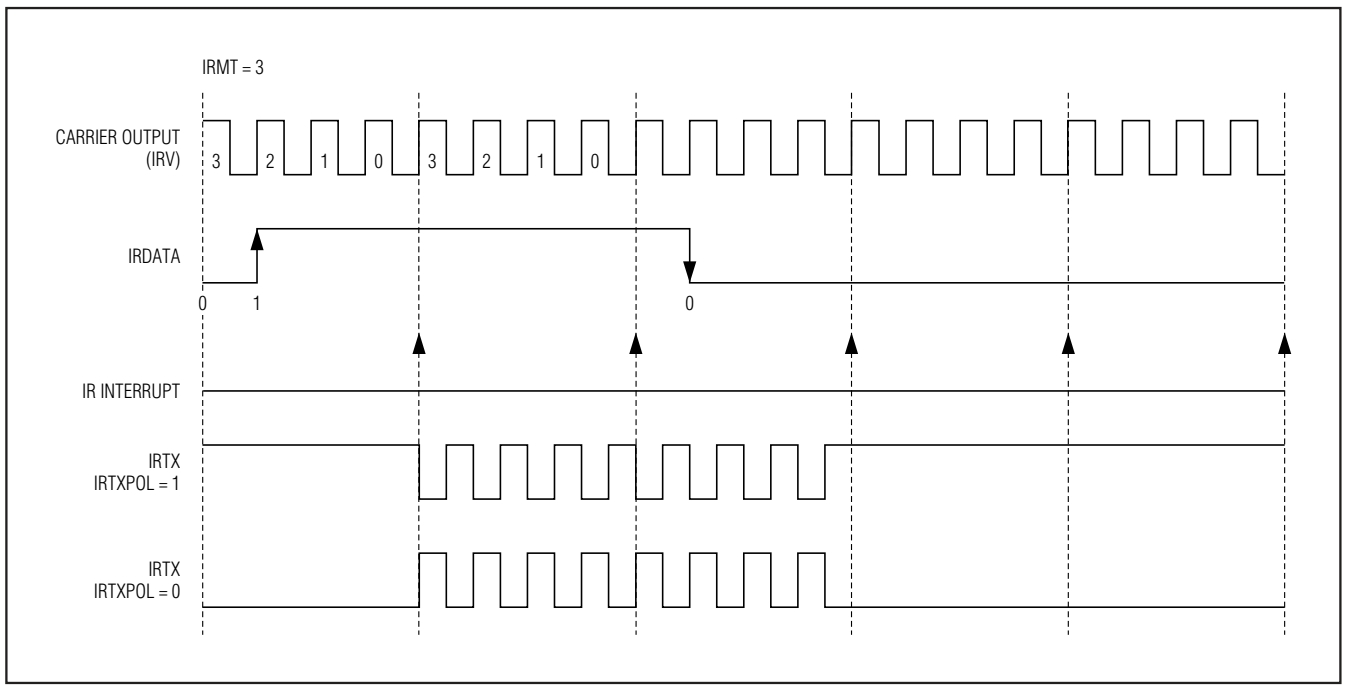


Figure 3. IR Transmission Waveform (IRCFME = 0)

IR Transmit—Independent External Carrier and Modulator Outputs

The normal transmit mode modulates the carrier based upon the IRDATA bit. However, the user has the option to input the modulator (envelope) on an external pin if desired. If the IRENV[1:0] bits are configured to 01b or 10b, the modulator/envelope is output to the IRTXM pin. The IRDATA bit is output directly to the IRTXM pin (if IRTXPOL = 0) on each IRV downcount interval boundary just as if it were being used to internally modulate the carrier frequency. If IRTXPOL = 1, the inverse of the IRDATA bit is output to the IRTXM pin on the IRV interval downcount boundaries. The envelope output is illustrated in Figure 4. When the envelope mode is enabled, it is possible to output either the modulated (IRENV[1:0] = 01b) or unmodulated (IRENV[1:0] = 10b) carrier to the IRTX pin.

IR Receive

When configured in receive mode (IRMODE = 0), the IR hardware supports the IRRX capture function. The IRRXSEL[1:0] bits define which edge(s) of the IRRX pin should trigger IR timer capture function.

The IR module starts operating in the receive mode when IRMODE = 0 and IREN = 1. Once started, the IR timer (IRV) starts up counting from 0000h when a qualified capture event as defined by IRRXSEL happens. The IRV register is, by default, counting carrier cycles as defined by the IRCA register. However, the IR carrier frequency detect (IRCFME) bit can be set to 1 to allow clocking of the IRV register directly with the IRCLK for finer resolution. When IRCFME = 0, the IRCA defined carrier is counted by IRV. When IRCFME = 1, the IRCLK clocks the IRV register.

On the next qualified event, the IR module does the following:

1) Captures the IRRX pin state and transfers its value to IRDATA. If a falling edge occurs, IRDATA = 0. If a rising edge occurs, IRDATA = 1.
2) Transfers its current IRV value to the IRMT.
3) Resets IRV content to 0000h (if IRXRL = 1).
4) Continues counting again until the next qualified event.

If the IR timer value rolls over from 0FFFFh to 0000h before a qualified event happens, the IR timer overflow (IROV) flag is set to 1 and an interrupt generated if enabled. The IR module continues to operate in receive mode until it is stopped by switching into transmit mode (IRMODE = 1) or clearing IREN = 0.

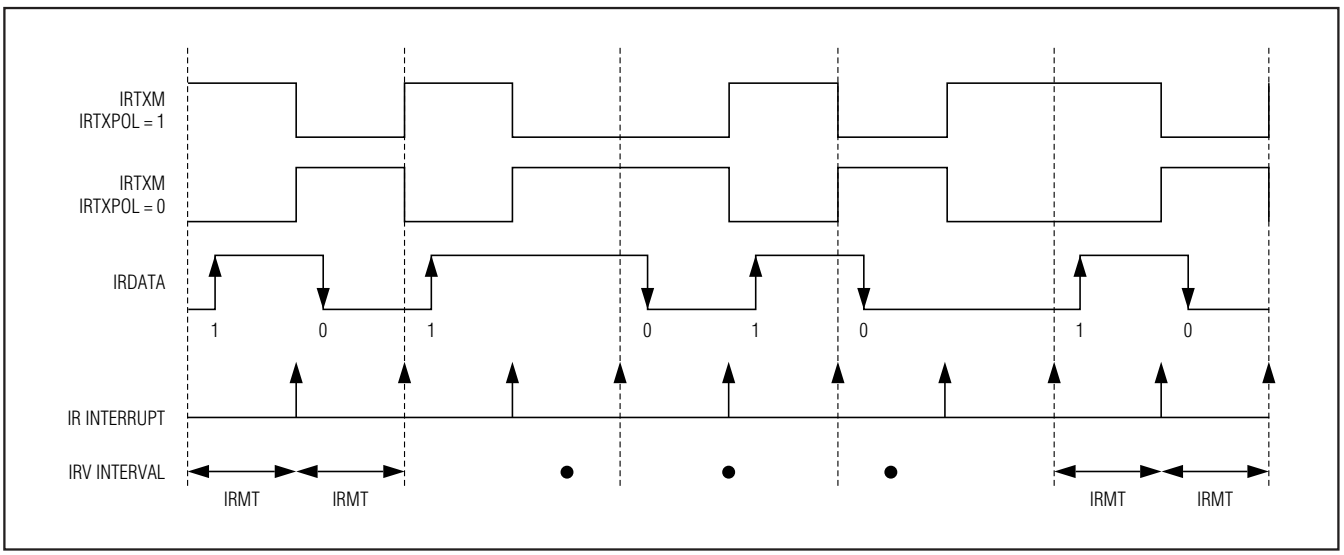


Figure 4. External IRTXM (Modulator) Output

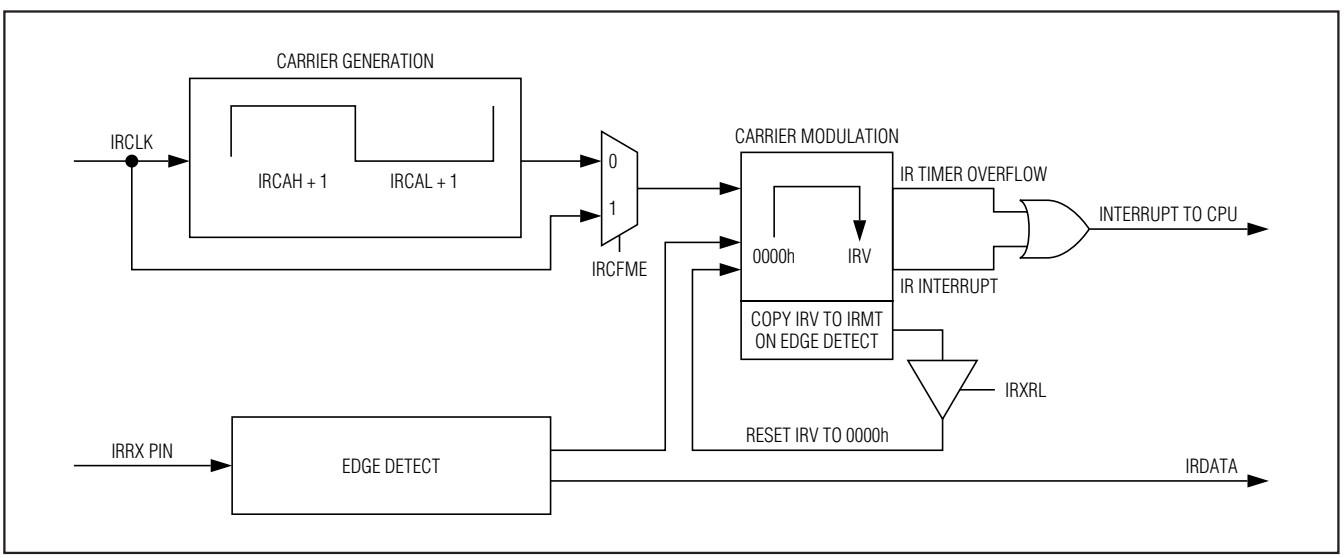
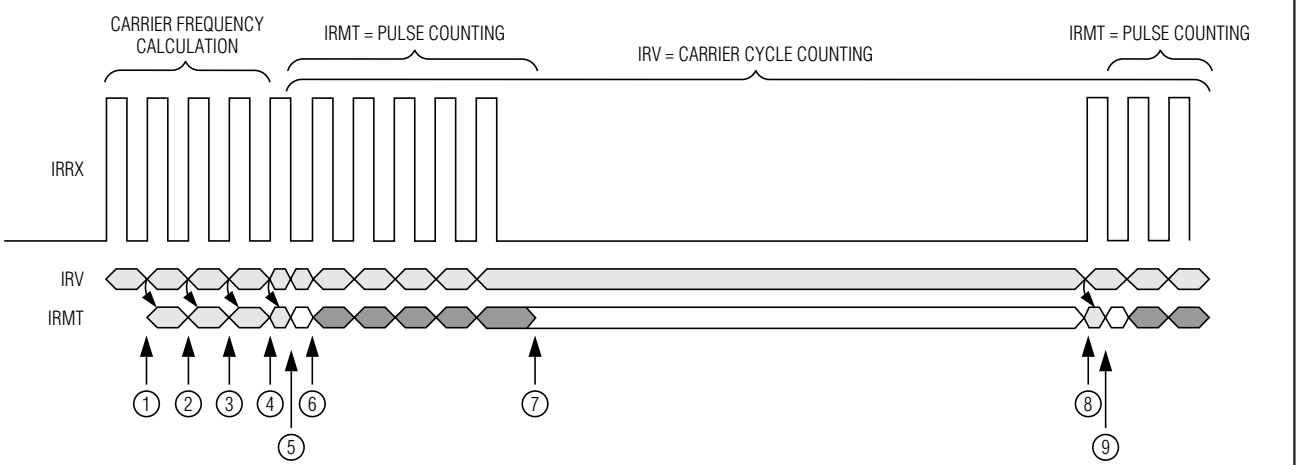


Figure 5. IR Capture

Carrier Burst-Count Mode

A special mode reduces the CPU processing burden when performing IR learning functions. Typically, when operating in an IR learning capacity, some number of carrier cycles are examined for frequency determination. Once the frequency has been determined, the IR receive function can be reduced to counting the number of carrier pulses in the burst and the duration of the combined mark-space time within the burst. To simplify this process, the receive burst-count mode (as enabled by the RXBCNT bit) can be used. When RXBCNT = 0, the standard IR receive capture functionality is in place. When RXBCNT = 1, the IRV capture operation is disabled and the interrupt flag associated with the capture no longer denotes a capture. In the carrier burst-count mode, the IRMT register is now used only to count qualified edges. The IRIF interrupt flag (normally used to signal a capture when RXBCNT = 0) now becomes set if



① TO ④ CAPTURE INTERRUPT (IRIF = 1).
IRV ≥ IRMT.
IRV = 0 (IF IRXRL = 1).

⑤ SOFTWARE SETS IRCA = CARRIER FREQUENCY.
SOFTWARE SETS RXBCNT = 1 (WHICH CLEARS IRMT = 0001 IN HARDWARE).
SOFTWARE CLEARS IRCFME = 0 SO THAT IRV COUNTS CARRIER CYCLES. IRV IS RESET TO 0 ON QUALIFIED EDGE DETECTION IF IRXRL = 1.
SOFTWARE ADDS TO IRMT THE NUMBER OF PULSES USED FOR CARRIER MEASUREMENT.
IRCA x 2x COUNTER FOR SPACE CAN BEGIN IMMEDIATELY (QUALIFIED EDGE RESETS).

⑥ QUALIFIED EDGE DETECTED: IRMT++
IRV RESET TO 0 IF IRXRL = 1.

⑦ IRCA x 2 PERIOD ELAPSES: IRIF = 1; CARRIER ABSENCE = SPACE.
BURST MARK = IRMT PULSES.
SOFTWARE CLEARS RXBCNT = 0 SO THAT WE CAPTURE ON THE NEXT QUALIFIED EDGE.

⑧ QUALIFIED EDGE DETECTED: IRIF = 1, CAPTURE IRV ≥ IRMT AS THE BURST SPACE (PLUS UP TO ONE CARRIER CYCLE).

⑨ SOFTWARE SET RXBCNT = 1 AS IN (5).
CONTINUE (5) TO (8) UNTIL LEARNING SPACE EXCEEDS SOME DURATION. IRV ROLLOVERS CAN BE USED.

Figure 6. Receive Burst-Count Example

ever two IRCA cycles elapse without getting a qualified edge. The IRIF interrupt flag thus denotes absence of the carrier and the beginning of a space in the receive signal. When the RXBCNT bit is changed from 0 to 1, the IRMT register is set to 0001h. The IRCFME bit is still used to define whether the IRV register is counting system IRCLK clocks or IRCA-defined carrier cycles. The IRXRL bit is still used to define whether the IRV register is reloaded with 0000h on detection of a qualified edge (per the IRXSEL[1:0] bits). Figure 6 and the descriptive sequence embedded in the figure illustrate the expected usage of the receive burst-count mode.

16-Bit Timers/Counters

The MAXQ61H provides two timers/counters that support the following functions:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2^n divider (for n = 0, 2, 4, 6, 8, 10)

16-Bit Microcontroller with Infrared Module

General-Purpose I/O

The MAXQ61H provides port pins for general-purpose I/Os that have the following features:

- CMOS output drivers
- Schmitt trigger inputs
- Optional weak pullup to V_{DD} when operating in input mode

While the microcontroller is in a reset state, all port pins become high impedance with weak pullups disabled, unless otherwise noted.

From a software perspective, each port appears as a group of peripheral registers with unique addresses. Special function pins can also be used as general-purpose I/O pins when the special functions are disabled. For a detailed description of the special functions available for each pin, refer to the part-specific user manual. The *MAXQ610 User's Guide* describes all special functions available on the MAXQ61H.

On-Chip Oscillator

An external quartz crystal or a ceramic resonator can be connected between HFXIN and HFXOUT on the MAXQ61H, as illustrated in Figure 7.

Noise at HFXIN and HFXOUT can adversely affect on-chip clock timing. It is good design practice to place the crystal and capacitors near the oscillator circuitry and connect HFXIN and HFXOUT to ground with a direct short trace. The typical values of external capacitors vary with the type of crystal to be used and should be initially selected based on the load capacitance as suggested by the crystal manufacturer.

Operating Modes

The lowest power mode of operation for the MAXQ61H is stop mode. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include external I/O interrupts, the power-fail warning interrupt, or a power-fail reset. Any time the microcontroller is in a state where code does not need to be executed, the user software can put the MAXQ61H into stop mode. The nanopower ring oscillator is an internal ultra-low-power (400nA) 8kHz ring oscillator that can be used to drive a wake-up timer that exits stop mode. The wake-up timer is programmable by software in steps of 125µs up to approximately 8s.

The power-fail monitor is always on during normal operation. However, it can be selectively disabled during stop mode to minimize power consumption. This feature is enabled using the power-fail monitor disable (PFD) bit in the PWCN register. The reset default state for the PFD bit is 1, which disables the power-fail monitor function during stop mode. If power-fail monitoring is disabled (PFD = 1) during stop mode, the circuitry responsible for generating a power-fail warning or reset is shut down and neither condition is detected. Thus, the $V_{DD} < V_{RST}$ condition does not invoke a reset state.

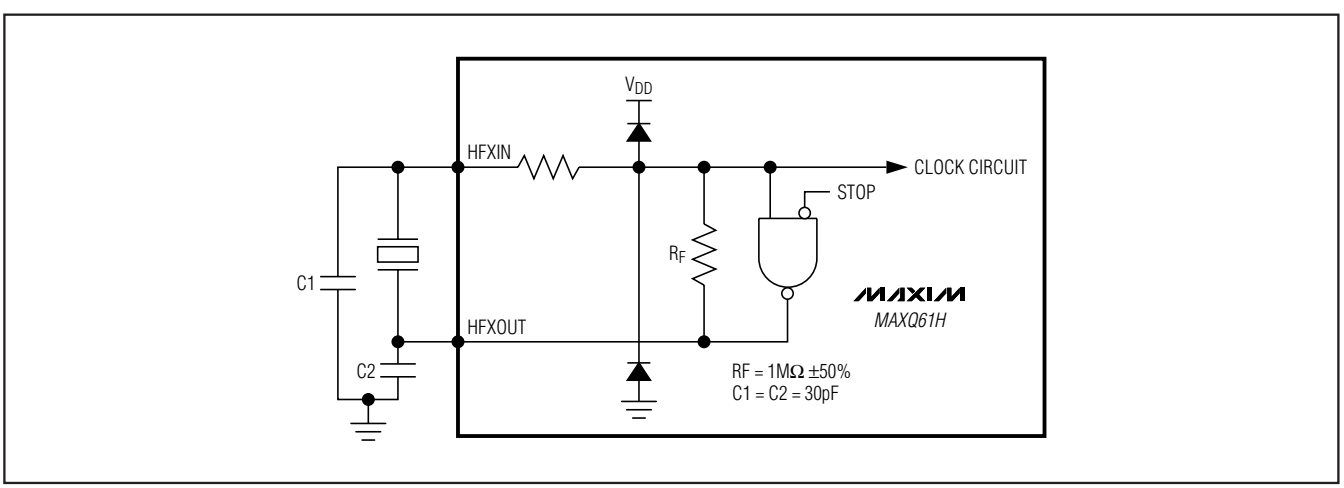


Figure 7. On-Chip Oscillator

However, in the event that V_{DD} falls below the POR level, a POR is generated. The power-fail monitor is enabled prior to stop mode exit and before code execution begins. If a power-fail warning condition ($V_{DD} < V_{PFW}$) is then detected, the power-fail interrupt flag is set on stop mode exit. If a power-fail condition is detected ($V_{DD} < V_{RST}$), the CPU goes into reset.

Power-Fail Detection

Figures 8, 9, and 10 show the power-fail detection and response during normal and stop mode operation.

If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2^{11} nanopower ring oscillator clocks (~256ms)
- 2^{12} nanopower ring oscillator clocks (~512ms)
- 2^{13} nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two nanopower ring oscillator cycles. If $V_{DD} > V_{RST}$ during detection, V_{DD} is monitored for an additional nanopower ring oscillator period. If V_{DD} remains above V_{RST} for the third nanopower ring period, the CPU exits the reset state and resumes normal operation from utility ROM at 8000h after satisfying the crystal warmup period.

If a reset is generated by any other event, such as the $\overline{\text{RESET}}$ pin being driven low externally or the watchdog timer, the power-fail, internal regulator, and crystal remain on during the CPU reset. In these cases, the CPU exits the reset state in less than 20 external clock cycles after the reset source is removed.

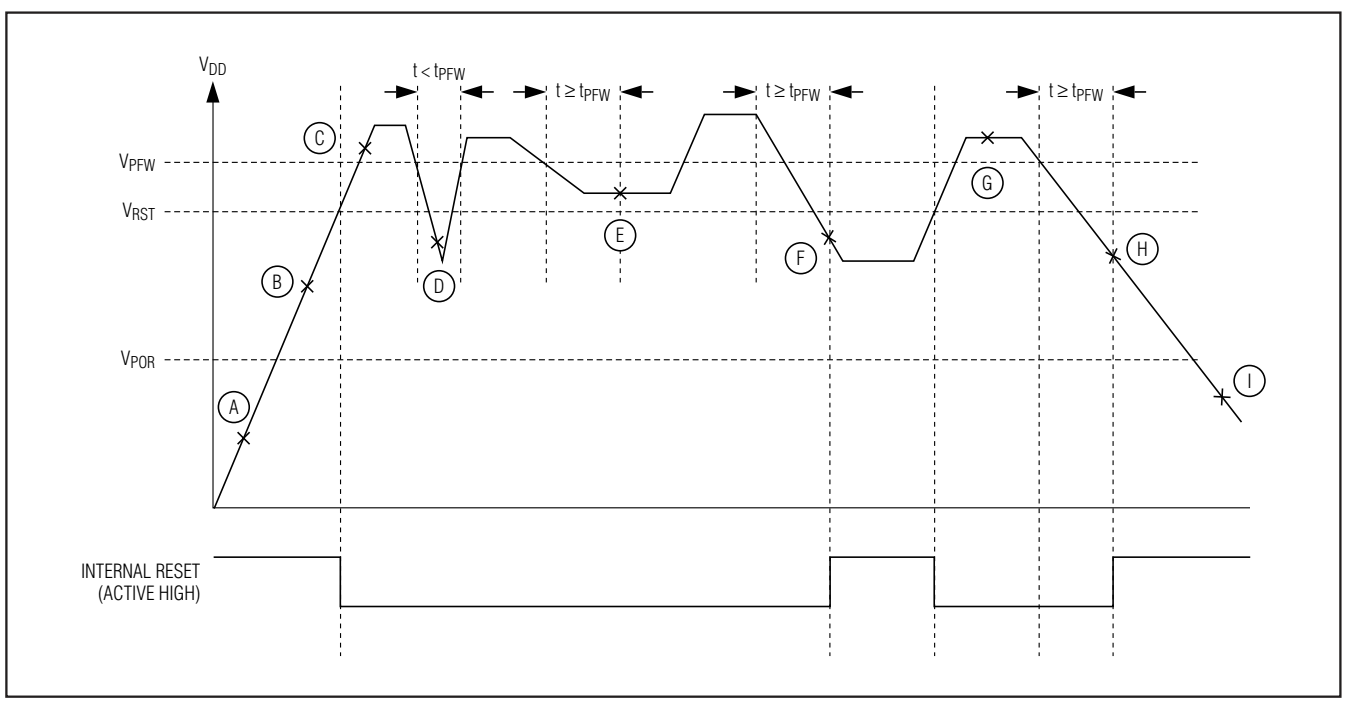


Figure 8. Power-Fail Detection During Normal Operation

Table 2. Power-Fail Detection States During Normal Operation

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	—	$V_{DD} < V_{POR}$.
B	On	On	On	—	$V_{POR} < V_{DD} < V_{RST}$. Crystal warmup time, t_{XTAL_RDY}. CPU held in reset.
C	On	On	On	—	$V_{DD} > V_{RST}$. CPU normal operation.
D	On	On	On	—	Power drop too short. Power-fail not detected.
E	On	On	On	—	$V_{RST} < V_{DD} < V_{PFW}$. PFI is set when $V_{RST} < V_{DD} < V_{PFW}$ and maintains this state for at least t_{PFW}, at which time a power-fail interrupt is generated (if enabled). CPU continues normal operation.
F	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
G	On	On	On	—	$V_{DD} > V_{RST}$. Crystal warmup time, t_{XTAL_RDY}. CPU resumes normal operation from 8000h.
H	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor is turned on periodically.
I	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

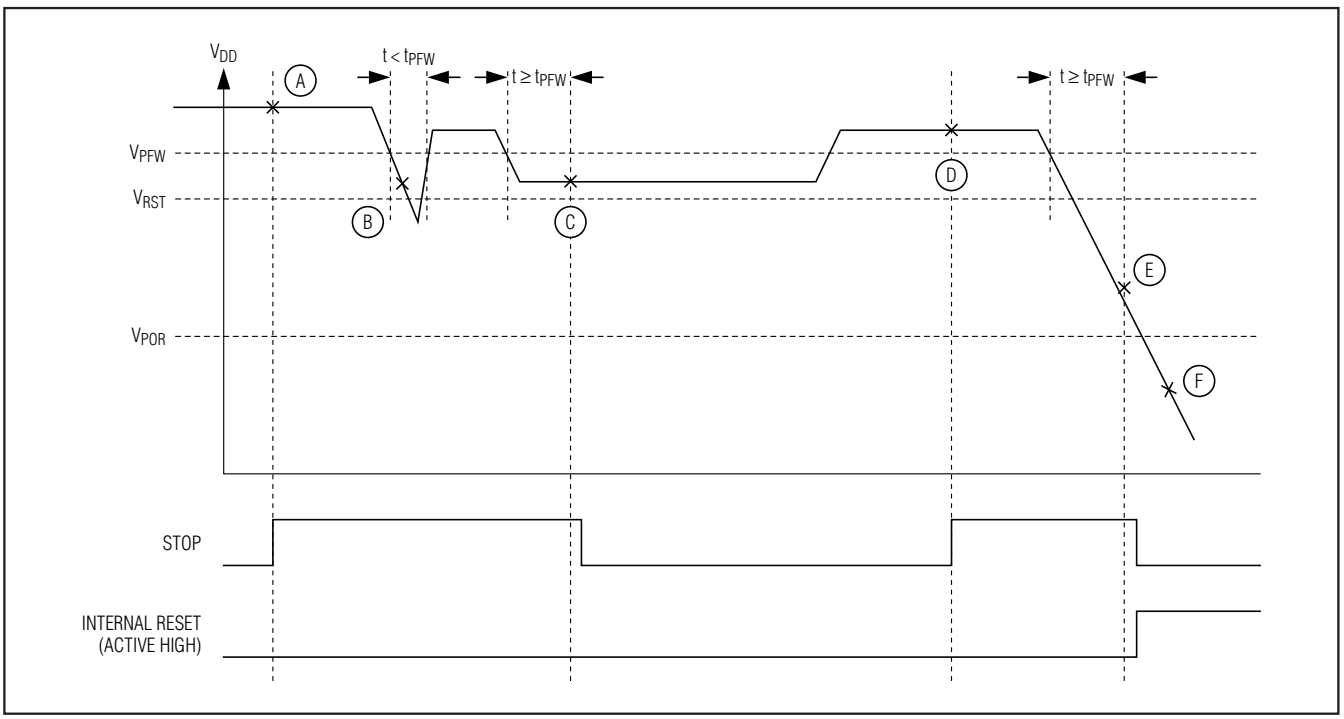


Figure 9. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 3. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

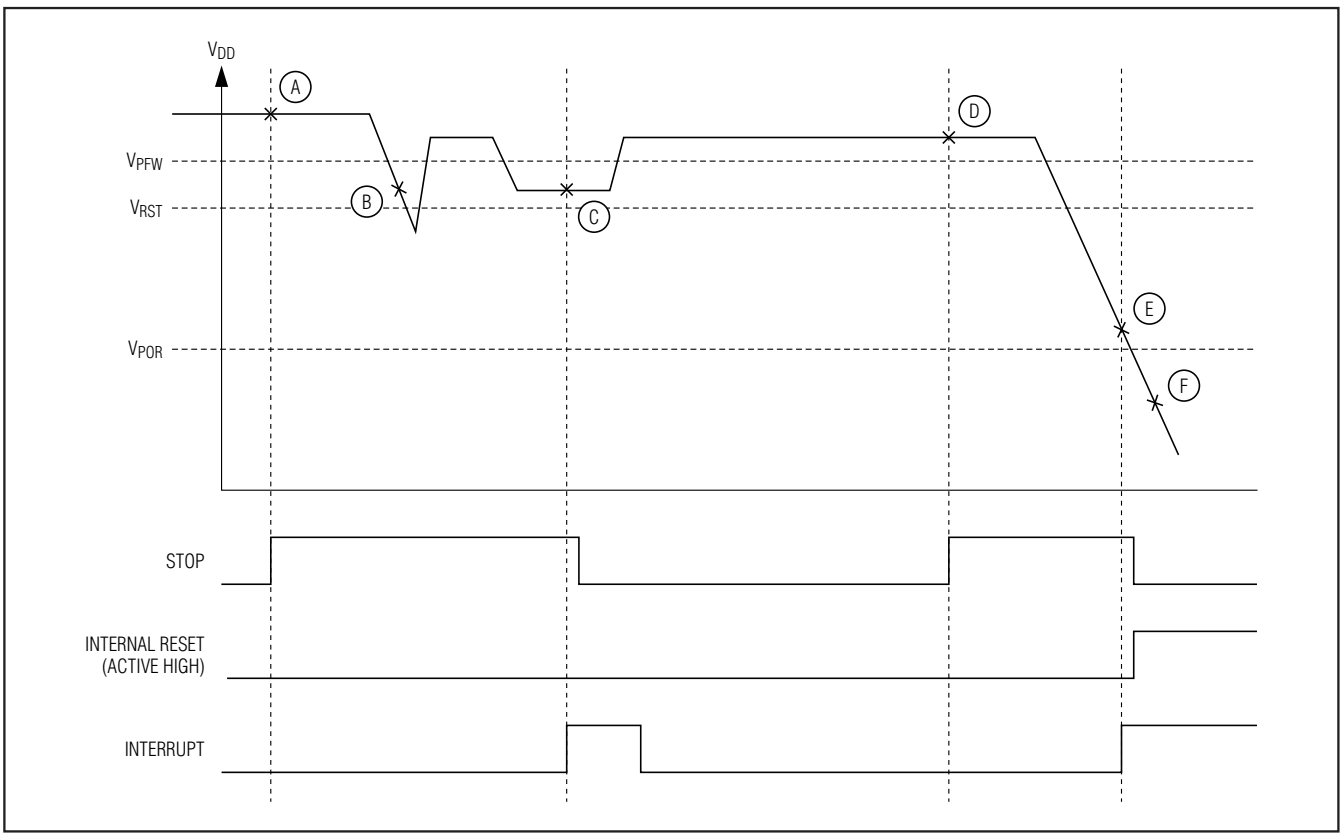


Figure 10. Stop Mode Power-Fail Detection with Power-Fail Monitor Disabled

Table 4. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

Table 4. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled (continued)

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
D	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail, puts CPU in reset. Power-fail monitor is turned on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

Applications Information

The low-power, high-performance RISC architecture of this device makes it an excellent fit for many portable or battery-powered applications. It is ideally suited for applications such as universal remote controls that require the cost-effective integration of IR transmit/receive capability.

Grounds and Bypassing

Careful PCB layout significantly minimizes system-level digital noise that could interact with the microcontroller or peripheral components. The use of multilayer boards is essential to allow the use of dedicated power planes. The area under any digital components should be a continuous ground plane if possible. Keep any bypass capacitor leads short for best noise rejection and place the capacitors as close to the leads of the devices as possible.

CMOS design guidelines for any semiconductor require that no pin be taken above V_{DD} or below GND. Violation of this guideline can result in a hard failure (damage to the silicon inside the device) or a soft failure (unintentional modification of memory contents). Voltage spikes above or below the device's absolute maximum ratings can potentially cause a devastating IC latchup.

Microcontrollers commonly experience negative voltage spikes through either their power pins or general-purpose I/O pins. Negative voltage spikes on power pins are especially problematic as they directly couple to the internal power buses. Devices such as keypads can conduct electrostatic discharges directly into the microcontroller and seriously damage the device. System designers must protect components against these transients that can corrupt system memory.

Additional Documentation

Designers must have the following documents to fully use all the features of this device. This data sheet contains pin descriptions, feature overviews, and electrical specifications. Errata sheets contain deviations from published specifications. The user's guides offer detailed information about device features and operation. The following documents can be downloaded from **www.maxim-ic.com/microcontrollers**.

- This MAXQ61H data sheet, which contains electrical/timing specifications and pin descriptions.
- The MAXQ61H revision-specific errata sheet (**www.maxim-ic.com/errata**).
- The *MAXQ610 User's Guide*, which contains detailed information on core features and operation, including programming.

16-Bit Microcontroller with Infrared Module

Development and Technical Support

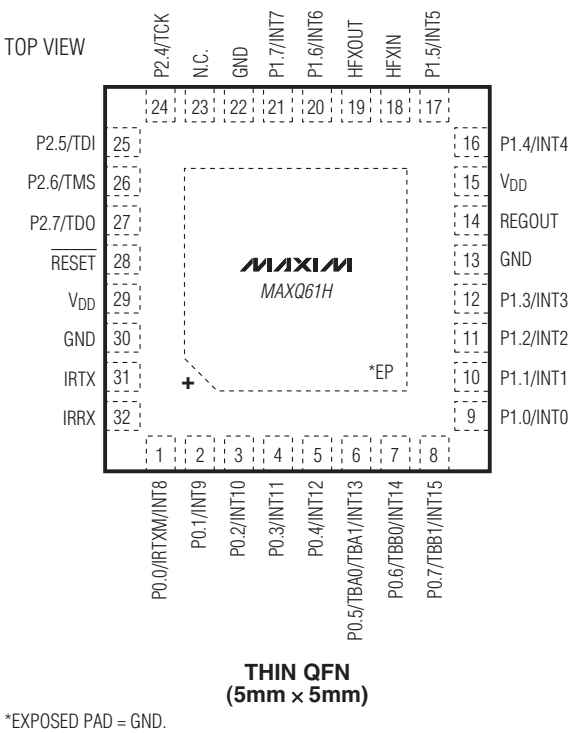
Maxim and third-party suppliers provide a variety of highly versatile, affordably priced development tools for this microcontroller, including the following:

- Compilers
- Integrated Development Environments (IDEs)
- JTAG-to-serial converters for programming and debugging

A partial list of development tool vendors can be found at **www.maxim-ic.com/MAXQ_tools**.

Technical support is available at **https://support.maxim-ic.com/micro**.

Pin Configuration



THIN QFN
(5mm × 5mm)

*EXPOSED PAD = GND.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3255+3	21-0140	90-0001

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/09	Initial release	—
1	7/09	Changed the DATA MEMORY from 2KB to 1.28KB in the *Ordering Information/Selector Guide* table	1
		Moved the stop-mode current value from the MIN to the TYP column in the *Recommended DC Operating Conditions* table	4
		Changed t_{IRRX_A} from 200ns (min) to 300ns (min) in the *Recommended DC Operating Conditions* table	5
2	5/10	Added the lead and soldering temperatures to the *Absolute Maximum Ratings* section; corrected the pinout in the *Pin Description* and *Pin Configuration*	4, 7, 8, 22
3	3/12	Removed the resistor requirement from REGOUT pin description in the *Pin Description* table; corrected the stack starting location in the *Stack Memory* section; changed IRDIV[1:0] to IRDIV[2:0] in the *Carrier Generation Module* section	7, 10, 11