S-8265C Series

BATTERY PROTECTION IC WITH CELL BALANCING FUNCTION FOR 3-SERIAL TO 5-SERIAL CELL PACK (SECONDARY PROTECTION)

www.ablic.com

Rev.1.5_00

The S-8265C Series is a secondary protection IC with cell balancing function for lithium-ion rechargeable batteries, which includes high-accuracy voltage detection circuits, delay circuits, and FETs for cell balancing discharge. The cell balancing function is effective for balancing the voltage of serially connected batteries. Short-circuiting between cells enables cell balancing for serial connection of three cells to five cells.

■ Features

- High-accuracy voltage detection circuit for each cell
  - Cell balancing detection voltage n (n = 1 to 5):
    - 2.700 V to 4.650 V (5 mV step) — Accuracy ±20 mV (Ta = +25°C); Accuracy ±25 mV (Ta = −10°C to +60°C)
  - Cell balancing release voltage n (n = 1 to 5)[*1]:
    - 2.700 V to 4.650 V — Accuracy ±50 mV (Ta = +25°C)
  - Overcharge detection voltage n (n = 1 to 5)[*2]:
    - 2.750 V to 4.700 V (5 mV step) — Accuracy ±20 mV (Ta = +25°C); Accuracy ±25 mV (Ta = −10°C to +60°C)
  - Overcharge release voltage n (n = 1 to 5)[*3, *4]:
    - 2.750 V to 4.700 V — Accuracy ±50 mV (Ta = +25°C)
- Built-in cell balancing discharging FET for each cell
- Output form: CMOS output, Nch open-drain output
- Output logic: Active "H", active "L"
- Built-in test mode function to check cell balancing detection voltage and overcharge detection voltage with shortened delay time
- High-withstand voltage: Absolute maximum rating 28 V
- Wide operation voltage range: 3.6 V to 26 V
- Wide operation temperature range: Ta = −40°C to +85°C
- Low current consumption
  - During operation: 0.3 µA typ., 0.7 µA max. (Ta = +25°C)
- Lead-free (Sn 100%), halogen-free

***1.** Cell balancing release voltage = Cell balancing detection voltage + Cell balancing hysteresis voltage
(Cell balancing hysteresis voltage can be selected from a range of 0 mV to −400 mV in 50 mV step.)

***2.** Satisfy Overcharge detection voltage ≥ Cell balancing detection voltage + 50 mV when selecting them.

***3.** Overcharge release voltage = Overcharge detection voltage + Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected from a range of 0 mV to −400 mV in 50 mV step.)

***4.** Satisfy Overcharge release voltage ≥ Cell balancing release voltage + 50 mV when selecting them.

■ Application

- Lithium-ion rechargeable battery pack

■ Packages

- TMSOP-8
- SNT-8A

■ Block Diagram

1. CMOS output product

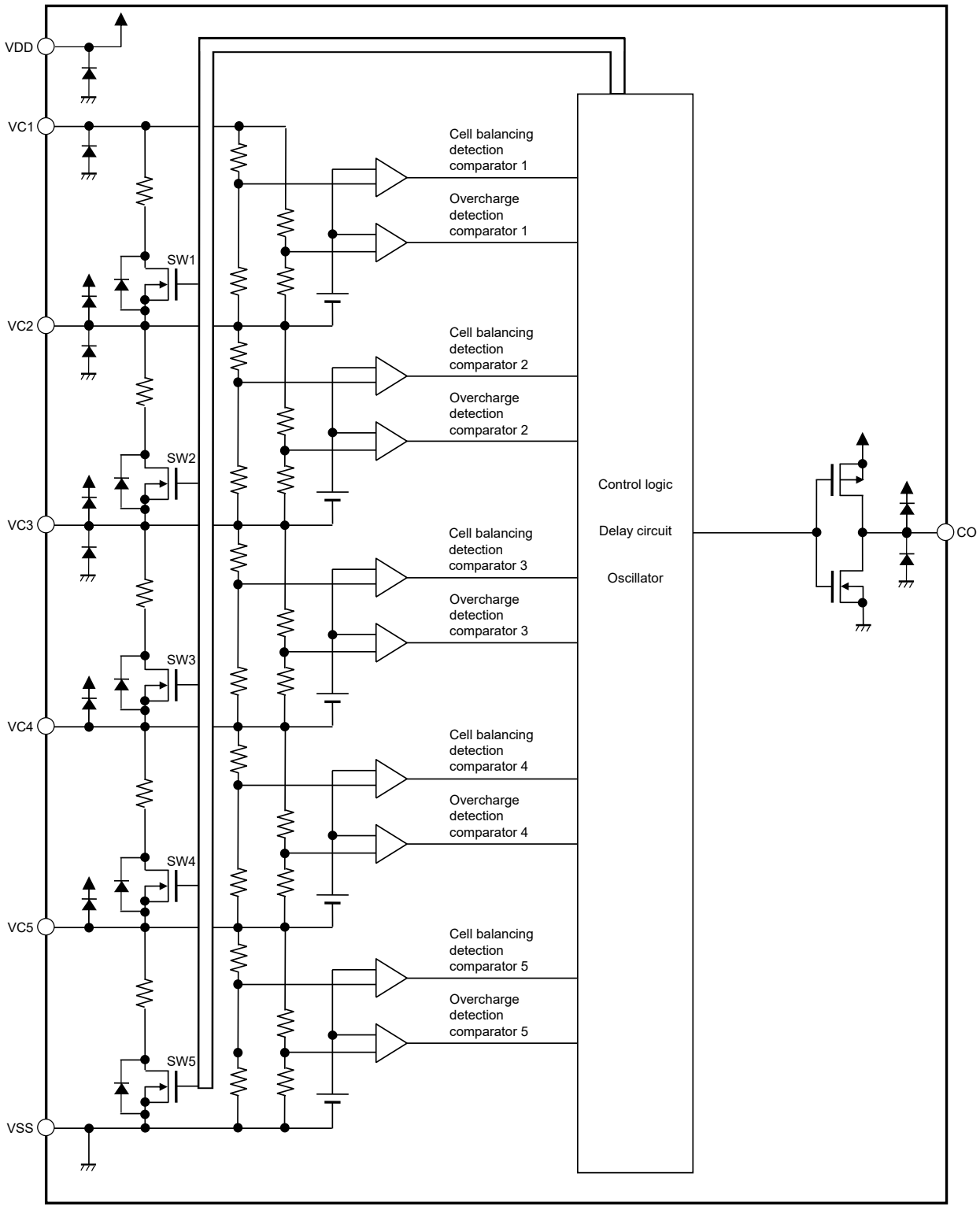


Figure 1

Remark The diodes in the figure are parasitic diodes.

2. Nch open-drain output product

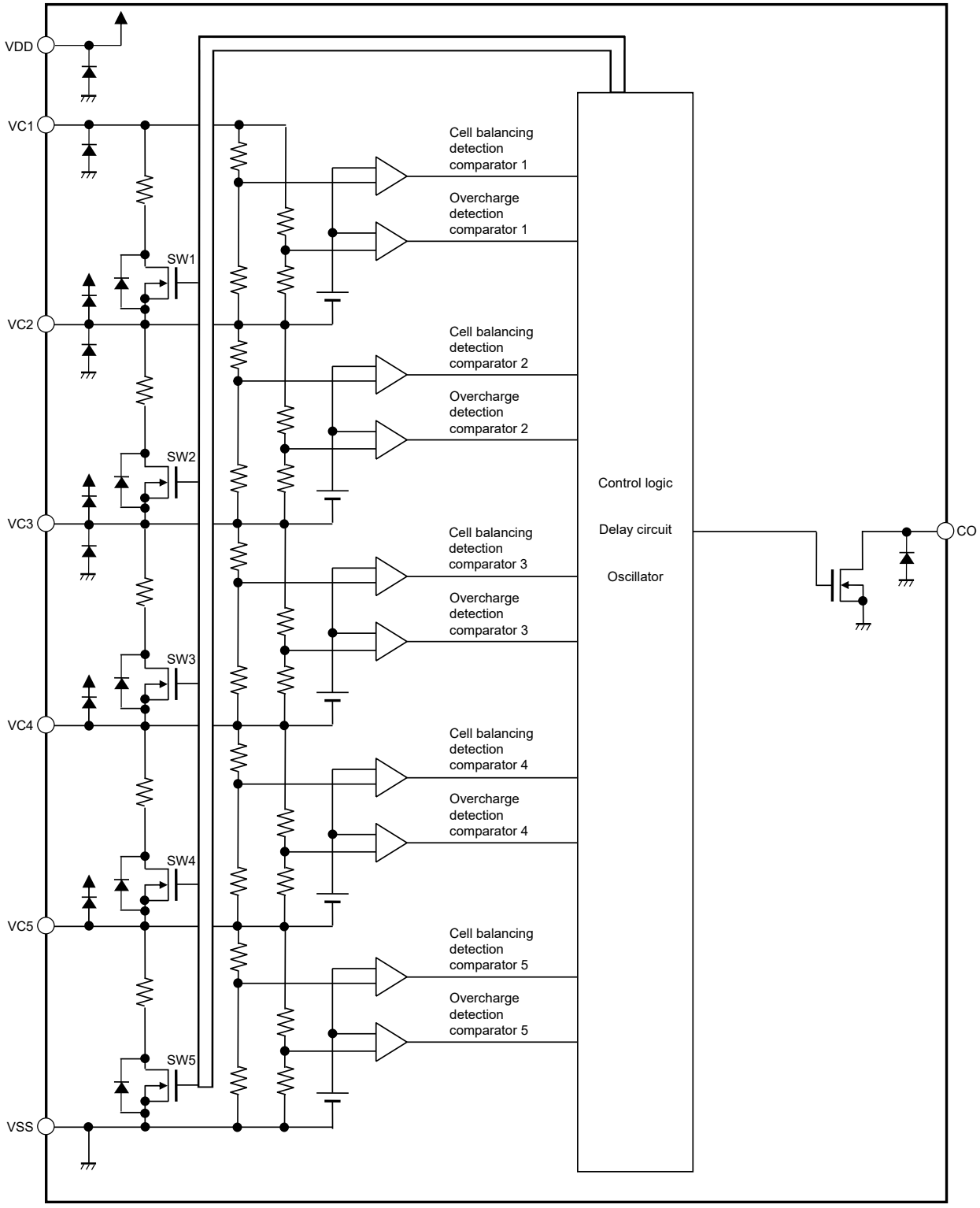


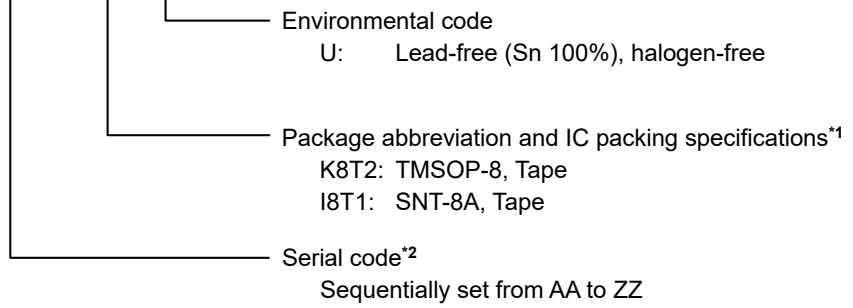
Figure 2

Remark The diodes in the figure are parasitic diodes.

■ Product Name Structure

1. Product name

S-8265C xx - xxxx U 7



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
TMSOP-8	FM008-A-P-SD	FM008-A-C-SD	FM008-A-R-SD	–
SNT-8A	PH008-A-P-SD	PH008-A-C-SD	PH008-A-R-SD	PH008-A-L-SD

3. Product name list

3. 1 TMSOP-8

Table 2

Product Name	Cell Balancing Detection Voltage [V_{BU}]	Cell Balancing Release Voltage [V_{BL}]	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Output Form	Output Logic
S-8265CAA-K8T2U7	4.145 V	4.145 V	4.275 V	4.275 V	CMOS output	Active "H"
S-8265CAB-K8T2U7	3.900 V	3.850 V	4.130 V	3.880 V	Nch open-drain output	Active "L"
S-8265CAC-K8T2U7	4.200 V	4.150 V	4.250 V	4.200 V	Nch open-drain output	Active "L"

Remark Please contact our sales representatives for products other than the above.

3. 2 SNT-8A

Table 3

Product Name	Cell Balancing Detection Voltage [V_{BU}]	Cell Balancing Release Voltage [V_{BL}]	Overcharge Detection Voltage [V_{CU}]	Overcharge Release Voltage [V_{CL}]	Output Form	Output Logic
S-8265CAA-I8T1U7	4.145 V	4.145 V	4.275 V	4.275 V	CMOS output	Active "H"

Remark Please contact our sales representatives for products other than the above.

■ Pin Configurations

1. TMSOP-8

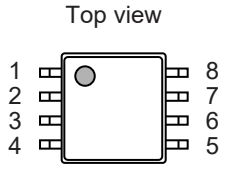


Figure 3

Table 4

Pin No.	Symbol	Description
1	VDD	Input pin for positive power supply
2	VC1	Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1, Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2, Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3, Positive voltage connection pin of battery 4
6	VC5	Negative voltage connection pin of battery 4, Positive voltage connection pin of battery 5
7	VSS	Input pin for negative power supply, Negative voltage connection pin of battery 5
8	CO	Overcharge detection output pin

2. SNT-8A

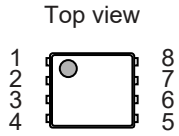


Figure 4

Table 5

Pin No.	Symbol	Description
1	VDD	Input pin for positive power supply
2	VC1	Positive voltage connection pin of battery 1
3	VC2	Negative voltage connection pin of battery 1, Positive voltage connection pin of battery 2
4	VC3	Negative voltage connection pin of battery 2, Positive voltage connection pin of battery 3
5	VC4	Negative voltage connection pin of battery 3, Positive voltage connection pin of battery 4
6	VC5	Negative voltage connection pin of battery 4, Positive voltage connection pin of battery 5
7	VSS	Input pin for negative power supply, Negative voltage connection pin of battery 5
8	CO	Overcharge detection output pin

■ Absolute Maximum Ratings

Table 6

(Ta = +25°C unless otherwise specified)

Item		Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin		V_{DS}	VDD	V_{SS} – 0.3 to V_{SS} + 28, VC1 – 0.3 to VC1 + 5.6	V
Input pin voltage		V_{IN}	VC1	VC2 – 0.3 to VC2 + 5.6	V
			VC2	VC3 – 0.3 to VC3 + 5.6	V
			VC3	VC4 – 0.3 to VC4 + 5.6	V
			VC4	VC5 – 0.3 to VC5 + 5.6	V
			VC5	V_{SS} – 0.3 to V_{SS} + 5.6	V
CO pin output voltage	CMOS output product	V_{CO}	CO	V_{SS} – 0.3 to V_{DD} + 0.3	V
	Nch open-drain output product			V_{SS} – 0.3 to V_{SS} + 28	V
Operation ambient temperature		T_{opr}	–	–40 to +85	°C
Storage temperature		T_{stg}	–	–40 to +125	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TMSOP-8	Board A	–	160	–	°C/W
			Board B	–	133	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		SNT-8A	Board A	–	211	–	°C/W
			Board B	–	173	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

■ Electrical Characteristics

Table 8

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection voltage							
Cell balancing detection voltage n (n = 1, 2, 3, 4, 5)	V_{BUn}	Ta = +25°C	V_{BU} − 0.020	V_{BU}	V_{BU} + 0.020	V	1
		Ta = −10°C to +60°C*1	V_{BU} − 0.025	V_{BU}	V_{BU} + 0.025	V	1
Cell balancing release voltage n (n = 1, 2, 3, 4, 5)	V_{BLn}	−	V_{BL} − 0.050	V_{BL}	V_{BL} + 0.050	V	1
Overcharge detection voltage n (n = 1, 2, 3, 4, 5)	V_{CUn}	Ta = +25°C	V_{CU} − 0.020	V_{CU}	V_{CU} + 0.020	V	1
		Ta = −10°C to +60°C*1	V_{CU} − 0.025	V_{CU}	V_{CU} + 0.025	V	1
Overcharge release voltage n (n = 1, 2, 3, 4, 5)	V_{CLn}	−	V_{CL} − 0.050	V_{CL}	V_{CL} + 0.050	V	1
Input voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	−	3.6	−	26	V	−
Input current							
Current consumption during operation	I_{OPE}	V1 = V2 = V3 = V4 = V5 = V_{BU} × 0.75 V	−	0.3	0.7	μA	2
Current consumption during overdischarge	I_{OPED}	V1 = V2 = V3 = V4 = V5 = V_{BU} × 0.4 V	−	0.05	0.30	μA	2
VC1 pin input current	I_{VC1}	V1 = V2 = V3 = V4 = V5 = V_{BU} × 0.75 V	−	−	0.3	μA	3
VCn pin input current (n = 2, 3, 4, 5)	I_{VCn}	V1 = V2 = V3 = V4 = V5 = V_{BU} × 0.75 V	−0.3	0.0	0.3	μA	3
Output current							
CO pin source current	I_{COH}	−	−	−	−20	μA	4
CO pin sink current	I_{COL}	CMOS output product	0.4	−	−	mA	4
CO pin leakage current	I_{COLL}	Nch open-drain output product	−	−	0.1	μA	4
Delay time							
Cell balancing detection delay time	t_{BU}	−	200	256	310	ms	−
Overcharge detection delay time	t_{CU}	−	200	256	310	ms	−
Overcharge timer reset delay time	t_{TR}	−	6	12	20	ms	−
Cell balancing ON time	t_{CBON}	−	5.7	7.2	8.7	s	−
Cell balancing OFF time	t_{CBOFF}	−	0.8	1.0	1.2	s	−
Transition time to test mode	t_{TST}	−	−	−	10	ms	1
Internal resistance							
Resistance between pins during cell balancing discharge 1	R_{VC1}	V_{BL} < 3.8V	0.15	0.35	0.55	kΩ	5
		V_{BL} ≥ 3.8V	0.15	0.30	0.45	kΩ	5
Resistance between pins during cell balancing discharge n (n = 2, 3, 4, 5)	R_{VCn}	V_{BL} < 3.8V	0.20	0.35	0.55	kΩ	5
		V_{BL} ≥ 3.8V	0.20	0.30	0.45	kΩ	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

S-8265C Series transitions to the test mode when V0 is increased up to 4 V and the conditions continue for 10 ms or longer after setting V0 = 0 V, V1 to V5 = 2.6 V.

1. Detection voltage (Test circuit 1)

1. 1 Cell balancing detection voltage n (V_{BUn}), cell balancing release voltage n (V_{BLn})

After transitioning to the test mode and then setting V0 = 4 V, V1 to V5 = V_{BU} – 0.05 V, V1 is gradually increased. When the CO pin output inverts, the voltage V1 is defined as V_{BU1}.
V0 is then returned to 0 V. After setting V1 = V_{BU} + 0.05 V, V2 to V5 = V_{BL} – 0.05 V, V1 is gradually decreased. When the CO pin output inverts again, the voltage V1 is defined as V_{BL1}.
V_{BUn} and V_{BLn} (n = 2 to 5) can be defined in the same way as when n =1.

1. 2 Overcharge detection voltage n (V_{CUn}), overcharge release voltage n (V_{CLn})

After transitioning to the test mode and then setting V0 = 0 V, V1 to V5 = V_{CU} – 0.05 V, V1 is gradually increased. When the CO pin output inverts, the voltage V1 is defined as V_{CU1}.
V0 is then returned to 0 V. After setting V1 = V_{CU} + 0.05 V, V2 to V5 = V_{CL} – 0.05 V, V1 is gradually decreased. When the CO pin output inverts again, the voltage V1 is defined as V_{CL1}.
V_{CUn} and V_{CLn} (n = 2 to 5) can be defined in the same way as when n = 1.

2. Output current (Test circuit 4)

2. 1 CMOS output product

SW6 and SW7 are set to OFF.

2. 1. 1 Active "H"

(1) CO pin source current (I_{COH})
After transitioning to the test mode and then setting V0 = 0 V, V1 = 4.8 V, V2 to V5 = 2.05 V and V6 = 0.5 V, SW6 is turned on. I6 is then defined as I_{COH}.

(2) CO pin sink current (I_{COL})
After setting V0 = 0 V, V1 to V5 = 2.6 V and V7 = 0.5 V, SW7 is turned on. I7 is then defined as I_{COL}.

2. 1. 2 Active "L"

(1) CO pin source current (I_{COH})
After setting V0 = 0 V, V1 to V5 = 2.6 V and V6 = 0.5 V, SW6 is turned on. I6 is then defined as I_{COH}.

(2) CO pin sink current (I_{COL})
After transitioning to the test mode and then setting V0 = 0 V, V1 = 4.8 V, V2 to V5 = 2.05 V and V7 = 0.5 V, SW7 is turned on. I7 is then defined as I_{COL}.

2. 2 Nch open-drain output product

SW6 and SW7 are set to OFF.

2. 2. 1 Active "H"

(1) CO pin leakage current "L" (I_{COLL})

After transitioning to the test mode and then setting V0 = 0 V, V1 = 4.8 V, V2 to V5 = 2.05 V and V7 = 28 V, SW7 is turned on. I7 is then defined as I_{COLL}.

(2) CO pin sink current (I_{COL})

After setting V0 = 0 V, V1 to V5 = 2.6 V and V7 = 0.5 V, SW7 is turned on. I7 is then defined as I_{COL}.

2. 2. 2 Active "L"

(1) CO pin leakage current "L" (I_{COLL})

After setting V0 = 0 V, V1 to V5 = 2.6 V, V7 = 28 V, SW7 is turned on. I7 is then defined as I_{COLL}.

(2) CO pin sink current (I_{COL})

After transitioning to the test mode and then setting V0 = 0 V, V1 = 4.8 V, V2 to V5 = 2.05 V and V7 = 0.5 V, SW7 is turned on. I7 is then defined as I_{COL}.

3. Transition time to test mode (t_{TST}) (Test circuit 1)

After setting V0 = 0 V, V1 to V5 = 2.6 V, V0 is increased to 4.0 V and decreased to 0 V again.
When the time interval from when V0 is increased until it is decreased is long, if V1 is then increased to 4.8 V, the CO pin output inverts within 40 ms. However, when the time interval from when V0 is increased until it is decreased is short, if V1 is then increased to 4.8 V, it takes more than 40 ms for the CO pin output to invert. t_{TST} is the minimum value of the time interval from V0 rise until V0 fall under the condition that the CO pin output inverts within 40 ms.

4. Resistance between pins during cell balancing discharge n (R_{VCn}) (Test circuit 5)

After setting V1 to V5 = V_{BL} – 0.05 V, V1 is increased to V_{BU} + 0.05 V, and then decreased to V_{BL} + 0.05 V after the cell balancing detection delay time (t_{BU}). When t_{BU} + cell balancing OFF time (t_{CBOFF}) have elapsed after the first rise of V1, cell balancing discharge starts. VI1 / I1 at that moment is defined as R_{VC1}. R_{VCn} (n = 2 to 5) can be defined in the same way as when n = 1.

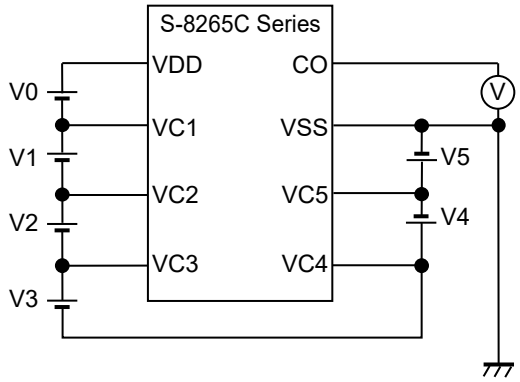


Figure 5 Test Circuit 1

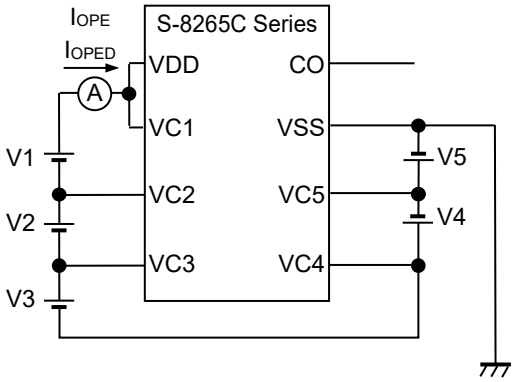


Figure 6 Test Circuit 2

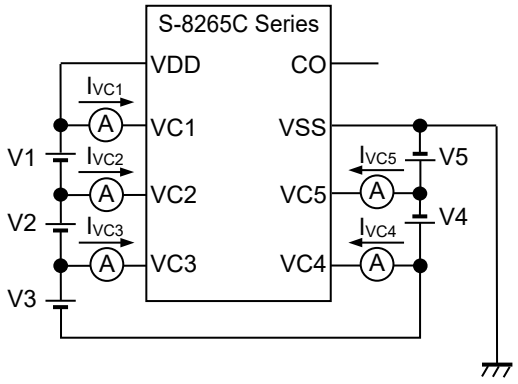


Figure 7 Test Circuit 3

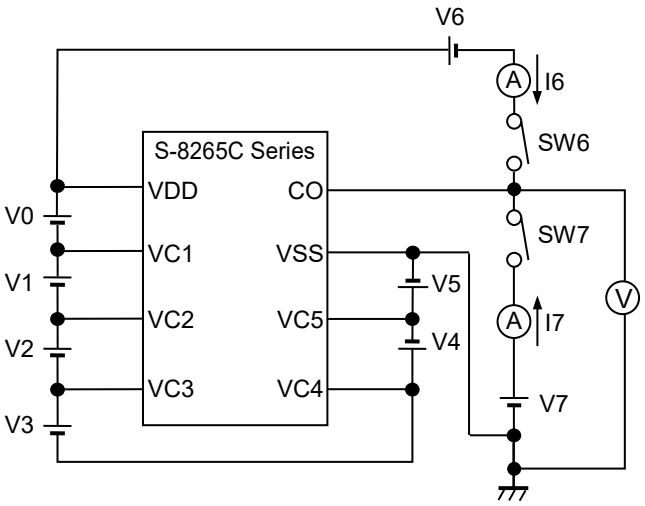


Figure 8 Test Circuit 4

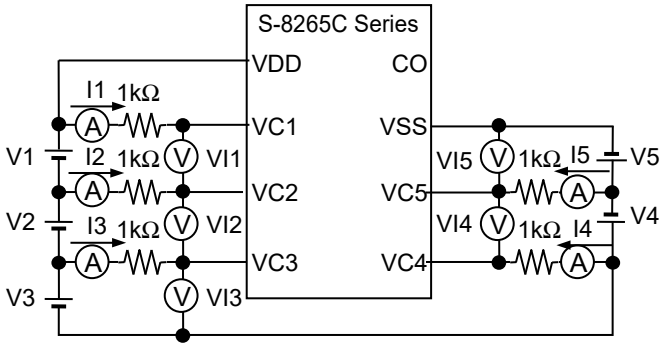


Figure 9 Test Circuit 5

■ Operation

Remark Refer to "■ **Battery Protection IC Connection Examples**".

1. Normal status

When the voltage of all batteries is lower than cell balancing release voltage n (V_{BLn}), "L" (Active "H") or "H" (Active "L") is output from the CO pin. This is the normal status.

2. Cell balancing status

When the voltage of any of all batteries exceeds the cell balancing detection voltage n (V_{BUn}) in the normal status and the conditions continue for the cell balancing detection delay time (t_{BU}) or longer, S-8265C Series changes to the cell balancing status. In the cell balancing status, the cell balancing OFF time (t_{CBOFF}) and cell balancing ON time (t_{CBON}) are repeated. S-8265C Series monitors V_{BLn} and overcharge detection voltage (V_{CUn}) during t_{CBOFF}. In addition, every cell balancing discharging FET (SWn) between pins is off during t_{CBOFF}, and cell balancing current does not flow. S-8265C Series returns to the normal status when the voltage of all batteries falls to V_{BLn} or lower during V_{BLn} monitoring time of t_{CBOFF}.
S-8265C Series turns on SWn with which a battery exceeding V_{BLn} is connected during t_{CBON}, and the cell balancing current flows. Note that the voltage of each battery is not monitored during t_{CBON}.
Every SWn is turned off during t_{CBON} when the voltage of all batteries exceeds V_{BLn} in the cell balancing status.

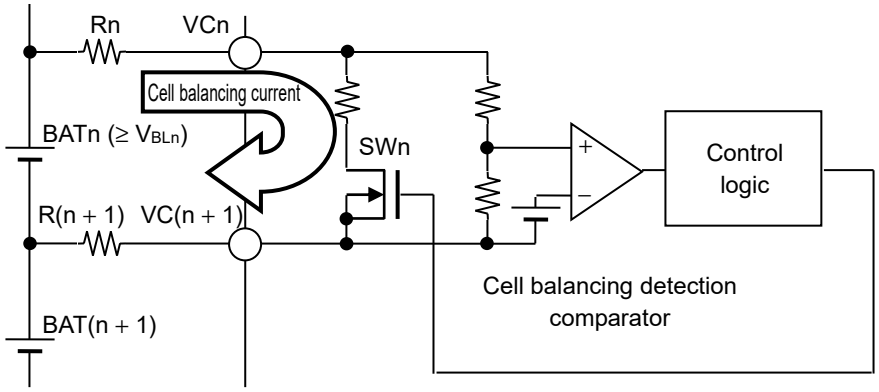
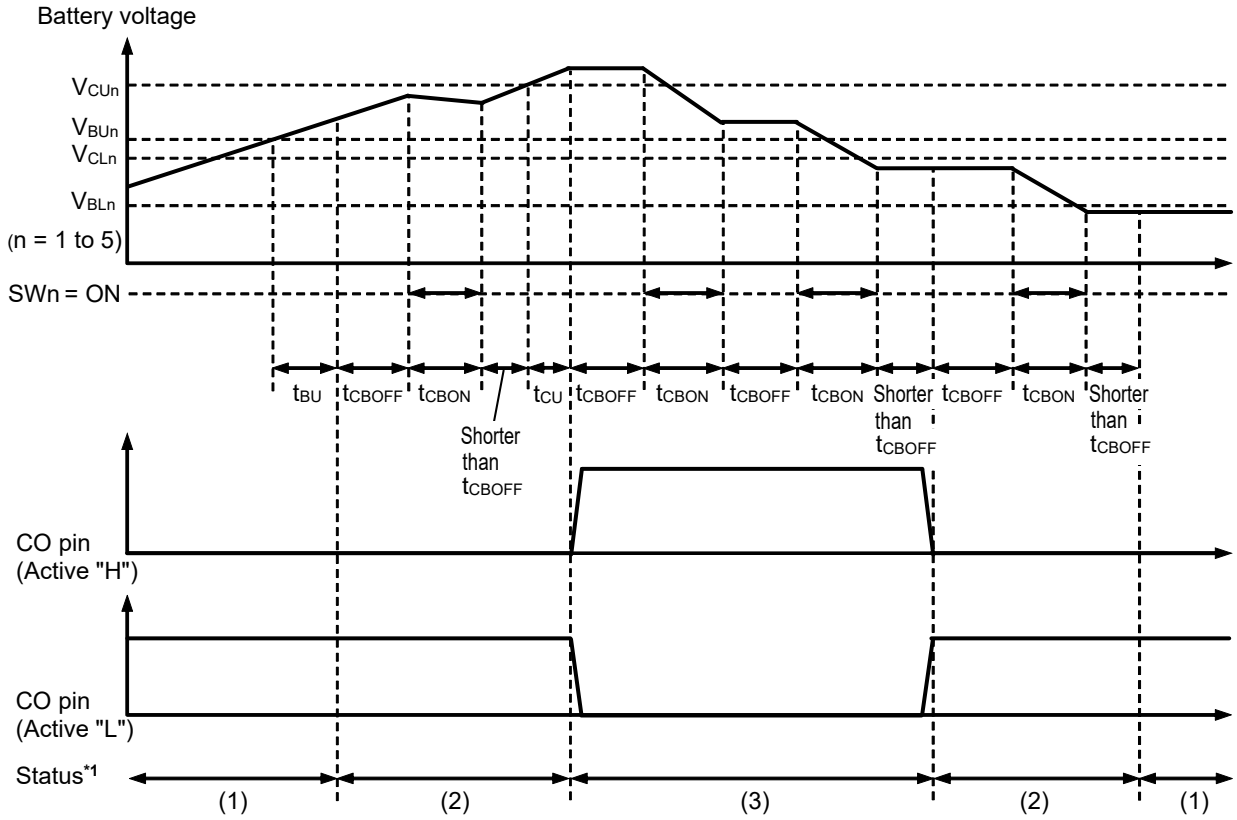


Figure 10

3. Overcharge cell balancing status

During the cell balancing status and V_{CUn} monitoring time of t_{CBOFF}, when the voltage of any of all batteries exceeds V_{CUn} and the conditions continue for the overcharge detection delay time (t_{CU}) or longer, the CO pin output inverts. S-8265C Series then changes to the overcharge cell balancing status.
In the cell balancing status, even when the voltage of any of all batteries exceeds V_{CUn} during t_{CBON}, the cell balancing status is retained. During V_{CUn} monitoring time of the following t_{CBOFF}, when the voltage of any of all batteries exceeds V_{CUn} and the conditions continue for the overcharge detection delay time (t_{CU}) or longer, the CO pin output inverts and S-8265C Series then changes to the overcharge cell balancing status.
In the overcharge cell balancing status, t_{CBOFF} and t_{CBON} are repeated. S-8265C Series monitors V_{BLn} and overcharge release voltage (V_{CLn}) during t_{CBOFF}. In addition, every SWn is off during t_{CBOFF}, and cell balancing current does not flow. The CO pin output inverts and S-8265C Series returns to the cell balancing status when the voltage of all batteries falls to V_{CLn} or lower during V_{CLn} monitoring time of t_{CBOFF}.
S-8265C Series turns on SWn with which a battery exceeding V_{BLn} is connected during t_{CBON}, and the cell balancing current flows. Note that the voltage of each battery is not monitored during t_{CBON}.
Every SWn is turned off during t_{CBON} when the voltage of all batteries exceeds V_{BLn} in the overcharge cell balancing status.

Remark n = 1 to 5

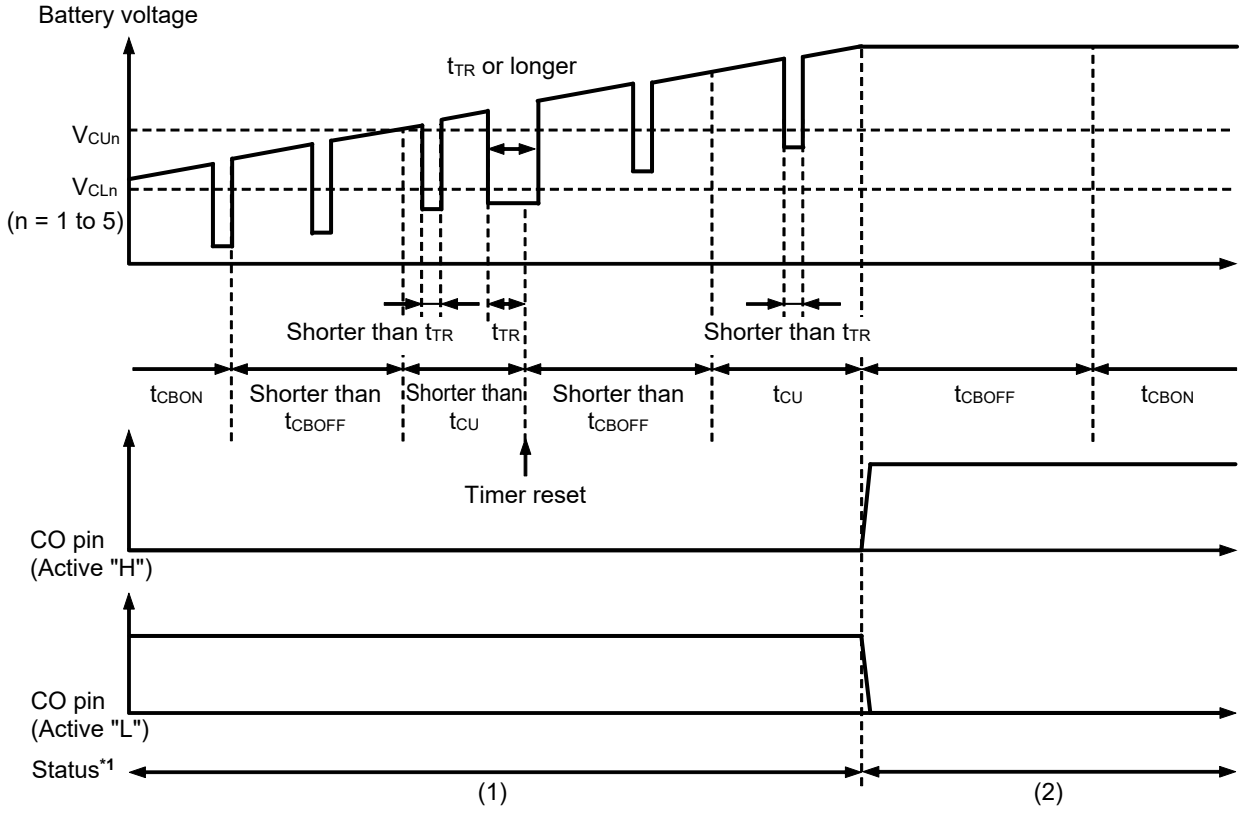


***1.** (1) : Normal status
(2) : Cell balancing status
(3) : Overcharge cell balancing status

Figure 11

4. Overcharge timer reset function

During the overcharge detection voltage monitoring time of t_{CBOFF} and additionally, the time interval of t_{CU} from when the voltage of any of the batteries exceeds V_{CUn} until the CO pin output inverts, S-8265C Series has the following operations.
Even if an overcharge release noise, which temporarily forces the battery voltage below V_{CUn}, is input, t_{CU} is continuously counted as long as the overcharge release noise time is shorter than the overcharge timer reset delay time (t_{TR}). Under the same conditions, if the overcharge release noise time is t_{TR} or longer, counting of t_{CU} is reset. After that, t_{CBOFF} resumes.

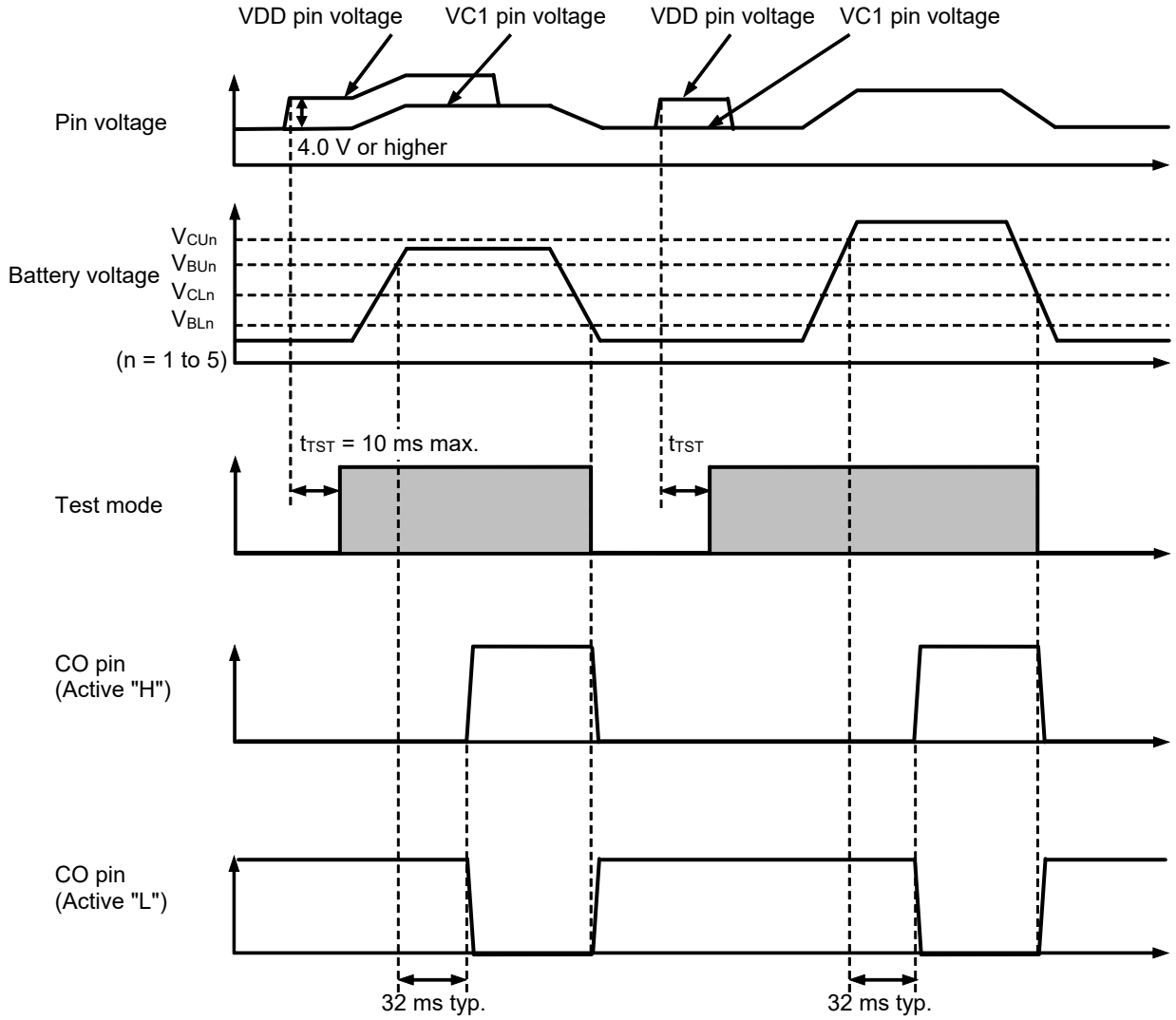


***1.** (1) : Cell balancing status
(2) : Overcharge cell balancing status

Figure 12

5. Test mode

Transition to the test mode enables S-8265C Series to check cell balancing detection voltage (V_{BUn}) and overcharge detection voltage (V_{CUn}) in a short time.
S-8265C Series transitions to the test mode by retaining the VDD pin voltage at 4.0 V above the VC1 pin voltage or higher for at least 10 ms. The status is retained by test mode retaining latch, and the test mode is retained even if the VDD pin voltage is returned to the same voltage as the VC1 pin voltage again.
In the test mode, when a battery voltage exceeds V_{BUn} while the VDD pin voltage is held at 4.0 V above the VC1 pin voltage or higher, the CO pin output inverts and S-8265C Series switches to the detection status. When the VDD pin voltage is then returned to the same voltage as VC1 pin voltage and the battery voltage falls to V_{BLn} or lower, the CO pin output inverts again and S-8265C Series switches to the release status.
When the CO pin output switches from the detection status to the release status, the test mode retaining latch is reset and S-8265C Series is released from the test mode. Make sure that the battery voltage does not fall to V_{BLn} or lower before returning the VDD pin voltage to the same voltage as the VC1 pin voltage.
After setting the VDD pin voltage to 4.0 V above the VC1 pin voltage or higher and transitioning to the test mode, the VDD pin voltage is returned to the same voltage as the VC1 pin voltage. When a battery voltage then exceeds V_{CUn}, the CO pin output inverts and S-8265C Series switches to the detection status. When the battery voltage then falls to V_{CLn} or lower, the CO pin output inverts again and switches to the release status. When the CO pin output switches from the detection status to the release status, the test mode retaining latch is reset and S-8265C Series is released from the test mode.
Note that cell balancing current does not flow in the test mode.



Caution 1. Transition to test mode when the voltage of all batteries is lower than V_{BUn}.
2. The overcharge timer reset delay time (t_{TR}) is not shortened in the test mode.

Figure 13

■ Battery Protection IC Connection Examples

1. 5-serial cell (CMOS output product)

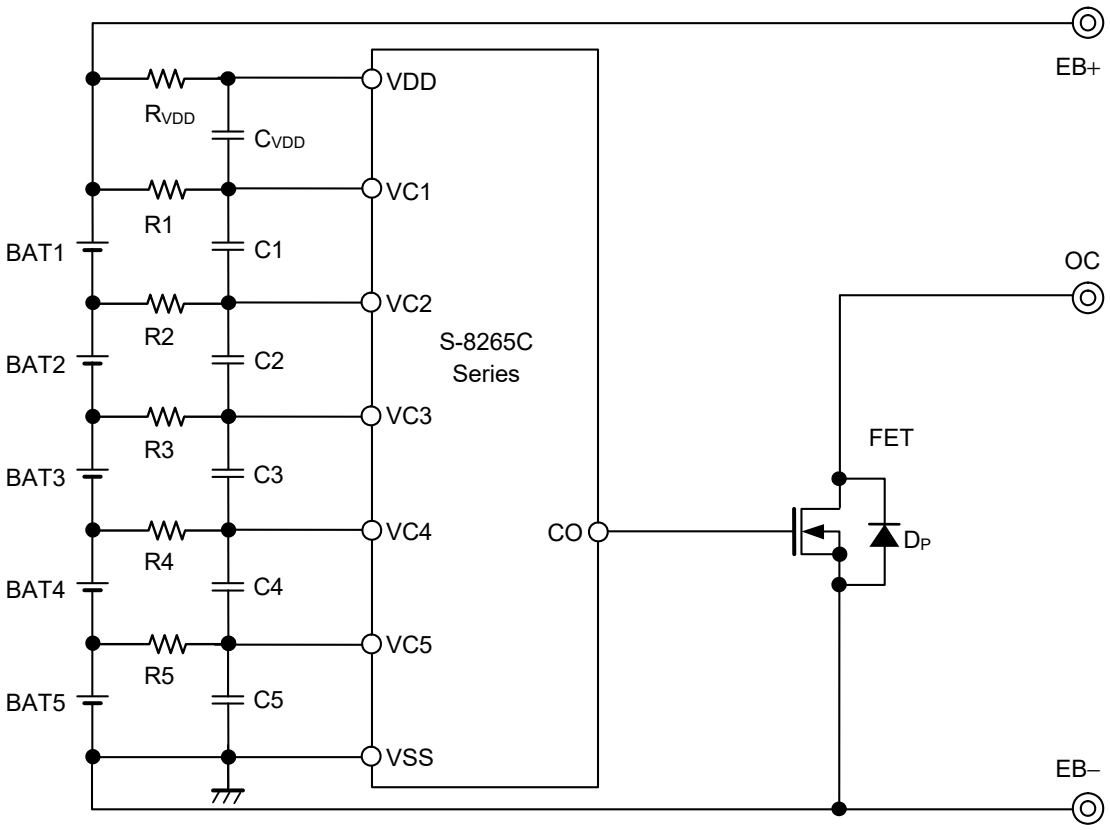


Figure 14

Table 9 Constants for External Components

No.	Symbol	Min.	Typ.	Max.	Unit
1	R1 to R5	100	100	1000	Ω
2	C1 to C5, C_{VDD}	0.1	0.1	0.1	μF
3	R_{VDD}	100	100	1000	Ω

Caution
1. **The constants may be changed without notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**
3. **R1 to R5 should be the same constant. C1 to C5 and C_{VDD} should be the same constant.**
4. **Set values for R1 to R5 so that the loss of the IC does not exceed the power dissipation by the cell balancing current.**

2. 4-serial cell (CMOS output product)

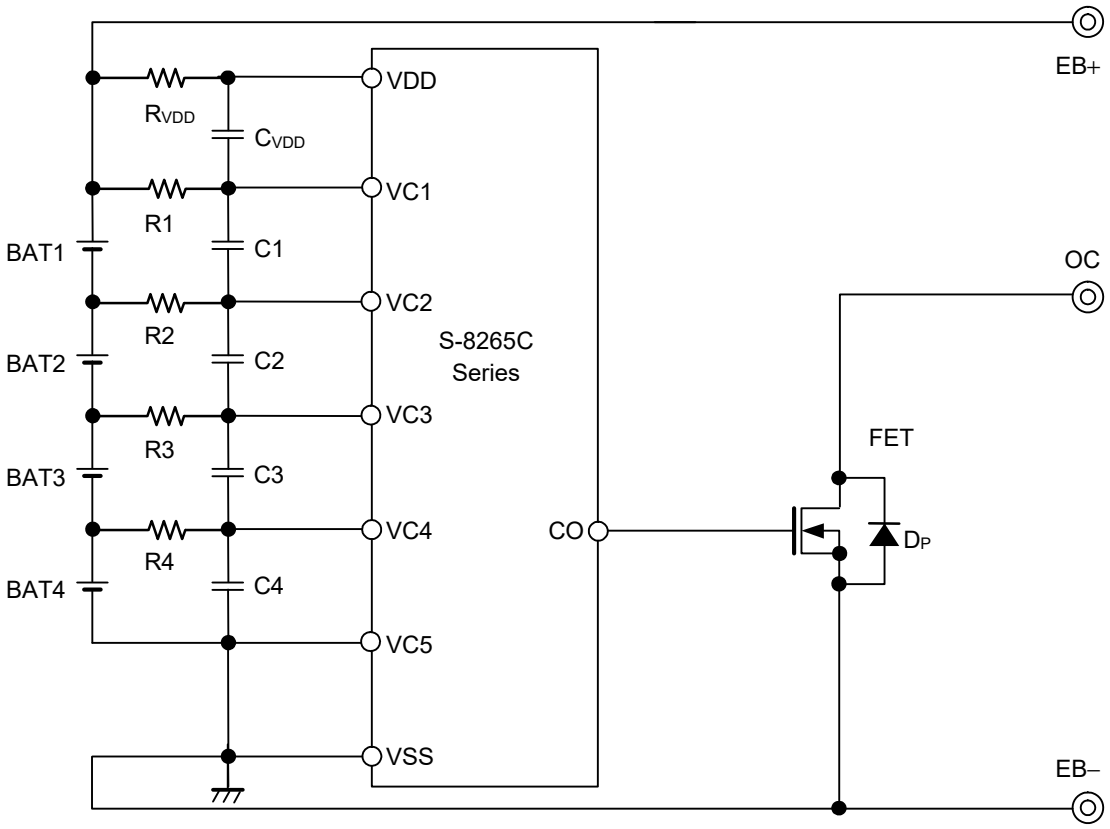


Figure 15

Table 10 Constants for External Components

No.	Symbol	Min.	Typ.	Max.	Unit
1	R1 to R4	100	100	1000	Ω
2	C1 to C4, C_{VDD}	0.1	0.1	0.1	μF
3	R_{VDD}	100	100	1000	Ω

Caution
1. **The constants may be changed without notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**
3. **R1 to R4 should be the same constant. C1 to C4 and C_{VDD} should be the same constant.**
4. **Set values for R1 to R4 so that the loss of the IC does not exceed the power dissipation by the cell balancing current.**

3. 3-serial cell (CMOS output product)

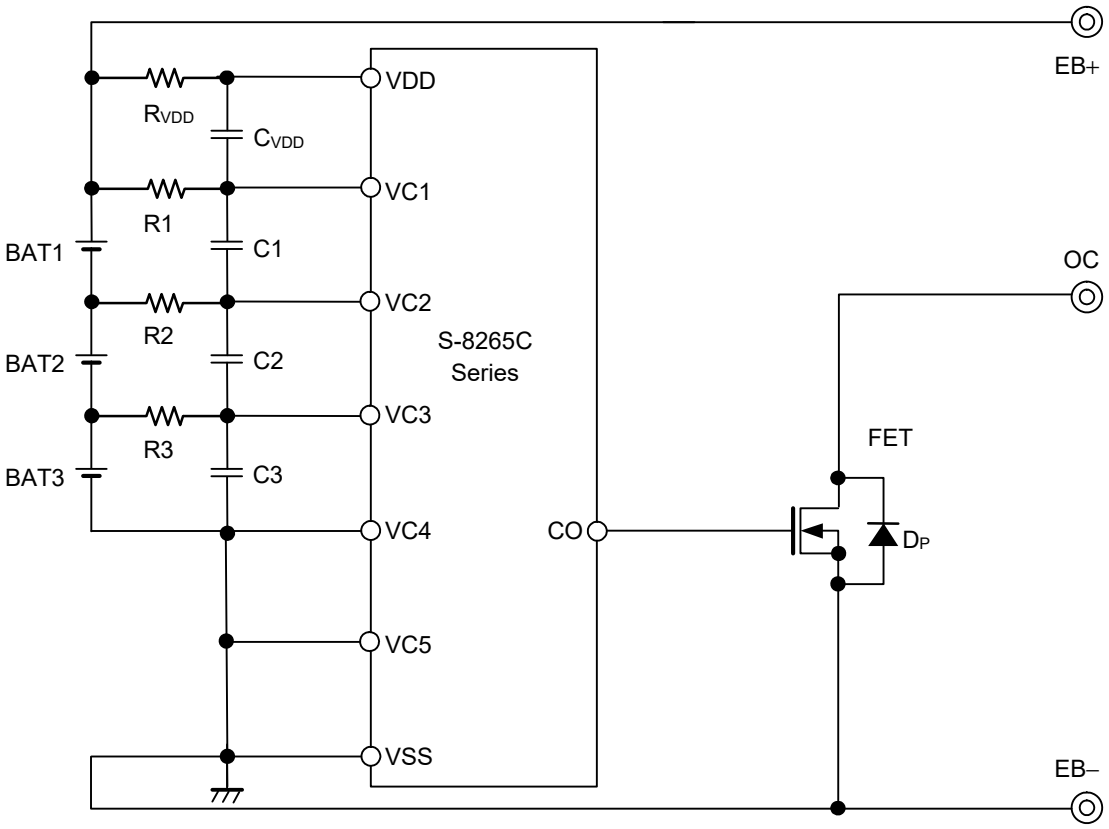


Figure 16

Table 11 Constants for External Components

No.	Symbol	Min.	Typ.	Max.	Unit
1	R1 to R3	100	100	1000	Ω
2	C1 to C3, C_{VDD}	0.1	0.1	0.1	μF
3	R_{VDD}	100	100	1000	Ω

Caution
1. **The constants may be changed without notice.**
2. **It has not been confirmed whether the operation is normal or not in circuits other than the connection example. In addition, the connection example and the constants do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constants.**
3. **R1 to R3 should be the same constant. C1 to C3 and C_{VDD} should be the same constant.**
4. **Set values for R1 to R3 so that the loss of the IC does not exceed the power dissipation by the cell balancing current.**

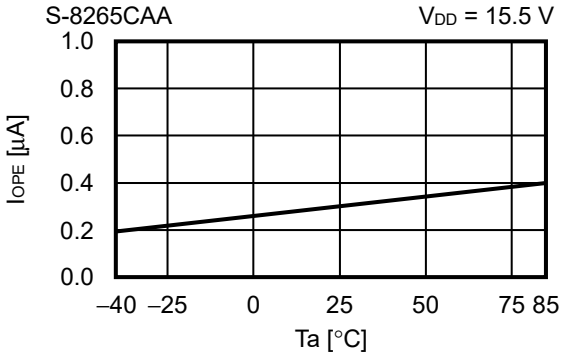
■ Precautions

- Do not connect batteries charged with V_{CLn} or higher. If the connected batteries include a battery charged with V_{CLn} or higher, the S-8265C Series may become overcharge status after all pins are connected.
- In some application circuits, even if an overcharged battery is not included, the order of connecting batteries may be restricted to prevent transient output of CO detection pulses when the batteries are connected. Perform thorough evaluation with the actual application circuit.
- Before the battery connection, short-circuit the battery side pins R_{VDD} and R1, shown in the figure in "**■ Battery Protection IC Connection Examples**".
- The application conditions for the input voltage, output voltage, and load current should not exceed the power dissipation.
- Do not apply to this IC an electrostatic discharge that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement of patents owned by a third party by products including this IC.

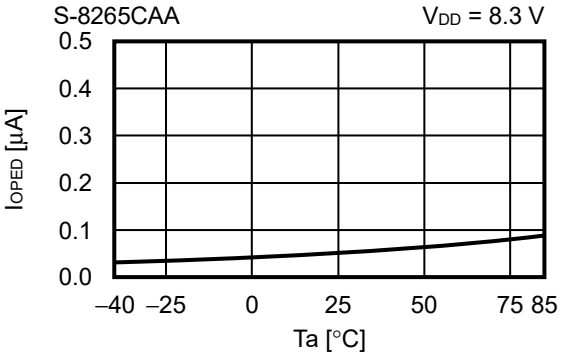
■ Characteristics (Typical Data)

1. Current consumption

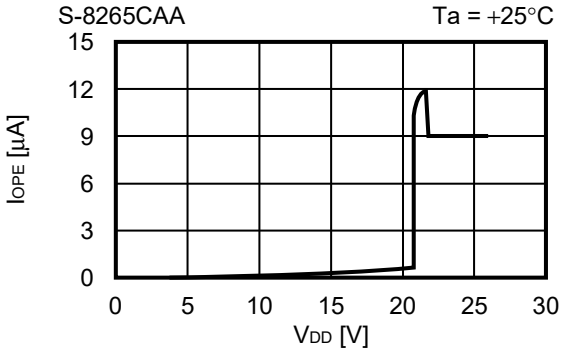
1. 1 I_{OPE} vs. Ta



1. 2 I_{OPED} vs. Ta

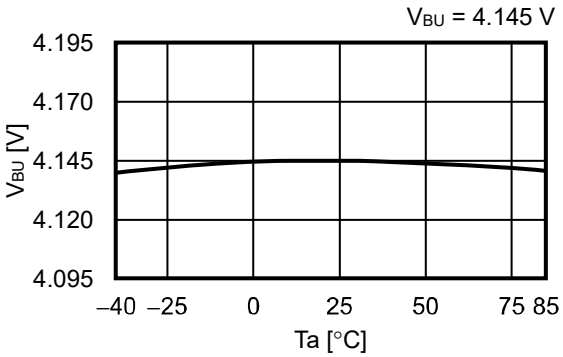


1. 3 I_{OPE} vs. V_{DD}

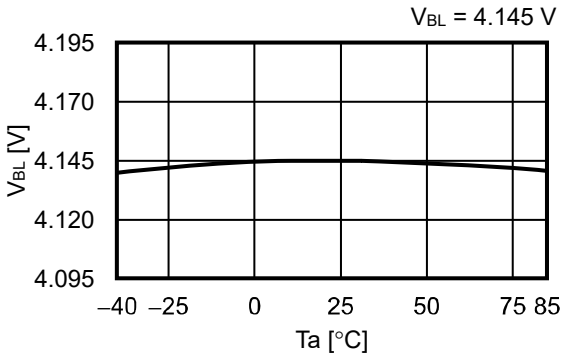


2. Detection voltage

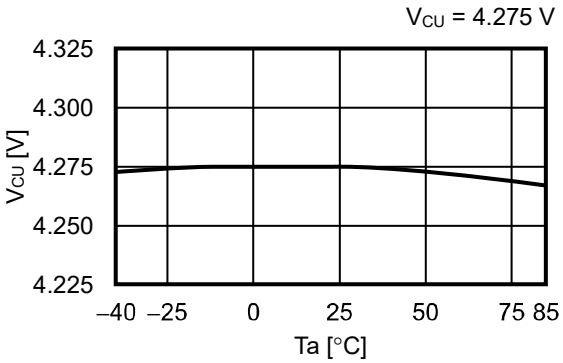
2. 1 V_{BU} vs. Ta



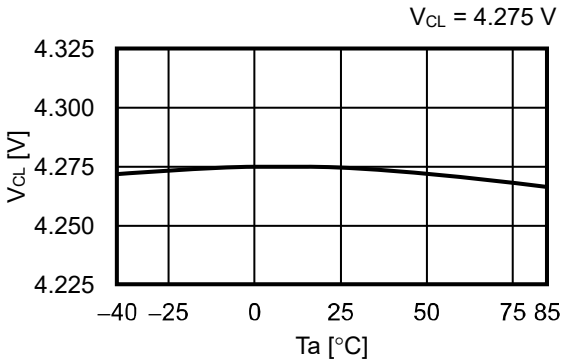
2. 2 V_{BL} vs. Ta



2. 3 V_{CU} vs. Ta

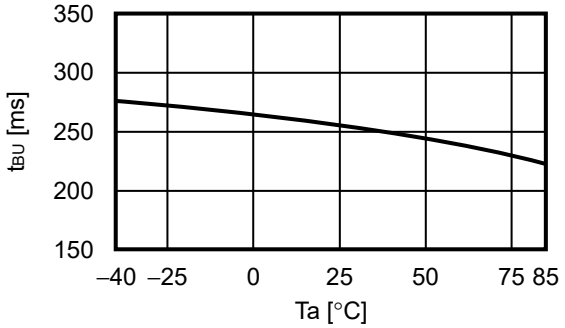


2. 4 V_{CL} vs. Ta

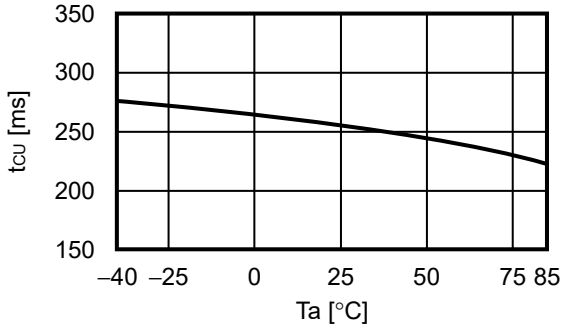


3. Delay time

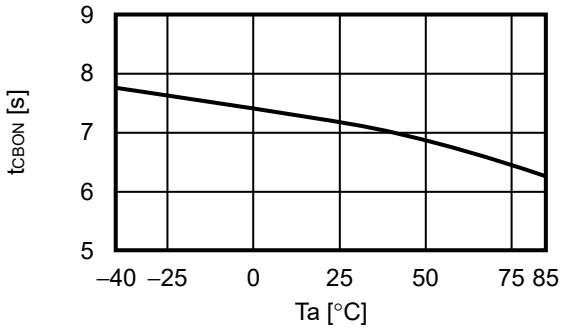
3. 1 t_{BU} vs. Ta



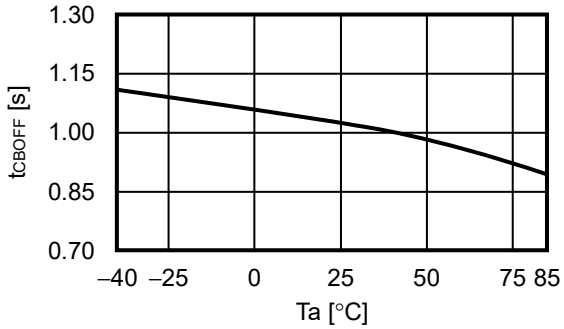
3. 2 t_{CU} vs. Ta



3. 3 t_{CBON} vs. Ta

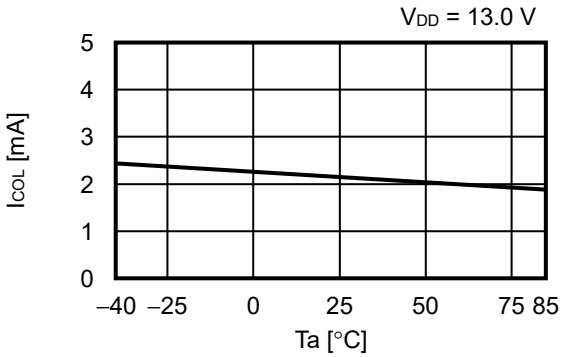


3. 4 t_{CBOFF} vs. Ta

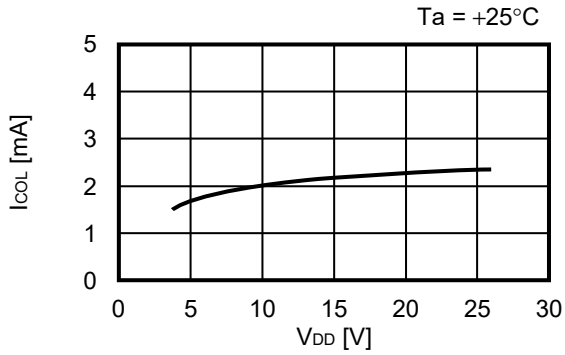


4. Output current

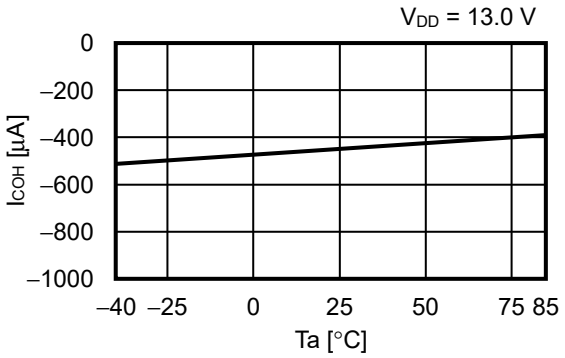
4. 1 I_{COL} vs. Ta



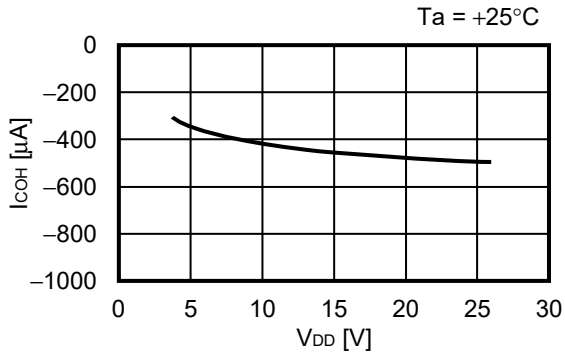
4. 2 I_{COL} vs. V_{DD}



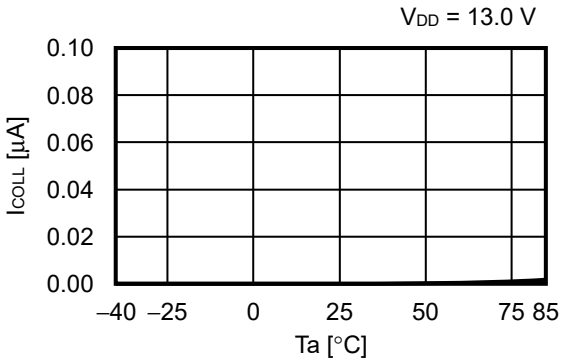
4. 3 I_{COH} vs. Ta



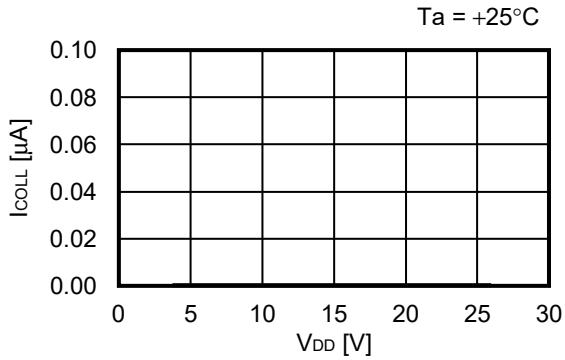
4. 4 I_{COH} vs. V_{DD}



4. 5 I_{COLL} vs. Ta

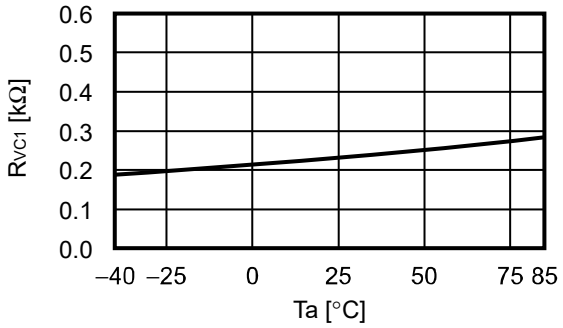


4. 6 I_{COLL} vs. V_{DD}

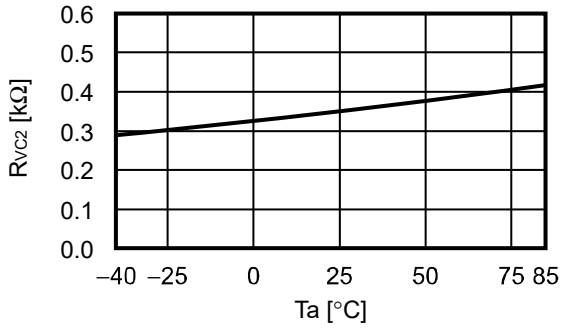


5. Internal resistance

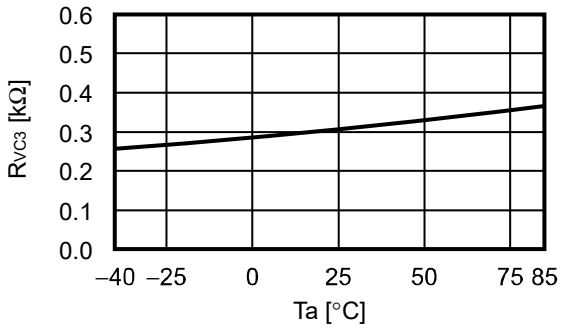
5. 1 R_{VC1} vs. Ta



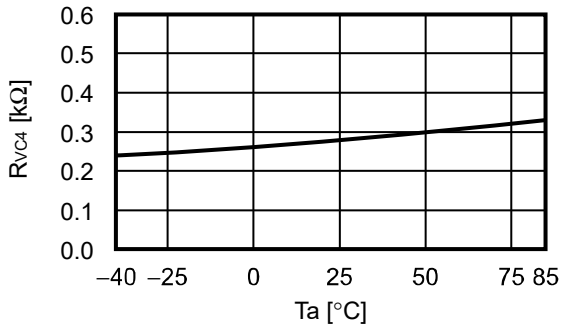
5. 2 R_{VC2} vs. Ta



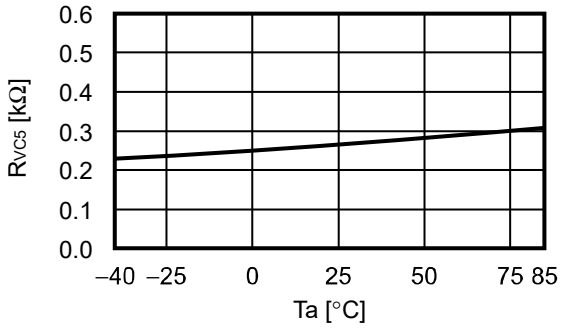
5. 3 R_{VC3} vs. Ta



5. 4 R_{VC4} vs. Ta

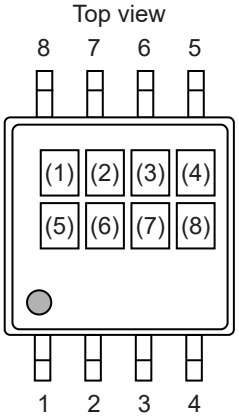


5. 5 R_{VC5} vs. Ta



■ Marking Specifications

1. TMSOP-8

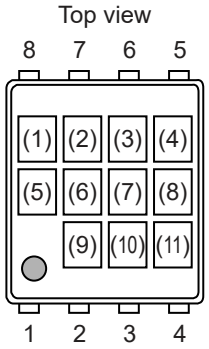


(1): Blank
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5): Blank
(6) to (8): Lot number

Product name vs. Product code

Product Name	Product Code		
	(2)	(3)	(4)
S-8265CAA-K8T2U7	8	J	A
S-8265CAB-K8T2U7	8	J	B
S-8265CAC-K8T2U7	8	J	C

2. SNT-8A



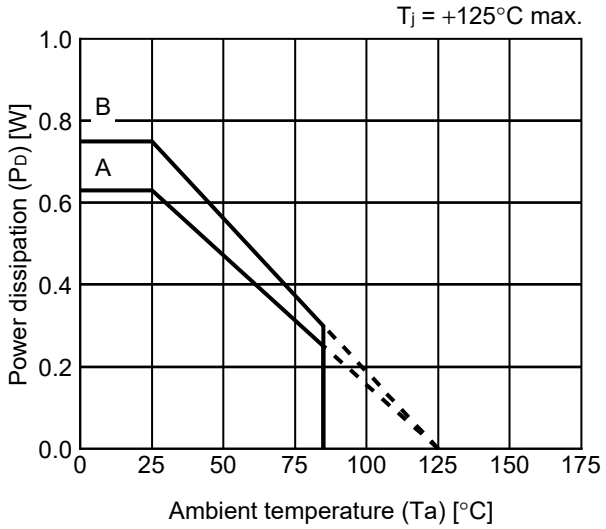
(1): Blank
(2) to (4): Product code (Refer to **Product name vs. Product code**)
(5), (6): Blank
(7) to (11): Lot number

Product name vs. Product code

Product Name	Product Code		
	(2)	(3)	(4)
S-8265CAA-I8T1U7	8	J	A

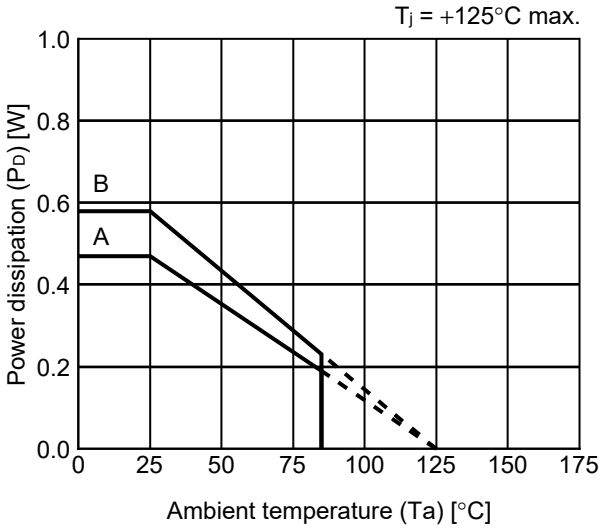
■ Power Dissipation

TMSOP-8



Board	Power Dissipation (P_D)
A	0.63 W
B	0.75 W
C	–
D	–
E	–

SNT-8A

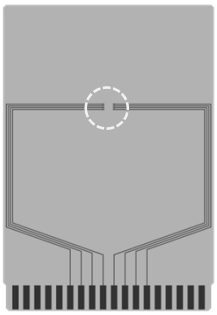


Board	Power Dissipation (P_D)
A	0.47 W
B	0.58 W
C	–
D	–
E	–

TMSOP-8 Test Board

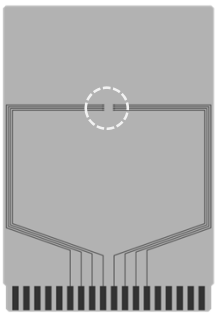
(1) Board A

IC Mount Area



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



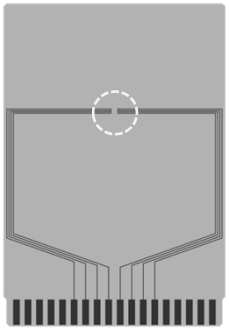
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

No. TMSOP8-A-Board-SD-1.0

SNT-8A Test Board

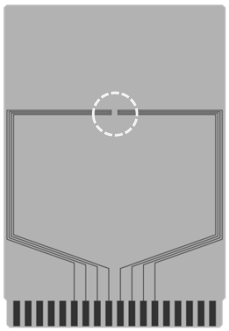
IC Mount Area

(1) Board A



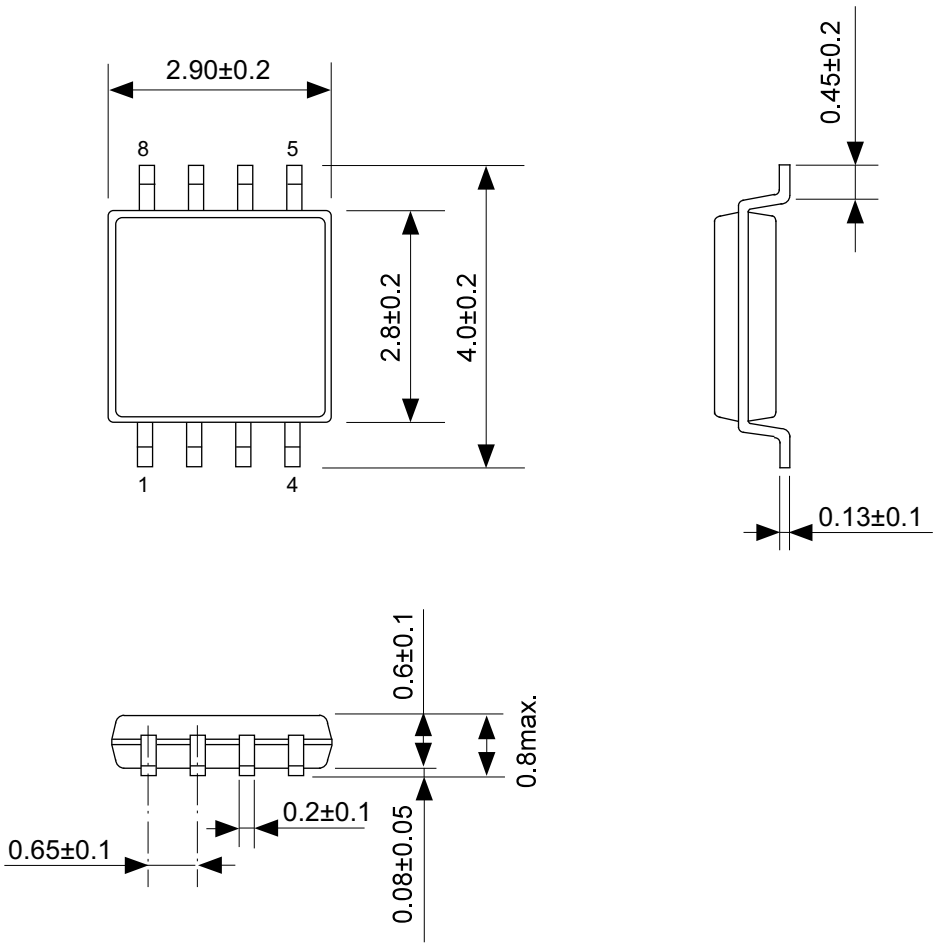
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



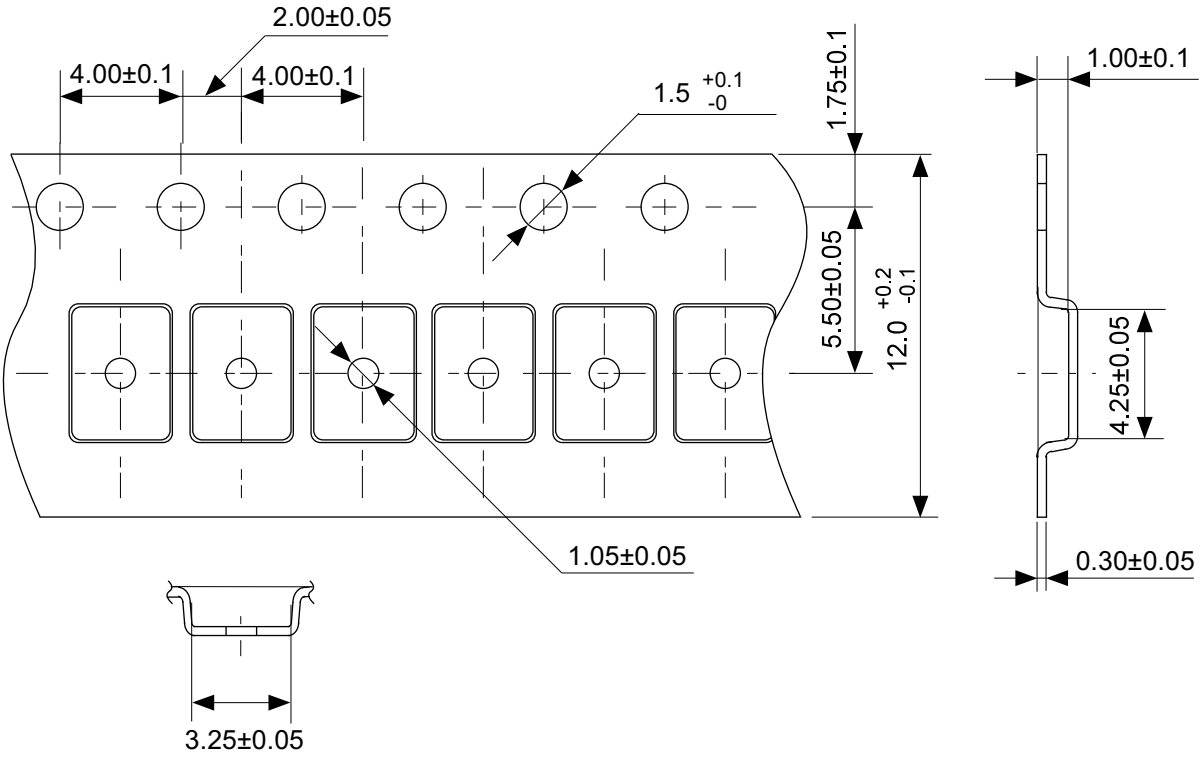
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

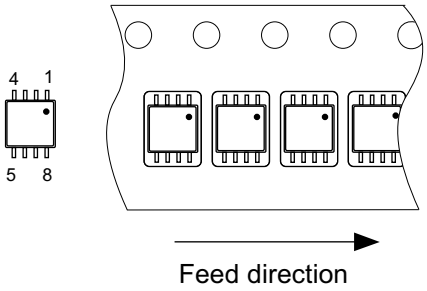
No. SNT8A-A-Board-SD-1.0



No. FM008-A-P-SD-1.2

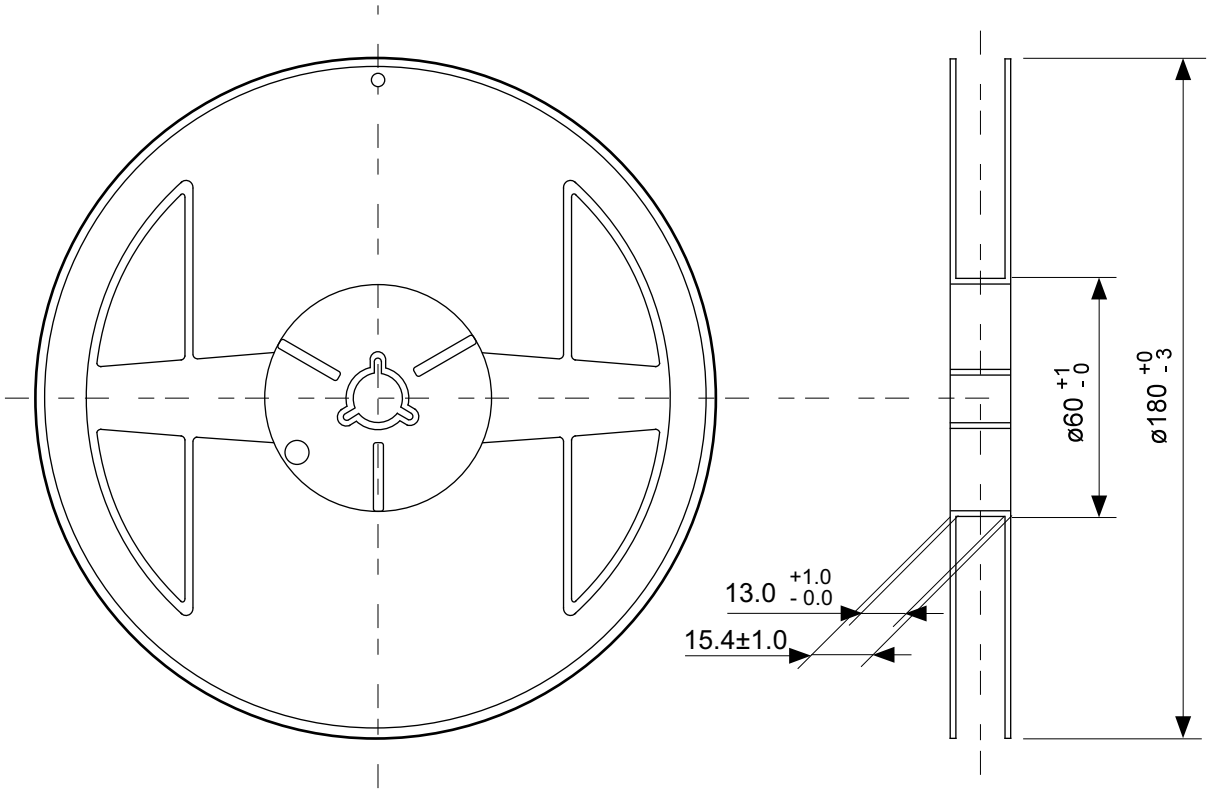
TITLE	TMSOP8-A-PKG Dimensions
No.	FM008-A-P-SD-1.2
ANGLE	
UNIT	mm
ABLIC Inc.	



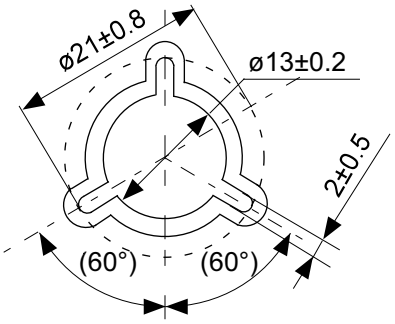


No. FM008-A-C-SD-2.0

TITLE	TMSOP8-A-Carrier Tape
No.	FM008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

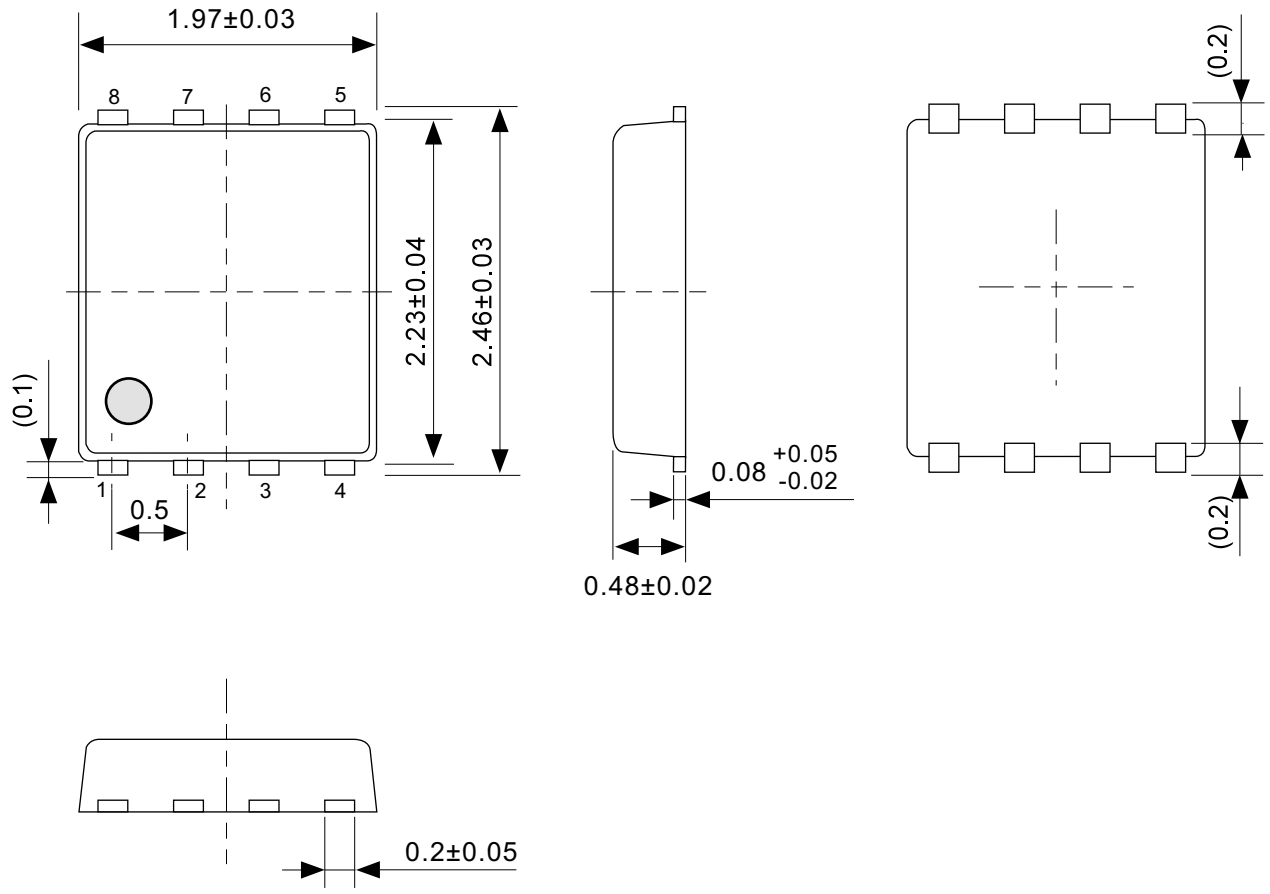


Enlarged drawing in the central part



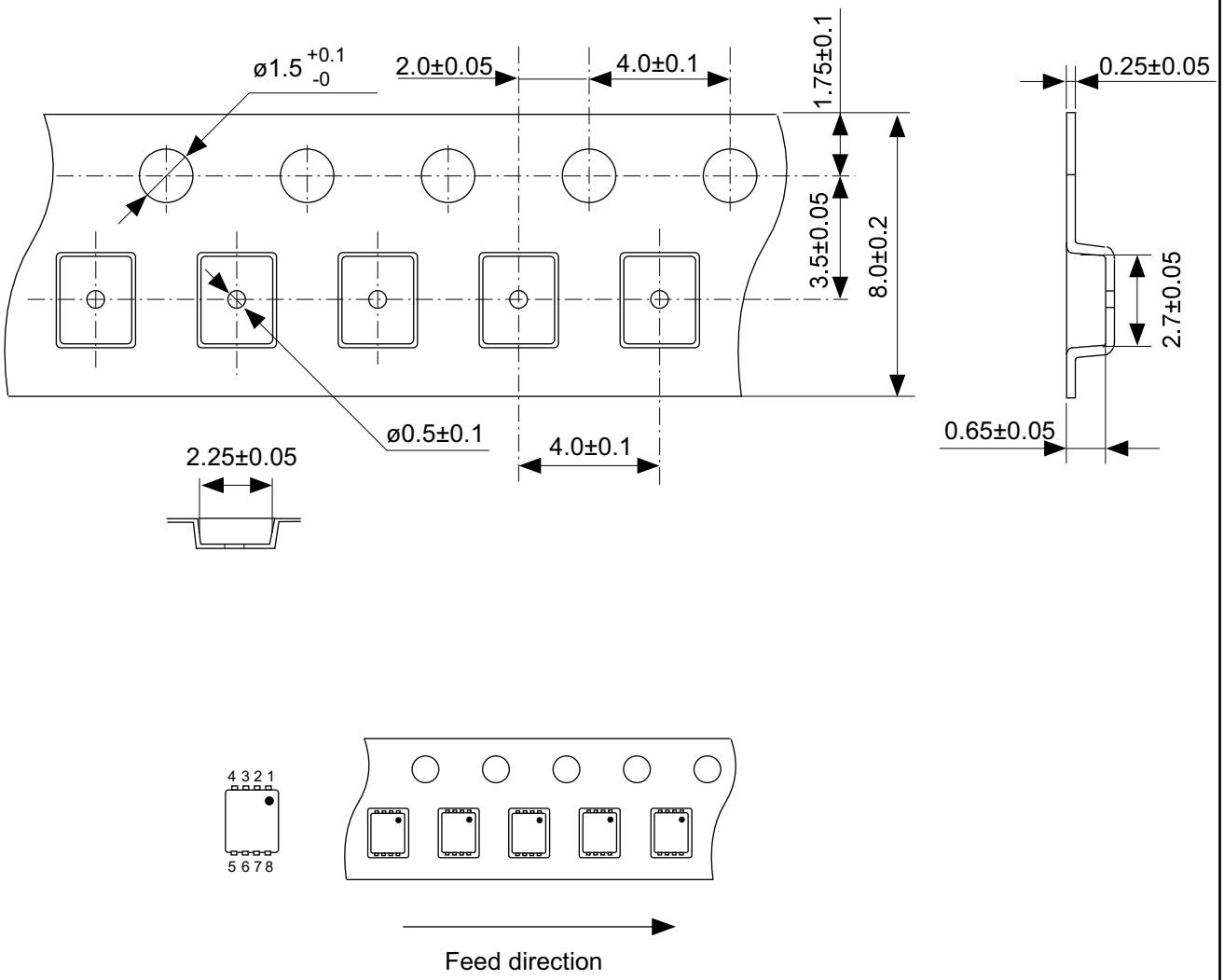
No. FM008-A-R-SD-2.0

TITLE	TMSOP8-A-Reel		
No.	FM008-A-R-SD-2.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			



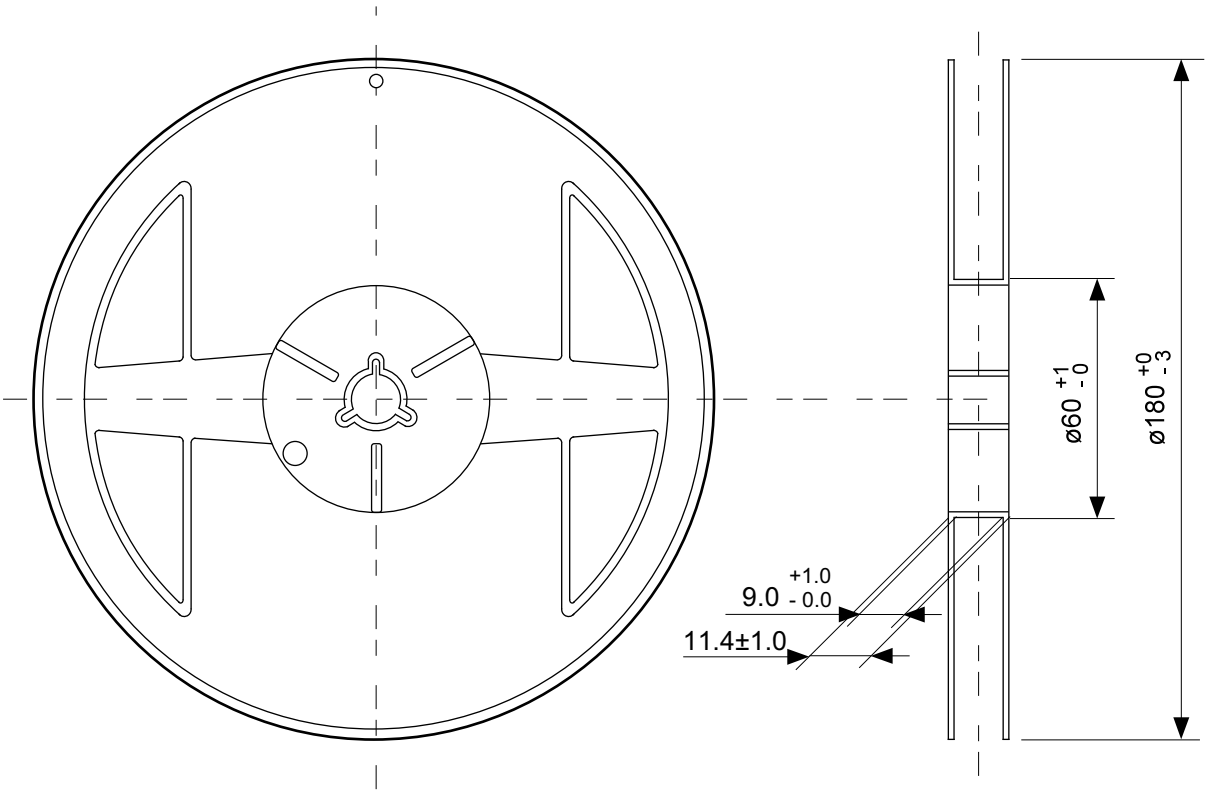
No. PH008-A-P-SD-2.1

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	

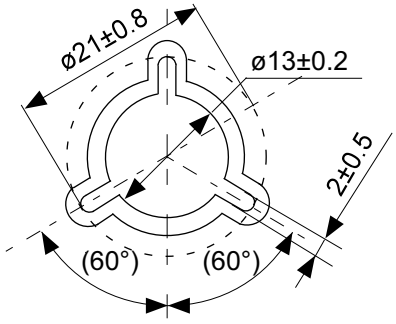


No. PH008-A-C-SD-2.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

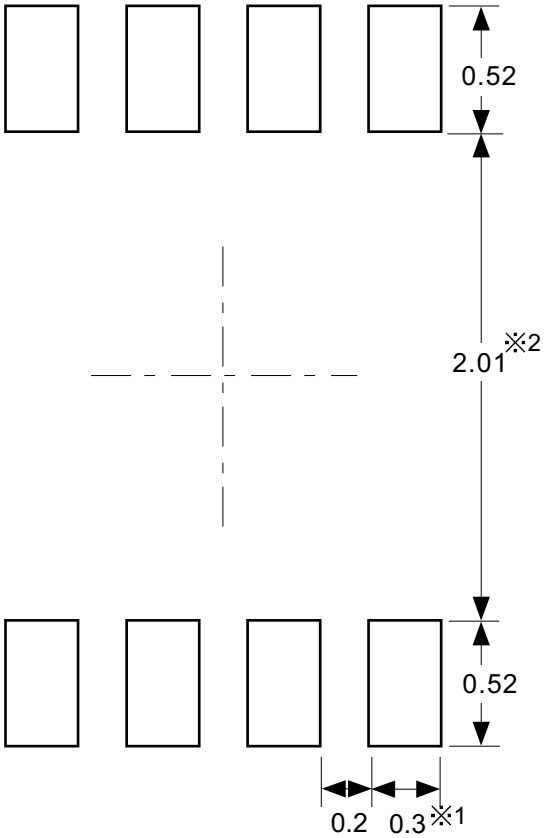


Enlarged drawing in the central part



No. PH008-A-R-SD-2.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			



※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
※2. パッケージ中央にランドパターンを広げないでください (1.96 mm ~ 2.06 mm)。

注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
3. マスク開口サイズと開口位置はランドパターンと合わせてください。
4. 詳細は〝SNTパッケージ活用の手引き〟を参照してください。

※1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).
※2. Do not widen the land pattern to the center of the package (1.96 mm to 2.06mm).

Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
3. Match the mask aperture size and aperture position with the land pattern.
4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。
※2. 请勿向封装中间扩展焊盘模式 (1.96 mm ~ 2.06 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。
2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
3. 钢网的开口尺寸和开口位置请与焊盘模式对齐。
4. 详细内容请参阅 "SNT 封装的应用指南"。

No. PH008-A-L-SD-4.1

TITLE	SNT-8A-A -Land Recommendation
No.	PH008-A-L-SD-4.1
ANGLE	
UNIT	mm
ABLIC Inc.	

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