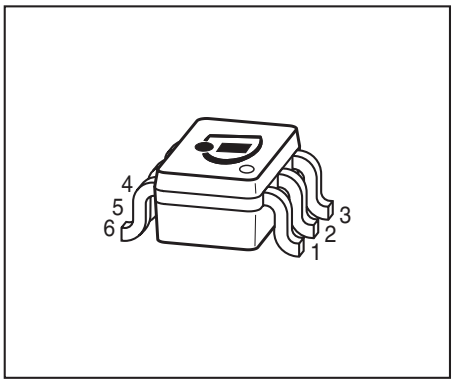
Dual N-Channel MOSFET Tetrode

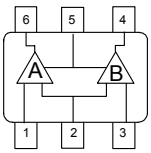


- Designed for input stages of 2 band tuners
- Two AGC amplifiers in one single package, with on-chip internal switch
- Only one switching line to control both FETs
- Integrated gate protection diodes
- Ultra low noise figure
- Excellent cross modulation at gain reduction
- Integrated ESD gate protection diodes
- Pb-free (RoHS compliant) package
- Qualified according AEC Q101

Detailed functional diagram on page 5

AEC Qualified RoHS

BG5412K



ESD (**E**lectro**s**tatic **d**ischarge) sensitive device, observe handling precaution!

Type	Package	Pin Configuration						Marking
BG5412K	SOT363	1=G1*	2=G2	3=G1**	4=D**	5=S	6=D*	K2s

* For amp. A; ** for amp. B
180° rotated tape loading orientation available

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	8	V
Continuous drain current amp. A amp. B	I_D	 25 25	mA
Gate 1/ gate 2-source current	I_{G1S}, I_{G2S}	± 1	mA
Gate 1/ gate 2-source voltage	V_{G1S}, V_{G2S}	± 6	V
Total power dissipation $T_S \leq 94$ °C	P_{tot}	200	mW
Storage temperature	T_{stg}	-55 ... 150	°C
Channel temperature	T_{ch}	150	

Thermal Resistance

Parameter	Symbol	Value	Unit
Channel - soldering point[1)]	R_{thchs}	≤ 280	K/W

[1]For calculation of R_{thJA} please refer to Application Note Thermal Resistance

Electrical Characteristics at T_A = 25°C, unless otherwise specified

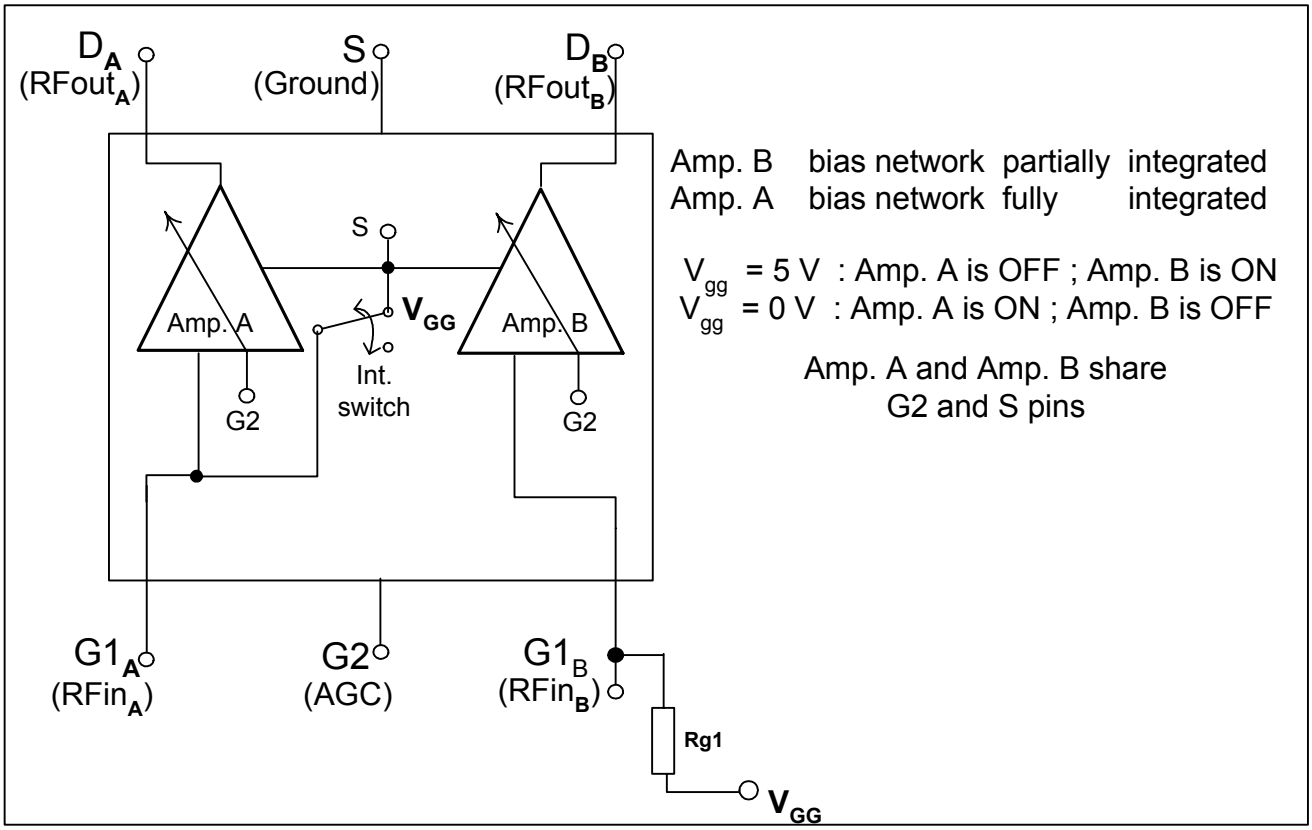
Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Drain-source breakdown voltage I_D = 100 µA, V_{G1S} = 0 , V_{G2S} = 0	$V_{(BR)DS}$	12	-	-	V
Gate1-source breakdown voltage +I_{G1S} = 10 mA, V_{G2S} = 0 , V_{DS} = 0	+$V_{(BR)G1SS}$	6	-	15	
Gate2-source breakdown voltage +I_{G2S} = 10 mA, V_{G1S} = 0 , V_{DS} = 0	+$V_{(BR)G2SS}$	6	-	15	
Gate1-source leakage current V_{G1S} = 6 V, V_{G2S} = 0 , V_{DS} = 0	+I_{G1SS}	-	-	50	nA
Gate2-source leakage current V_{G2S} = 8 V, V_{G1S} = 0	+I_{G2SS}	-	-	50	
Drain current V_{DS} = 5 V, V_{G1S} = 0 , V_{G2S} = 4 V	I_{DSS}	-	-	100	µA
Drain-source current V_{DS} = 5 V, V_{G2S} = 4 V, R_{G1} = 120 kΩ, amp. B V_{DS} = 5 V, V_{G2S}= 4 V, selfbiased, amp. A	I_{DSX}	 - -	 14 18	 - -	mA
Gate1-source pinch-off voltage V_{DS} = 5 V, V_{G2S} = 4 V, I_D = 100 µA	$V_{G1S(p)}$	-	0.7	-	V
Gate2-source pinch-off voltage V_{DS} = 5 V, I_D = 100 µA	$V_{G2S(p)}$	-	0.7	-	

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics V_{DS} = 5 V, V_{G2} = 4 V, I_D = 10 mA (verified by random sampling)					
Forward transconductance	g_{fs}				mS
amp. A		-	33	-	
amp. B		-	30	-	
Gate1 input capacitance	C_{g1ss}				pF
amp. A		-	2.2	-	
amp. B		-	2	-	
Output capacitance	C_{dss}				
amp. A		-	0.9	-	
amp. B		-	0.8	-	
Power gain	G_p				dB
f= 800 MHz, amp. A		-	24	-	
f= 800 MHz, amp. B		-	24	-	
f= 45 MHz, amp. A		-	34	-	
f= 45 MHz, amp. B		-	31	-	
Noise figure	F				dB
f= 800 MHz, amp. A		-	1.1	-	
f= 800 MHz, amp. B		-	1.2	-	
f= 45 MHz, amp. A		-	0.8	-	
f= 45 MHz, amp. B		-	0.9	-	
Gain control range V_{G2S} = 4...0 V, f = 800 MHz	ΔG_p	-	45	-	
Cross-modulation k=1%, f_W=50MHz, f_{unw}=60MHz	X_{mod}				-
amp. A, AGC = 0 dB		-	97	-	
amp. B, AGC = 0 dB		-	96	-	
amp. A, AGC = 10 dB		-	94	-	
amp. B, AGC = 10 dB		-	91	-	
amp. A, AGC = 40 dB		-	105	-	
amp. B, AGC = 40 dB		-	103	-	

Functional diagram

shows pinning of BG5412K, switching pin at PIN 3

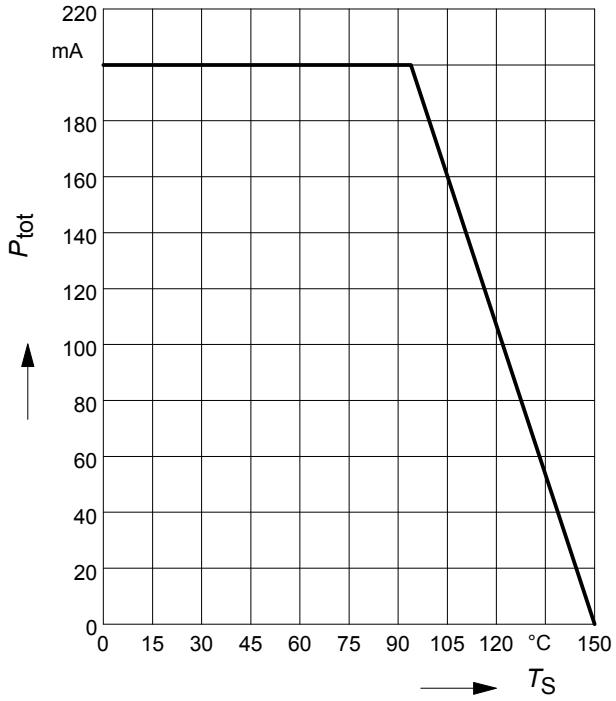


Amp. B bias network partially integrated
Amp. A bias network fully integrated

V_{gg} = 5 V : Amp. A is OFF ; Amp. B is ON
V_{gg} = 0 V : Amp. A is ON ; Amp. B is OFF

Amp. A and Amp. B share
G2 and S pins

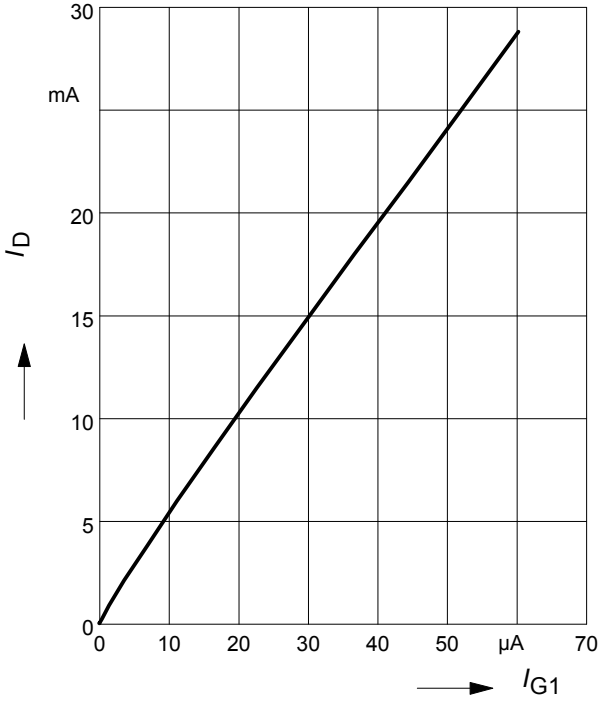
Total power dissipation $P_{tot} = f(T_S)$



Drain current $I_D = f(I_{G1})$

V_{G2S} = 4V, amp. B

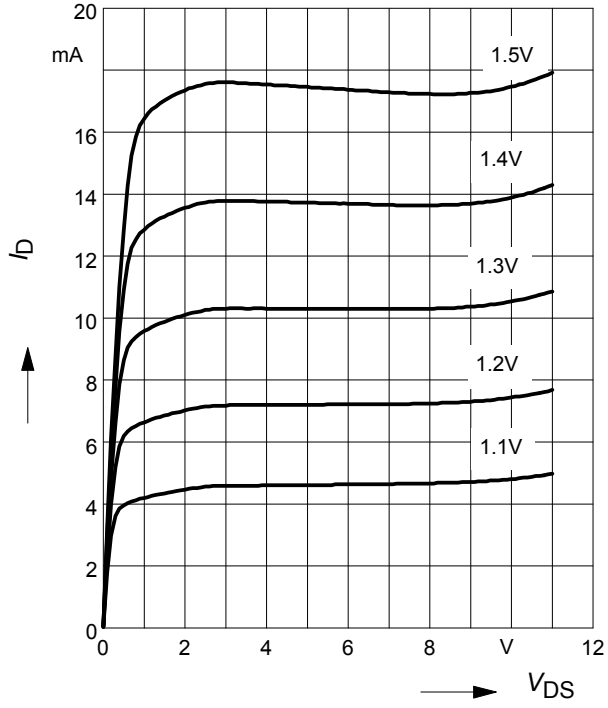
V_{DS}= 5 V



Output characteristics $I_D = f(V_{DS})$

V_{G2} = 4 V, amp. A

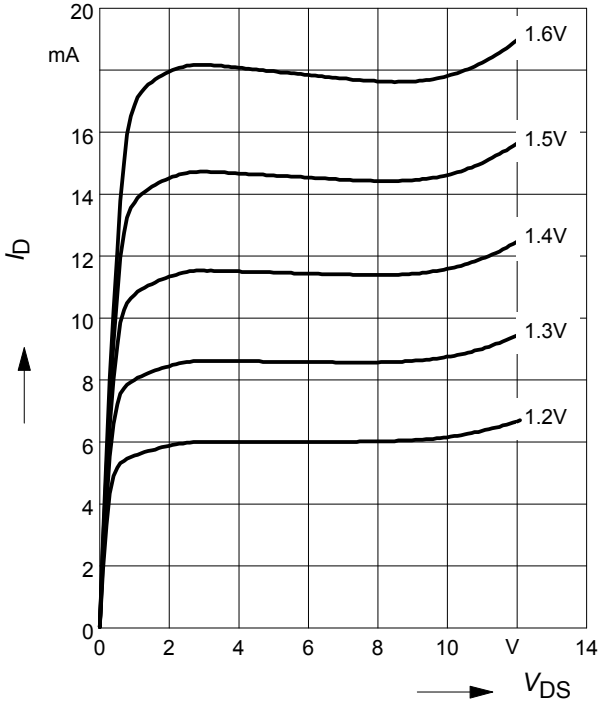
V_{G1} = Parameter



Output characteristics $I_D = f(V_{DS})$

V_{G2} = 4 V, amp. B

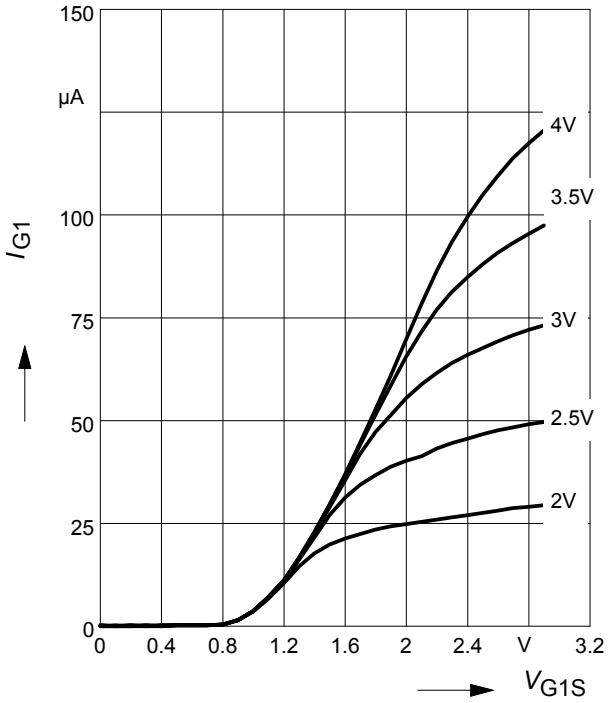
V_{G1} = Parameter



Gate 1 current $I_{G1} = f(V_{G1S})$

V_{DS} = 5V

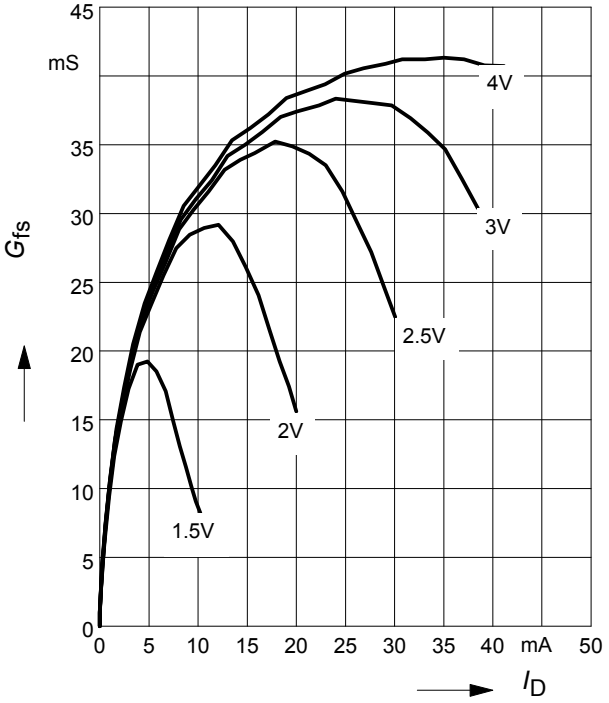
V_{G2S} = Parameter



Gate 1 forward transconductance

$g_{fs} = f(I_D)$; amp.A

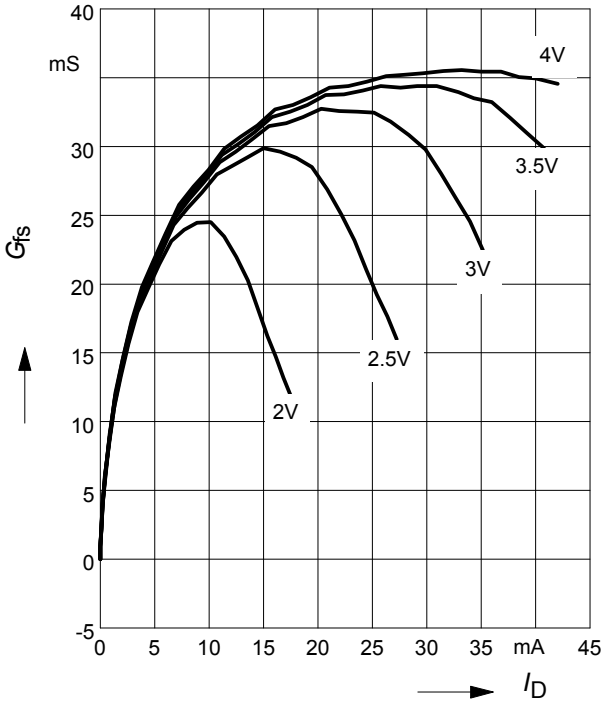
V_{DS} = 5V, V_{G2S} = Parameter



Gate 1 forward transconductance

$g_{fs} = f(I_D)$, amp. B

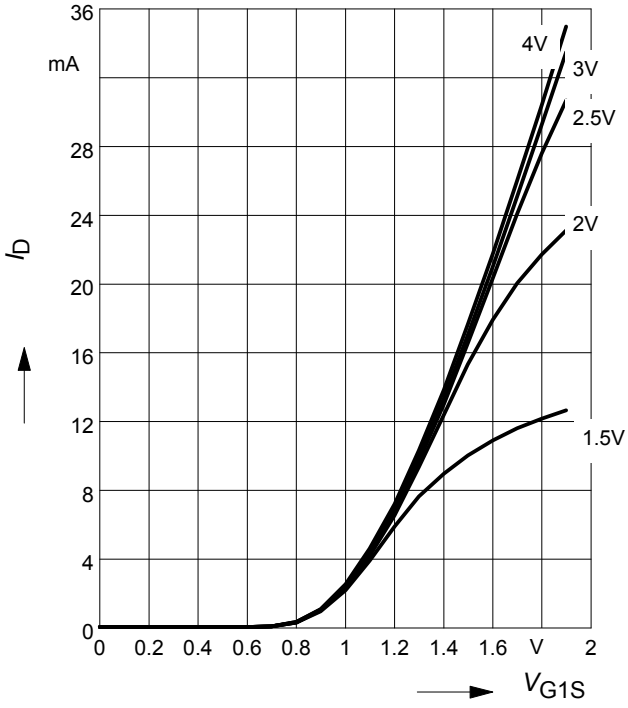
V_{DS} = 5V, V_{G2S} = Parameter



Drain current $I_D = f(V_{G1S})$

V_{DS} = 5V, amp. A

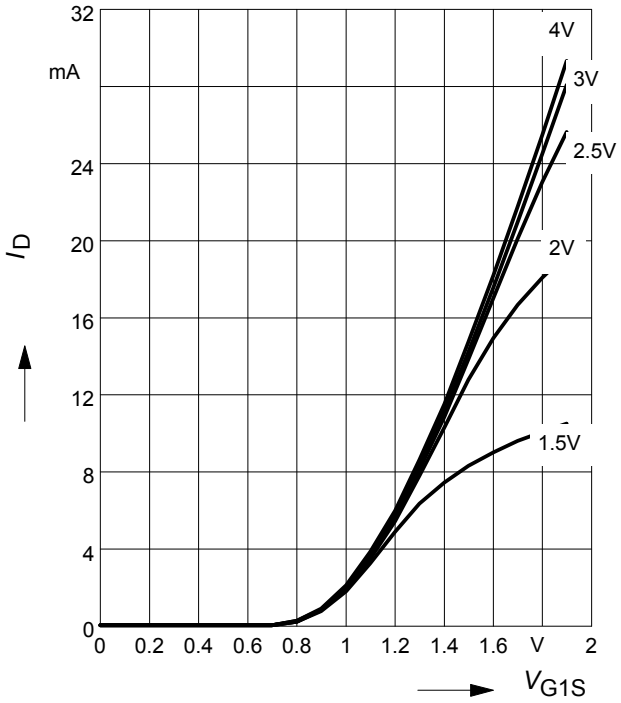
V_{G2S} = Parameter



Drain current $I_D = f(V_{G1S})$

V_{DS} = 5V, amp. B

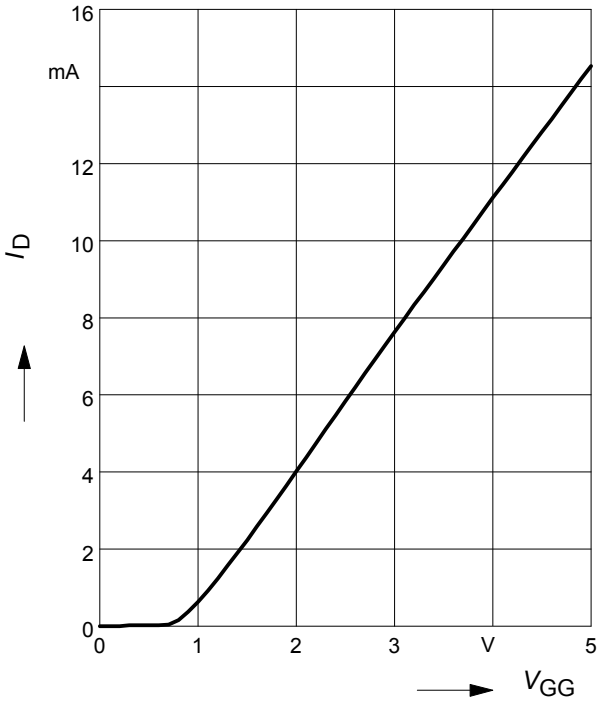
V_{G2S} = Parameter



Drain current $I_D = f(V_{GG})$, amp. B

V_{DS} = 5V, V_{G2S} = 4V, R_{G1} = 100kΩ

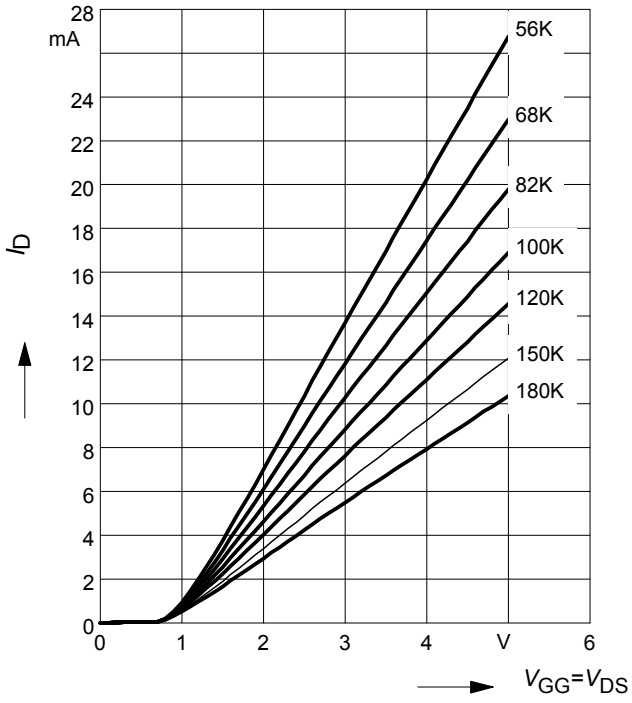
(connected to V_{GG}, V_{GG}=gate1 supply voltage)



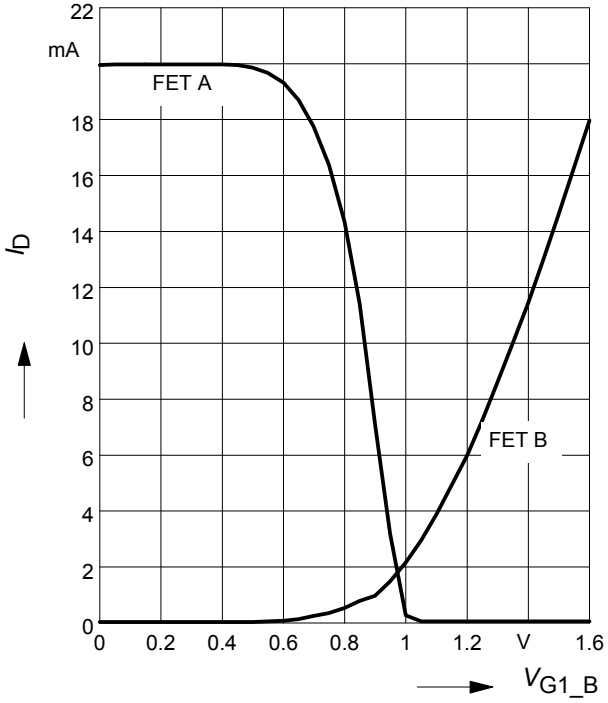
Drain current $I_D = f(V_{GG})$, amp. B

V_{DS} = 5V, V_{G2S} = 4V

(connected to V_{GG}, V_{GG}=gate1 supply voltage)

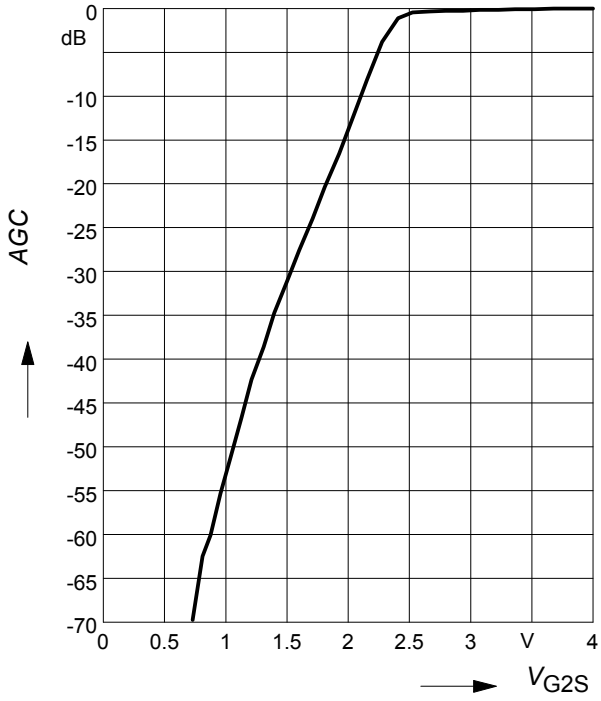


Drain current of FET A and FET B as function of Gate 1 FET B



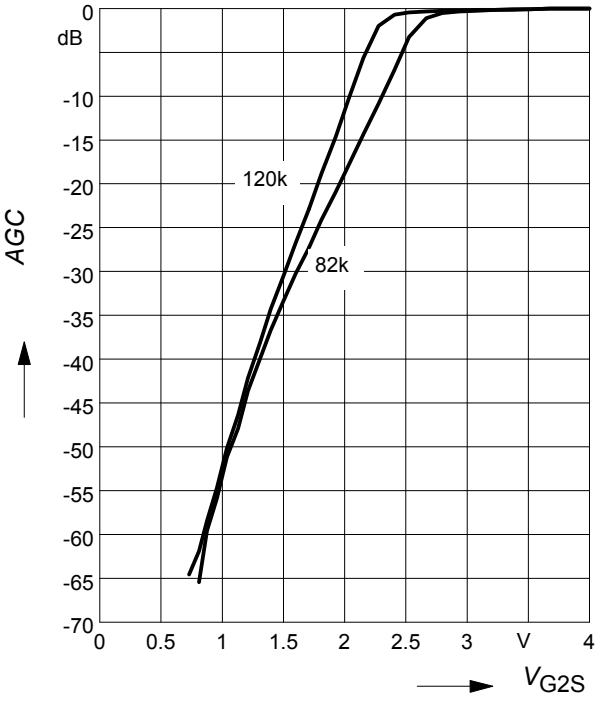
AGC characteristic $AGC = f(V_{G2S})$

f= 45 MHz, amp. A



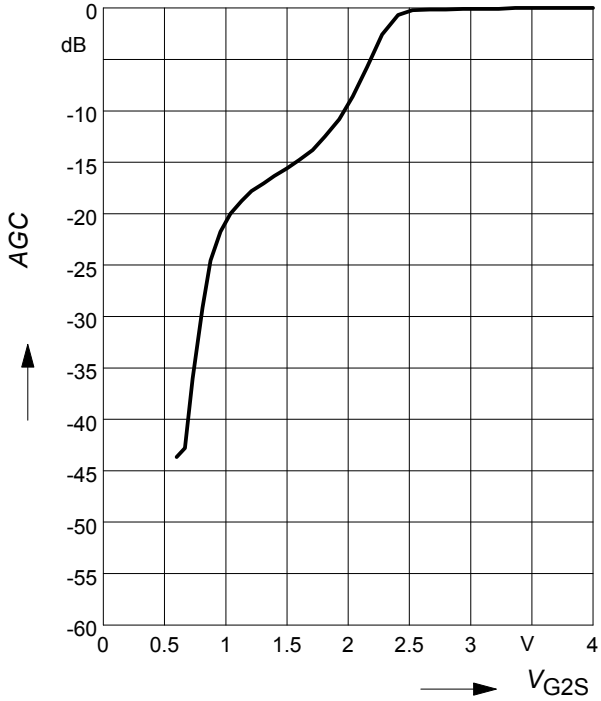
AGC characteristic $AGC = f(V_{G2S})$

f= 45 MHz, amp. B



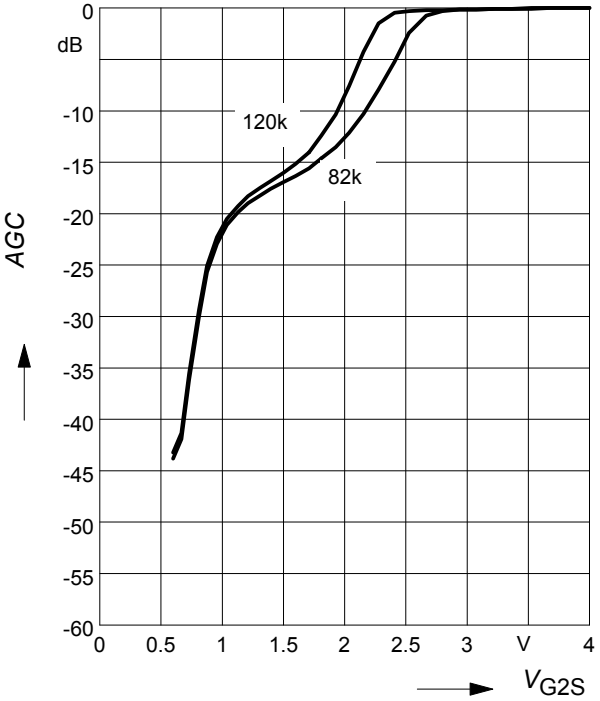
AGC characteristic $AGC = f(V_{G2S})$

f= 800MHz, amp. A



AGC characteristic $AGC = f(V_{G2S})$

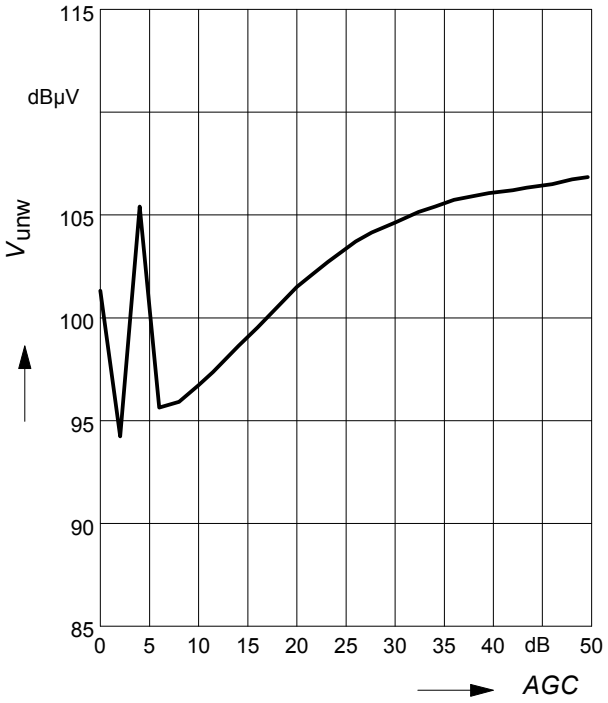
f= 800 MHz, amp. B



Crossmodulation V_{unw} = (*AGC*)

V_{DS} = 5 V, R_{g1} = 120 kΩ

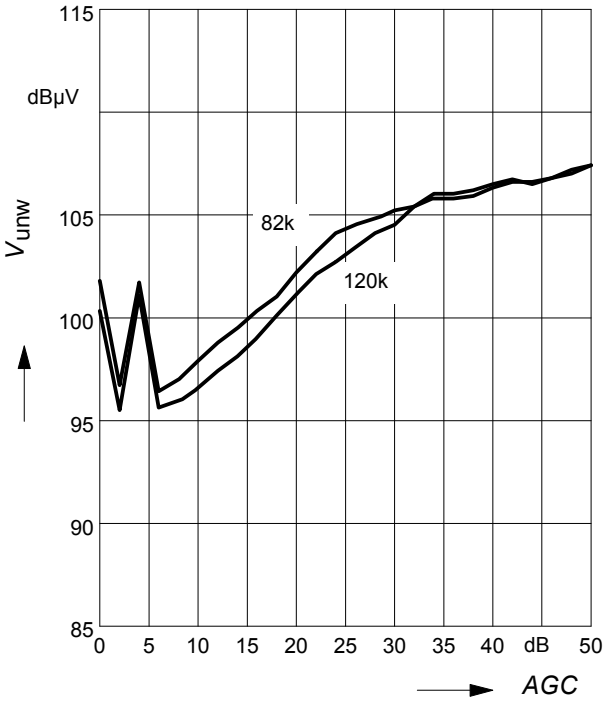
amp.A



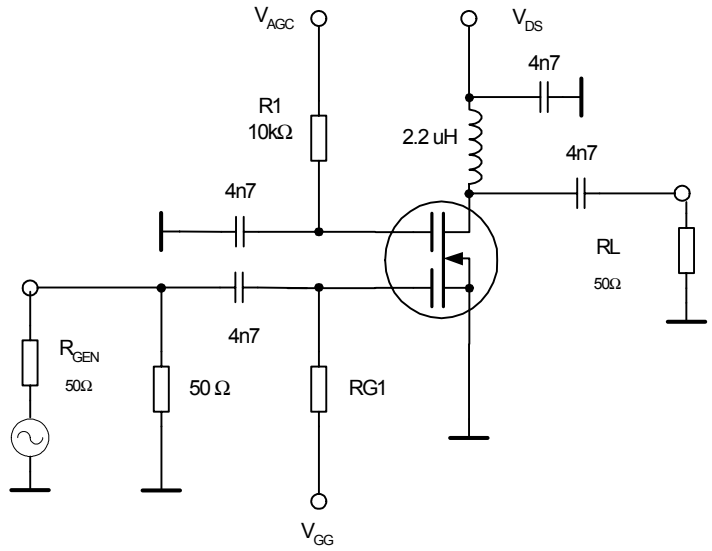
Crossmodulation V_{unw} = (*AGC*)

V_{DS} = 5 V, R_{g1} = 56 kΩ

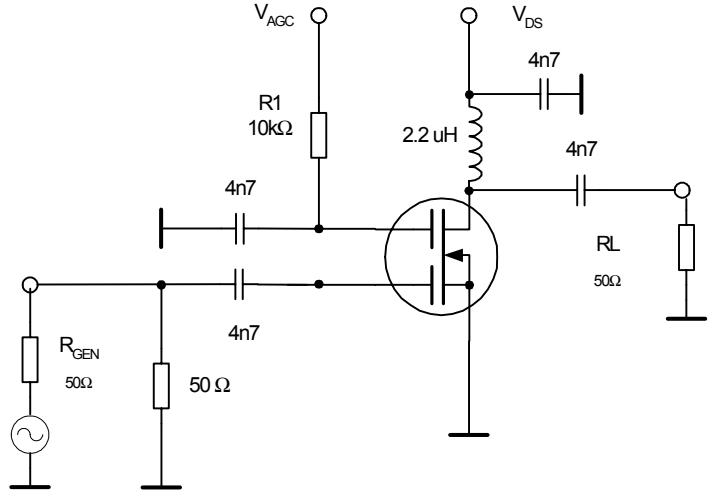
amp.B



Crossmodulation test circuit

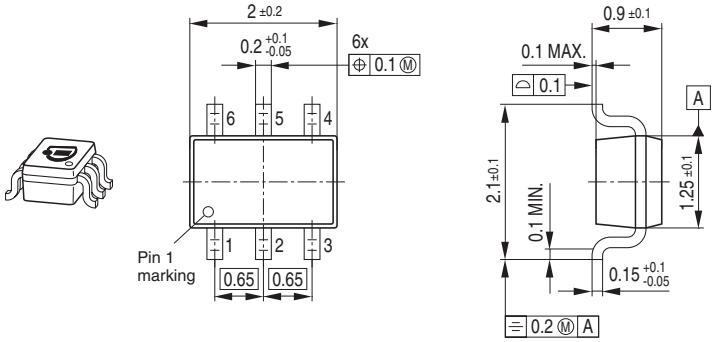


Semibiased

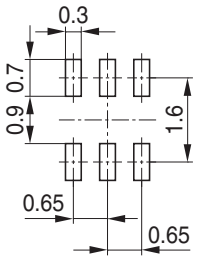


fullbiased

Package Outline

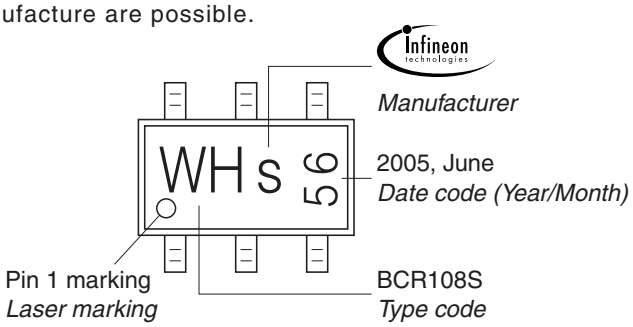


Foot Print



Marking Layout (Example)

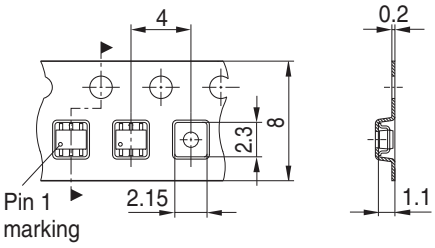
Small variations in positioning of
Date code, Type code and Manufacture are possible.



Standard Packing

Reel ø180 mm = 3.000 Pieces/Reel
Reel ø330 mm = 10.000 Pieces/Reel

For symmetric types no defined Pin 1 orientation in reel.



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