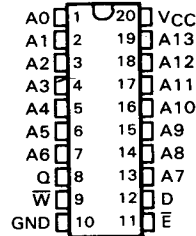


# SM61CD16, SMJ61CD16 16,384-WORD BY 1-BIT STATIC RAMS

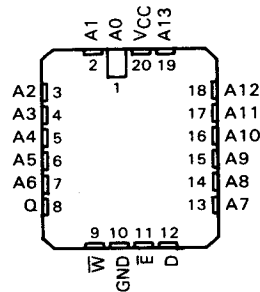
APRIL 1987—REVISED NOVEMBER 1987

- 16,384 × 1 Organization
- Separate I/O
- Military Temperature Range . . . -55°C to 125°C (M Suffix)
- Fast Static Operation
- Battery Back-Up Operation . . . 2 Volt Data Retention
- Maximum Access Time from Address or Chip Enable
  - '61CD16-25 . . . 25 ns
  - '61CD16-35 . . . 35 ns
  - '61CD16-45 . . . 45 ns
- Single 5-V Supply (10% Tolerance)
- JEDEC Standardized Pinout
- Complementary Silicon Gate MOS Technology with a 6-Transistor Memory Cell
- TTL Compatible Inputs and Outputs
- Automatic Powerdown When Deselected
  - 125 μA MAX Standby Current at CMOS Levels
- Low Power Dissipation (VCC = 5.5 V)
  - Active . . . 660 mW MAX
  - Standby . . . 110 mW MAX (TTL Inputs)
  - Standby . . . 0.68 mW MAX (CMOS Inputs)
- Standard and Class B Processing
  - SM Prefix . . . Standard Processing
  - SMJ Prefix . . . Class B Processing
- Three State Output
- Packaging Options:
  - 20-Pin Ceramic 300-mil DIP
  - 20-Pad Leadless Ceramic Chip Carrier

JD PACKAGE  
(TOP VIEW)



FG PACKAGE  
(TOP VIEW)



| PIN NOMENCLATURE |                        |
|------------------|------------------------|
| A0-A13           | Address Inputs         |
| D                | Data Input             |
| Q                | Data Output            |
| E                | Chip Enable/Power Down |
| GND              | Ground                 |
| VCC              | 5-V Supply             |
| W                | Write Enable           |

## description

The '61CD16 is a separate I/O, 16,384-bit static random-access memory organized as 16,384 words by 1 bit. This memory is fabricated using complementary MOS technology utilizing a full CMOS (six transistor cell) memory array. The six transistor cell provides for inherently lower soft error rates, improved stability across the operating temperature range, and extremely low standby power compared to the four transistor/two poly load cell making it ideal for military applications.

The '61CD16's static design and control signals ( $\bar{E}$  and  $\bar{W}$ ) remove the need for refresh circuitry and simplify timing requirements. The chip-enable pin allows for easy memory expansion and automatic power-down. Access time from either address or chip enable is a maximum of 25, 35, or 45 ns, allowing speed upgrades for new and existing designs.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SM61CD16, SMJ61CD16 16,384-WORD BY 1-BIT STATIC RAMS

## operation

### addresses (A0-A13)

The 14 address inputs select one of the 16,384-bit words in the RAM. The address inputs must be stable for the duration of a read or write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

### chip enable/power down ( $\bar{E}$ )

The chip enable/power down terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

### write enable ( $\bar{W}$ )

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode.  $\bar{W}$  or  $\bar{E}$  must be high when changing addresses to prevent inadvertently writing data into a memory location. The  $\bar{W}$  input can be driven directly from standard TTL circuits.

### data in (D)

Data can be written into a selected device when the write-enable input is low. The input terminal can be driven directly from standard TTL circuits. Data on the input pin (D) is written into the memory location specified on the address pins (A0-A13).

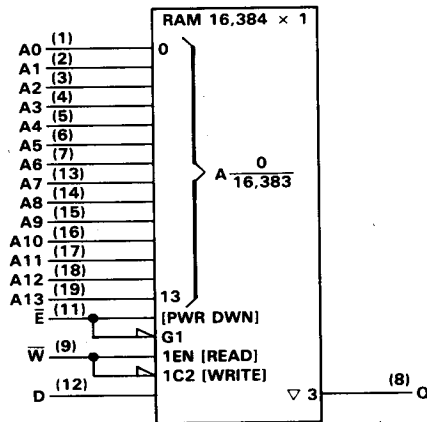
### data out (Q)

The three-state output buffer provides direct TTL compatibility with a fanout of two Series 54 TTL gates, one Series 54S TTL gate, or eight Series 54LS TTL gates. The output terminal is in the high-impedance state when chip enable ( $\bar{E}$ ) is high or whenever a write operation is being performed. Data out is the same polarity as data in.

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## logic symbol†



FUNCTION TABLE

| INPUTS    |           | OUTPUTS     | MODE    | POWER   |
|-----------|-----------|-------------|---------|---------|
| $\bar{E}$ | $\bar{W}$ | Q           |         |         |
| H         | X         | HI-Z        | Standby | Standby |
| L         | H         | Data Output | Read    | Active  |
| L         | L         | HI-Z        | Write   | Active  |

X = Don't Care.

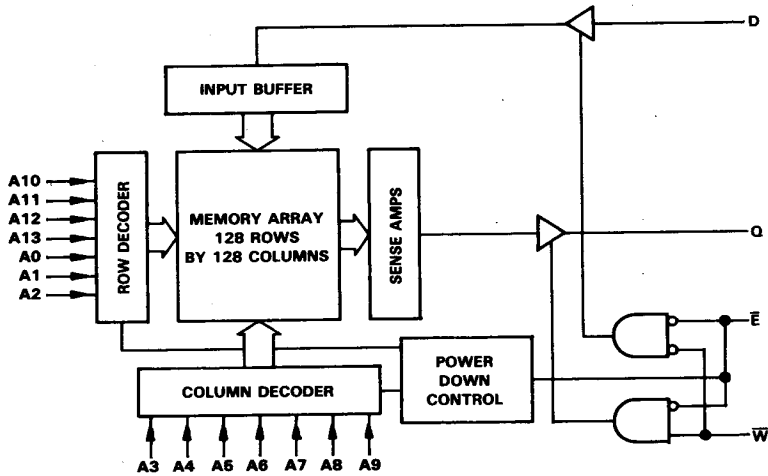
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the JD package.

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functional block diagram



**SM61CD16, SMJ61CD16**  
**16,384-WORD BY 1-BIT STATIC RAMS**

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

|                                              |                |
|----------------------------------------------|----------------|
| Supply voltage range (see Note 1)            | -0.5 V to 7 V  |
| Input voltage range (see Note 2)             | -1 V to 7 V    |
| Output voltage range in high-impedance state | -0.5 V to 7 V  |
| Output current                               | 20 mA          |
| Minimum operating free-air temperature       | -55°C          |
| Maximum operating case-temperature           | 125°C          |
| Storage temperature range                    | -65°C to 150°C |
| Latch-up current                             | 200 mA         |

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values in this data sheet are with respect to GND.

2.  $V_{IL}$  (MIN) of -3 V for short pulse durations of 20 ns or less. Prolonged operation at  $V_{IL}$  levels below -1 V will result in excessive currents that may damage the device.

**recommended operating conditions**

|                                               | MIN | NOM        | MAX | UNIT |
|-----------------------------------------------|-----|------------|-----|------|
| $V_{CC}$ Supply voltage                       | 4.5 | 5          | 5.5 | V    |
| $V_{IH}$ High-level input voltage             | 2   | $V_{CC}+1$ |     | V    |
| $V_{IL}$ Low-level input voltage (see Note 2) | -1  | 0.8        |     | V    |
| $T_C$ Operating case temperature              |     | 125        |     | °C   |
| $T_A$ Operating free-air temperature          | -55 |            |     | °C   |

**electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)**

| PARAMETER                                          | TEST CONDITIONS                              | '61CD16-25                                |     |      | '61CD16-35 |     |      | UNIT    |
|----------------------------------------------------|----------------------------------------------|-------------------------------------------|-----|------|------------|-----|------|---------|
|                                                    |                                              | MIN                                       | TYP | MAX  | MIN        | TYP | MAX  |         |
| $V_{OH}$ High-level output voltage                 | $V_{CC} = 4.5 V, I_{OH} = -4 mA$             | 2.4                                       |     |      | 2.4        |     |      | V       |
| $V_{OL}$ Low-level output voltage                  | $V_{CC} = 4.5 V, I_{OL} = 8 mA$              |                                           |     | 0.4  |            |     | 0.4  | V       |
| $I_I$ Input current (load)                         | $0 V \leq V_I \leq V_{CC}$                   | -10                                       | 10  |      | -10        | 10  |      | $\mu A$ |
| $I_O$ Output current (leakage)                     | $0 V \leq V_O \leq V_{CC}$ , Output disabled | -50                                       | 50  |      | -50        | 50  |      | $\mu A$ |
| $I_{OS}$ Short circuit output current (see Note 3) | $V_{CC} = 5.5 V, V_O = GND$                  |                                           |     | -350 |            |     | -350 | mA      |
| $I_{CC}$ $V_{CC}$ operating supply current         | $V_{CC} = 5.5 V, I_O = 0 mA$                 |                                           | 120 |      |            | 120 |      | mA      |
| $I_{CCI}$ $V_{CC}$ supply current (standby)        | TTL-level inputs                             |                                           | 20  |      |            | 20  |      | mA      |
|                                                    | CMOS-level inputs                            | Inputs = $V_{CC} \pm 0.3, V_{CC} = 5.5 V$ | 125 |      | 125        |     |      | $\mu A$ |

**electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)**

| PARAMETER                                          | TEST CONDITIONS                              | '61CD16-45                                |     |      | UNIT    |
|----------------------------------------------------|----------------------------------------------|-------------------------------------------|-----|------|---------|
|                                                    |                                              | MIN                                       | TYP | MAX  |         |
| $V_{OH}$ High-level output voltage                 | $V_{CC} = 4.5 V, I_{OH} = -4 mA$             | 2.4                                       |     |      | V       |
| $V_{OL}$ Low-level output voltage                  | $V_{CC} = 4.5 V, I_{OL} = 8 mA$              |                                           |     | 0.4  | V       |
| $I_I$ Input current (load)                         | $0 V \leq V_I \leq V_{CC}$                   | -10                                       | 10  |      | $\mu A$ |
| $I_O$ Output current (leakage)                     | $0 V \leq V_O \leq V_{CC}$ , Output disabled | -50                                       | 50  |      | $\mu A$ |
| $I_{OS}$ Short circuit output current (see Note 3) | $V_{CC} = 5.5 V, V_O = GND$                  |                                           |     | -350 | mA      |
| $I_{CC}$ $V_{CC}$ operating supply current         | $V_{CC} = 5.5 V, I_O = 0 mA$                 |                                           | 120 |      | mA      |
| $I_{CCI}$ $V_{CC}$ supply current (standby)        | TTL-level inputs                             |                                           | 20  |      | mA      |
|                                                    | CMOS-level inputs                            | Inputs = $V_{CC} \pm 0.3, V_{CC} = 5.5 V$ | 125 |      | $\mu A$ |

NOTE 3: Not more than one output should be shorted at a time. The duration of the short circuit should not exceed 30 seconds.

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data retention characteristics

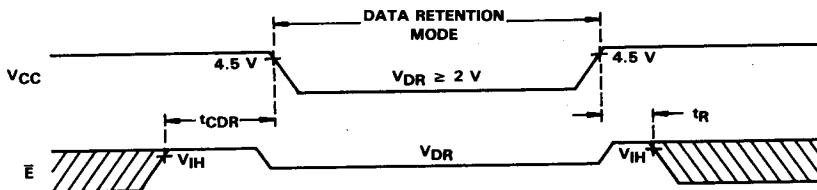
| PARAMETER                                             | TEST CONDITION                                                                                | MIN                             | TYP <sup>†</sup>        |                         | MAX                     |                         | UNIT |
|-------------------------------------------------------|-----------------------------------------------------------------------------------------------|---------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------|
|                                                       |                                                                                               |                                 | V <sub>CC</sub> @ 2.0 V | V <sub>CC</sub> @ 3.0 V | V <sub>CC</sub> @ 2.0 V | V <sub>CC</sub> @ 3.0 V |      |
| V <sub>D</sub> R V <sub>CC</sub> for data retention   | E ≥ V <sub>CC</sub> - 0.2 V,<br>V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V<br>or ≤ GND + 0.2 V | 2.0                             | —                       | —                       | —                       | —                       | V    |
| I <sub>CCDR</sub> Data retention current              |                                                                                               | 3                               | 5                       | 50                      | 75                      | —                       | μA   |
| t <sub>CDR</sub> Chip deselect to data retention time |                                                                                               | 0                               | —                       | —                       | —                       | —                       | ns   |
| t <sub>R</sub> Operation recovery time                |                                                                                               | t <sub>c(RD)</sub> <sup>‡</sup> | —                       | —                       | —                       | —                       | ns   |
| I <sub>LI</sub> <sup>§</sup> Input leakage current    |                                                                                               | —                               | —                       | —                       | 1                       | —                       | μA   |

<sup>†</sup>TYP values listed are typical values at 25 °C.

<sup>‡</sup>t<sub>c(RD)</sub> = read cycle time.

<sup>§</sup>This parameter is guaranteed but not tested.

data retention waveform



capacitance, T<sub>A</sub> = 25 °C, f = 1 MHz<sup>†</sup>

| PARAMETER                         | TEST CONDITIONS                                          | MIN | TYP | MAX | UNIT |
|-----------------------------------|----------------------------------------------------------|-----|-----|-----|------|
| C <sub>i</sub> Input capacitance  | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5 V | —   | —   | 4   | pF   |
| C <sub>o</sub> Output capacitance | T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5 V | —   | —   | 7   | pF   |

<sup>†</sup>Capacitance measurements are made on sample basis only.

timing requirements over recommended supply voltage range and operating temperature range

|                                                                           | '61CD16-25 |     |     | '61CD16-35 |     |     | UNIT |
|---------------------------------------------------------------------------|------------|-----|-----|------------|-----|-----|------|
|                                                                           | MIN        | TYP | MAX | MIN        | TYP | MAX |      |
| t <sub>c(rd)</sub> Read cycle time                                        | 25         | —   | —   | 35         | —   | —   | ns   |
| t <sub>c(wr)</sub> Write cycle time                                       | 25         | —   | —   | 35         | —   | —   | ns   |
| t <sub>w(W)</sub> Write-enable pulse duration                             | 15         | —   | —   | 20         | —   | —   | ns   |
| t <sub>ELWH</sub> Chip-enable low to end of write                         | 25         | —   | —   | 30         | —   | —   | ns   |
| t <sub>su(A)</sub> Address setup time to write start                      | 0          | —   | —   | 0          | —   | —   | ns   |
| t <sub>su(D)</sub> Data setup time to write end                           | 12         | —   | —   | 15         | —   | —   | ns   |
| t <sub>h(A)</sub> Address hold from write end                             | 0          | —   | —   | 0          | —   | —   | ns   |
| t <sub>h(D)</sub> Data hold from write end                                | 0          | —   | —   | 0          | —   | —   | ns   |
| t <sub>ELIH</sub> Delay time, chip-enable low to power up <sup>§</sup>    | 5          | —   | —   | 5          | —   | —   | ns   |
| t <sub>EHIL</sub> Delay time, chip-enable high to power down <sup>§</sup> | —          | —   | 35  | —          | —   | 35  | ns   |
| t <sub>AVWH</sub> Address setup to write end                              | 25         | —   | —   | 30         | —   | —   | ns   |

<sup>§</sup>This parameter is guaranteed but not tested.



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**timing requirements over recommended supply voltage range and operating temperature range**

|             |                                                         | '61CD16-45 |     |     | UNIT |
|-------------|---------------------------------------------------------|------------|-----|-----|------|
|             |                                                         | MIN        | TYP | MAX |      |
| $t_{C(rd)}$ | Read cycle time                                         | 45         |     |     | ns   |
| $t_{C(wr)}$ | Write cycle time                                        | 45         |     |     | ns   |
| $t_{w(W)}$  | Write-enable pulse duration                             | 20         |     |     | ns   |
| $t_{ELWH}$  | Chip-enable low to end of write                         | 40         |     |     | ns   |
| $t_{su(A)}$ | Address setup time to write start                       | 0          |     |     | ns   |
| $t_{su(D)}$ | Data setup time to write end                            | 15         |     |     | ns   |
| $t_{h(A)}$  | Address hold from write end                             | 0          |     |     | ns   |
| $t_{h(D)}$  | Data hold from write end                                | 0          |     |     | ns   |
| $t_{ELIH}$  | Delay time, chip-enable low to power up <sup>†</sup>    | 5          |     |     | ns   |
| $t_{EHIL}$  | Delay time, chip-enable high to power down <sup>†</sup> |            |     | 35  | ns   |
| $t_{AVWH}$  | Address setup to write end                              | 40         |     |     | ns   |

<sup>†</sup>This parameter is guaranteed but not tested.

**switching characteristics over recommended supply voltage range and operating temperature range**

| PARAMETER    | TEST CONDITIONS                                        | '61CD16-25 |     |     | '61CD16-35 |     |     | UNIT |
|--------------|--------------------------------------------------------|------------|-----|-----|------------|-----|-----|------|
|              |                                                        | MIN        | TYP | MAX | MIN        | TYP | MAX |      |
| $t_{a(A)}$   | Access time from address                               | 25         |     |     | 35         |     |     | ns   |
| $t_{a(E)}$   | Access time from chip enable low                       | 25         |     |     | 35         |     |     | ns   |
| $t_{v(A)}$   | Output data valid after address change                 | 0          | 3   |     | 0          | 3   |     | ns   |
| $t_{en(W)}$  | Output enable time from write enable high <sup>‡</sup> | 0          |     | 15  | 0          |     | 20  | ns   |
| $t_{en(E)}$  | Output enable time from chip enable low <sup>‡</sup>   | 5          |     |     | 5          |     |     | ns   |
| $t_{dis(E)}$ | Output disable time from chip enable high <sup>‡</sup> | 10         |     |     | 15         |     |     | ns   |
| $t_{dis(W)}$ | Output disable time from write enable low <sup>‡</sup> | 10         |     |     | 15         |     |     | ns   |

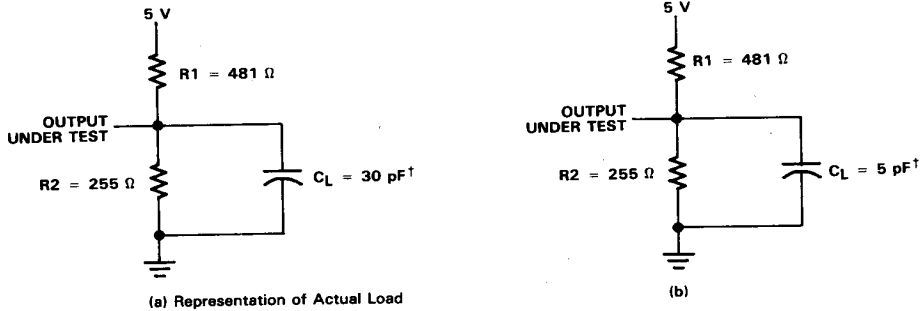
**switching characteristics over recommended supply voltage range and operating temperature range**

| PARAMETER    | TEST CONDITIONS                                        | '61CD16-45 |     |     | UNIT |
|--------------|--------------------------------------------------------|------------|-----|-----|------|
|              |                                                        | MIN        | TYP | MAX |      |
| $t_{a(A)}$   | Access time from address                               | 45         |     |     | ns   |
| $t_{a(E)}$   | Access time from chip enable low                       | 45         |     |     | ns   |
| $t_{v(A)}$   | Output data valid after address change                 | 0          | 3   |     | ns   |
| $t_{en(W)}$  | Output enable time from write enable high <sup>‡</sup> | 0          |     | 20  | ns   |
| $t_{en(E)}$  | Output enable time from chip enable low <sup>‡</sup>   | 5          |     |     | ns   |
| $t_{dis(E)}$ | Output disable time from chip enable high <sup>‡</sup> | 20         |     |     | ns   |
| $t_{dis(W)}$ | Output disable time from write enable low <sup>‡</sup> | 20         |     |     | ns   |

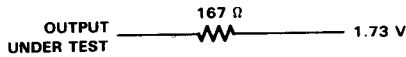
<sup>‡</sup>Transition is measured  $\pm 500$  mV from steady state voltage; this parameter is guaranteed but not tested.

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PARAMETER MEASUREMENT INFORMATION

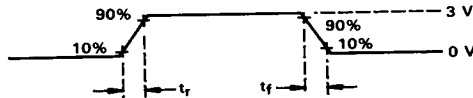


THEVENIN EQUIVALENT OF (a) OR (b)



<sup>†</sup> $C_L$  includes jig and scope capacitances.

FIGURE 1. OUTPUT LOAD CIRCUIT

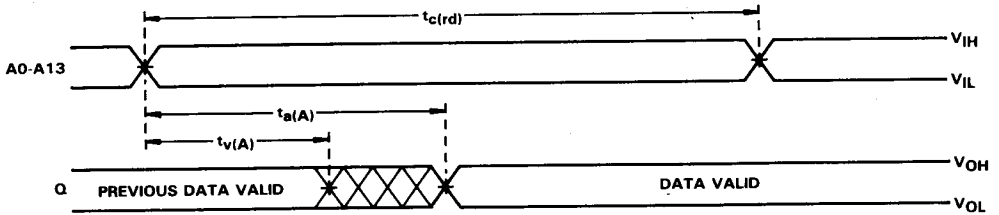


NOTE 4:  $t_r$  and  $t_f \leq 5$  ns.

FIGURE 2. TRANSITION TIMES

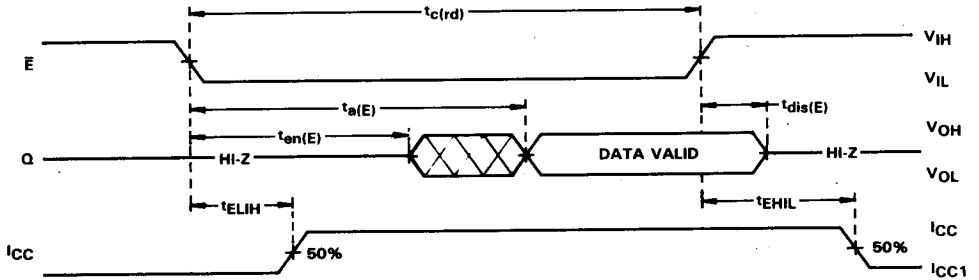
**SM61CD16, SMJ61CD16**  
**16,384-WORD BY 1-BIT STATIC RAMS**

read cycle timing from address<sup>†</sup>



<sup>†</sup> $\bar{W}$  is high, and  $\bar{E}$  is low.

read cycle timing from chip enable<sup>‡</sup>



<sup>‡</sup> $\bar{W}$  is high, address is valid prior to or simultaneously with the high-to-low transition of  $\bar{E}$ .

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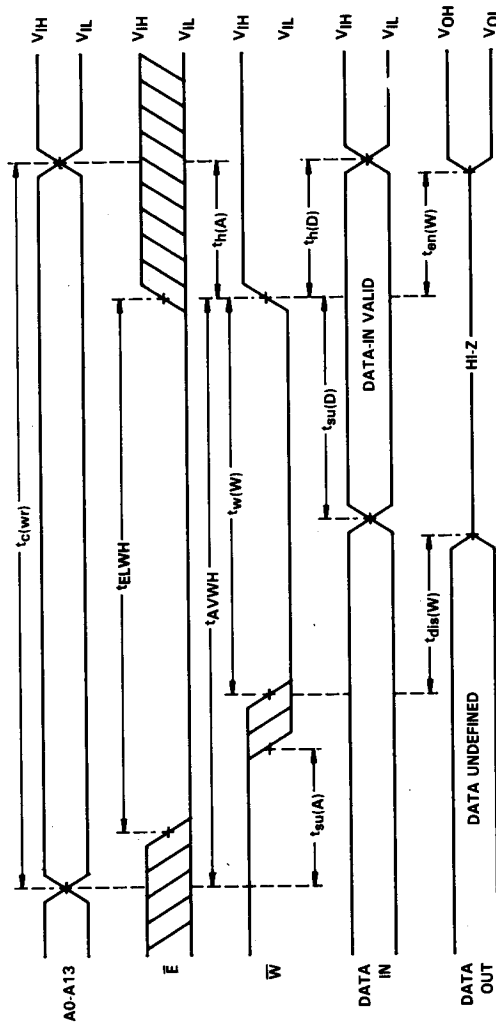
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write cycle timing controlled by write enable†



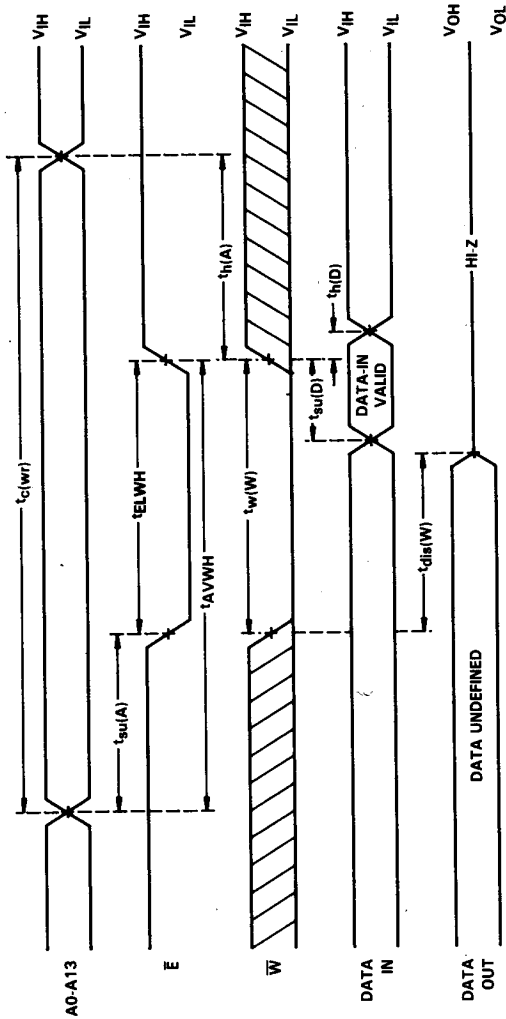
†E or W must be high during address transitions.  
NOTE: For both W-controlled and E-controlled Write operations, the internal write time of the memory is defined by the overlap of E low and W low. Both signals must be low to initiate a write, and either signal can terminate a write by going high. The data input setup and hold times should be referenced to the edge that terminates the write.

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write cycle timing controlled by chip enable†



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†E or  $\bar{W}$  must be high during address transitions.