MP86972

60A, Intelli-Phase Solution™ with Integrated HS-FETs, LS-FETs, and Driver in a TLGA-35 (3mmx6mm) Package

DESCRIPTION

The MP86972 is a monolithic half-bridge driver with built-in internal power MOSFETs and gate drivers. It achieves 60A of continuous output current across a wide input supply range.

The device can drive up to 60A per phase. The integrated drivers and MOSFETs result in high efficiency due to an optimal dead time and reduced parasitic inductance. The device operates from 100kHz to 3MHz.

The MP86972 offers many features to simplify system design, and works with controllers with a tri-state PWM signal. It also comes with an accurate current sense to monitor the inductor current, and temperature sense to report junction temperature.

MP86972 is ideal for server applications where efficiency and small size are a premium. The device is available in a TLGA-35 (3mmx6mm) package.

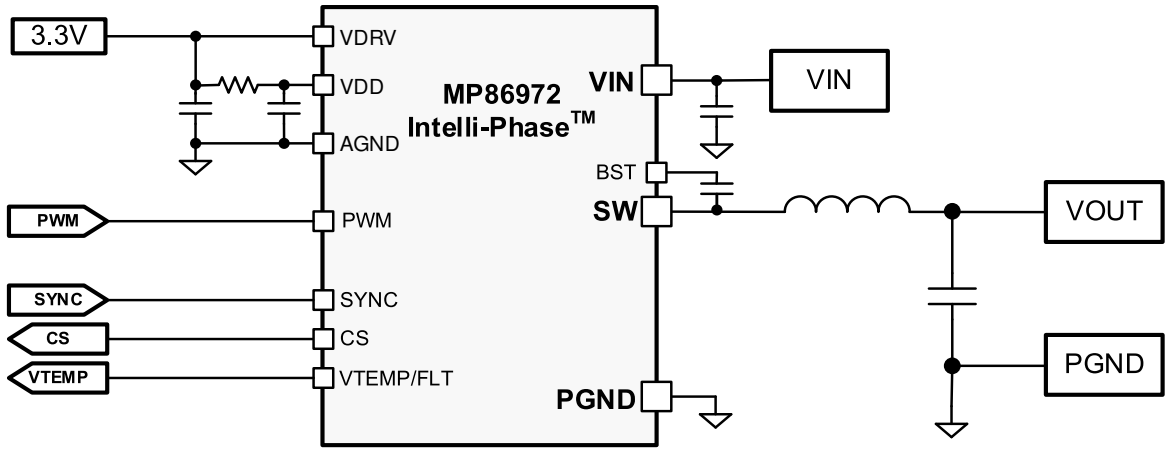
FEATURES

- Wide 3V to 12V Operating Input Range
- 60A Output Current
- Accu-Sense™ Current Sense
- Temperature Sense
- Accepts Tri-State PWM Signal
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in a TLGA (3mmx6mm) Package

APPLICATIONS

- Server Core Voltages
- Graphic Card Core Regulators
- Power Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP86972GLJTH*	TLGA-35 (3mmx6mm)	*See Below*	3

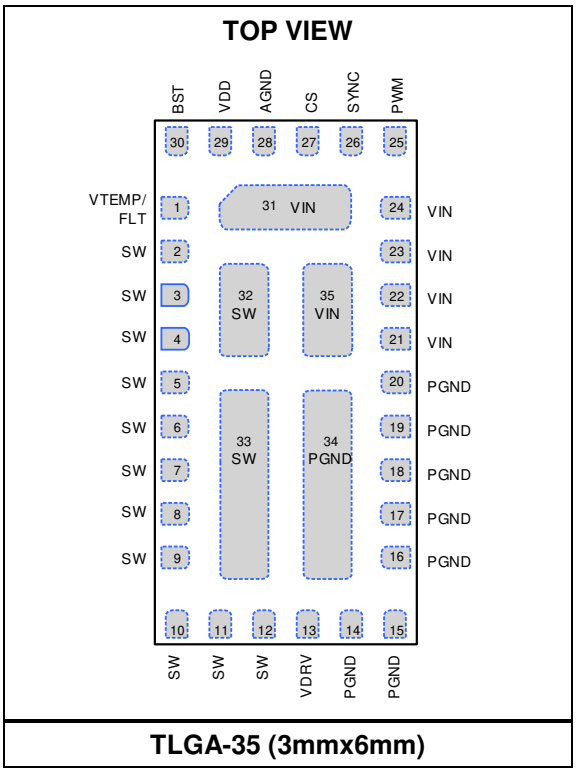
* For Tape & Reel, add suffix -Z (e.g. MP86972GLJTH-Z).

TOP MARKING

MPYW
8697
2LLL
TH

MP: MPS prefix
Y: Year code
W: Week code
86972: First five digits of the part number
LLL: Lot number
TH: Thin package

PACKAGE REFERENCE



TLGA-35 (3mmx6mm)

PIN FUNCTIONS

Pin #	Name	Description
1	VTEMP/FLT	**Single-pin temperature sense and fault reporting.** If a fault occurs, this pin is pulled up to 3.3V.
2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 32, 33	SW	**Phase node.**
13	VDRV	**Driver voltage.** Connect VDRV to a 3.3V supply and decouple it with a 1µF to 4.7µF ceramic capacitor.
14, 15, 16, 17, 18, 19, 20, 34	PGND	**Power ground.**
21, 22, 23, 24, 31, 35	VIN	**Supply voltage.** Place a capacitor (C_{IN}) close to the device to support the switching current and reduce voltage spikes at the input.
25	PWM	**Pulse-width modulation input.** Float the PWM pin or drive it to a middle-state to put SW in a high impedance state.
26	SYNC	**Diode emulation mode and standby mode selection.** Float the SYNC pin or drive SYNC to a middle-state to enter standby mode. Pull SYNC high for continuous conduction mode (CCM). Pull SYNC low to enable diode emulation mode.
27	CS	**Current-sense output.** Use an external resistor to adjust the voltage so that it is proportional to the inductor current.
28	AGND	**Analog ground.**
29	VDD	**Internal circuitry voltage.** Connect VDD to VDRV via a 2.2Ω resistor. Decouple VDD with a 1µF capacitor connected to AGND. Connect AGND and PGND at the VDD capacitor.
30	BST	**Bootstrap.** BST requires a 0.1µF to 1µF capacitor to drive the power switch's gate above the supply voltage. Connect the capacitor between the SW and BST pins to form a floating supply across the power switch driver.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} to PGND..... -0.3V to +16V
V_{IN} to V_{SW}..... -0.3V to +16V
V_{IN} to V_{SW} (10ns).....22V
V_{SW} to PGND ..... -0.3V to +14V
V_{SW} to PGND (25ns) ..... -10V to +20V
V_{BST} .....V_{SW} + 4V
V_{DD}, V_{DRV}..... -0.3V to +4V
All other pins.....-0.3V to V_{DD} + 0.3V
Instantaneous current 95A
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....±2kV
Charged device model (CDM).....±1.5kV

Recommended Operating Conditions (2)

Supply voltage (V_{IN}) ..... 3V to 12V
Driver voltage (V_{DRV}) ..... 3.0V to 3.6V
Logic voltage (V_{DD})..... 3.0V to 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

TLGA-35 (3mmx6mm).....2.2.....8.0....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB}: Thermal resistance from the junction to the board around the PGND soldering point.
   θ_{JC_TOP}: Thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{IN} = 6V, V_{DRV} = V_{DD} = SYNC = 3.3V, T_A = 25°C for typical values, T_J = -40°C to +125°C for maximum and minimum values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown	I_{IN_OFF}	SYNC = Hi-Z		90	180	µA
VIN under-voltage lockout threshold rising				2.5	2.9	V
VIN under-voltage lockout threshold hysteresis				450		mV
I_{VDRV} quiescent current		PWM = low			400	µA
I_{VDD} quiescent current		PWM = low		3		mA
VDD voltage UVLO rising				2.75	2.9	V
VDD voltage UVLO hysteresis				250		mV
High-side current limit (4)	I_{LIM_FLT}	Cycle by cycle up to 4 cycles		90		A
Low-side current limit (4)		Negative current limit, cycle by cycle, no fault report		-30		A
Negative current limit low-side off time (4)				200		ns
High-side current limit shutdown counter (4)				4		Times
Dead-time rising (4)				2		ns
Dead-time falling (4)		Positive inductor current		8		ns
		Negative inductor current		35		ns
SYNC logic high voltage		V_{DD} = 3V	2.4			V
		V_{DD} = 3.6V	2.6			V
SYNC tri-state region		V_{DD} = 3V	1.1		1.65	V
		V_{DD} = 3.6V	1.3		1.95	V
SYNC logic low voltage		V_{DD} = 3V			0.6	V
		V_{DD} = 3.6V			0.7	V
PWM high to SW rising delay (4)	t_{RISING}			15		ns
PWM low to SW falling delay (4)	$t_{FALLING}$			15		ns
PWM tri-state to SW Hi-Z delay (4)	t_{LT}			40		ns
	t_{TL}			50		ns
	t_{HT}			40		ns
	t_{TH}			50		ns

ELECTRICAL CHARACTERISTICS *(continued)*

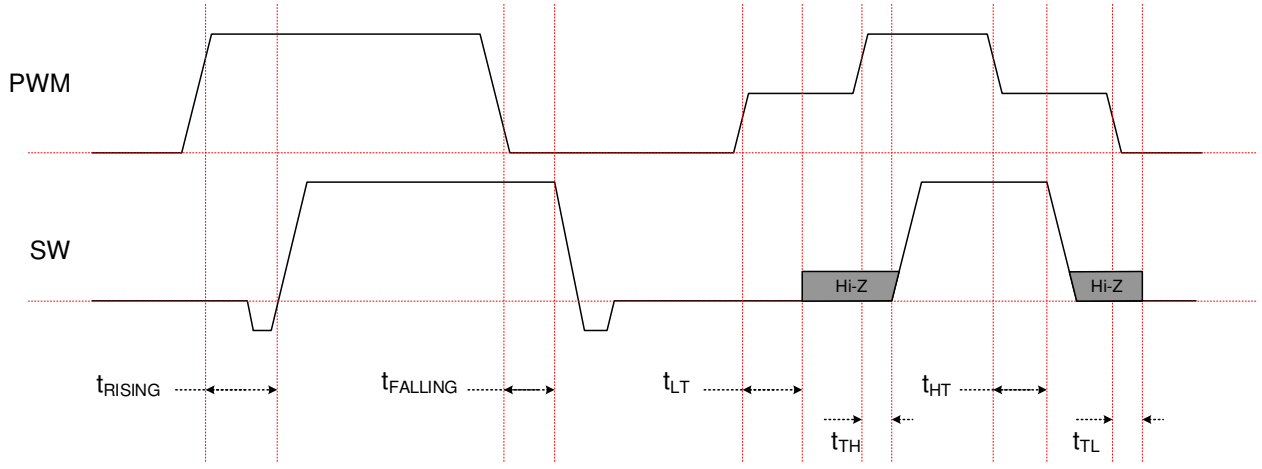
V_{IN} = 6V, V_{DRV} = V_{DD} = SYNC = 3.3V, T_A = 25°C for typical values, T_J = -40°C to +125°C for maximum and minimum values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Minimum PWM pulse width (4)				20		ns
Current-sense gain accuracy (4)		20A ≤ I_{SW} ≤ 60A	-2		+2	%
Current-sense gain				8		µA/A
Current-sense offset		I_{SW} = 0A, V_{CS} = 1.2V, T_J = 25°C	-2		+2	µA
		SW Hi-Z, V_{CS} = 1.2V	-1		+1	µA
CS voltage range (4)	V_{CS}		0.7		2.1	V
VTEMP/FLT sense gain (4)				10		mV/°C
VTEMP/FLT sense offset (4)		T_J = 25°C		-100		mV
Over-temperature shutdown and fault flag (4)				160		°C
VTEMP/FLT if a fault occurs (4)				V_{DD}		V
PWM resistor		Pull-up, SYNC= low or high		6		kΩ
		Pull down		5		kΩ
PWM logic high voltage		V_{DD} = 3V	2.4			V
		V_{DD} = 3.6V	2.4			V
PWM tri-state region		V_{DD} = 3V	1.1		1.8	V
		V_{DD} = 3.6V	1.1		1.8	V
PWM logic low voltage		V_{DD} = 3V			0.8	V
		V_{DD} = 3.6V			0.8	V

Notes:

4) Guaranteed by design or characterization data. Not tested in production.

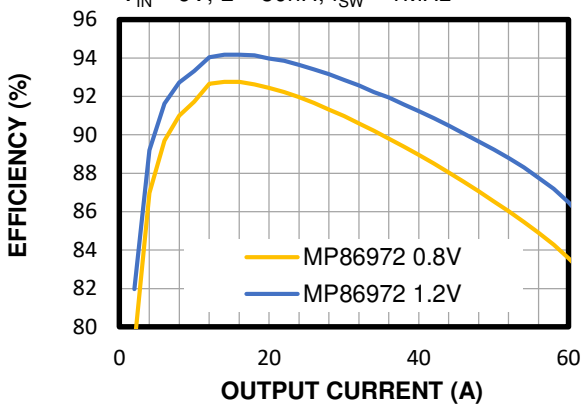
PWM TIMING DIAGRAM



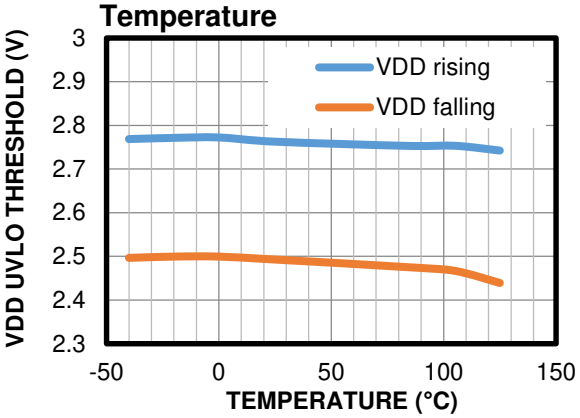
TYPICAL CHARACTERISTICS

Efficiency

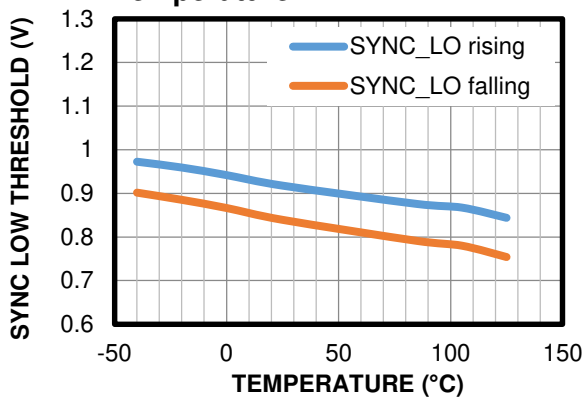
V_{IN} = 6V, L = 50nH, f_{SW} = 1MHz



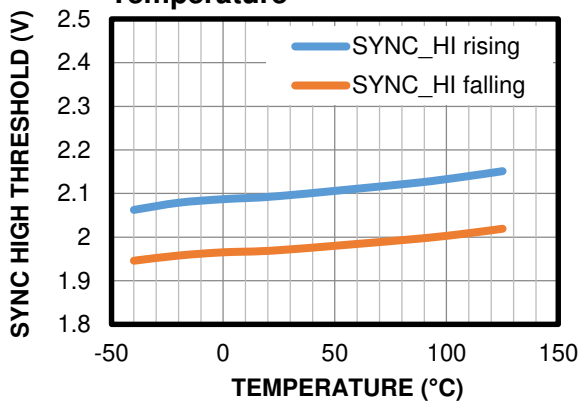
VDD UVLO Threshold vs. Temperature



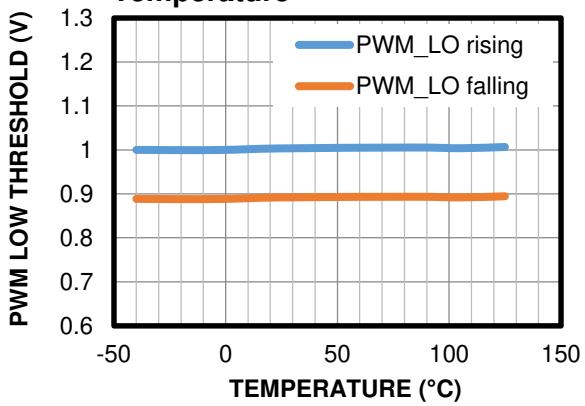
SYNC Low Threshold vs. Temperature



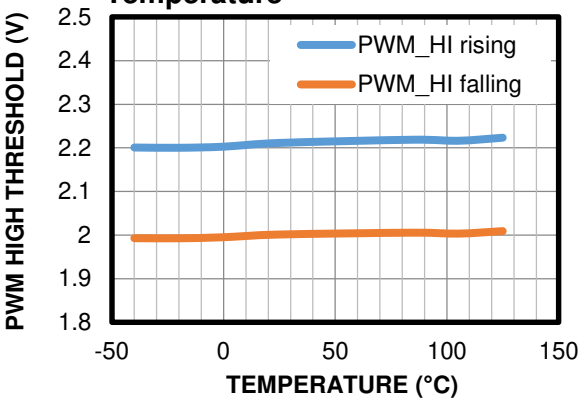
SYNC High Threshold vs. Temperature



PWM Low Threshold vs. Temperature



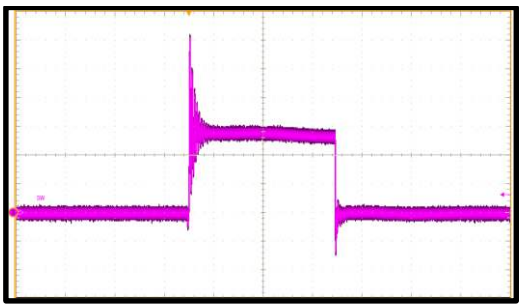
PWM High Threshold vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

Switching Waveform

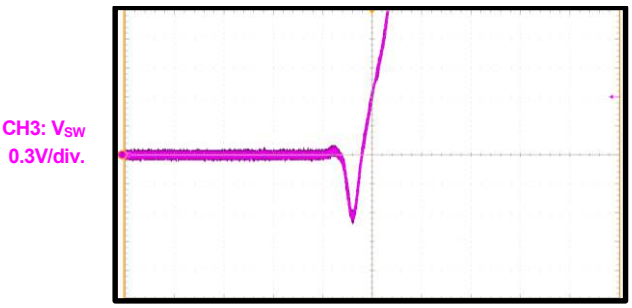
V_{IN} = 6V,L = 50nH, I_{OUT} = 30A



100ns/div.

Dead Time at SW Rising

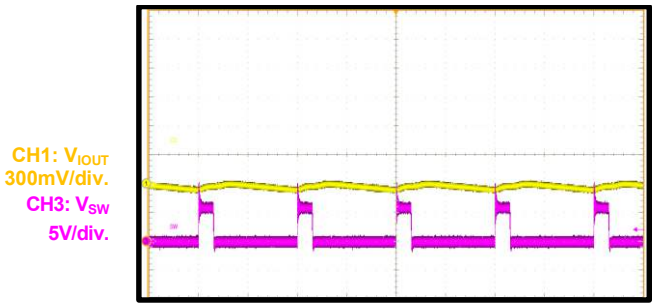
I_{OUT} = 30A



2.5ns/div.

CS Output Waveform

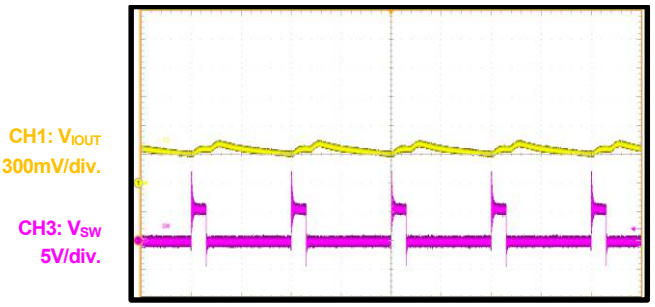
I_{OUT} = 0A



500ns/div.

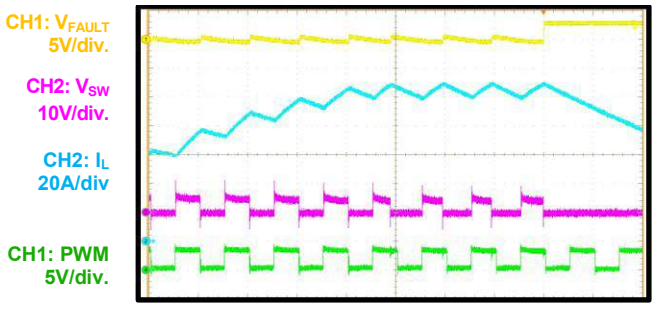
CS Output Waveform

I_{OUT} = 30A



500ns/div.

High-Side Current Limit



2µs/div.

FUNCTIONAL BLOCK DIAGRAM

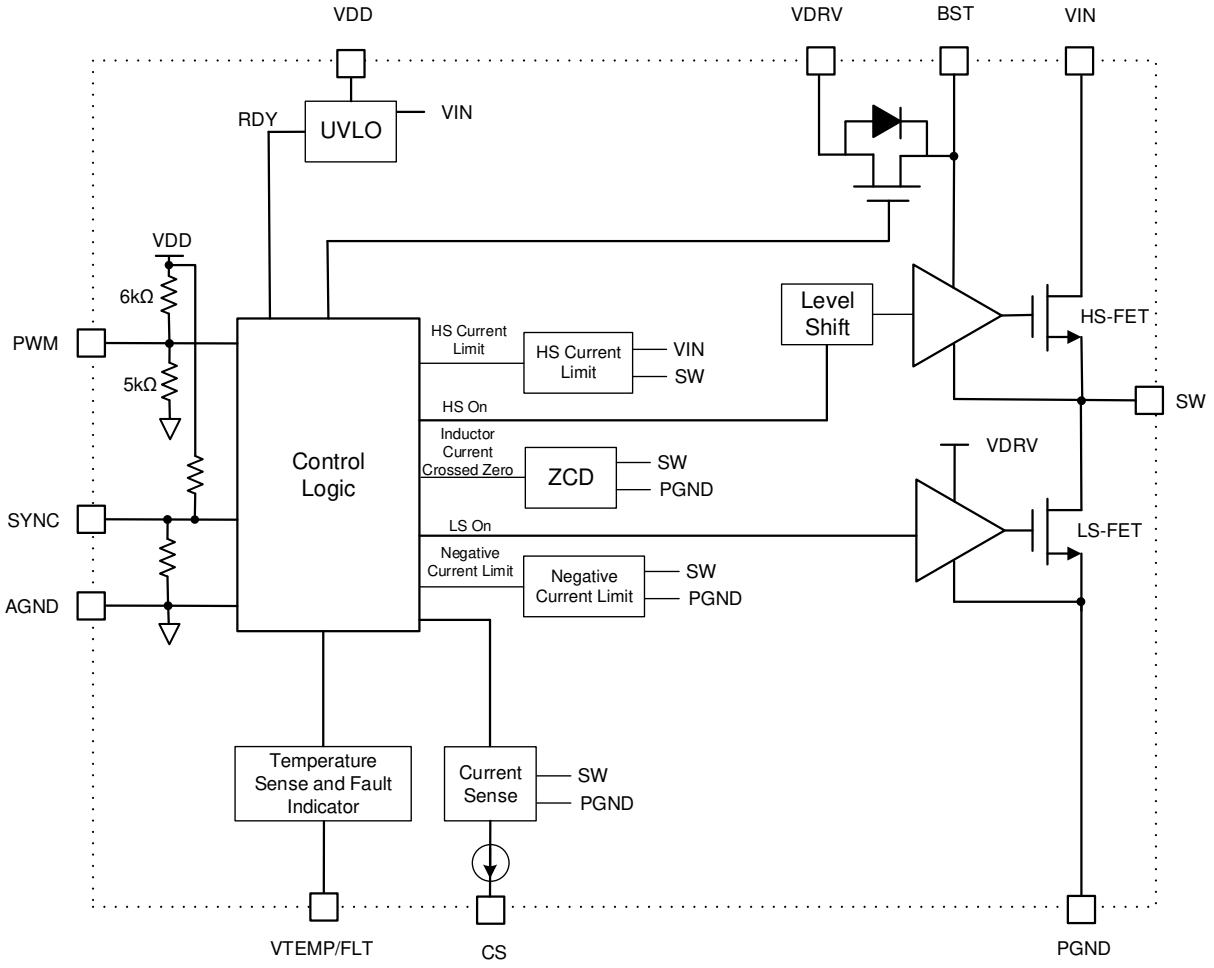


Figure 1: Functional Block Diagram

OPERATION

The MP86972 is a 60A, monolithic half-bridge driver with MOSFETs. It is well-suited for multi-phase buck regulators. An external 3.3V is required to supply both VDD and VDRV. When the VIN and VDD signals are sufficiently high, operation begins.

PWM

The PWM input pin is capable of tri-state input. If the PWM input signal is within the tri-state threshold window for about 50ns (t_{HL} or t_{LT}), the high-side MOSFET (HS-FET) turns off immediately. The low-side MOSFET (LS-FET) enters diode emulation mode, and stays on until zero-current detection (ZCD).

The tri-state PWM input is enabled by forcing a middle-voltage PWM signal, or by floating the PWM input. The internal current source charges the signal to a middle voltage. See the PWM Timing Diagram on page 6 to define the propagation delay from PWM to the SW node.

Standby Mode

When the SYNC pin is floating or forced to a middle-state voltage for 2µs, the MP86972 enters standby mode. While in standby mode, the MP86972 shuts down, and both the CS and VTEMP/FLT outputs are disabled. The fault (VTEMP/FLT) latch is not be reset by entering standby mode.

Diode Emulation Mode

When PWM is low or in tri-state input in diode emulation mode, the LS-FET turns on when the inductor current is positive. The LS-FET turns off if the inductor current reaches 0A or becomes negative. There are three ways to enable diode emulation mode, listed below:

- Pull the SYNC pin low.
- Drive the PWM pin to s middle-state.
- Float the PWM pin.

Current Sense (CS)

CS is a bidirectional current source that is proportional to the inductor current. The current-sense gain is 8µA/A. If required, a resistor can be used to configure the voltage gain proportional to the inductor current.

The CS output has two states (see Table 1). In standby mode, the CS circuit is disabled. It takes the device 40µs to exit standby mode and enter active mode.

Table 1: CS Output States

PWM	SYNC	CS
PWM	High	Active
PWM	Low	Active
x	Hi-Z (or middle)	Standby

To obtain an accurate CS output up to +480µA/-240µA (e.g. +60A/-30A), the CS pin's voltage must be between 0.7V and 2.1V. Generally, there is a resistor (R_{CS}) connected from the CS pin to an external voltage that is capable of sinking small currents. This provides a sufficient voltage level to meet the required operating voltage range.

Choose a value for R_{CS} to determine a proper reference voltage (V_{CM}). The relationship between R_{CS} and V_{CM} can be calculated with Equation (1):

$$0.7V < I_{CS} \times R_{CS} + V_{CM} < 2.1V \quad (1)$$

Where V_{CM} is a reference voltage connected to R_{CS}, and I_{CS} can be estimated with Equation (2):

$$I_{CS} = I_L \times G_{CS} \quad (2)$$

The Intelli-Phase's™ current-sense output can be used by the controller to accurately monitor the output current. The cycle-by-cycle current information from the CS pin can be used for phase current balancing, over-current protection, and active voltage positioning (output voltage droop).

Positive and Negative Inductor Current limit

If an over-current (OC) condition is detected on the HS-FET, the HS-FET turns off for that PWM cycle. If the OC conditions lasts four consecutive cycles, the HS-FET latches off, VTEMP/FLT is pulled up to VDD, and the LS-FET turns on, and stays on until ZCD. To release the latch and restart the device, power must be cycled on VIN or VDD.

If the LS-FET detects a -30A current, the part turns off the LS-FET for 200ns to limit the

negative current. The LS-FET's negative current limit does not trigger a fault report.

Temperature-Sense Output with Fault Indication (VTEMP/FLT)

The VTEMP/FLT pin can sense the junction temperature or indicate if certain faults have occurred.

Junction Temperature Sense

When VDD exceeds its under-voltage lockout (UVLO) threshold and the part is in active mode, the VTEMP/FLT pin has an output voltage that is proportional to the junction temperature. The gain is 10mV/°C, and it has a -100mV offset at 25°C. For example, the voltage is 0V when T_J < 10°C, 0.15V when T_J = 25°C, and 0.9V when T_J = 100°C.

Fault Indication

If any fault occurs, VTEMP/FLT is typically pulled up to 3.3V (or a 3.0V minimum) to report the fault event, regardless of the temperature. After the fault occurs for 200ns, the PWM impedance changes according to the fault type. Table 2 lists how the PWM status changes for each fault type.

Table 2: PWM Resistance if a Fault Occurs

Fault Type	PWM
Current-limit protection	10kΩ to AGND
Over-temperature protection	20kΩ to AGND
SW-to-PGND short protection	1kΩ to VDD

The three fault events are described below:

1. Over-current limit: The current limit fault condition must remain for eight consecutive cycles to trigger this fault. If this fault occurs, the part latches off to turn off the HS-FET. The LS-FET turns on and stays on until the current reaches 0A. The PWM pin is pulled to GND through a 10kΩ resistor to indicate this fault type.
2. Over-temperature fault when T_J > 160°C: If an over-temperature fault occurs, the part latches off, and the HS-FET turns off. The LS-FET turns on and stays on until the current reaches 0A. The PWM is pulled to GND through a 20kΩ resistor to indicate this fault type.
3. SW-to-PGND short: If a short fault occurs, the part latches off to turn off the HS-FET. The PWM pin is pulled high (1kΩ to VDD) to indicate the fault type.

The fault latch is not be reset by entering standby mode. The fault latch can be released by cycling power on VIN or VDD.

For multi-phase operation, connect the VTEMP/FLT pins of each Intelli-Phase™ together (see Figure 2).

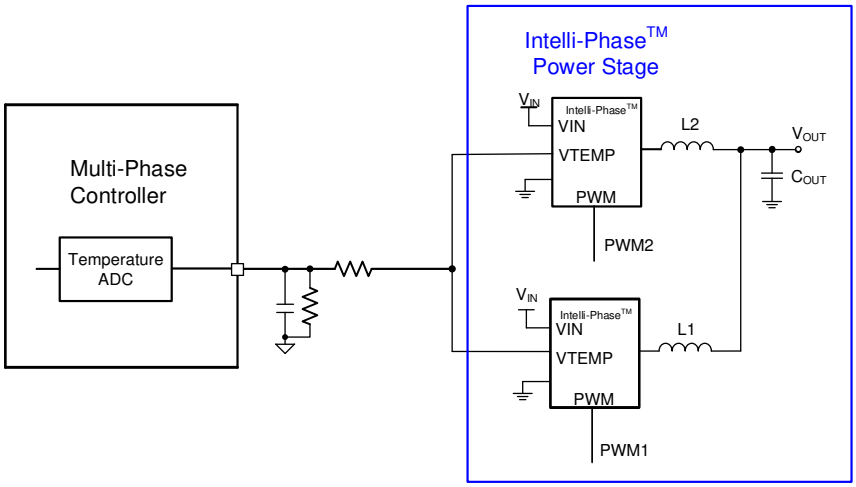


Figure 2: Multi-Phase Temperature Sense Utilization

APPLICATION INFORMATION

PCB Layout Guidelines

PCB layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the VIN and PGND pins as possible.
2. Place the major MLCC capacitors on the same layer as the MP86972.
3. Place as many VIN and PGND vias underneath the package as possible, as well as between the VIN or PGND long pads.
4. Place a VIN copper plane on the second inner layer to form the PCB stack as positive/negative/positive to reduce the parasitic impedance from the input MLCC capacitor.
5. Ensure that the inner layer copper planes cover the VIN vias that are beneath the package and input MLCC capacitors.
6. Place more PGND vias close to the PGND pin/pad to minimize parasitic resistance, parasitic impedance, and thermal resistance.
7. Place the BST capacitor and VDRV capacitor as close to the device's pins as possible, using trace paths at least 20mils wide.
8. Avoid using a via for the BST driving path. It is recommended to use a 0.1µF to 1µF bootstrap capacitor.
9. Place the VDD decoupling capacitor close to the device.
10. Connect AGND and PGND at the VDD capacitor's ground connection.
11. Keep the CS signal trace away from high-current paths, such as SW and PWM.

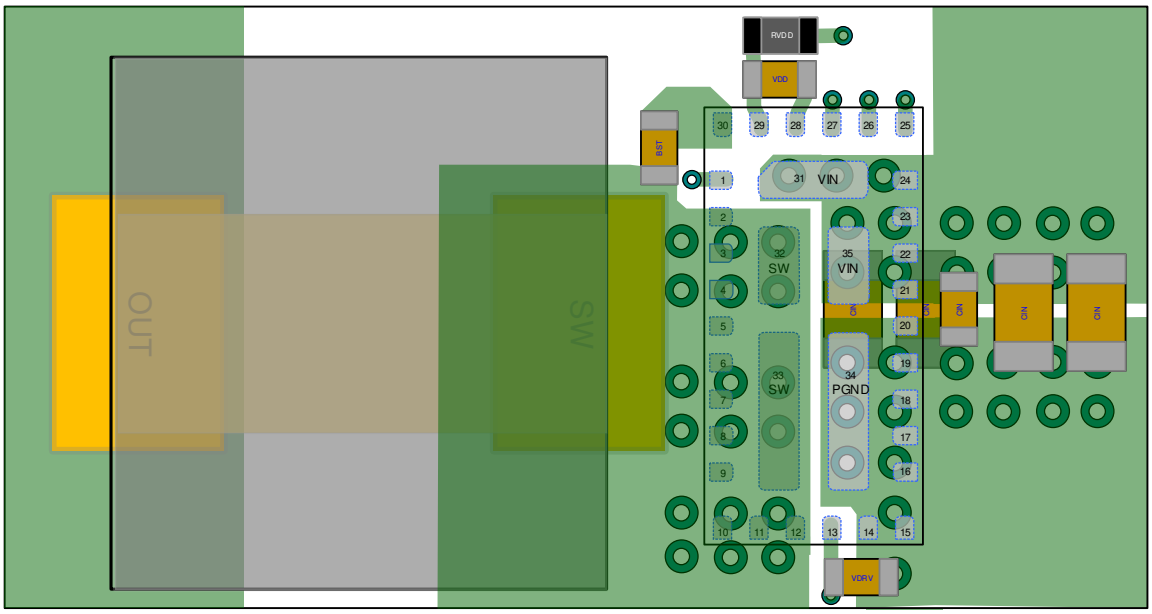


Figure 3: Recommended PCB Layout (Placement and Top Layer)

Input Capacitor: 0603 Package (Top Side and Bottom Side) and 0402 Package (Top Side)
Inductor: 6mmx7mm Package
VDD/BST/VDRV Capacitor: 0402 Package
Via Size: 20/10mils

TYPICAL APPLICATION CIRCUIT

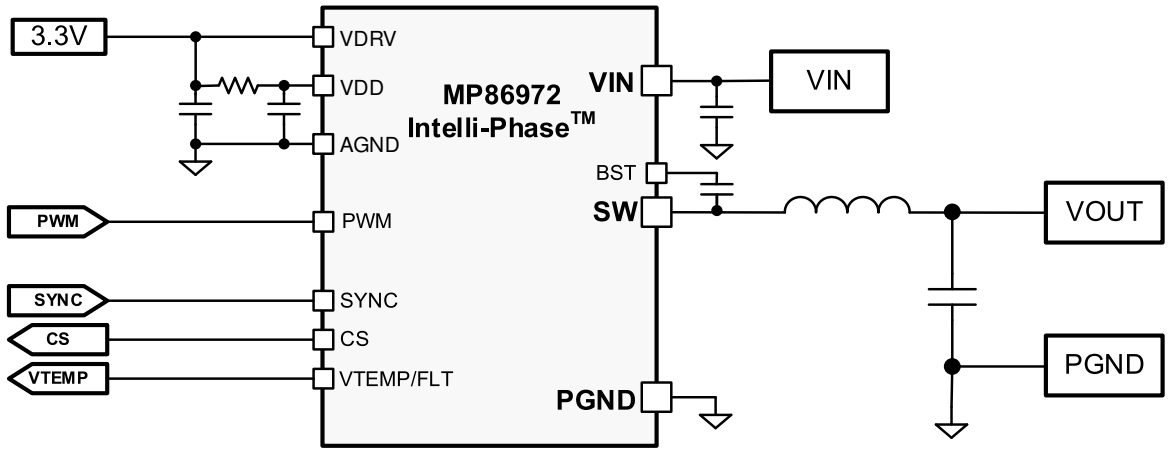
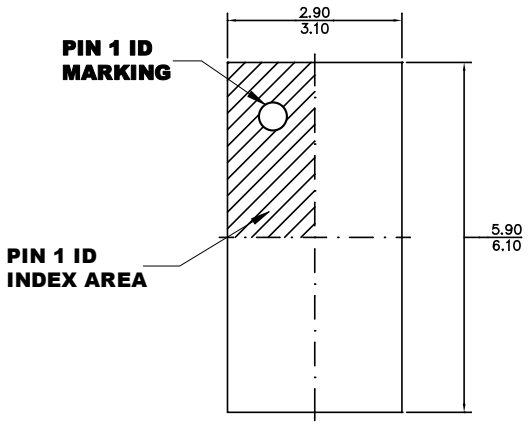


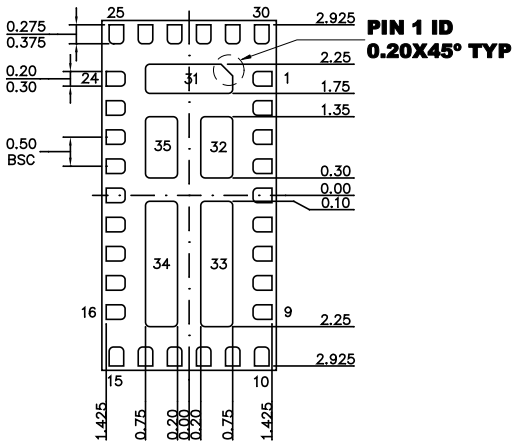
Figure 4: Typical Application Circuit

PACKAGE INFORMATION

TLGA-35 (3mmx6mm)

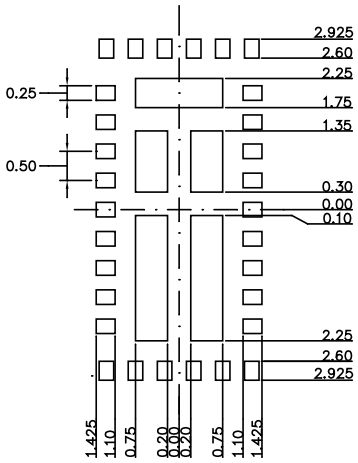


TOP VIEW

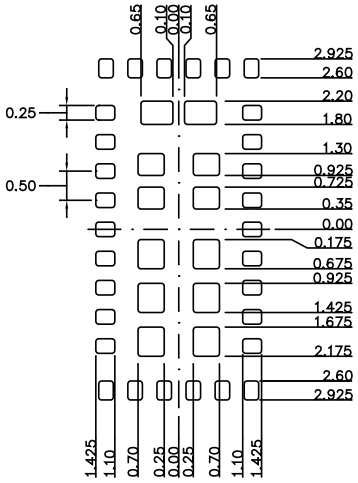


BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN

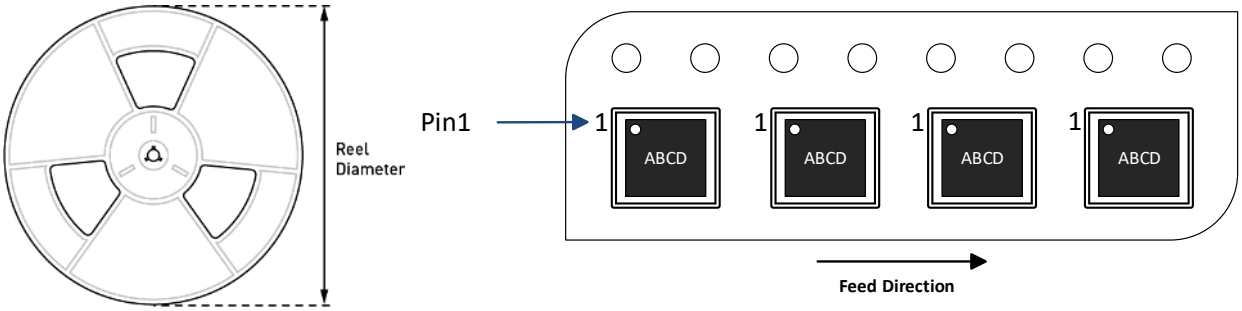


RECOMMENDED STENCIL DESIGN

NOTES:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP86972GLJTH-Z	TLGA-35 (3mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	06/28/2021	Initial Release	-