Benchmarq Products from Texas Instruments

bq2013H

Gas Gauge IC for Power-Assist Applications

Features

- Accurate measurement of available charge in rechargeable batteries
- Designed for electric assist bicycles and other applications
- Measures a wide dynamic current range
- Supports NiCd, NiMH or lead acid
- Designed for battery pack integration
  - 120µA typical standby current (self-discharge estimation mode)
  - Small size enables implementations in as little as ½ square inch of PCB
- Direct drive of LEDs for capacity display
- Automatic charge and self-discharge compensation using internal temperature sensor
- Simple single-wire serial communications port for subassembly testing
- 16-pin narrow SOIC

General Description

The bq2013H Gas Gauge IC is intended for battery-pack installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. The bq2013H is designed for high cpaacity battery packs used in high-discharge rate systems.

Battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature, rate of charge, and self-discharge are applied to the charge counter to provide available capacity information across a wide range of operating conditions. Initial battery capacity, self-discharge rate, display mode, and charge compensation are set using the $PROG_{1-6}$ pins. Actual battery capacity is automatically "learned" in the course of a discharge cycle from full to empty.

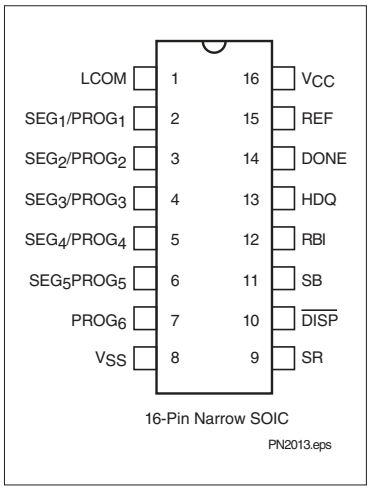
Nominal available charge may be directly indicated using a five-segment LED display. These segments are used to graphically indicate nominal available charge.

The bq2013H supports a simple single-line bi-directional serial link to an external processor (common ground). The bq2013H outputs battery information in response to external commands over the serial link. To support battery pack testing, the outputs may also be controlled by command. The external processor may also overwrite some of the bq2013H gas gauge data registers.

The bq2013H may operate directly from four nickel cells or three lead acid. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} from a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, and battery status.

Pin Connections



16-Pin Narrow SOIC

PN2013.eps

Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ Program 1 input	DONE	Fast charge complete input
$SEG_2/PROG_2$	LED segment 2 / Program 2 input	HDQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ Program 3 input	RBI	Register backup input
		SB	Battery sense input
$SEG_4/PROG_4$	LED segment 4/ Program 4 input	$\overline{DISP}$	Display control input
$SEG_5/PROG_5$	LED segment 5/ Program 5 input	SR	Sense resistor input
		V_{CC}	Supply voltage
$PROG_6$	Program 6 input		

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Pin Descriptions

LCOM **LED common**

This open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of $PROG_{1-5}$ pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

SEG_1–SEG_5 **LED display segment outputs (dual function with $PROG_1$–$PROG_5$**

Each output may activate an LED to sink the current sourced from LCOM.

$PROG_1$–$PROG_6$ **Programmed full count selection inputs (dual function with SEG_1 - SEG_5)**

These three-level input pins define the programmed full-count (PFC), display mode, self-discharge rate, offset compensation, overload threshold, and charge compensation.

SR **Sense resistor input**

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input (see Figure 1) is connected between the negative terminal of the battery and ground. $V_{SR} > V_{SS}$ indicates charge, and $V_{SR} < V_{SS}$ indicates discharge. The effective voltage drop, V_{SRO}, as seen by the bq2013H is $V_{SR} + V_{OS}$.

DONE **Charge complete input**

This input/output is used to communicate the status of an external charge controller to the bq2013H.

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ pulled high disables the display. $\overline{DISP}$ floating allows the LED display to be active during certain charge and discharge conditions. Transitioning $\overline{DISP}$ low activates the display.

SB **Secondary battery input**

This input monitors the scaled battery voltage through a high-impedance resistive divider network for the end-of-discharge voltage (EDV) thresholds.

RBI **Register backup input**

This input is used to provide backup potential to the bq2013H registers during periods when $V_{CC} < 3V$. A storage capacitor can be connected to RBI.

HDQ **Serial I/O pin**

This is an open-drain bidirectional communications port.

REF **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

V_{CC} **Supply voltage input**

V_{SS} **Ground**

Functional Description

General Operation

The bq2013H determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2013H measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the battery's negative terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2013H using the LED display. The bq2013H can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for enabling the LED display.

The bq2013H monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin is required.

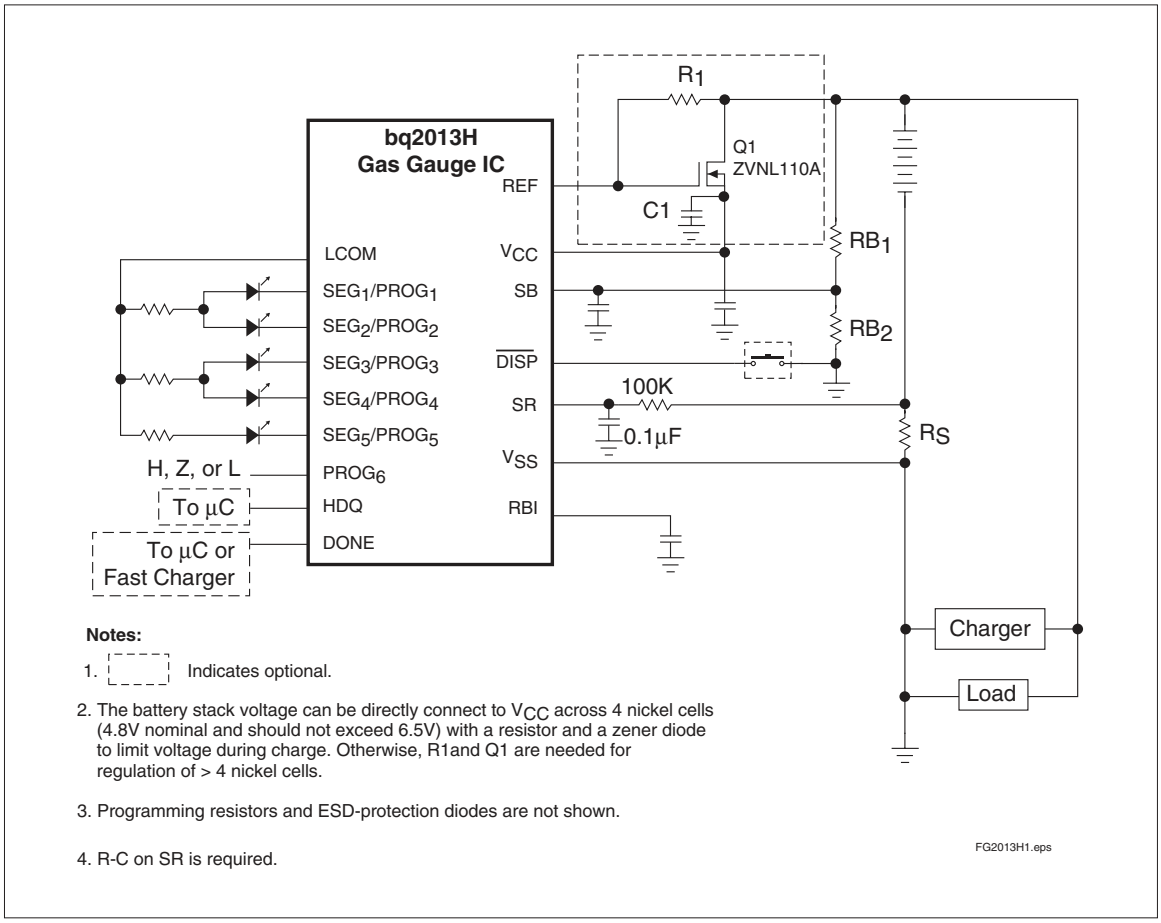


Figure 1. Application Diagram: LED Display

Register Backup

The bq2013H RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2013H registers when V_{CC} momentarily drops below 3.0V. V_{CC} is output on RBI when V_{CC} is above 3.0V.

After V_{CC} rises above 3.0V, the bq2013H checks the internal registers for data loss or corruption. If data has changed, then the NAC register is cleared, and the LMD register is loaded with the initial PFC.

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2013H monitors the battery potential through the SB pin for the end-of-discharge voltage (EDV) thresholds.

The EDV threshold levels are used to determine when the battery has reached an "empty" state.

The EDV thresholds for the bq2013H are set as follows:

EDV1 (first) = 1.00V

EDVF (final) = EDV1 - 100mV

The battery voltage divider (RB1 and RB2 in Figure 1) is used to scale these values to the desired threshold.

If VSB is below either of the two EDV thresholds for the specified delay times in Table 1, the associated flag is latched and remains latched, independent of VSB, until the next valid charge. EDV monitoring is disabled if the OVLD bit in FLGS2 is set.

Table 1. Delay Time in Seconds

Capacity	Temperature		
	< 10°C	10°C to 30°C	> 30°C
> 40%	7	6	5
20% to 40%	4	3	2
< 20%	2	2	2

Reset

The bq2013H can be reset by removing V_{CC} and grounding the RBI pin for 15 seconds or with a command over the serial port. The serial port reset command sequence requires writing 00h to register PPFC (address = leh) and the writing 00h to register LMD (address = 05h.)

Temperature

The bq2013H internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge rate compensations and self-discharge counting. The temperature range is available over the serial port in 10°C increments as shown in the following table:

TMPGG (hex)	Temperature Range
0x	< -30°C
1x	-30°C to -20°C
2x	-20°C to -10°C
3x	-10°C to 0°C
4x	0°C to 10°C
5x	10°C to 20°C
6x	20°C to 30°C
7x	30°C to 40°C
8x	40°C to 50°C
9x	50°C to 60°C
Ax	60°C to 70°C
Bx	70°C to 80°C
Cx	> 80°C

Layout Considerations

The bq2013H measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors should be placed as close as possible to the SB and V_{CC} pins and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for V_{CC}.
- The sense resistor (R_S) should be as close as possible to the bq2013H.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 100K.

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2013H. The bq2013H accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. The bq2013H compensates charge current for charge rate and tem-

perature. Discharge current is load compensated based on the value stored in location LCOMP (address = 0eh). LCOMP allows the bq2013H to automatically adjust for continuous small discharge currents. The bq2013H compensates self discharge for the load value as well as temperature.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging, self-discharge decrement the NAC register and increment the DCR (Discharge Count Register). NAC is also corrected automatically for offset error based on the value in the offset location OFFSET (address = 0bh.)

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2013H adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV. The maximum decrease in LMD because of a DCR update is 25% of LMD. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. **Programmed Full Count (PFC) or initial battery capacity:**

   The initial LMD and gas gauge rate values are programmed by using PFC. The PFC also provides the 100% reference for the absolute display mode. The bq2013H is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

   Battery capacity (mAh) $*$ sense resistor (Ω) =

   PFC (mVh)

   Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

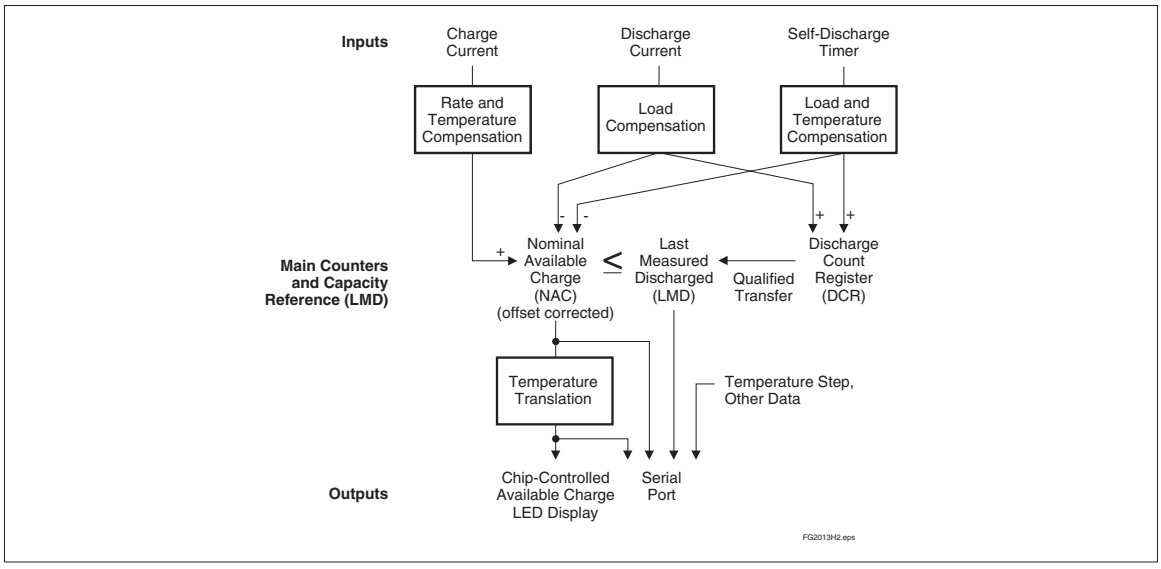


Figure 2. Operational Overview

Example: Selecting a PFC Value

Given:

Sense resistor = 0.0075Ω
Number of cells = 14
Capacity = 5000mAh, NiCd cells
Current range = 1A to 30A
Relative display mode with 4 second timer
Self-discharge = 1% per day
Trickle charge compensation = 0.85
Typical offset = -75µV
Voltage drop across sense resistor = 5mV to 225 mV

Therefore:

$$5000\text{mAh} * 0.0075\Omega = 37.5\text{mVh}$$

Select:

PFC = 44,800 counts or 35mVh
$PROG_1$, $PROG_2$ = Z, L
$PROG_3$ = Z
$PROG_4$ = H
$PROG_5$ = L
$PROG_6$ = Z

Table 2. bq2013H Programmed Full Count mVh Selections

Programmed Full Count (PFC)	mVh	Scale	$PROG_1$	$PROG_2$
27136	84.8	1/320	H	H
24064	75.2	1/320	H	Z
41472	64.8	1/640	H	L
35072	54.8	1/640	Z	H
28672	44.8	1/640	Z	Z
44800	35	1/1280	Z	L
30720	24	1/1280	L	H
38400	15	1/2560	L	Z
12800	5	1/2560	L	L

Table 3. Programmed Self-Discharge

$PROG_3$	Self-Discharge
H	1.6% per day
Z	0.8% per day
L	0.2% per day

Table 4. Programmed Display Mode

$PROG_4$	Overload Threshold	Display Mode
H	V_{OVLD} = -75mV	Relative/4s timer after push-button release
Z	V_{OVLD} = -75mV	Relative/4s timer after push-button release
L	V_{OVLD} = -25mV	Absolute/4s timer after push-button release

Table 5. Programmed Charge Compensation

$PROG_5$	Trickle			Fast		
	<30°C	30°C—50°C	>50°C	<30°C	30°C—50°C	>50°C
H	0.80	0.75	0.70	0.95	0.90	0.85
Z	1.00	1.00	1.00	1.00	1.00	1.00
L	0.85	0.80	0.75	0.95	0.90	0.85

Table 6. Programmed Discharge Offset Adjustment

$PROG_6$	Offset
H	-150µV
Z	-75µV
L	0µV

The initial full battery capacity is 35mVh (4667mAh) until the bq2013H "learns" a new capacity with a qualified discharge from full to EDV1.

3. **Nominal Available Capacity (NAC):**

   NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD. When the DONE input is asserted high, indicating full charge completion, NAC is set to LMD.

4. **Discharge Count Register (DCR):**

   The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

   The DCR value becomes the new LMD value on the first charge after a valid discharge to EDV1 if all of the following conditions are met:

   - No valid charge initiations (charges greater than 2 NAC updates) occurred during the period between NAC = LMD and EDV1.
   - The self-discharge count is less than 6% of NAC.
   - The temperature is ≥ 0°C when the EDV1 level is reached during discharge.
   - VDQ is set.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2013H increments NAC at a rate proportional to V_{SRO} (V_{SR} + V_{OS}) and, if enabled, activates an LED display if V_{SRO} > 500µV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2013H detects charge activity with V_{SRO} > 250µV. A valid charge equates to a sustained charge activity greater than 2 NAC updates. Once a valid charge is detected, charge counting continues until V_{SRO} drops below 250µV.

Discharge Counting

All discharge counts where V_{SRO} < -250µV cause the NAC register to decrement and the DCR to increment. If enabled, the display is activated when V_{SRO} < -2mV. The display remains active for 10 seconds after V_{SRO} rises above - 2mV.

Self-Discharge Estimation

The bq2013H decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed per Table 3. This is the rate for a battery temperature between 20–30°C. The NAC register cannot be decremented below 0.

Count Compensations

The bq2013H determines fast charge when the NAC updates at a rate of ≥ 2 counts/s. Charge activity is compensated for temperature and rate before updating NAC. Self-discharge estimation is compensated for temperature before updating NAC or DCR.

Charge Compensation

Charge efficiency factors are selected using Table 5 for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in ≥ 2 NAC counts/s (0.16C to 0.6C, depending on PFC selections; see Table 2).

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. Program pin 5 is used to select one of three compensation programs. These values are shown in Table 5.

Self-Discharge Compensation

The self-discharge compensation can be programmed for three different rates. The rates vary across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 7.

Table 7. Self-Discharge Compensation

Temperature Range	Self-Discharge Compensation Typical Rate/Day		
	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L
< 10°C	NAC/256	NAC/512	NAC/2048
10–20°C	NAC/128	NAC/256	NAC/1024
20–30°C	NAC/64	NAC/128	NAC/512
30–40°C	NAC/32	NAC/64	NAC/256
40–50°C	NAC/16	NAC/32	NAC/128
50–60°C	NAC/8	NAC/16	NAC/64
60–70°C	NAC/4	NAC/8	NAC/32
> 70°C	NAC/2	NAC/4	NAC/16

Offset Compensation

The bq2013H uses a voltage to frequency converter to measure the voltage across a resistor used to monitor the current into and out of the battery. This converter has an offset value that can be influenced by the V_{CC} supply and the bypassing of this supply. The typical value found on a well designed PCB is about -75µV. Program pin 6 can be used to compensate for this offset, reducing the effective V_{OS}. Offset compensation occurs when V_{SRO} < -250µV or V_{SRO} > 250µV.

Error Summary

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description in the "Layout Considerations" section). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

DONE Input

A fast-charge controller IC or micro-controller uses the DONE input to communicate charge status to the bq2013H. When the DONE input is asserted high on fast-charge completion, the bq2013H sets NAC = LMD. The DONE input should be maintained high as long as the fast-charge controller or microcontroller keeps the batteries full; otherwise, the pin should be held low.

Communicating With the bq2013

The bq2013H includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2013H registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2013H should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2013H. The command directs the bq2013H to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte. (See Figure 3.)

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/s. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2013H may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g., t_{CYCB} > 250µs, the bq2013H should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2013H is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2013H taking the HDQ pin to a logic-low state for a period, $t_{STRH;B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period, $t_{DH;DV}$, to allow the host or bq2013H to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial com-

Table 8. bq2013H Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

munication timing specification and illustration sections.

Communication with the bq2013H is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2013H NACH register.

bq2013H Command Code and Registers

The bq2013H status registers are listed in Table 9 and described below.

Command Code

The bq2013H latches the command code when eight valid command bits have been received by the bq2013H. The command code register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ location is:

Command Code Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

Where W/$\overline{R}$ is:

0 The bq2013H outputs the requested register contents specified by the address portion of command code.

1 The following eight bits should be written to the register specified by the address portion of command code.

The lower seven-bit field of command code contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

Command Code Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

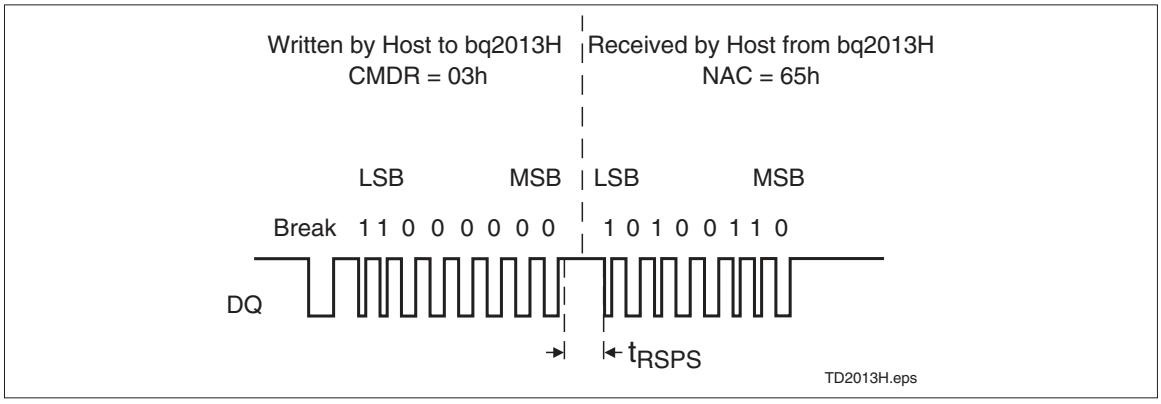


Figure 3. Typical Communication With the bq2013H

Table 9. bq2013H Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
FLGS1	Primary status flags register	01h	R	CHGS	BRP	RSVD	RSVD	VDQ	RSVD	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capacity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	R/W	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	R	CR	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	OVLD
PPD	Program pull down register	07h	R	RSVD	RSVD	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pull up register	08h	R	RSVD	RSVD	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
OCTL	Output control register	0ah	R/W	OC6	OC5	OC4	OC3	OC2	OC1	OCE	OCC
OFFSET	Offset adjustment regisiter	0bh	R/W	OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0
SDR	Self discharge rate	0ch	R/W	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
DMF	Digital magnitude filter	0dh	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
LCOMP	Load compensation	0eh	R/W	LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0
CCOMP	Fast charge compensation	0fh	R/W	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
PPFC	Program pin data	leh	R/W	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
VSB	Battery voltage register	7eh	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Notes: RSVD = reserved.
All other registers not documented are reserved.

Primary Status Flags Register (FLGS1)

The FLGS1 register (address=01h) contains the primary bq2013H flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. The bq2013H deems the charge valid if it results in two NAC updates with V_{SRO} > 250µV. A V_{SRO} of less than 250µV or discharge activity clears CHGS.

The CHGS location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

where CHGS is

0 Either discharge activity detected or V_{SRO} < 250µV

1 Two NAC updates with V_{SRO} > 250µV

The ***battery replaced*** flag (BRP) is asserted whenever the bq2013H is reset by application of V_{CC} or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or when a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

where BRP is

0 bq2013H is charged until NAC = LMD or on the first charge after or a discharge which sets the EDV1 flag

1 bq2013H is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2013H is discharged from NAC=LMD. The flag remains set until either LMD is updated or until one of three actions that can clear VDQ occurs:

- NAC has been reduced by more than 6% during because of self-discharge since VDQ was set
- A valid charge action sustained at V_{SRO} > V_{SRQ} for at least two NAC updates
- The EDV1 flag was set at a temperature below 0°C.

The VDQ location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

where VDQ is

0 Self-discharge reduces NAC by 6%, valid charge action detected, EDV1 asserted with the temperature less than 0°C, or reset

1 On first discharge after NAC = LMD

The first ***end-of-discharge warning*** flag (EDV1) warns the user that the battery is empty. SEG1 blinks at a 4Hz rate and DONE is asserted low. EDV1 detection is disabled if OVLD = 1. The EDV flag is latched until a valid charge has been detected.

The EDV1 location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

where EDV1 is

0 Valid charge action detected or $V_{SB} \geq V_{EDV1}$

1 $V_{SB} < V_{EDV1}$ for the delay time, provided that the OVLD bit is not set

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EDVF threshold is set 100mV below the EDV1 threshold.

The EDVF location is:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected or $V_{SB} \geq V_{EDVF}$

1 $V_{SB} < V_{EDVF}$, providing the OVLD bit is not set

Table 10. Temperature Register Contents

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

Temperature and Gas Gauge Register (TMPGG)

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

The bq2013H contains an internal temperature sensor. The temperature is used to set charge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 10.

The bq2013H calculates the available charge as a function of NAC and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Nominal Available Charge Register (NAC)

The NACH register (address=03h) and the NACL register (address=17h) are the main gas gauging registers for the bq2013H. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC. NACH and NACL are set to 0 during a bq2013H reset.

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{RBI} is greater than 2V. The contents of BATID have no effect on the operation of the bq2013H. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2013H uses as a measured full reference. The bq2013H adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2013H updates the capacity of the battery. LMD is set to PFC during a bq2013H reset.

Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2013H flags.

The ***charge rate*** flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 NAC counts/s.

The CR location is:

FLGS2 Bits							
7	6	5	4	3	2	1	0
CR	-	-	-	-	-	-	-

Where CR is:

0 When charge rate falls below 2 counts/sec

1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency fac-

tors are used. The time to change CR varies due to the user-selectable count rates.

The ***overload*** flag (OVLD) is asserted when a discharge overload is detected. PROG4 defines the overload threshold, as defined in Table 4. OVLD remains asserted as long as the condition is valid.

The OVLD location is:

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Where OVLD is:

0 If $V_{SRO} > V_{OVLD}$

1 If $V_{SRO} < V_{OVLD}$

Program Pin Pull-Down Register (PPD)

The PPD register (address=07h) contains some of the programming pin information for the bq2013H. The program pins have a corresponding PPD bit location, $PPD_{1–6}$. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if $PROG_1$ and $PROG_4$ have pull-down resistors, the contents of PPD are xx001001.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
RSVD	RSVD	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
RSVD	RSVD	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Program Pin Pull-Up Register (PPU)

The PPU register (address=08h) contains the rest of the programming pin information for the bq2013H. The program pins have a corresponding PPU bit location, $PPU_{1–6}$. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if $PROG_3$ and $PROG_5$ have pull-up resistors, the contents of PPU are xx010100.

Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2013H. The segment drivers may be overwritten by data from OCTL when bit 1 of OCTL, OCE, is set. The data in bits $OC_{5–1}$ of the OCTL register (see Table 9 for details) is output onto the segment pins, $SEG_{5–1}$, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2013H to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2013H.

Offset Adjustment Register

The value in this register (address = 0bh) is used to correct NAC for the offset of the VFC. This register is initialized from the state of $PROG_6$. The following are the initial values:

- 0 = no offset correction
- 46 = -75µV correction
- 23 = -150µV correcton

The value is set by the equation:

$$\text{Offset} = \frac{1}{289 * V_{COS}}$$

where V_{COS} is the desired offset correction in volts.

Self-Discharge Rate Compensation

This register contains the value used to correct for the self-discharge compensation. This value is initialized from the state of $PROG_3$. The following are the initial values:

- 235 = 1.6% per day $\left(\frac{1}{64}\right)$
- 214 = 0.8% per day $\left(\frac{1}{128}\right)$
- 88 = 0.2% per day $\left(\frac{1}{512}\right)$

The value is set by the equation:

$$\text{SDR} = 256 - \left(\frac{0.3296}{C_{SD}}\right)$$

where C_{SD} is the self-discharge rate per day.

Digital Magnitude Filter (DMF)

The read-write DMF register (address=0dh) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted. The default value for the DMF is 250µV. The value is set by the equation:

$$\text{DMF} = \frac{45}{V_{SRD,Q}}$$

where $V_{SRD,Q}$ is the desired filter threshold in mV.

Note: Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2013H.

Load Compensation

The load compensation value (address = 0eh) allows the bq2013H to compensate for small discharge loads that are below the digital filter. Each increment in the LCOMP register represents 2µVh. The value in LCOMP represents the additional amount of discharge applied to NAC and DCR at a constant rate when $V_{SRO} < V_{SRQ}$. LCOMP compensation is applied in addition to self-discharge. LCOMP is set to 0 on a full reset. The value is set by the equation:

$$LCOMP = \frac{1}{289 * V_{CLD}}$$

where V_{CLD} is the desired load correction in volts.

Charge Compensation

The charge-compensation value (address = 0fh) allows the bq2013H to compensate for battery charge inefficiencies. This value is initialized from the state of $PROG_5$ and represents the fast-charge compensation factor for < 30°C. The value can be overwritten via the serial port and is stored in percent. The bq2013H scales the value in 0fh to determine the compensation at other rates and temperatures. For example, if $PROG_5$ = H, the applied efficiency drops by 5% for each temperature range, and the trickle rates are 15% below the fast-charge rates. If the value 55h (85%) is written to CCOMP, the compensation for trickle charge at > 50°C is 60%.

Program Pin Data (PPFC)

The PPFC register provides the means to perform a software controlled reset of the device. The recommended reset method for the bq2013H is:

- Write PPFC to zero
- Write LMD to zero

After these operations, a software reset occurs.

Resetting the bq2013H sets the following:

- LMD = PFC
- VDQ, OCE, LCOMP, and NAC = 0
- BRP = 1

Battery Voltage Register (VSB)

The battery voltage register is used to read the battery voltage on the SB pin. The VSB register (address = 7eh) is updated approximately once per second with the present value of the battery voltage. The battery voltage on the SB pin is determined by the equation:

$$V_{SB} = 1.2V * \left(\frac{VSB}{256}\right)$$

Display

The bq2013H can directly display capacity information using low-power LEDs. If LEDs are used, the segment pins should be tied to V_{CC}, the battery, or the LCOM pin through resistors for programming the bq2013H.

The bq2013H displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC. As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on, representing the reduction in the actual battery capacity.

When $\overline{DISP}$ is tied to V_{CC}, the $SEG_{1–5}$ outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active during charge if the NAC registers are counting at a rate equivalent to V_{SRO} > 500µV or fast discharge if the NAC registers are counting at a rate equivalent to V_{SRO} < -2mV. When $\overline{DISP}$ is pulled low and held, the segment outputs become active continuously. When released to high Z, the segment outputs will remain active for 4 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 320Hz, with each bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} to indicate a low-battery condition or NAC is less than 10% of the LMD or PFC, depending on the display mode.

Microregulator

The bq2013H can operate directly from 4 nickel or 3 lead acid cells. To facilitate the power supply requirements of the bq2013H, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2013H can be inexpensively built using the FET and an external resistor.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	Vcc+0.7	V	100kΩ series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	0	+70	°C	Commercial

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Voltage Thresholds (TA = TOPR; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV}	End-of-discharge warning	0.96 * V_{EDV}	V_{EDV}	1.04 * V_{EDV}	V	SB
V_{SRO}	SR sense range	-300	-	+500	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	250	-	-	µV	V_{SR} + V_{OS}
V_{SRD}	Valid discharge	-	-	-250	µV	V_{SR} + V_{OS}

Note: VOS is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See “LayoutConsiderations.”

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
VOS	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, HDQ = 0
		-	120	180	µA	V_{CC} = 4.25V, HDQ = 0
		-	170	250	µA	V_{CC} = 6.5V, HDQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	$0 < V_{SB} < V_{CC}$
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
I_{RBI}	RBI data-retention current	-	-	100	nA	$V_{RBI} > V_{CC} < 3V$
R_{HDQ}	Internal pulldown	500	-	-	KΩ	
R_{SR}	SR input impedance	10	-	-	MΩ	$-200mV < V_{SR} < V_{CC}$
V_{IHPFC}	PROG logic input high	V_{CC} - 0.2	-	-	V	$PROG_{1-6}$
V_{ILPFC}	PROG logic input low	-	-	V_{SS} + 0.2	V	$PROG_{1-6}$
V_{IZPFC}	PROG logic input Z	float	-	float	V	$PROG_{1-6}$
V_{OLSL}	SEG output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, $I_{OLS} \leq$ 1.75mA SEG_1–SEG_5, DONE
V_{OLSH}	SEG output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, $I_{OLS} \leq$ 11.0mA SEG_1–SEG_5, DONE
V_{OHML}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHMH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	$V_{CC} > 3.5V$, I_{OHLCOM} = -33.0mA
I_{OLS}	SEG sink current	11.0	-	-	mA	At V_{OLSH} = 0.4V, V_{CC} = 6.5V
I_{OL}	Open-drain sink current	5.0	-	-	mA	At $V_{OL} = V_{SS}$ + 0.3V, HDQ
V_{OL}	Open-drain output low	-	-	0.3	V	$I_{OL} \leq$ 5mA, HDQ
V_{IHDQ}	HDQ input high	2.5	-	-	V	HDQ
V_{ILDQ}	HDQ input low	-	-	0.8	V	HDQ
V_{IH}	DONE input high	2.5	-	-	V	DONE
V_{IL}	DONE input low	-	-	0.5	V	DONE
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	kΩ	$PROG_{1–6}$
R_{FLOAT}	Float state external impedance	-	5	-	MΩ	$PROG_{1-6}$

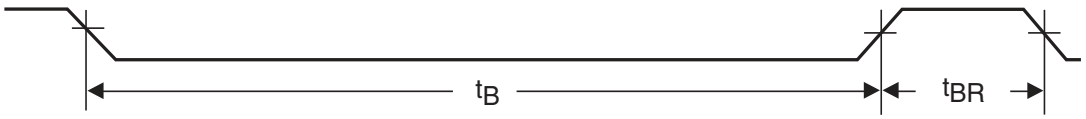
Note: All voltages relative to V_{SS}.

High-Speed Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
t_{CYCH}	Cycle time, host to bq2013H (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2013H to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2013H (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2013H to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DSUB}	Data setup	-	-	50	µs	
t_{DH}	Data hold	100	-	-	µs	
t_{DV}	Data valid	80	-	-	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SSUB}	Stop setup	-	-	145	µs	
t_{RSPS}	Response time, bq2013H to host	190	-	320	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	

Note: The open-drain HDQ pin should be pulled to at least V_{CC} by the host system for proper HDQ operation. HDQ may be left floating if the serial interface is not used.

Break Timing



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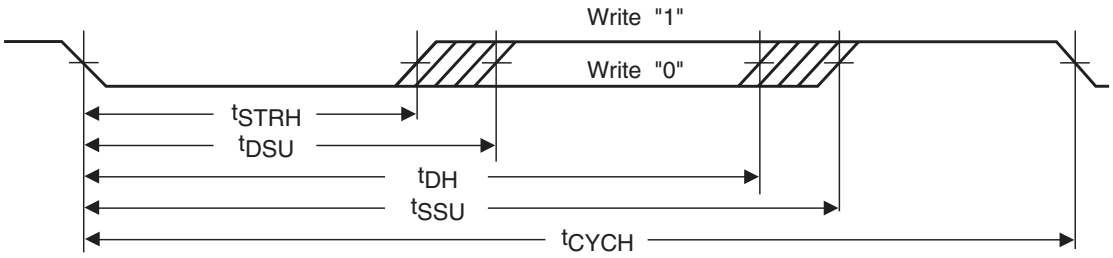
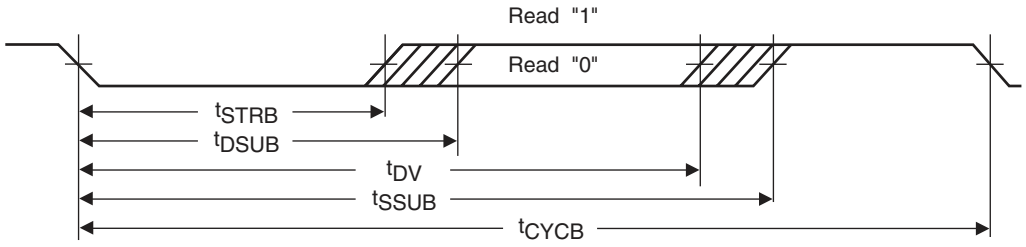
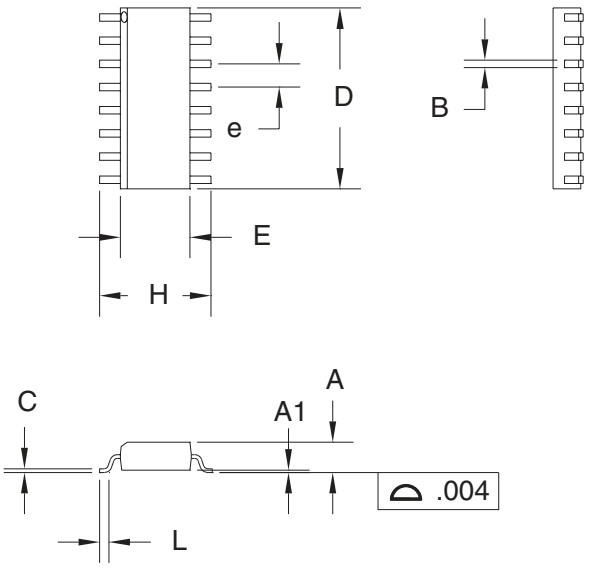
Host to bq2013H



bq2013H to Host



16-Pin SOIC Narrow (SN)



16-Pin SN (SOIC Narrow)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

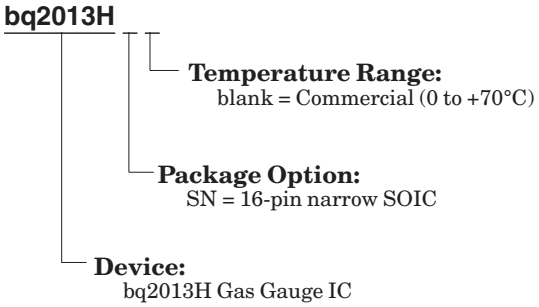
All dimensions are in inches.

Data Sheet Revision History

ChangeNo.	Page No.	Description of Change
1	All	"Final" changes from "Preliminary" version
2	3	Updated application diagram
2	8	Changed charge/discharge default threshold from 200µV to 250µV.
2	9	Changed offset compensation window range from ±200µV to ±250µV
2	11	Designated appropriate locations from "R/W" to "R"
2	12	Changed charge threshold from 200µV to 250µV
2	14	Changed default DMF from 200µV to 250µV
2	16	Added REF absolute maximum rating
2	16	Changed charge/discharge default threshold from 200µV to 250µV
2	16	Added V_{SRO} parameter
2	17	Changed DQ designation to HDQ
2	17	Changed V_{OL} from 0.5V to 0.3V (max.)
2	17	Added R_{PROG}
3	9	Changed the DONE Input section

Note: Change 1 = Dec. 1998 changes from July 1998 "Preliminary."
Change 2 = May 1999 A changes from Dec. 1998.
Change 3 = December 2013 B changes from May 1999

Ordering Information



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2013HSN-A514	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2013H A514	Samples
BQ2013HSN-A514G4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2013H A514	Samples
BQ2013HSN-A514TR	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2013H A514	
BQ2013HSN-A514TRG4	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	2013H A514	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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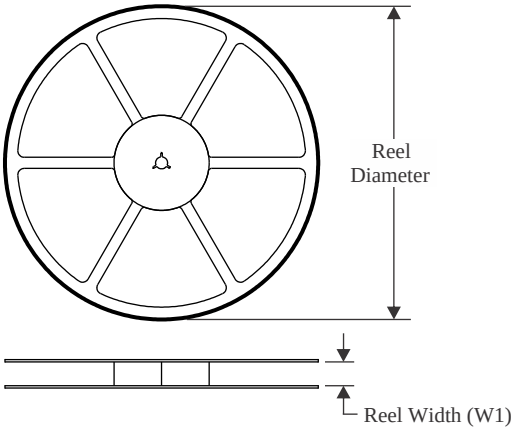
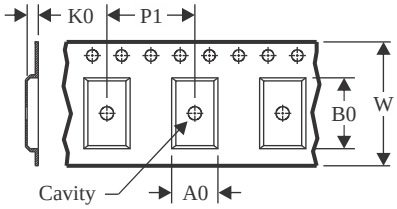
TAPE AND REEL INFORMATION

REEL DIMENSIONS

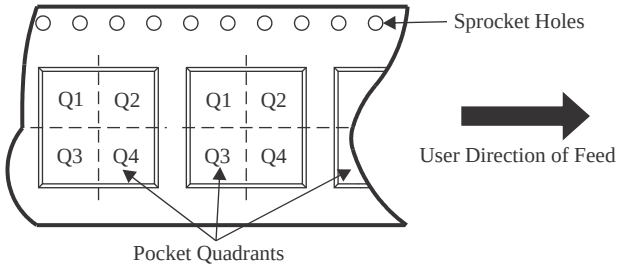


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

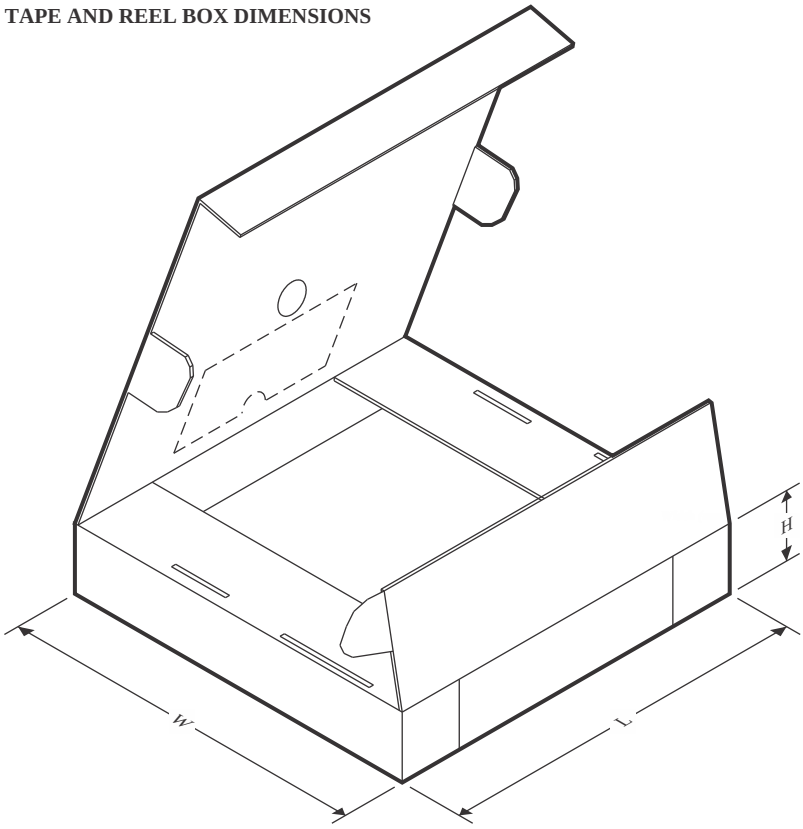
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2013HSN-A514TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

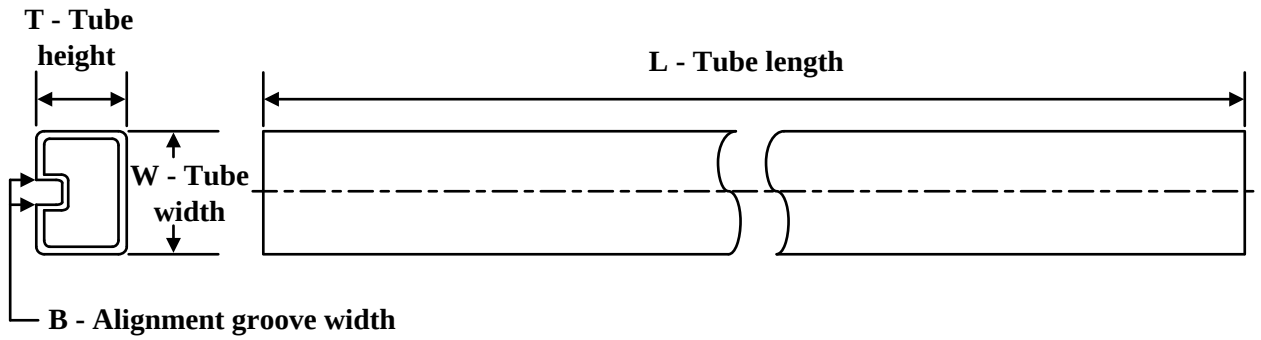
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2013HSN-A514TR	SOIC	D	16	2500	356.0	356.0	35.0

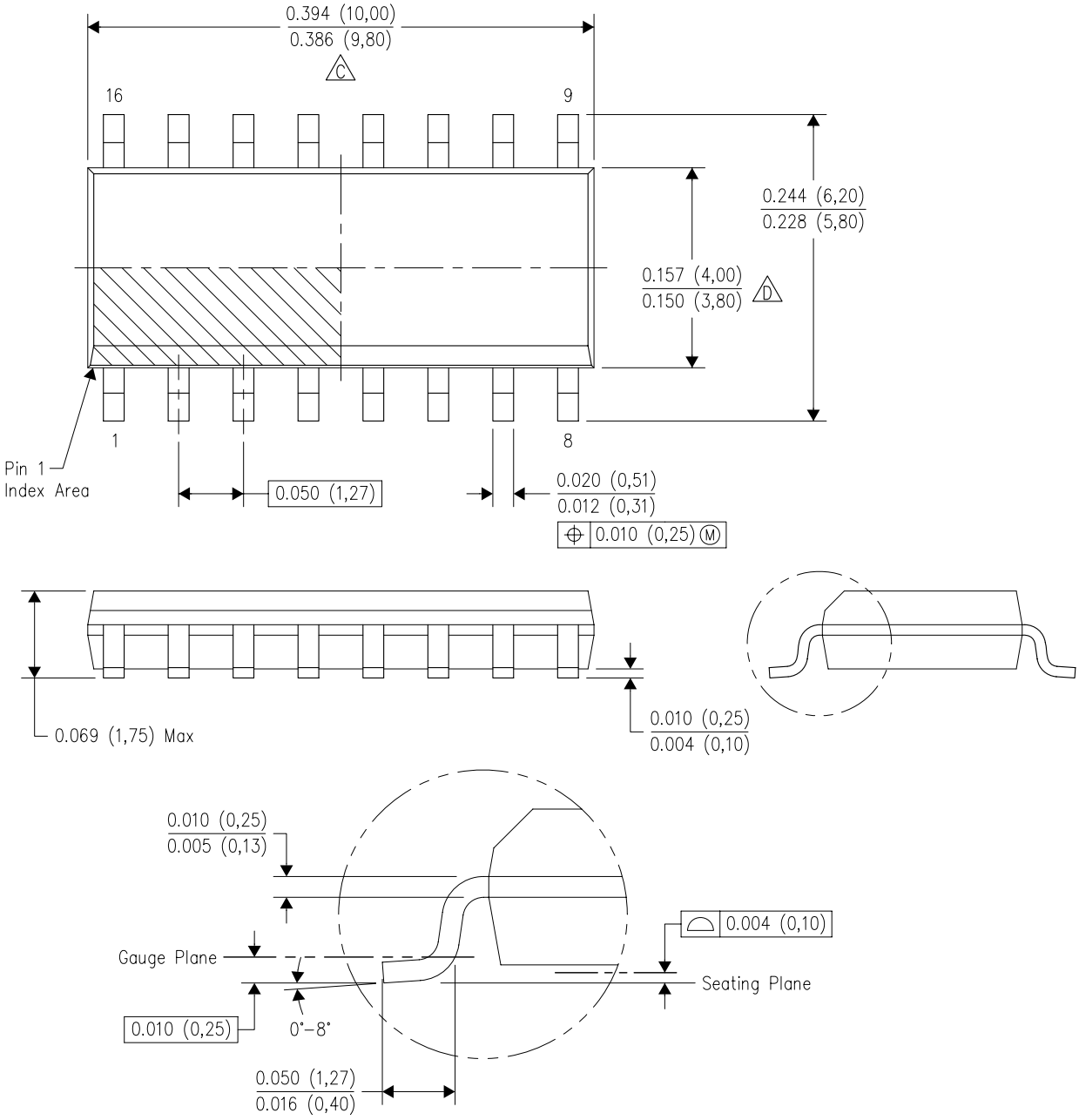
TUBE



*All dimensions are nominal

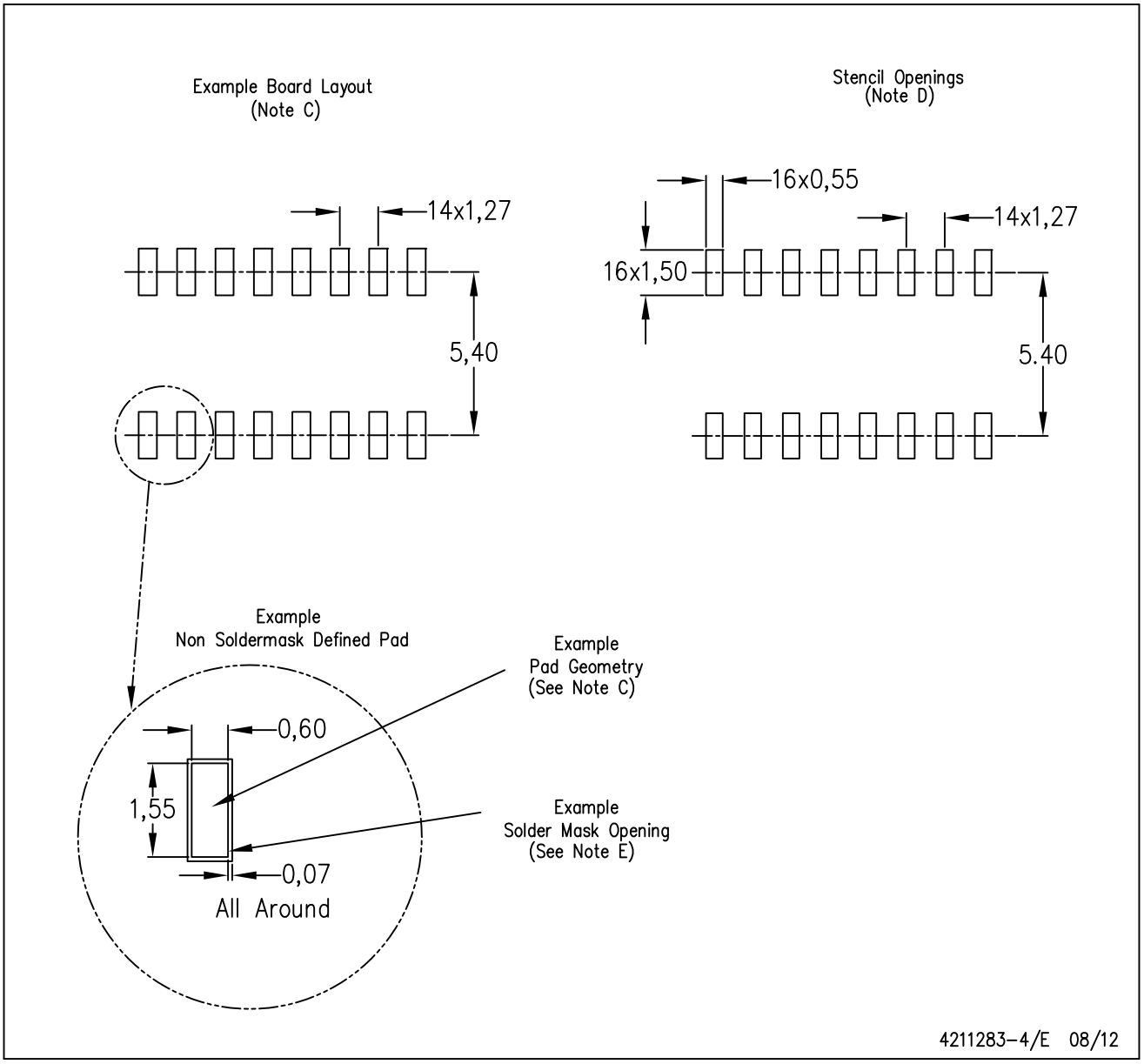
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ2013HSN-A514	D	SOIC	16	40	506.6	8	3940	4.32
BQ2013HSN-A514G4	D	SOIC	16	40	506.6	8	3940	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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