ICL8018A/8019A/8020A
4-Bit Expandable Current-Switch

HARRIS SEMICONDUCTOR

GENERAL DESCRIPTION

The Intersil ICL8018A family are high speed precision current switches for use in current summing digital-to-analog converters. They consist of four logically controlled current switches and a reference device on a single monolithic silicon chip. The reference transistor, combined with precision resistors and an external source, determines the magnitude of the currents to be summed. By weighting the currents in proportion to the binary bit which controls them, the total output current will be proportional to the binary number represented by the input logic levels.

The performance and economy of this family make them ideal for use in digital-to-analog converters for industrial process control and instrumentation systems.

FEATURES

- TTL Compatible
- 12 Bit Accuracy
- 40ns, Switching Speed
- Wide Power Supply Range
- Low Temperature Coefficient

APPLICATIONS:

- D/A and A/D Converters
- Digital Threshold Control
- Programmable Voltage Source
- Meter Drive
- X-Y Plotters

ORDERING INFORMATION

ACCURACY	MILITARY TEMP RANGE CERDIP	COMMERCIAL TEMP RANGE PLASTIC DIP
Individual Devices		
.01%	ICL8018AMJD	ICL8018ACPD
0.1%	ICL8019AMJD	ICL8019ACPD
1.0%	ICL8020AMJD	ICL8020ACPD
Matched Sets*		
.01%	ICL8018AMXJD	ICL8018ACXPD
0.1%	ICL8019AMXJD	ICL8019ACXPD
1.0%	ICL8020AMXJD	ICL8020ACXPD

*NOTE: Units ordered in equal quantities will be matched such that the V_{BE}'s of the 8019 will be within ±10mV of the 8018 compensating transistor, and the V_{BE}'s of the 8020 will be within ±50mV. The ICL8018-X matched sets consist of one 8018, one 8019, and one 8020. The 8019-X contains one 8019 and one 8020, while the 8020-X contains two 8020's. Units shipped as matched sets will be marked with a unique set number.

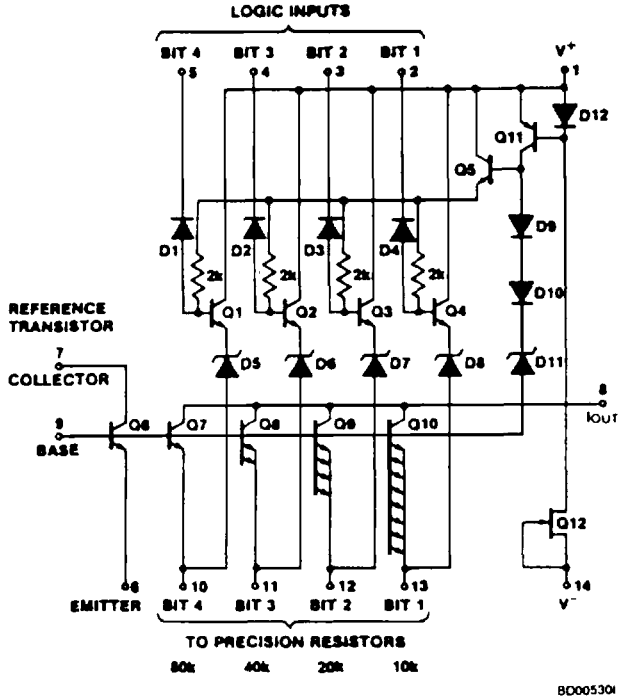

Figure 1: Functional Diagram

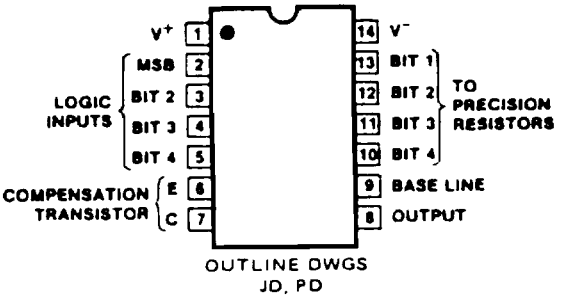

Figure 2: Pin Configuration

6

Note: All typical values have been guaranteed by characterization and are not tested.

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INTERSIL

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Logic Input Voltage ..... −2V to V^+
$V_{BASELINE}$ ..... V^- to +5V
Output Voltage ..... $V_{BASELINE}$ to +20V
Storage Temperature ..... −65°C to +150°C

Operating Temperature ICL8018AM
ICL8019/20AM ..... −55°C to +125°C
ICL8018/19/20AC ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS ($4.5V \le V^+ \le 20V$, $V^- = -15V$, $T_A = 25°C$, Voltage @ pin 6 = −5V)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Absolute Error ICL8018A ICL8019A ICL8020A	V_{INHI} = 5.0V V_{INLO} = 0.0V			±.01 ±0.1 ±1	%
Error Temperature Coefficient ICL8018A ICL8019A ICL8020A			±2 ±2 ±2	±5 ±25 ±50	ppm/°C
Settling Time To ±1/2 LSB, R_L = 1kΩ 8 BIT 12 BIT			100 200		ns
Switching Time To Turn On LSB			40		ns
Output Current (Nominal) BIT 1 (MSB) BIT 2 BIT 3 BIT 4 (LSB)			1.0 0.5 0.25 0.125		mA
Zero Output Current	V_{IN} = 5.0V		10	50	nA
Output Voltage Range		$V_{BASELINE}$ + 1V		+ 10	V
Input Coding-Complementary Binary (See Truth Table) Logic Input Voltage "0" (Switch ON) "1" (Switch OFF)	ΔI_{OUT} < 400nA	 2.0		 0.8	 V
Logic Input Current "0" "1" (into device)	V_{IN} = 0V V_{IN} = 5V		−1.0 0.01	−2 0.1	mA μA
Power Supply Rejection V^+ V^-			.005 .0005		%/V
Supply Voltage Range V^+ V^-		4.5 −5	5 −15	20 −20	V
Supply Current (V_{SUPP} = ±20V) I^+ I^-			7 1	10 3	mA

Note: All typical values have been guaranteed by characterization and are not tested.

BASIC D/A THEORY

The majority of digital to analog converters contain the elements shown in Figure 3. The heart of the D/A converter is the logic controlled switching network, whose output is an analog current or voltage proportional to the digital number on the logic inputs. The magnitude of the analog output is determined by the reference supply and the array of precision resistors, see Figure 4. If the switching network has a current output, often a transconductance amplifier is used to provide a voltage output.

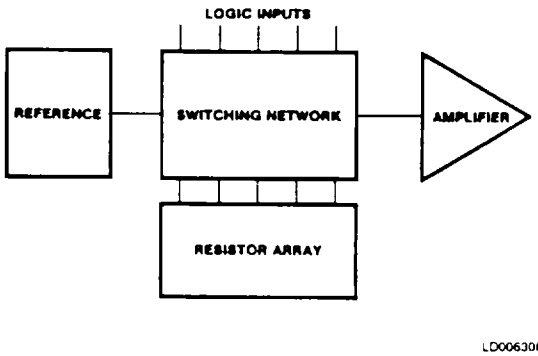

Figure 3: Elements of a D/A Converter

DEFINITION OF TERMS

The **resolution** of a D/A converter refers to the number of logic inputs used to control the analog output. For example, a D/A converter using two quad current sources would be an 8 bit converter. If three quads were used, a 12 bit converter would be formed. Resolution is often stated in terms of one part in, e.g., 256 since the number of controlling bits is related to total number of identifiable levels by the power of 2. The four bit quad has sixteen different levels (see Table 1) each output corresponding to a particular logic input word.

Table 1: ICL8018/19/20 Truth Table

LOGIC INPUT	NOMINAL OUTPUT CURRENT (mA)
0 0 0 0	1.875
0 0 0 1	1.750
0 0 1 0	1.625
0 0 1 1	1.500
0 1 0 0	1.375
0 1 0 1	1.250
0 1 1 0	1.125
0 1 1 1	1.000
1 0 0 0	0.825
1 0 0 1	0.750
1 0 1 0	0.625
1 0 1 1	0.500
1 1 0 0	0.375
1 1 0 1	0.250
1 1 1 0	0.125
1 1 1 1	0.000

Note that **maximum output** of the quad switch is 1 + 1/2 + 1/4 + 1/8 = 1-7/8 = 1.875 mA. If this series of bits were continued as 1/16 + 1/32 + 1/64 . . . . . $1/2^{(n-1)}$, the maximum output limit would approach 2.0 mA. This limiting value is called **full scale output.** The maximum output is always less than the full scale output by one least significant bit, LSB. For a twelve bit system (resolution 1 part in 4096) with a full scale output of 10.0 volts the maximum output would be 4095/4096 x 10V. Since the numbers are extremely close for high resolution systems, the terms are often used interchangeably.

The **accuracy** of a D/A converter is generally taken to mean the largest error of any output level from its nominal value. The accuracy or **absolute error** is often expressed as a **percentage of the full scale output.**

Linearity relates the maximum error in terms of the deviation from the best straight line drawn through all the possible output levels. Linearity is related to accuracy by the scale factor and output offset. If the scale factor is exactly the nominal value and offset is adjusted to zero, then accuracy and linearity are identical. Linearity is usually specified as being within ±1/2 LSB of the best straight line.

Another desirable property of D/A converter is that it be **monotonic.** This simply implies that each successive output level is greater than the preceding one. A possible worst case condition would be when the output changes from most significant bit (MSB) OFF, all other bits ON to the next level which has the MSB ON and all other bits OFF, e.g., 10000 . . . to 01111.

In applications where a quad current switch drives a transconductance amplifier (current to voltage converter), transient response is almost exclusively determined by the output amplifier itself. Where the quad output current drives a resistor to ground, switching time and settling time are useful parameters.

Switching time is the familiar 10% to 90% rise time type of measurement. Low capacitance scope probes must be used to avoid masking the high speeds that current source switching affords. The **settling time** is the elapsed time between the application of a fast input pulse and the time at which the output voltage has settled to or approached its final value within a specified limit of accuracy. This limit of accuracy should be commensurate with the resolution of the DAC to be used.

Typically, the settling time specification describes how soon after an input pulse the output can be relied upon as accurate to within ±1/2 LSB of an N bit converter. Since the 8018A family has been designed with all the collectors of the current switching transistors tied together, the output capacitance is constant. The transient response is, therefore, a simple exponential relationship, and from this the settling time can be calculated and related to the measured rise time as shown in Table 2.

Table 2: Settling Time vs. Rise Time Resistor Load

BITS OF RESOLUTION	±1/2 LSB ERROR % FULL SCALE	NUMBER OF TIME CONSTANTS	NUMBER OF RISE TIMES
8	.2%	6.2	2.8
10	05%	7 6	3.4
12	01%	9.2	4 2

Rise Time (10% - 90%) = 2.2 R_L C_{eff}

Note: All typical values have been guaranteed by characterization and are not tested

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DETAILED DESCRIPTION

An example of a practical circuit for the ICL8018A quad current switch is shown in Figure 4. The circuit can be analyzed in two sections; the first generates very accurate currents and the second causes these currents to be switched according to input logic signals. A reference current of 125μA is generated by a stable reference supply and a precision resistor. An op-amp with low offset voltage and low input bias current, such as the ICL8008, is used in conjunction with the internal reference transistor, Q_6, to force the voltage on the common base line, so that the collector current of Q_6 is equal to the reference current. The emitter current of Q_6 will be the sum of the reference current and a small base current causing a drop of slightly greater than 10 volts across the 80kΩ resistor in the emitter of Q_6. Since this resistor is connected to −15V, this puts the emitter of Q_6 at nearly −5V and the common base line at one V_{BE} more positive at −4.35V typically.

Also connected to the common base line are the switched current source transistors Q_7 through Q_{10}. The emitters of these transistors are also connected through weighted precision resistors to −15V and their collector currents summed at pin 8. Since all these transistors, Q_6 through Q_{10}, are designed to have equal emitter-base voltages, it follows that all the emitter resistors will have equal voltage drops across them. It is this constant voltage and the precision resistors at the emitter that determine the exact value of switched output current. The emitter resistor of Q_7 is equal to that of Q_6, therefore, Q_7's collector current will be I_{REF} or 125μA. Q_8 has 40kΩ in the emitter so that its collector current will be twice I_{REF} or 250μA. In the same way, the 20kΩ and 10kΩ in the emitters of Q_9 and Q_{10} contribute 0.5mA and 1mA to the total collector current.

The reference transistor and four current switching transistors are designed for equal emitter current density by making the number of emitters proportional to the current switched.

The remaining circuitry provides switching signals from the logic inputs. In the switch ON mode, zener diodes D_5 through D_8, connected to the emitter of each current switch transistor Q_7 thru Q_{10}, are reverse biased allowing the transistors to operate, producing precision currents summed in the collectors. The transistors are turned off by raising the voltage on the zeners high enough to turn on the zeners and raise the emitters of the switching transistor. This reverse biases the emitter base diode thereby shutting off that transistor's collector current.

The analog output current can be used to drive one load directly, (1kΩ to ground for FS = 1.875V for example) or can be used to drive a transconductance amplifier to give larger output voltages.

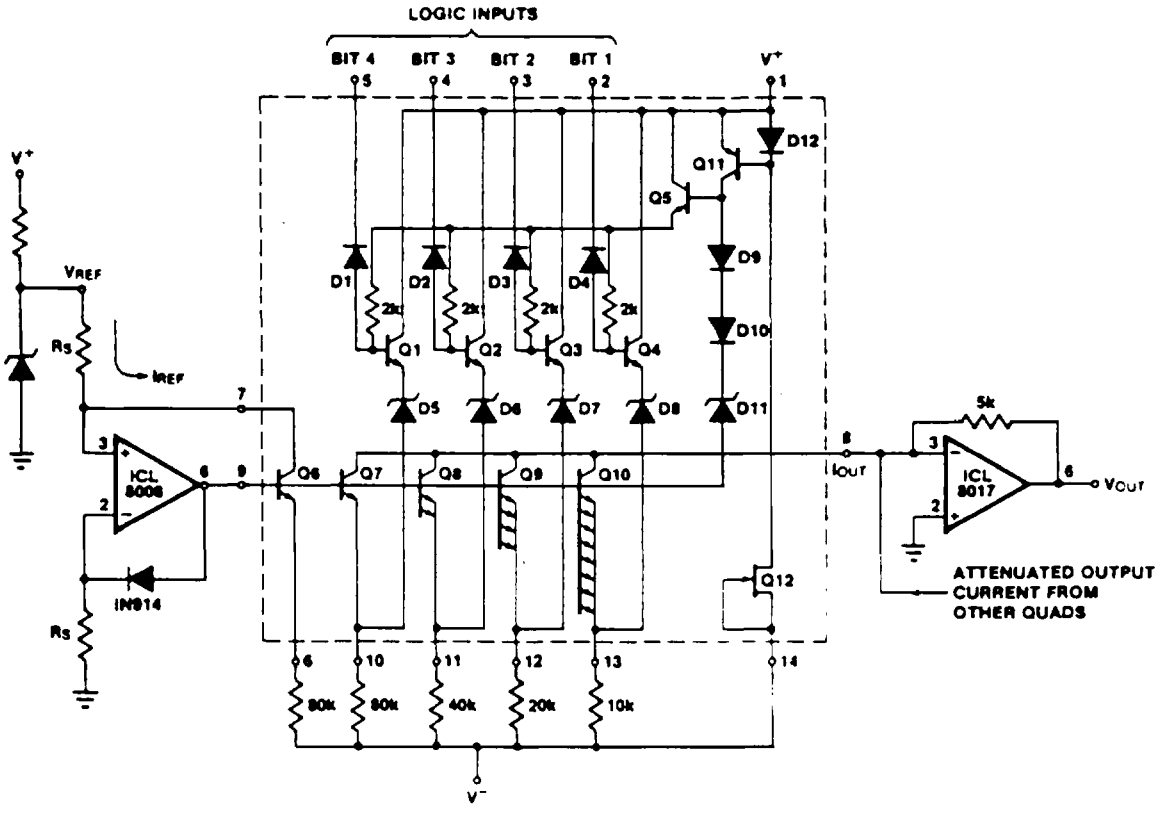

Figure 4: Typical Circuit

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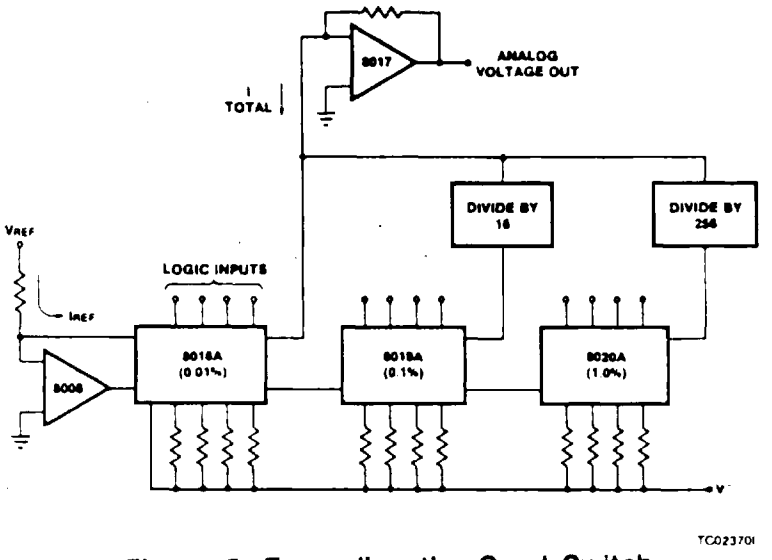

Figure 5: Expanding the Quad Switch

XPANDING THE QUAD SWITCH

While there are few requirements for only 4 bit D to A onverters, the 8018A is readily expanded to 8 and 12 bits ith the addition of other quads and resistor dividers as nown in Figure 5.

To maintain the progression of binary weighted bit urrents, the current output of the first quad drives the input f the transconductance amplifier directly, while a resistor ivider network divides the output current of the second uad by 16 and the output current of the third by 256.

$$\text{e.g., } I_{Total} = 1 \times (1 + 1/2 + 1/4 + 1/8) + 1/16(1 + 1/2 + 1/4 + 1/8) + 1/256(1 + 1/2 + 1/4 + 1/8)$$
$$= 1 + 1/2 + 1/4 + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256 + 1/512 + 1/1024 + 1/2048.$$

Note that each current switch is operating at the same igh speed current levels so that standard 10k, 20k, 40k nd 80kΩ resistor networks can be used. Another advan- age of this technique is that since the current outputs of the econd and third quad are attenuated, so are the errors hey contribute. This allows the use of less accurate witches and resistor networks in these positions; hence, he three accuracy grades of .01%, 0.1%, and 1% for the 8018A, 8019A and 8020A, respectively. It should be noted hat only the reference transistor on the most significant quad is required to set up the voltage on the common base ine joining the three sets of switching transistors (Pin 9).

GENERATING REFERENCE CURRENTS — ZENER REFERENCE

As mentioned above, the 8018A switches currents deter- mined by a constant voltage across the external precision esistors in the emitter of each switch. There are several ways of generating this constant voltage. One of the simplest is shown in Figure 6. Here an external zener diode is driven by the same current source line used to bias internal Zener D_{11}.

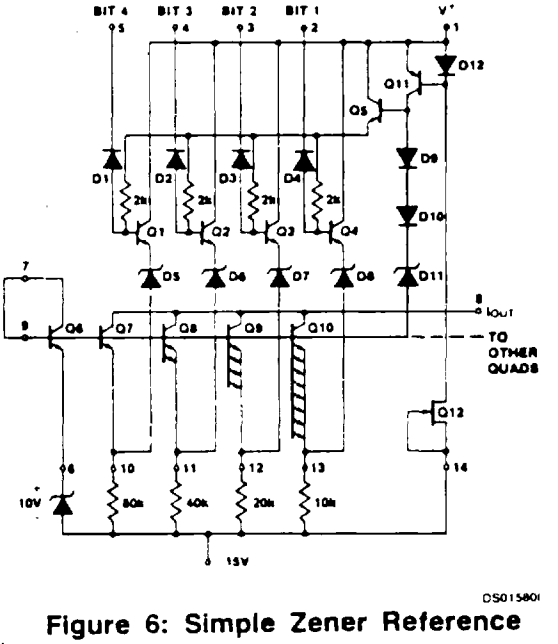

Figure 6: Simple Zener Reference

The zener current will be typically 1 mA per quad. The compensation transistor Q_6 is connected as a diode in series with the external zener. The V_{BE} of this transistor will approximately match the V_{BE}'s of the current switching transistors, thereby forcing the external zener voltage across each of the external resistors. The temperature coefficient of the external zener will dominate the temperature dependence of this scheme, however using a temperature compensated zener minimizes this problem. Since Q_6 is operating at a higher current density than the other switching transistors, the temperature matching of V_{BE}'s is not optimum, but should be adequate for a simple 8 or 10 bit converter.

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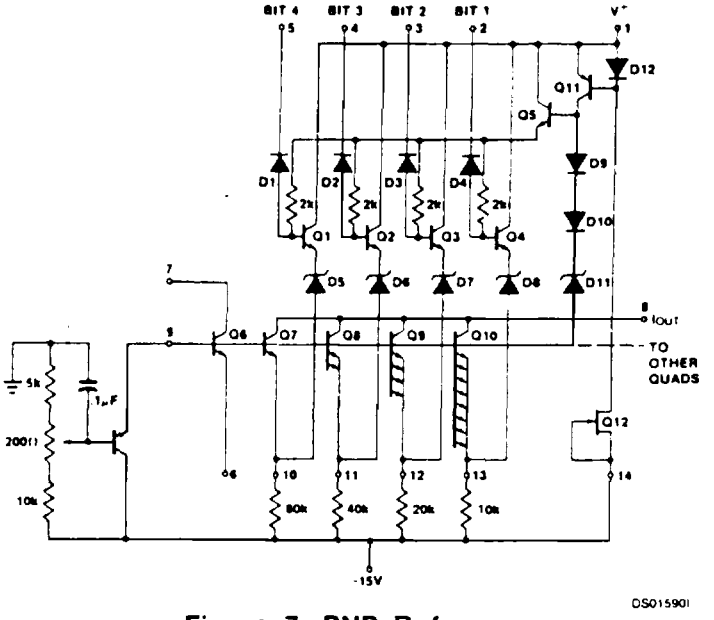

Figure 7: PNP Reference

The 8018A series is tested for accuracy with 10V reference voltage across the precision resistors, implying use of a 10 volt zener. Using a different external zener voltage will only slightly degrade accuracy if the zener voltage is above 5 or 6 volts.

When using other than 10 volt reference, the effects on logic thresholds should also be noted (see logic levels below). Full scale adjustment can be made at the output amplifier.

PNP REFERENCE

Another simple reference scheme is shown in Figure 7. Here an external PNP transistor is used to buffer a resistor divider. In this case, the −15 volt supply is used as a reference. Holding the V^- supply constant is not too difficult since the 8018A is essentially a constant current load. In this scheme, the internal compensation transistor is not necessary, since the V_{BE} matching is provided by the emitter-base junction of the external transistor. A small pot in series with the divider facilitates full scale output adjustment. A capacitor from base to collector of the external PNP will lower output impedance and minimize transient effects.

FULL COMPENSATION REFERENCE

For high accuracy, low drift applications, the reference scheme of Figure 4, offers excellent performance. In this circuit, a high gain op-amp compares two currents. The first is a reference current generated in R_S by the temperature compensated zener and the virtual ground at the non-inverting op-amp input. The second is the collector current of the reference transistor Q_6, provided on the quad switch. The output of the op-amp drives the base of Q_6 keeping its collector current exactly equal to the reference current. Since the switching transistor's emitter current densities are equal and since the precision resistors are proportional, all of the switched collector currents will have the proper value.

The op-amp feedback loop using the internal reference transistor will maintain proper currents in spite of V_{BE} drift, beta drift, resistor drift and changes in V^-. Using this circuit, temperature drifts of 2 ppm/°C are typical. A discrete diode connected as shown will keep Q_6 from saturating and prevent latch up if V^- is disconnected.

In any reference scheme, it is advisable to capacitively decouple the common base line to minimize transient effects. A capacitor, .001μF to .1μF from Pin 9 to analog ground is usually sufficient.

IMPROVED ACCURACY

As a final note on the subject of setting up reference levels, it should be pointed out that the largest contributor of error is the mismatch of V_{BE}'s of the current switching transistors. That is, if all the V_{BE}'s were identical, then all precision resistors would have exactly the same reference voltage across them. A one millivolt mismatch compared with ten volt reference across the precision resistors will cause a .01% error. While decreasing the reference voltage will decrease the accuracy, the voltage can be increased to achieve better than .01% accuracies. The voltage across the emitter resistors can be doubled or tripled with a proportional increase in resistor values resulting in improved absolute accuracy as well as improved temperature drift performance. This technique has been used successfully to implement up to 16 bit D/A converters.

For further information see the following Applications Bulletins.

A016 "Selecting A/D Converters" by Dave Fullagar.
A018 "Do's and Don'ts of Applying A/D Converters" by Peter Bradshaw and Skip Osgood.
A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing" by Ed Sliger.

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