KAI-1003

1024 (H) x 1024 (V) Interline CCD Image Sensor

Description

The KAI−1003 Image Sensor is a high-performance megapixel monochrome image sensor designed for a wide range of medical imaging and machine vision applications.

The 12.8 μm square pixels with microlenses provide high sensitivity and the large capacity results in large dynamic range. The two output, split horizontal register and several binning modes allow a 15 to 60 frame per second (fps) video rate for the progressively scanned images.

The vertical overflow drain structure provides anti-blooming protection, and enables electronic shuttering for precise exposure control. Other features include low dark current, negligible lag and low smear.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CDD; Progressive Scan
Total Number of Pixels	1056 (H) × 1032 (V)
Number of Effective Pixels	1028 (H) × 1028 (V)
Number of Active Pixels	1024 (H) × 1024 (V)
Pixel Size	12.8 μm(H) × 12.8 μm (V)
Active Image Size	13.1 mm (H) × 13.1 mm (V), 18.5 mm (Diagonal), 4/3″ Optical Format
Aspect Ratio	1:1
Number of Outputs	1 or 2
Charge Capacity	170,000 e^-
Output Sensitivity	7.5 μV/e^-
Quantum Efficiency (500 nm)	45%
Read Noise (f = 20 MHz)	40 e^- rms
Dark Current	< 0.5 nA/cm^2
Dynamic Range	72 dB
Blooming Suppression	> 100 X
Smear	−80 dB
Maximum Pixel Clock Speed	20 MHz
Maximum Frame Rate Single Output Dual Output Dual Output 2×2 Bin	 15 fps 30 fps 60 fps
Package	28-Pin CERDIP
Cover Glass	AR Coated, 2 Sides

NOTE: All Parameters are specified at T = 40°C unless otherwise noted.

ON Semiconductor®

www.onsemi.com

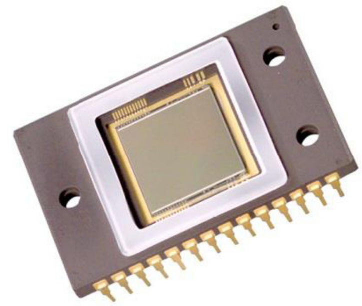

Figure 1. KAI−1003 Interline CCD Image Sensor

Features

- Megapixel Progressive Scan Interline CCD
- 1024 (H) × 1024 (V) Imaging Pixels
- 12.8 μm Square Pixels
- 13.1 mm Square Imaging Area
- Microlenses for Increased Sensitivity
- Large Capacity (170 ke^-)
- Split Horizontal Register for 1 or 2 Outputs
- Binning to 1 × 2 or 2 × 2

Applications

- Machine Vision
- Medical
- Scientific

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAI−1003 IMAGE SENSOR

Part Number	Description	Marking Code
KAI−1003−AAA−CR−AE	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	KAI−1003 Serial Number
KAI−1003−AAA−CR−B2	Monochrome, No Microlens, CERDIP Package (Sidebrazed), Taped Clear Cover Glass with AR Coating (Both Sides), Grade 2	
KAI−1003−ABA−CD−AE	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Engineering Sample	KAI−1003M Serial Number
KAI−1003−ABA−CD−B2	Monochrome, Telecentric Microlens, CERDIP Package (Sidebrazed), Clear Cover Glass with AR Coating (Both Sides), Grade 2	

Table 3. ORDERING INFORMATION − EVALUATION SUPPORT

Part Number	Description
KAI−1003−12−20−A−EVK	Evaluation Board (Complete Kit)

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

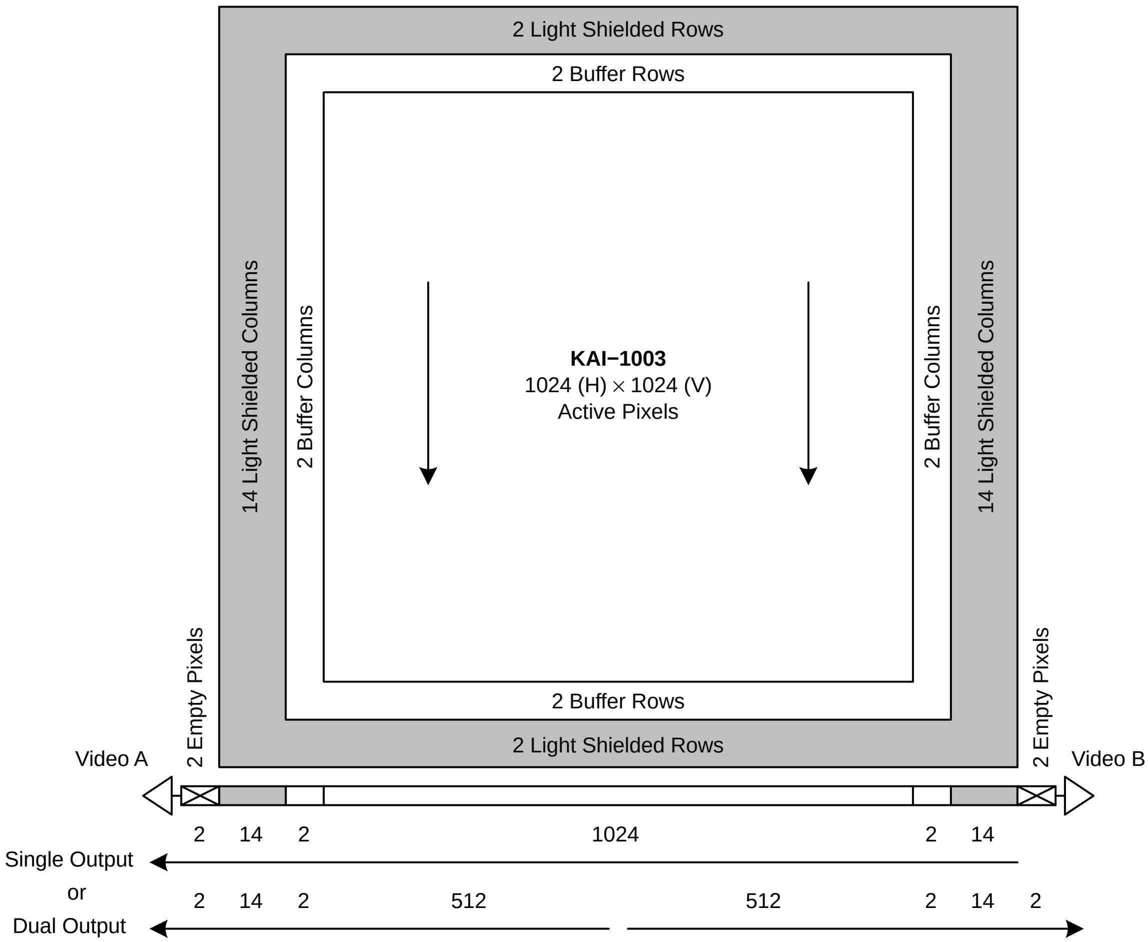

Figure 2. Sensor Architecture

The KAI−1003 is a high-performance, interline charge-coupled device (CCD) designed for a wide range of medical imaging and machine vision applications. The device is built using an advanced two-phase, double-polysilicon, NMOS CCD technology. The p+npn− photodiodes eliminate image lag while providing anti-blooming protection and electronic shutter capability. The 12.8 μm square pixels with microlenses provide high sensitivity and large dynamic range. The two output, split horizontal register and several binning modes enable a 15 to 60 frame per second (fps) video rate with this megapixel progressive scan imager.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photodiode. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent on light level and integration time and non-linearly dependent on wavelength. When the photodiode's charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming. The integration time can be decreased below the frame time by using an electronic shutter, which is a voltage pulse applied to the substrate to empty the photodiodes.

Charge Transport

The integrated charge from each photodiode is transported to the output by a three-step process. The charge is first transferred from the photodiodes to the vertical shift registers by applying a large positive voltage to one of the vertical CCD phases. This transfer occurs simultaneously for all photodiodes. The charge is then transported from the vertical CCD registers to the horizontal CCD line by line in parallel. Finally, the horizontal CCD register transports each line of charge pixel by pixel serially to one or both of the output structures.

The single horizontal CCD register is split into two halves to allow a variety of line readout modes, as shown in

Figure 2 and Figure 3. The A output half of the register is a true two-phase design, which results in unidirectional transport using phases H1A and H2A. The B output half of the register is a pseudo two-phase design, which allows bi-directional transport using phases H1B, H2B, H1C and H2C. Dual output is achieved with all of the first phases identical and all the second phases identical. If the clocks of H1A and H2A phases are shifted by one half cycle, the output remains dual with the outputs alternating, so that only one analog-to-digital converter is necessary. Finally, single output of the entire image from the A output is obtained by complementing the C phases, which reverses transport in the B half of the horizontal CCD.

Binning can be used in a 1×2 and a 2×2 mode. Two successive vertical transfers vertically bin the charge directly onto the horizontal CCD, as shown in Figure 13 and Figure 14. Horizontal binning is accomplished by two successive horizontal transfers onto the H22 gate, which then transfers the charge to the output structure, as shown in Figure 15.

Combinations of output modes, binning and horizontal clock frequency allow the range of frame rates listed in.

Table 4. KAI−1003 CALCULATED CLOCK PARAMETERS

Parameter	Binning (H × V)	1×1	1×2	2×1	2×2	1×1	Unit
	Output	**Dual**	**Dual**	**Dual**	**Dual**	**Single**	
HORIZONTAL CLOCK							
Frequency		20	20	20	40	20	MHz
Period	Actual Effective	50 50	50 50	50 100	25 50	50 50	ns
Pixel Counts	Actual Effective	532 532	532 532	532 266	532 266	1060 1060	
VERTICAL TO HORIZONTAL TRANSFER (HORIZONTAL RETRACE TIME)							
Equivalent H-Clock Counts (m)		80	80	80	160	80	
Duration		4.0	4.0	4.0	4.0	4.0	μs
HORIZONTAL LINE TIME							
Total H-Clock Counts		612	612	612	692	1140	
Line time		30.6	30.6	30.6	17.3	57.0	μs
VERTICAL CLOCK							
Line Counts	Actual Effective	1032 1032	1032 516	1032 516	1032 516	1032 1032	
PHOTODIODE READ (VERTICAL RETRACE TIME)							
Equivalent Line Counts (n)		4	4	4	7	2	
Duration		122.4	122.4	122.4	121.1	114.0	μs
FRAME RATE							
Total Effective Line Counts		1036	520	520	523	1034	
Frame Time		31.7	15.9	15.9	9.0	58.9	ms
Frame Rate		31.5	62.8	62.8	110.5	17.0	frames/s

1. Time values have been rounded.
2. The number of counts (n and m) shown here are nominal integers, but in general they do not need be integers. They can be adjusted for frame time, so long as the horizontal and vertical retrace times exceed the minimums specified in AC Timing Requirements.
3. Operation at 40 MHz will have increased readout noise.

Output Structure

Charge presented to the floating diffusion (FD) is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and the FD is reset to the potential applied by the reset drain (RD). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the output pin of the device.

Non-Imaging Pixels

In addition to the 1024 (H) by 1024 (V) imaging pixels, there are active buffer, light shielded and empty pixels, as shown in Figure 2. A two-pixel border of active buffer pixels surrounds the imaging area. These buffer pixels respond to illumination but are not tested for defects and non-uniformities. Two light shielded rows lead and follow each frame, and 14 light shielded columns lead and follow each line. The light shielded columns are tested for column defects and can be used for dark reference. Only the center 10 columns by 1028 rows of light shielded region on each side can be used for dark reference due to light leakage into the border of two pixels at the edges. Finally, two empty pixels occur at the beginning of each line, which are empty shift register cycles not associated with any vertical CCD columns. Empty pixels may also occur at the end of the line, depending on the timing.

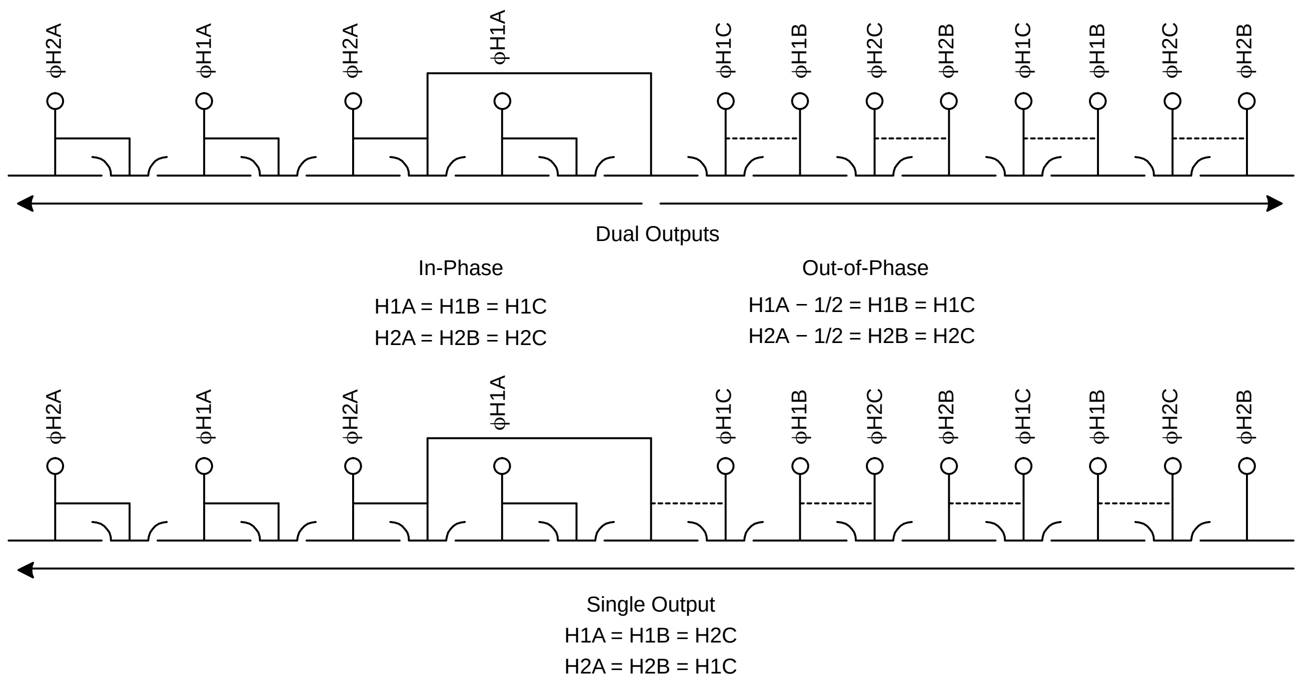

Figure 3. Horizontal CCD Registers

Pin Description and Device Orientation

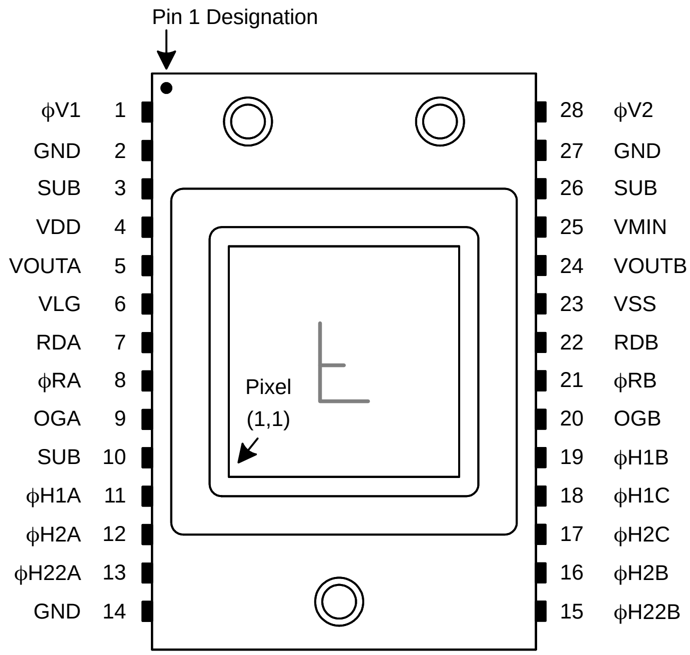

Figure 4. Pin Description (Top View)

Table 5. PIN DESCRIPTION

Pin No.	Label
1	φV1
2	GND
3	SUB
4	VDD
5	VOUTA
6	VLG
7	RDA
8	φRA
9	OGA
10	SUB
11	φH1A
12	φH2A
13	φH22A
14	GND

Pin No.	Label
15	φH22B
16	φH2B
17	φH2C
18	φH1C
19	φH1B
20	OGB
21	φRB
22	RDB
23	VSS
24	VOUTB
25	VMIN
26	SUB
27	GND
28	φV2

PERFORMANCE SPECIFICATIONS

Table 6. PERFORMANCE SPECIFICATIONS
(All values measured at 40°C and 30 fps (integration time = 33 ms, f_H = 20 MHz) for nominal operating parameters unless otherwise noted. These parameters exclude defective pixels.)

Description	Symbol	Min.	Nom.	Max.	Unit
Saturation Charge Capacity with Blooming Control	Q_{SAT}	170	−	−	ke^-
Output Gain		6.5	7.5	8.5	$\mu V/e^-$
Output Voltage at the Saturation Level	V_{SAT}	−	1.3	−	V
Quantum Efficiency at 500 nm		−	32	−	%
Quantum Efficiency at 540 nm		−	30	−	%
Quantum Efficiency at 600 nm		−	24	−	%
CCD Readout Noise with CDS		−	40	50	e^- rms
Dark Current	I_{DARK}	−	0.25	0.45	nA/cm^2
Anti-Blooming Factor (Notes 1, 2)	X_{AB}	100	−	−	
Vertical Smear (Notes 2, 6)		−	0.005	0.01	%
Non-Uniformity of Sensitivity (Notes 3, 4)		−	0.3	0.5	% rms
Non-Uniformity of Dark Current (Note 4)		−	14	−	e^- rms
Output Signal Non-Linearity (Note 5)		−	1	2	%
Gain Difference between the Two Video Outputs (Note 5)		−	−	10	%
Non-Uniformity of Gain between the Two Outputs (Note 5)		−	0.5	1.5	%

1. The illumination required to bloom the image sensor reported as a multiple of the saturation intensity. Blooming is defined as doubling the vertical height of a spot that is 10% of the vertical CCD height at the saturation intensity.
2. Measured with continuous green light centered at 550 nm, F/4 optics and a spot size that is 10% of the vertical CCD height.
3. Measured at 90% of 150 ke^- output.
4. Measured in the center 50 × 50 pixels.
5. Between 10% and 90% of 150 ke^- output.
6. Measured without electronic shutter operation.

Typical Quantum Efficiency

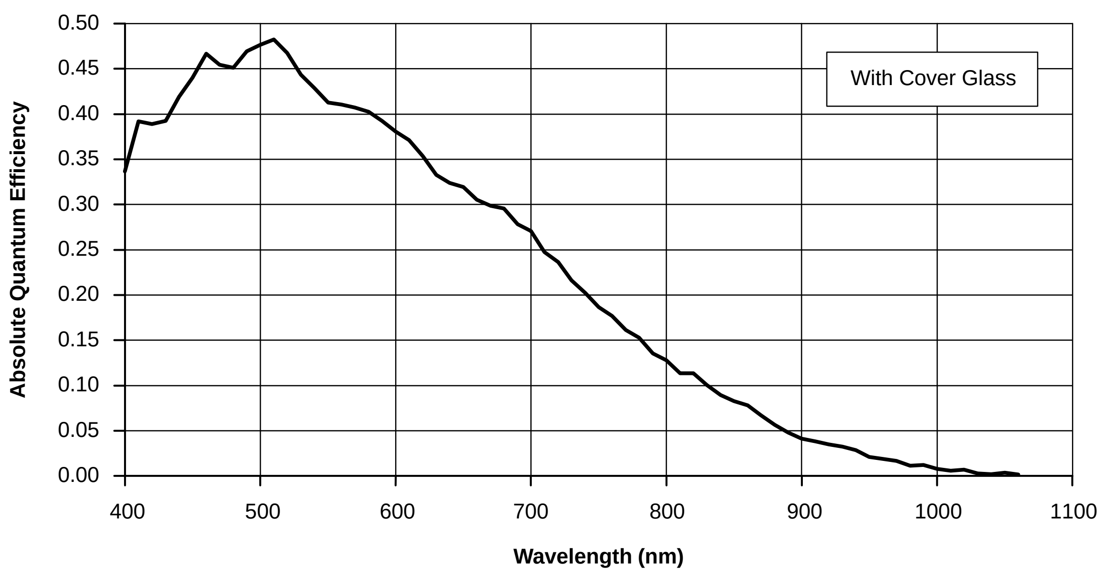

Figure 5. Quantum Efficiency Spectrum

Angular Dependance of Quantum Efficiency

For the curve marked “Horizontal”, the incident light angle is varied in a plane parallel to the HCCD.

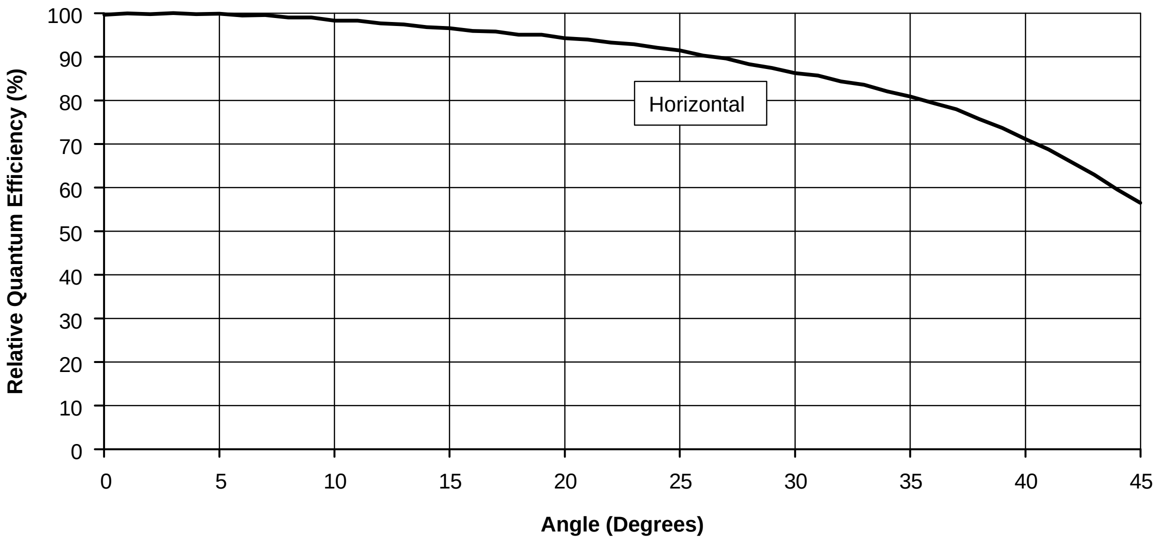

Figure 6. Angular Dependance of Quantum Efficiency

DEFECT SPECIFICATIONS

Defect Test Conditions

Temperature:	40°C
Integration Time:	33 ms (20 MHz HCCD Frequency, No Binning, 30 fps Frame Rate)
Light Source:	Continuous Green Light Centered at 550 nm
Operation:	Nominal Voltages and Timing

Table 7. DEFECT DEFINITIONS

Name	Maximum Number	Definition
Major Defective Pixel	20	A pixel whose signal deviates by more than 25 mV from the mean value of all active pixels under dark field condition or by more than 8% from the mean value of all active pixels under uniform illumination at 105 ke^{-} output signal.
Minor Defective Pixel	100	A pixel whose signal deviates by more than 8 mV from the mean value of all active pixels under dark field condition.
Cluster Defect	4	A group of 2 to 6 contiguous major defective pixels, but no more than 2 adjacent defects horizontally.
Column Defect	0	A group of more than 6 contiguous major defective pixels along a single column.

Defect Proximity

Minimum Distance between Defective Clusters:	2 Pixels in All Directions without Major Pixel Defects
Minimum Distance between Defective Columns:	3 Columns without Column Defects or Cluster Defects

OPERATION

Table 8. ABSOLUTE MAXIMUM RATINGS

Item	Description	Min.	Max	Unit
Temperature	Operation to Specification	0	40	°C
	Operation without Damage	−10	70	°C
	Storage	−55	80	°C
Relative Humidity	Operation without Damage (Note 1)	0	95	%
Voltage (Between Pins)	SUB − GND (Notes 2, 5)	−0.6	50	V
	V_{RD}, V_{SS}, V_{DD} − GND	−0.6	25	V
	V_{MIN} − GND	−15	0.6	V
	All Clocks − GND	−	17	V
	ϕV1 − ϕV2 (Note 3)	−	17	V
	ϕH1 − ϕH2	−	17	V
	ϕH1, ϕH2 − ϕV2	−	17	V
	ϕH2 − OG	−	17	V
	V_{LG}, OG – GND	−	17	V
	ϕR, ϕH1, ϕH2 − V_{MIN}	−	17	V
Capacitance	Output Load Capacitance (C_{LOAD}) (Note 4)	−	10	pF
Current	Output Bias Current (I_{DD}) (Note 4)	−	10	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Without condensation.
2. Under normal operating conditions, the substrate voltage should be maintained above 8.0 V. The substrate voltage should not remain above 25 V for longer than 100 μs.
3. Maximum of 20 V for ϕV1H − ϕV2L, with 20 μs maximum duration.
4. Each output.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Table 9. DC OPERATING CONDITIONS

Description	Symbol	Min.	Nom.	Max.	Unit
Output Gate	OG	1.8	2.0	2.2	V
Reset Drain	V_{RD}	10.0	10.5	11.0	V
Output Amplifier Return (Note 1)	V_{SS}	−	0.0	−	V
Output Amplifier Load Gate	V_{LG}	1.4	1.5	1.6	V
Output Amplifier Supply	V_{DD}	14.5	15.0	15.5	V
Disable ESD Protection (Note 2)	V_{MIN}	−	−8.5	−	V
Substrate (Notes 3, 4, 5)	V_{SUB}	8.0	TBS	18.0	V
Ground, P-Well (Note 4)	GND	−	0.0	−	V

1. Current sink.
2. Connect a 0.001 μF capacitor between V_{MIN} and GND. V_{MIN} must be more negative than the low voltage of any of the ϕH clocks and should be established before the ϕH voltage is applied.
3. DC value when electronic shutter is not in use. See AC Clock Level Conditions for electronic shutter pulse voltage. The operating value of the substrate voltage, V_{SUB}, will be supplied with each shipment.
4. Ground and substrate biases should be established before other gate and diode potentials are applied.
5. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Table 10. AC CLOCK LEVEL CONDITIONS

Description	Level	Symbol	Min.	Nom.	Max.	Unit
Vertical CCD Clocks (Note 1)	High	ϕV2H	9.5	10.5	11.5	V
	Mid	ϕV1M, ϕV2M	−0.8	−0.5	0.0	V
	Low	ϕV1L, ϕV2L	−9.0	−8.5	−8.0	V
Horizontal CCD Clocks (Note 1)	High	ϕH1H, ϕH2H	4.5	5.0	5.5	V
	Low	ϕH1L, ϕH2L	−6.5	−6.0	−5.5	V
Reset Clock	Amplitude	ϕR_{SWING}	−	5.0	−	V
	Low (Note 2)	$V_{\phi Rlow}$	0	TBS	5.0	V
Electronic Shutter Pulse (Notes 3, 4)	Shutter	$V_{SHUTTER}$	37	40	45	V

1. For best results, the CCD clock swings must be greater than or equal to the nominal values.
2. Reset clock low level voltage will be supplied with each shipment.
3. Electronic shutter pulse voltage referenced to GND. See DC Operating Conditions for DC level when electronic shutter is not in use.
4. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions*.

Electronic Shutter Operation

Electronic shuttering is accomplished by pulsing the substrate voltage to empty the photodiodes. See Figure 16 for timing. The pulse must not occur while useful information is being read from a line.

Table 11. CALCULATED CLOCK CAPACITANCE

Description	Phase	Symbol	Typical	Unit
Vertical CCD Clocks (Note 1)	1 to GND	C ϕV1	55/37	nF
	2 to GND	C ϕV2	50/32	nF
	1 to 2	C ϕV1 − ϕV2	4	nF
Horizontal CCD Clocks (Notes 1, 2)	1A	C ϕH1A	58/21	pF
	1B	C ϕH1B	41/13	pF
	1C	C ϕH1C	15/10	pF
	2A	C ϕH2A	48/22	pF
	2B	C ϕH2B	30/11	pF
	2C	C ϕH2C	18/13	pF
HCCD Summing Clock		C ϕH22A/B	3	pF
Reset Clock − GND		C ϕRA/B	5	pF

1. Accumulation/depletion capacitances.
2. Capacitance of this gate to GND and all other gates.

Table 12. AC TIMING REQUIREMENTS

Description	Symbol	Min.	Nom.	Max.	Unit
Vertical High Level Duration	t_{V2H}	15	−	20	μs
Vertical Transfer Time (Note 1)	t_V	1.0	2.0/1.0	−	μs
Vertical Pedestal Delay 1 & 3	t_{VPD1}, t_{VPD3}	40	−	−	μs
Vertical Pedestal Delay 2	t_{VPD2}	15	−	−	μs
Horizontal Delay (Note 1)	t_{HD}	1.5/0.5	−	−	μs
Reset Duration (Note 2)	t_R	−	10	−	ns
Horizontal CCD Clock Frequency (Note 3)	f_H	−	20	−	MHz
Pixel Time	t_H	−	50	−	ns
Line Time (Note 4)	t_L	−	−	−	
Frame Time (Note 4)	t_F	−	−	−	
Clamp Delay (Note 5)	t_{CD}	−	−	−	ns
Sample Delay (Note 5)	t_{SD}	−	−	−	ns
Electronic Shutter Pulse Duration	t_{ES}	5	7.5	10	μs
Electronic Shutter Horizontal Delay	t_{ESHD}	1.0	−	−	μs

1. Non-binning/binning times.
2. The rising edge of ϕR should be coincident with the rising edge of ϕH22, within ±5 ns.
3. Horizontal CCD clock frequency can be increased to 40 MHz, with increased readout noise.
4. See Table 4 for nominal line and frame time in each mode.
5. The clamp delay and sample delay should be adjusted for optimum results.

Table 13. CCD CLOCK WAVEFORM CONDITIONS

Description	Phase	Symbol	t_{WH}	t_{WL}	t_R	t_F	Unit
NON-BINNING							
Vertical CCD Clocks	1	ϕV1M/L	−	1.5	0.5	0.5	μs
	2	ϕV2M/L	1.5	−	0.5	0.5	μs
	2, High	ϕV2H	15		1.0	1.0	μs
Horizontal CCD Clocks	1	ϕH1	20.5	21.5	4.0	4.0	ns
	2	ϕH2	20.5	21.5	4.0	4.0	ns
	2, Binning (Note 1)	ϕH22	20.5	21.5	4.0	4.0	ns
Reset clock		ϕR	5	39	3	3	ns
2×2 BINNING							
Vertical CCD Clocks	1 (Note 2)	ϕV1M/L	0.5	0.5	0.5	0.5	μs
	2 (Note 2)	ϕV2M/L	0.5	0.5	0.5	0.5	μs
	2, High	ϕV2H	15	−	1.0	1.0	μs
Horizontal CCD Clocks	1	ϕH1	20.5	21.5	4.0	4.0	ns
	2	ϕH2	20.5	21.5	4.0	4.0	ns
	2, Binning	ϕH22	46.0	46.0	4.0	4.0	ns
Reset clock		ϕR	5	89	3	3	ns

1. Typical values measured with clocks connected to image sensor device. The actual values should be optimized for particular board layout.
2. ϕH22 may be connected to ϕH2 in 1×1 mode.
3. t_{WH} and t_{WL} for ϕV1M/L and ϕV2M/L are the time periods during the double pulses.

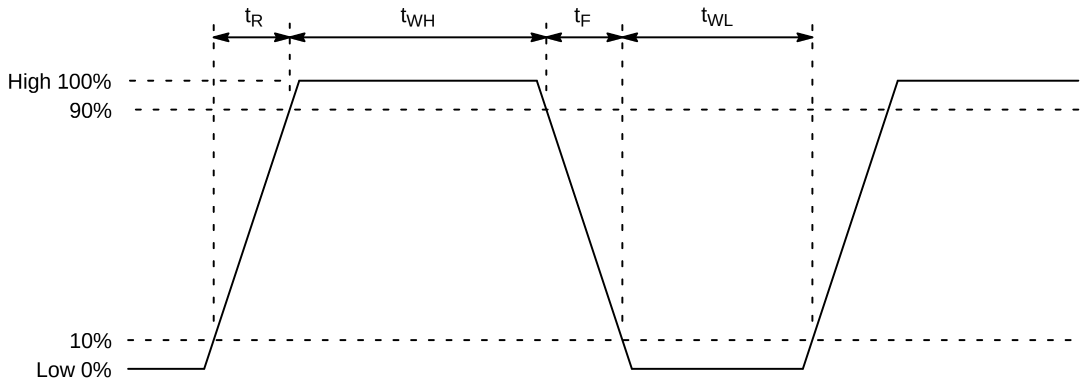

Figure 7. CCD Clock Waveform

TIMING

Frame Timing − 1×1

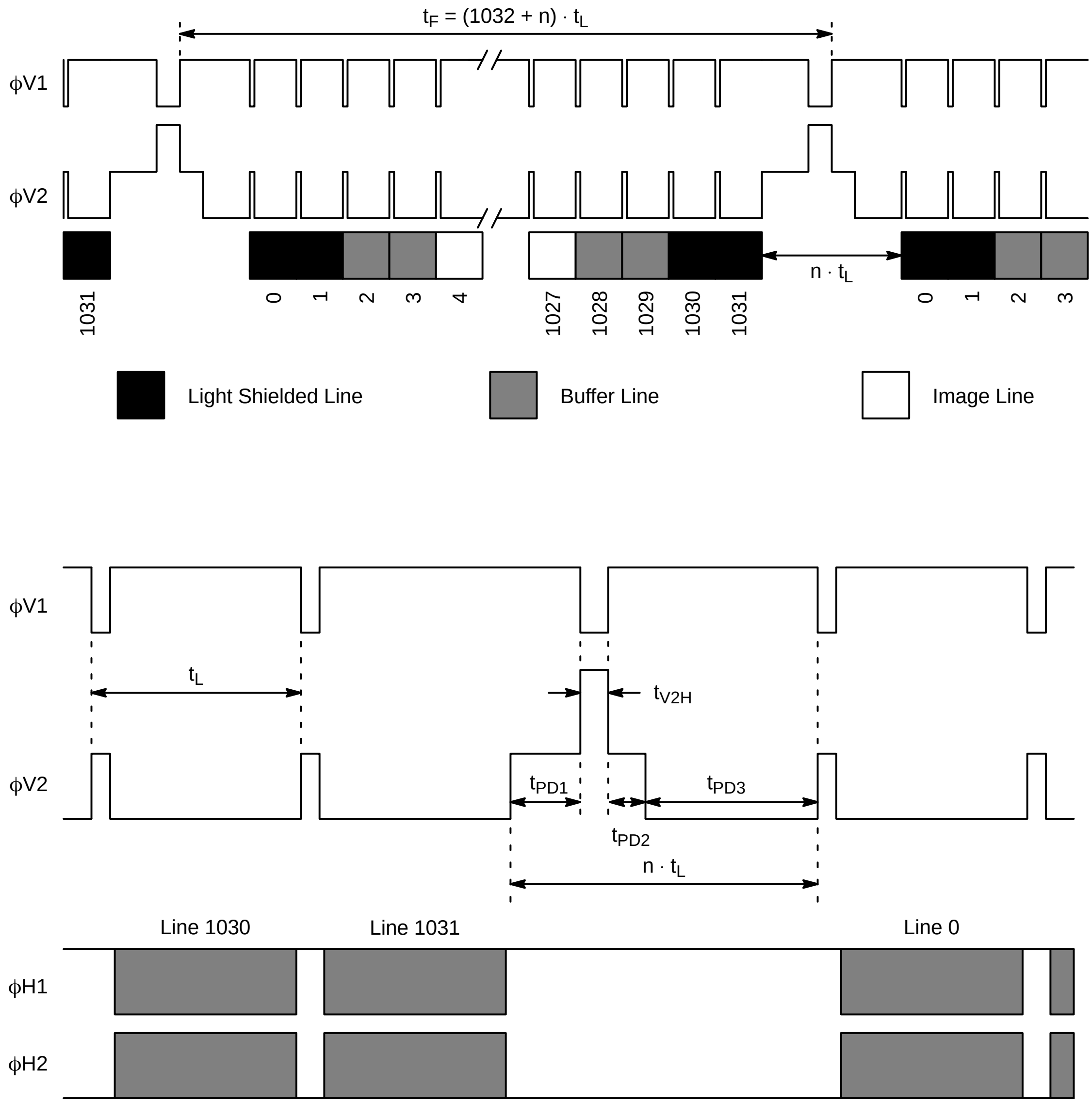

Figure 8. Frame Timing − 1×1

Line Timing − 1×1 − Single Output

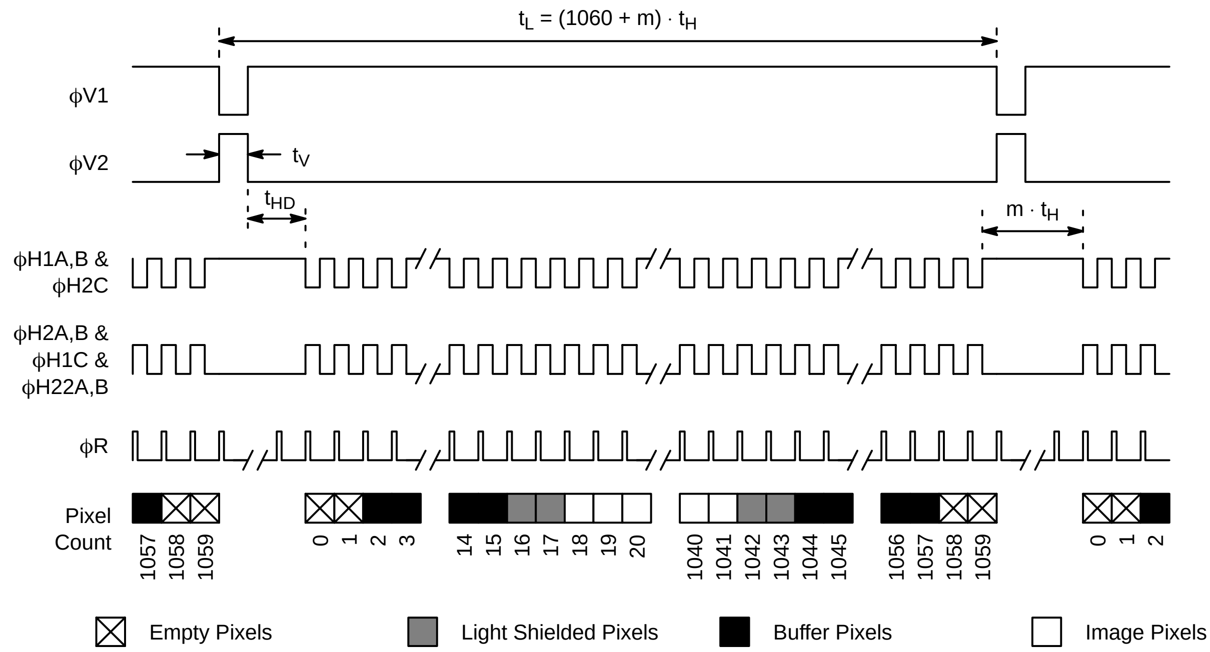

Figure 9. Line Timing − 1×1 − Single Output

Line Timing − 1×1 − Dual Output, In-Phase

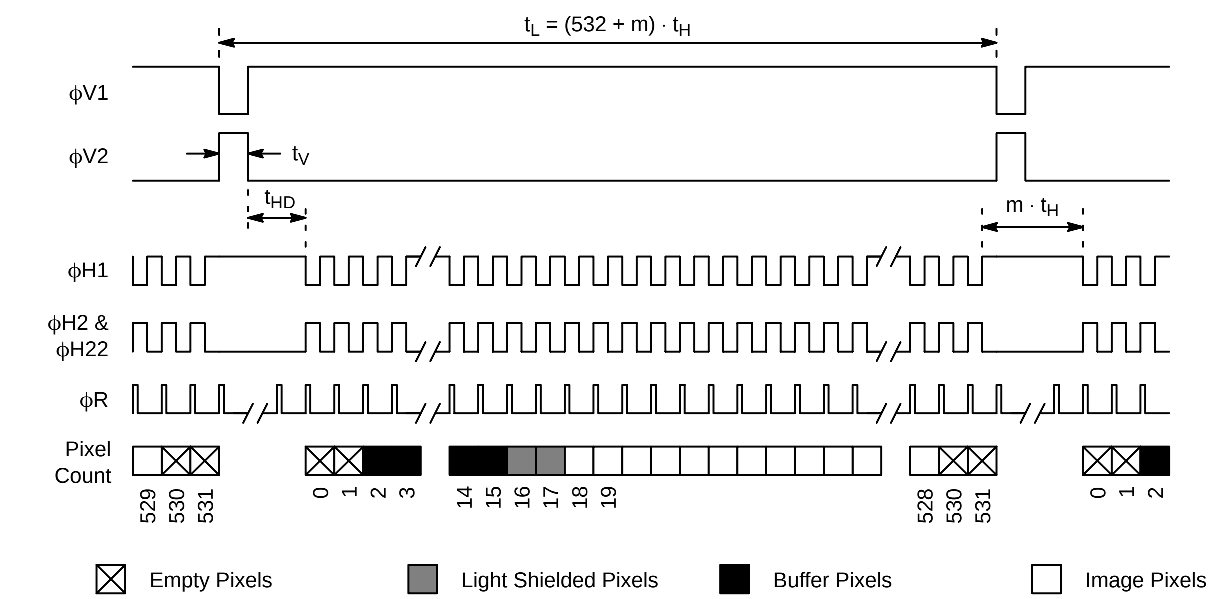

Figure 10. Line Timing − 1×1 − Dual Output, In-Phase

Line Timing − 1×1 − Dual Output, Out-of-Phase

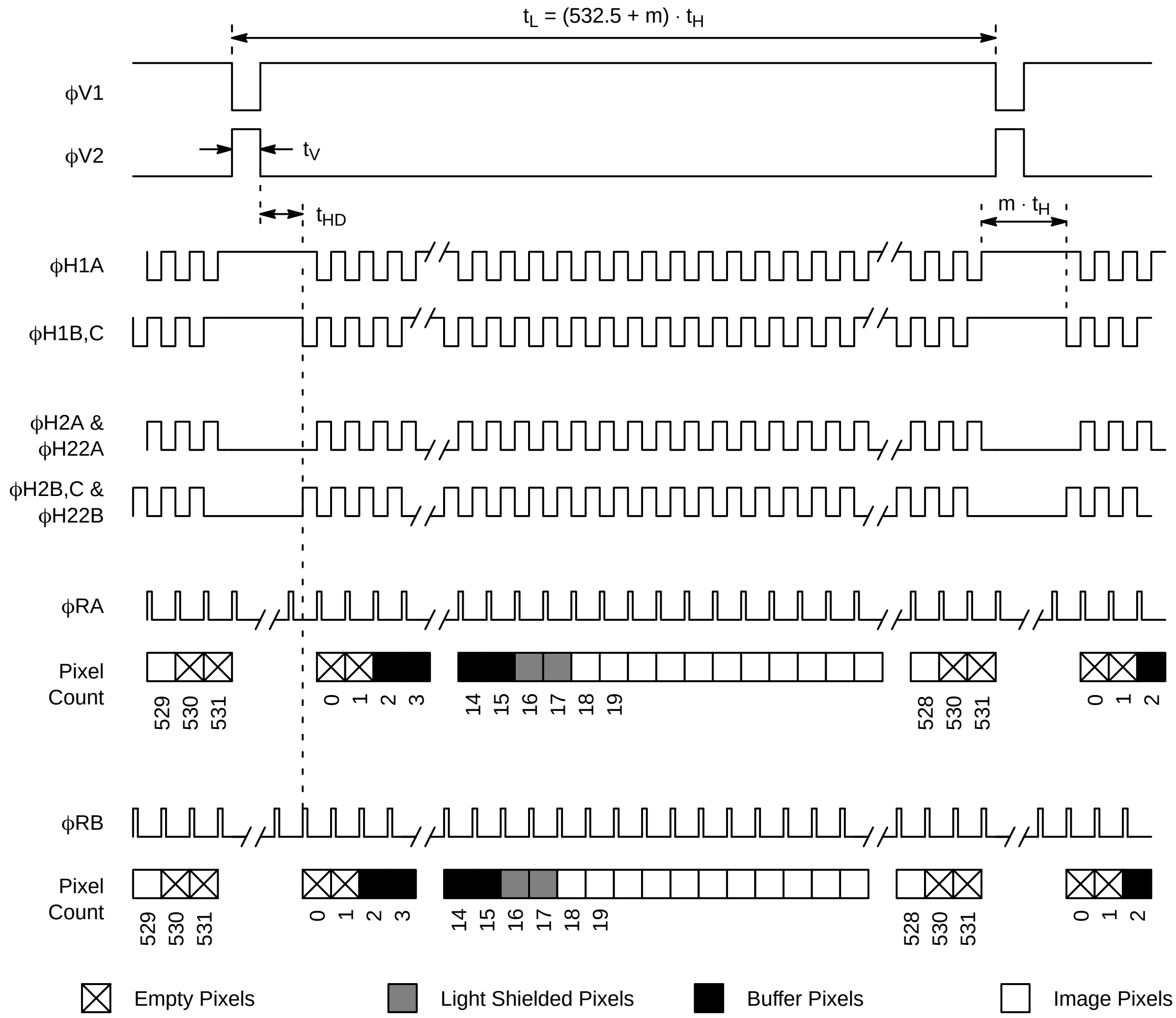

Figure 11. Line Timing − 1×1 − Dual Output, Out-of-Phase

Pixel Timing − 1×1

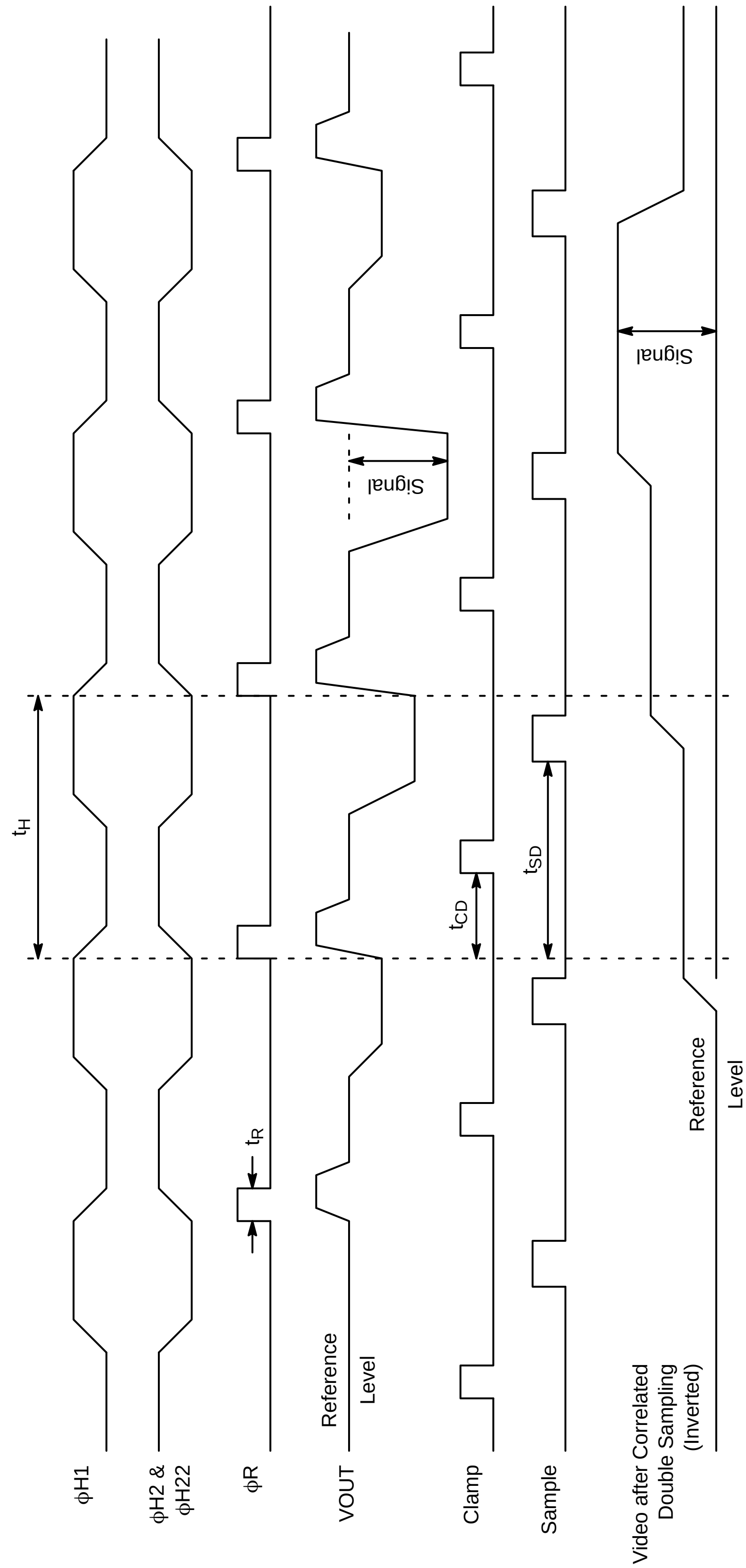

Figure 12. Pixel Timing − 1×1

Frame Timing − 2×2

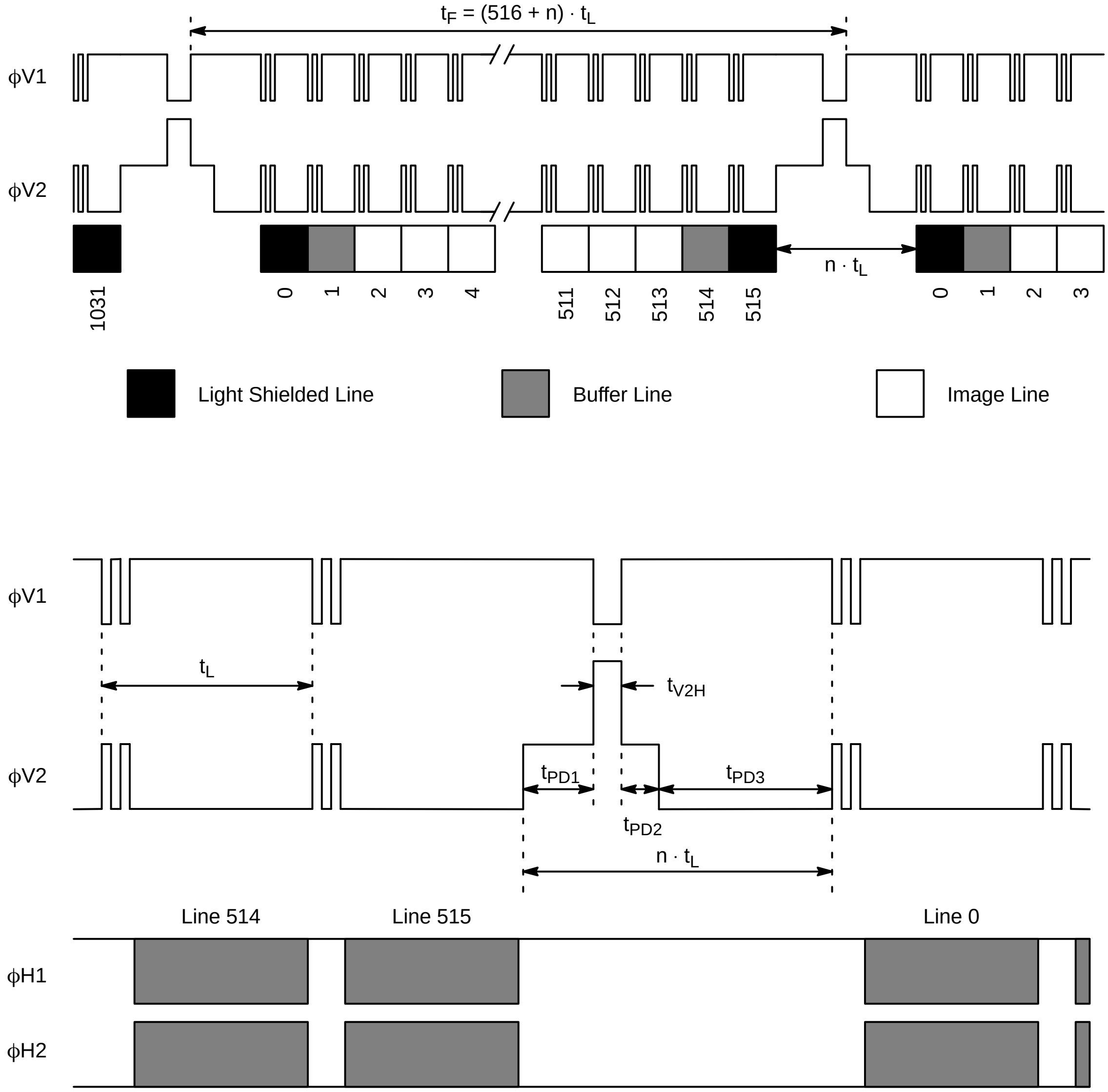

Figure 13. Frame Timing − 2×2

Line Timing − 2×2

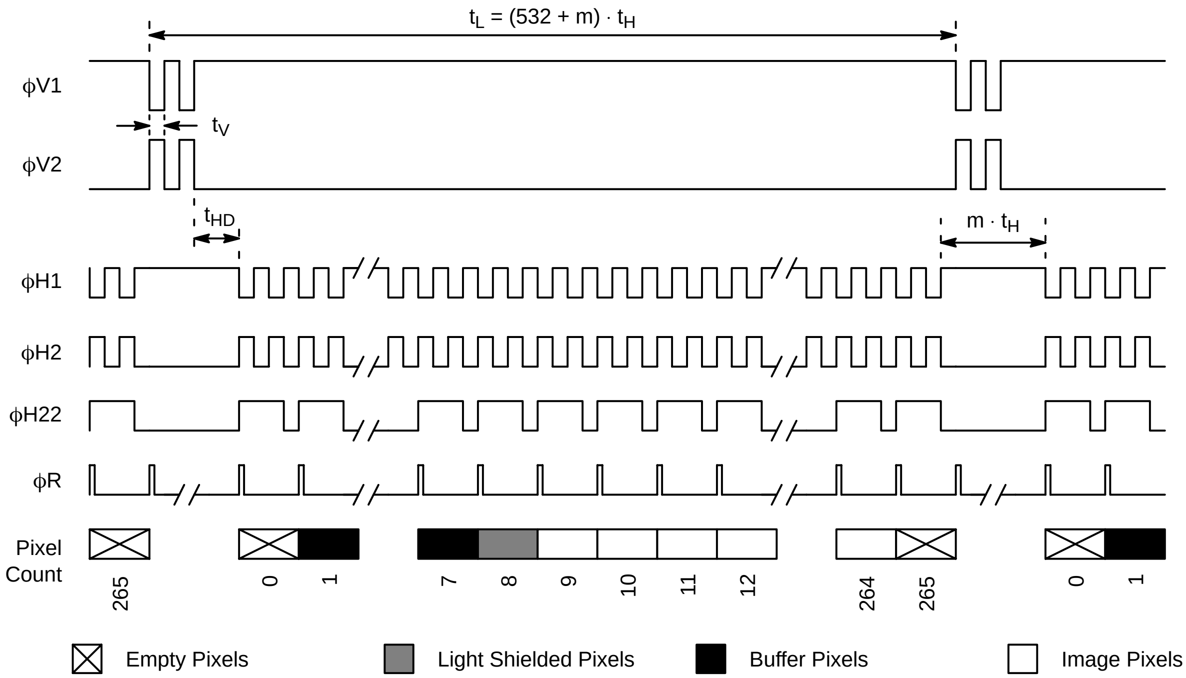

Figure 14. Line Timing − 2×2

Pixel Timing − 2×2

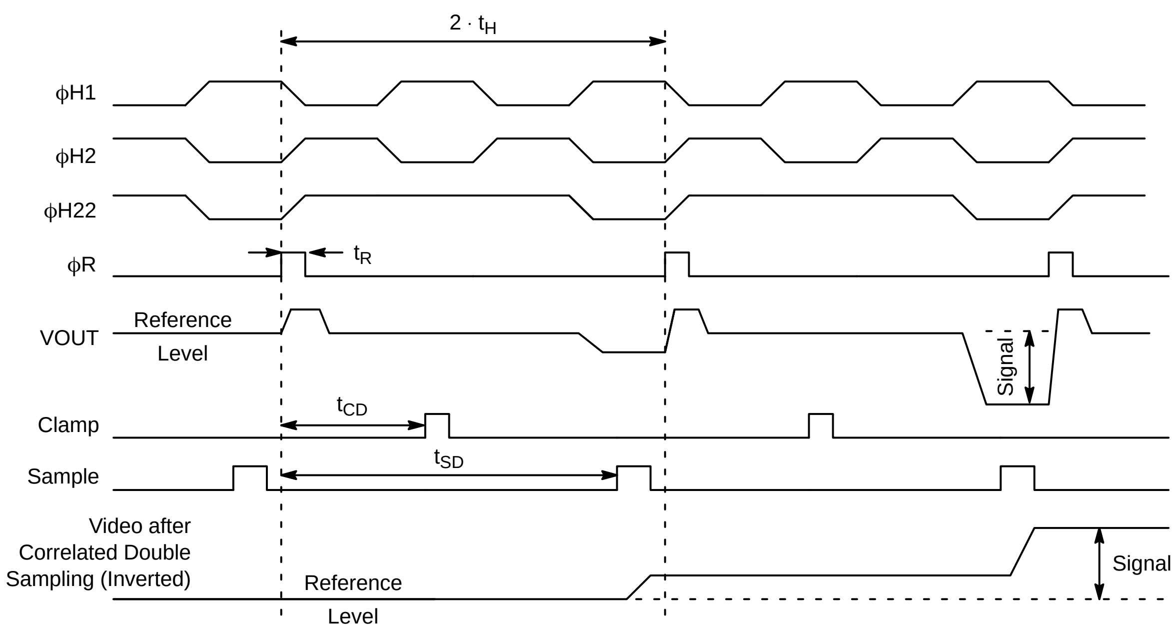

Figure 15. Pixel Timing − 2×2

Electronic Shutter Line Timing

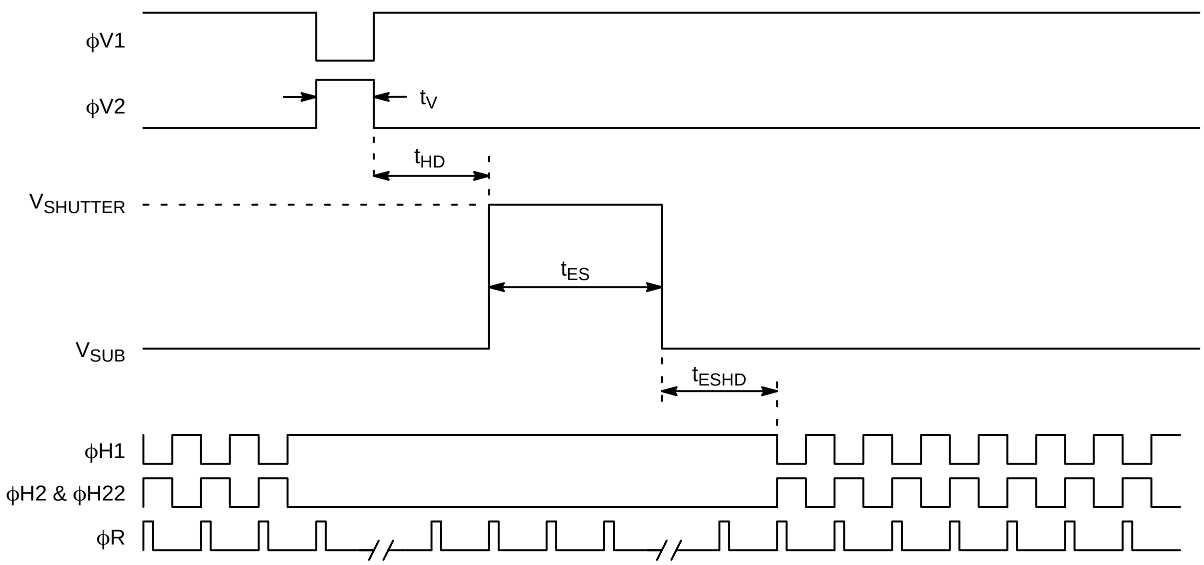

Figure 16. Electronic Shutter Line Timing

Integration Time Definition

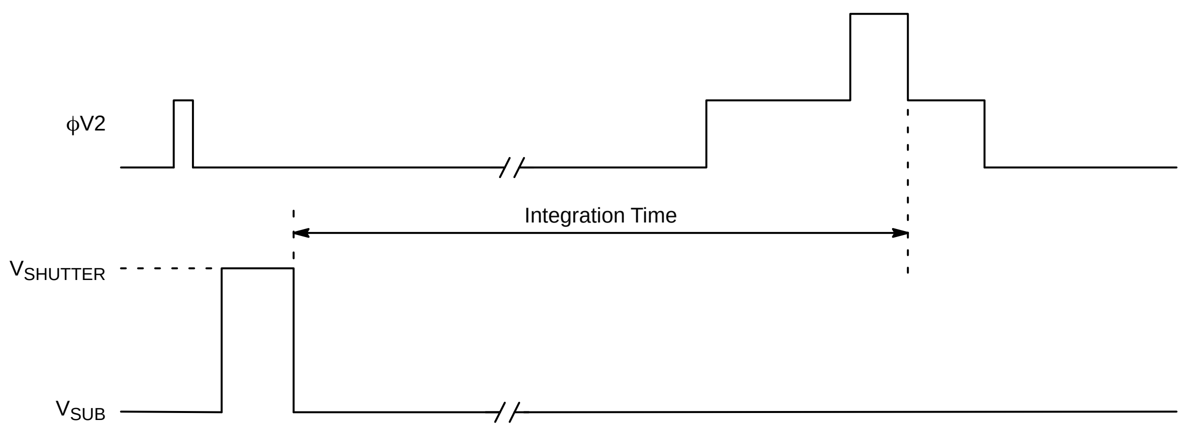

Figure 17. Integration Time Definition

REFERENCES

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on environmental exposure, please download the *Using Interline CCD Image Sensors in High Intensity Lighting Conditions* Application Note (AND9183/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL DRAWINGS

Completed Assembly

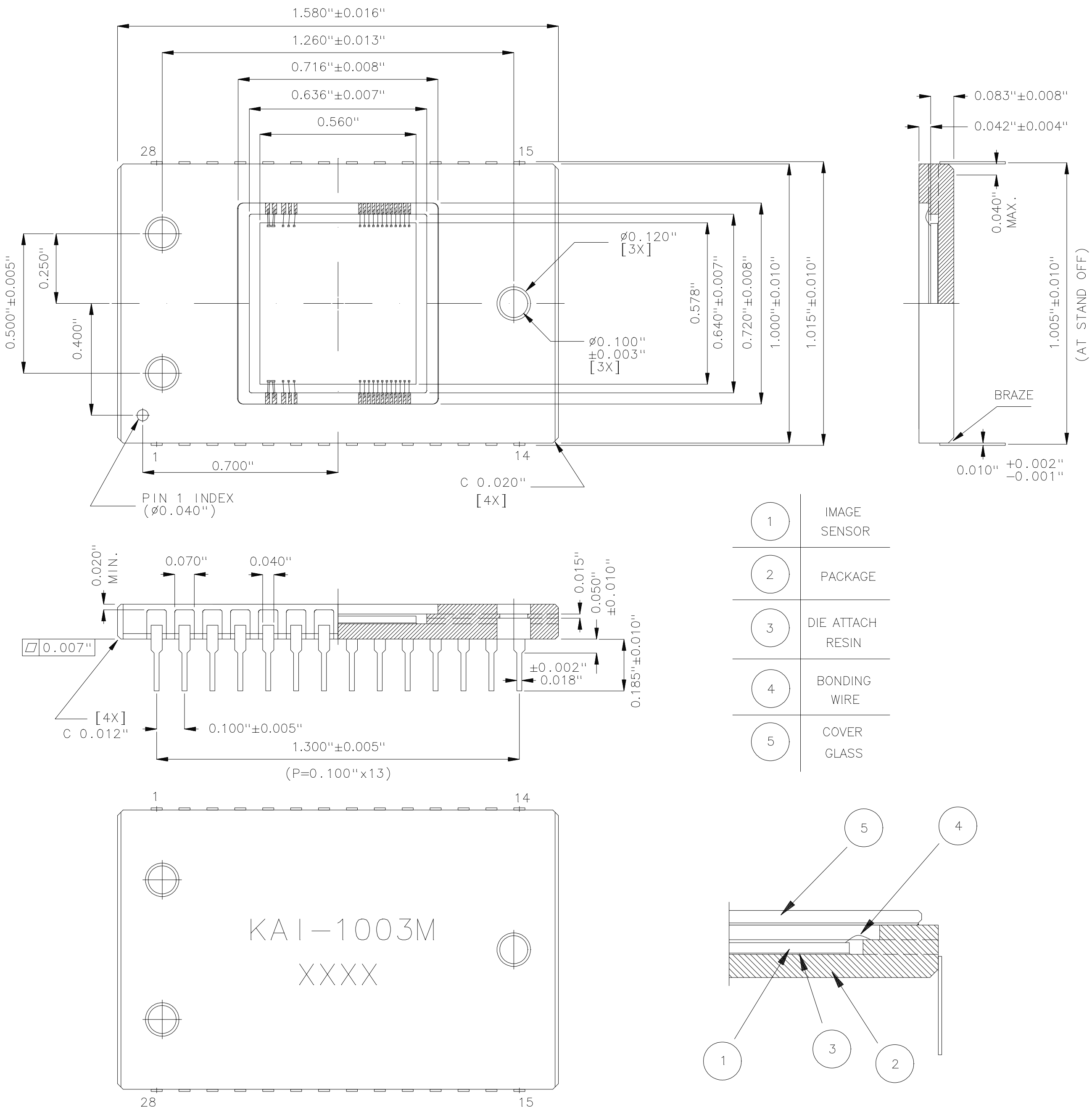

Figure 18. Completed Assembly

Cover Glass Specification

Table 14. COVER GLASS SPECIFICATION

Item	Specification
Substrate	Schott D263T eco or equivalent
Thickness	0.030″ ± 0.002″
Coating	Double-sided anti-reflecting coating on a 0.660″ × 0.660″ square for a transmission minimum of 98% in the 400 to 700 nm wavelength
Scratch	No scratch greater than 10 microns

Cover Glass Care and Cleanliness:

1. The cover glass is highly susceptible to particles and other contamination. Perform all assembly operations in a clean environment.
2. Touching the cover glass must be avoided
3. Improper cleaning of the cover glass may damage these devices. Improper cleaning of the cover glass may damage these devices. Refer to Application Note *Image senosr Handling and Best Practices.*

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative