STK57FU394A-E

PFC Converter + Inverter IPM for 3-phase Motor Drive

ON Semiconductor®

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This IPM (Intelligent Power Module) includes the PFC, the output stage of a 3-phase inverter, pre-drive circuits, as well as protection circuits in one package.

Features

- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit
- All control input and status outputs are at low voltage levels directly compatible with microcontrollers
- Built-in cross conduction prevention
- Under-voltage lockout for all channels
- Protective terminals including for over current protection each of Inverter section and PFC section are built in.
- Externally accessible embedded thermistor for substrate temperature measurement

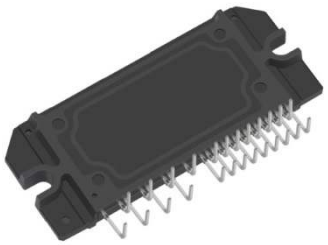
Certification

- UL1557 (File Number : E339285)

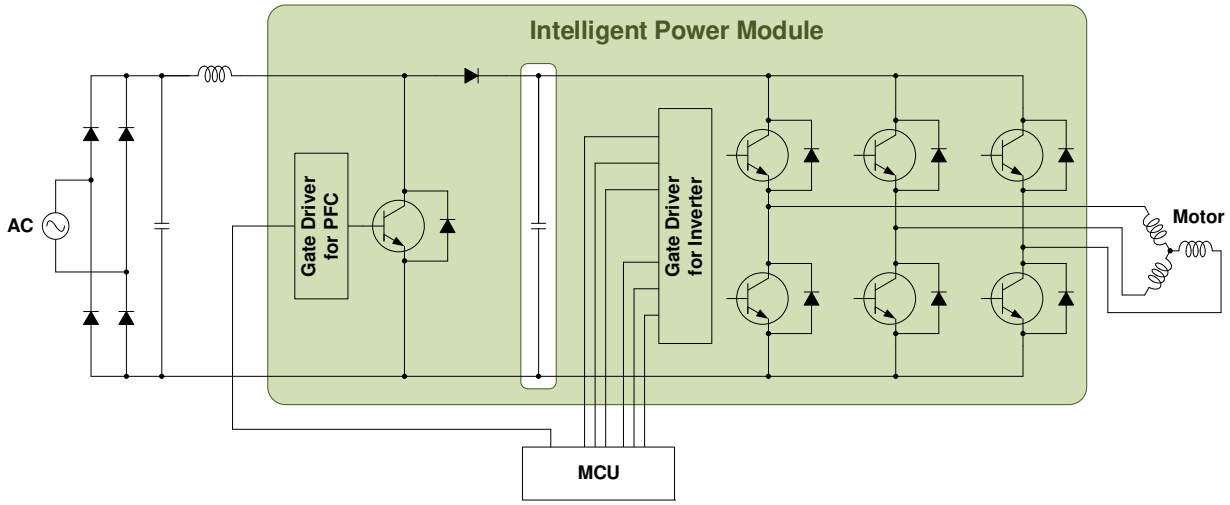
Typical Applications

- Motor Control System
- Industrial/ General Control System
- HVAC

PACKAGE PICTURE



SIP35 56x25.8 / SIP2A



ORDERING INFORMATION

See detailed ordering and shipping information on page 15 of this data sheet.

BLOCK DIAGRAM

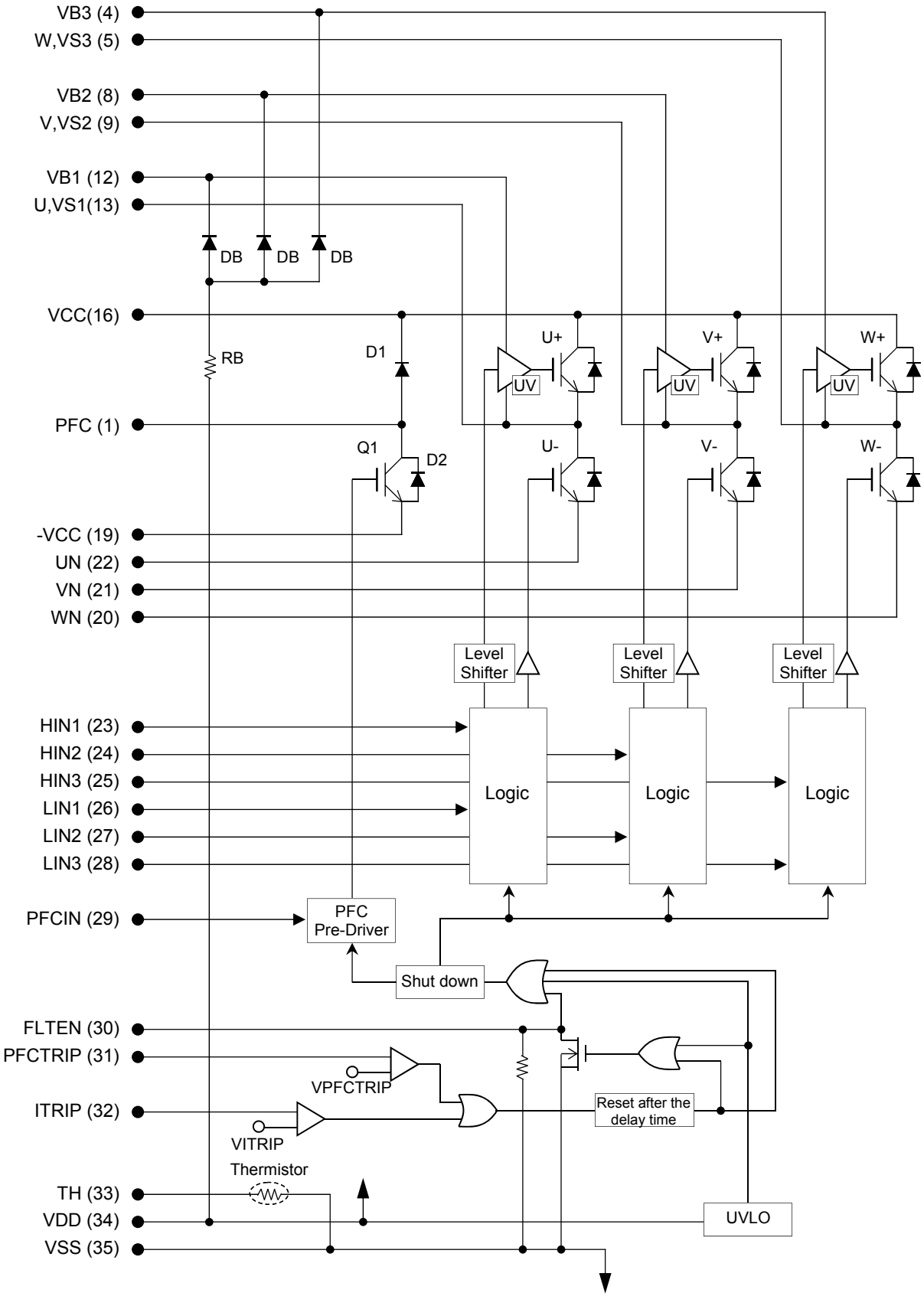


Figure 1. STK57FU394A-E Block diagram

APPLICATION CIRCUIT EXAMPLES

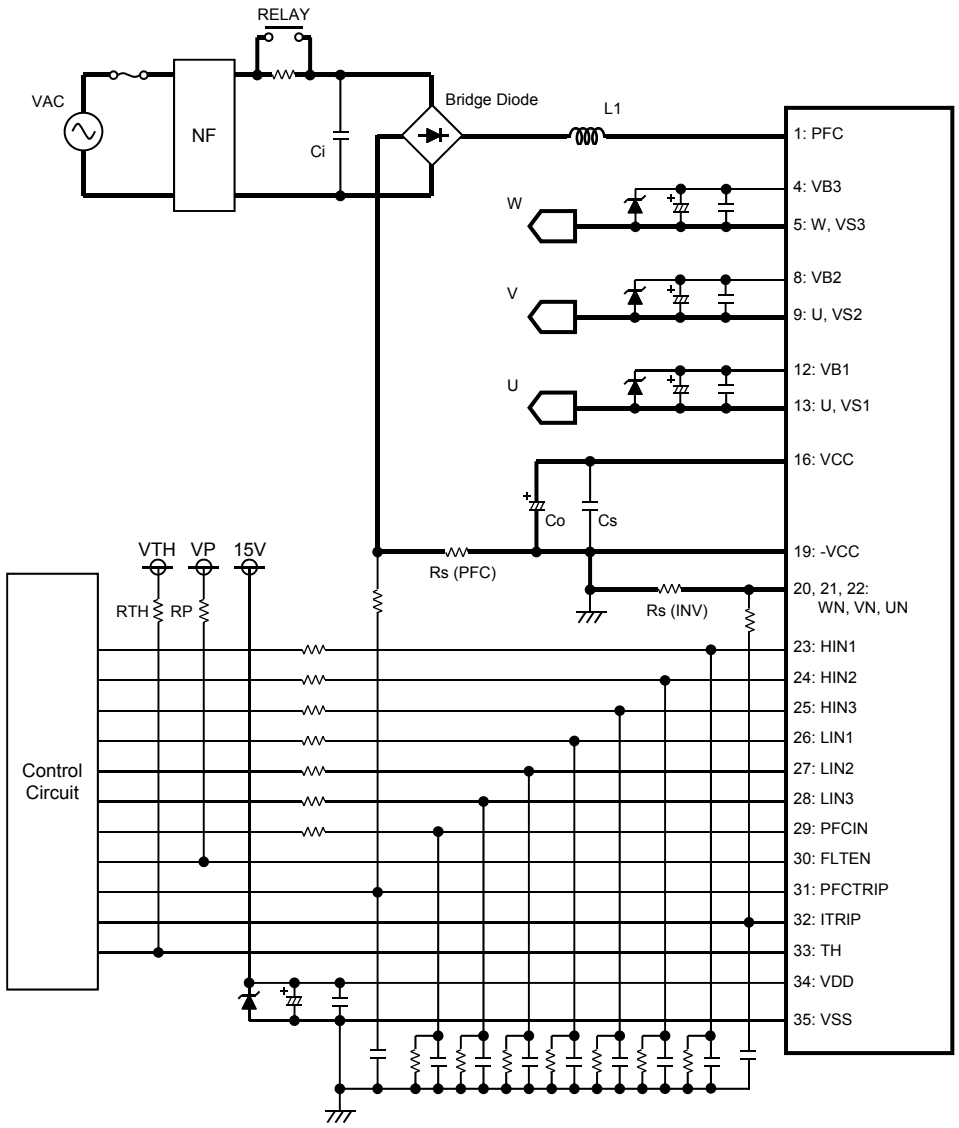


Figure 2. Motor drive application using STK57FU394A-E

PIN FUNCTION DISCRIPTION

Pin	Name	Description
1	PFC	Input the Rectified AC Voltage
2	-	Without pin
3	-	Without pin
4	VB3	High Side Floating Supply Voltage 3
5	W,VS3	Output 3 – High Side Floating Supply Offset Voltage
6	-	Without pin
7	-	Without pin
8	VB2	High Side Floating Supply Voltage 2
9	V,VS2	Output 2 – High Side Floating Supply Offset Voltage
10	-	Without pin
11	-	Without pin
12	VB1	High Side Floating Supply Voltage 1
13	U,VS1	Output 1 – High Side Floating Supply Offset Voltage
14	-	Without pin
15	-	Without pin
16	VCC	Positive PFC Output voltage / Positive Bus Input Voltage
17	-	Without pin
18	-	Without pin
19	-VCC	Negative PFC Output Voltage
20	WN	Low Side Emitter Connection – Phase W
21	VN	Low Side Emitter Connection – Phase V
22	UN	Low Side Emitter Connection – Phase U
23	HIN1	Logic Input High Side Gate Driver – Phase U
24	HIN2	Logic Input High Side Gate Driver – Phase V
25	HIN3	Logic Input High Side Gate Driver – Phase W
26	LIN1	Logic Input Low Side Gate Driver – Phase U
27	LIN2	Logic Input Low Side Gate Driver – Phase V
28	LIN3	Logic Input Low Side Gate Driver – Phase W
29	PFCIN	Logic Input PFC Gate Driver
30	FLTEN	Enable input / Fault output
31	PFCTRIP	Current protection pin for PFC
32	ITRIP	Current protection pin for Inverter
33	TH	Thermistor output
34	VDD	+15V Main Supply
35	VSS	Negative Main Supply

MAXIMUM RATINGS (Note *1)

(1) PFC Section

Parameter		Symbol	Conditions	Ratings	Unit
IGBT (Q1)	Collector-emitter voltage	V_{CE}	PFC to $-V_{CC}$	600	V
	Repetitive peak collector current	ICP	P.W.=1ms	40	A
	Collector current	IC	Tc=25°C	27	A
			Tc=100°C	13	A
	Power dissipation	PC		62	W
FRD1 (D1)	Diode reverse voltage	VR	PFC to V_{CC}	600	V
	Repetitive peak forward current	IFP1	P.W.=1ms	60	A
	Diode forward current	IF1		30	A
	Power dissipation	PD1		56	W
FRD2 (D2)	Repetitive peak forward current	IFP2	P.W.=1ms	11	A
	Diode forward current	IF2		5	A
	Power dissipation	PD2		10	W
Maximum AC input voltage		VAC	Single-phase Full-rectified	264	V
Maximum output voltage		Vo	Under the Application Circuit (VAC=200V)	450	V
Input AC current (steady state)		Iin		15	Arms

(2) Inverter Section

Parameter	Symbol	Remarks	Ratings	Unit
Supply voltage	V_{CC}	V_{CC} to UN, VN, WN surge < 500V (*2)	450	V
Collector-emitter voltage	V_{CE}	V_{CC} to U, V, W or U, V, W to UN, VN, WN	600	V
Output current	Io	V_{CC}, UN, VN, WN, U, V, W terminal current	±15	A
		V_{CC}, UN, VN, WN, U, V, W terminal current at Tc=100°C	±8	A
Output peak current	Iop	V_{CC}, UN, VN, WN, U, V, W terminal current for a Pulse width of 1ms	±30	A
Maximum loss	Pd	IGBT per channel	37	W

(3) Control (Pre-driver) Section

Parameter	Symbol	Remarks	Ratings	Unit
Pre-driver supply voltage	VD1,2,3,4	VB1−VS1, VB2−VS2, VB3−VS3, $V_{DD}-V_{SS}$	−0.3 to 20	V
Input signal voltage	V_{IN}	HIN1, 2, 3, LIN1, 2, 3, PFCIN terminal	−0.3 to V_{DD}	V
FLTEN terminal voltage	VFLTEN	FLTEN terminal	−0.3 to V_{DD}	V
ITRIP terminal voltage	VITRIP	ITRIP terminal	−0.3 to 10	V
PFCTRIP terminal voltage	VPFCTRIP	PFCTRIP terminal	−1.5 to 2.0	V

(4) Total

Parameter	Symbol	Remarks	Ratings	Unit
Junction temperature	Tj	IGBT, FRD	150	°C
Storage temperature	Tstg		−40 to +125	°C
Operating Case temperature	Tc	IPM case temperature	−20 to +100	°C
Tightening torque	MT	Case mounting screws (*3)	0.9	N·m
Withstand voltage	Vis	50Hz sine wave AC 1 minute (*4)	2000	Vrms

***1.** Stresses exceeding those listed in the Absolute Maximum Rating table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
***2.** Surge voltage developed by the switching operation due to the wiring inductance between VCC and UN(VN, WN) terminal.
***3.** Flatness of the heat-sink should be less than 0.15mm.
***4.** Test conditions : AC2500V, 1s.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
PFC IGBT(Q1) Thermal Resistance, Junction-to-Case	θj-c(T)	2.3	°C/W
PFC FRD(D1) Thermal Resistance, Junction-to-Case	θj-c(D)	2.5	°C/W
Inverter Single IGBT Thermal Resistance, Junction-to-Case	θj-c(T)	3.5	°C/W
Inverter Single FRD Thermal Resistance, Junction-to-Case	θj-c(D)	6.0	°C/W

RECOMMENDED OPERATING RANGES (Note *5)

Parameter	Symbol	Conditions	min	typ	max	Unit
Supply voltage	V_{CC}	V_{CC} to $-V_{CC}$, UN, VN, WN	0	280	400	V
Pre-driver supply voltage	VD1,2,3	VB1 to U,VB2 to V,VB3 to W	12.5	15	17.5	V
	VD4	V_{DD} to V_{SS} (*6)	13.5	15	16.5	
ON-state input voltage	V_{IN}(ON)	HIN1,HIN2,HIN3,LIN1,LIN2,LIN3, PFCIN	2.5	-	5.0	V
OFF-state input voltage	V_{IN}(OFF)		0	-	0.3	
PWM frequency (PFC part)	fPWMp		1	-	40	kHz
PWM frequency (Inverter part)	fPWMi		1	-	20	kHz
Dead time	DT	Upper/lower input signal downtime	1.5	-	-	μs
Allowable input pulse width	PWIN	ON and OFF	1	-	-	μs
Tightening torque	MT	'M3' type screw	0.6	-	0.9	N·m

***5.** Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

***6.** Pre-driver power supply (VD4=15±1.5V) must have the capacity of Io=20mA(DC), 0.5A(Peak).

ELECTRICAL CHARACTERISTICS

Tc=25°C, VB1, VB2, VB3, VDD=15V unless otherwise noted. (Notes *7, *8)

(1) PFC Section

Parameter	Symbol	Conditions	min	typ	max	Unit
Power output section						
Collector-emitter cut-off current	I_{CE}	V_{CE}=600V	-	-	0.1	mA
Reverse leakage current(FRD1)	IR	VR=600V	-	-	0.1	mA
Collector-emitter saturation voltage	VCE(sat)	IC=30A, Tj=25°C	-	2.2	2.8	V
		IC=15A, Tj=100°C	-	1.8	-	
Diode forward voltage(FRD1)	VF1	IF=30A, Tj=25°C	-	1.8	2.4	V
		IF=15A, Tj=100°C	-	1.3	-	
Diode forward voltage(FRD2)	VF2	IF=5A, Tj=25°C	-	1.7	2.3	V
Switching characteristics						
Switching time	tON	Io=30A, V_{CC}=300V VD=15V,L=0.5mH, Tc=25°C	0.1	0.4	0.9	μs
	tOFF		0.1	0.4	0.9	μs
Diode reverse recovery time	trr	Io=15A, V_{CC}=300V VD=15V, Tc=100°C	-	80	-	ns

(2) Inverter Section

Parameter	Symbol	Conditions	min	typ	max	Unit
Power output section						
Collector-emitter cut-off current	I_{CE}	V_{CE}=600V	-	-	0.1	mA
Bootstrap diode reverse current	IR(DB)	VR(DB)=600V	-	-	0.1	mA
Collector-emitter saturation voltage	V_{CE}(sat)	IC=15A, Tj=25°C	-	2.0	2.6	V
		IC=8A, Tj=100°C	-	1.7	-	
Diode forward voltage	VF	IF=15A, Tj=25°C	-	2.1	2.7	V
		IF=8A, Tj=100°C	-	1.7	-	
Switching characteristics						
Switching time	tON	Io=15A Inductive load	0.1	0.5	1.0	μs
	tOFF		0.2	0.7	1.2	μs
Reverse bias safe operating area	RBSOA	Io=30A, VCE=450V	Full square			
Short circuit safe operating area	SCSOA	V_{CE}=400V	4	-	-	μs
Allowable offset voltage slew rate	dv/dt	Between U,V,W to UN, VN, WN	−50	-	50	V/ns

(3) Control (Pre-driver) Section

Parameter	Symbol	Conditions	min	typ	max	Unit
Pre-driver current consumption	ID	VD1, 2, 3=15V	-	0.08	0.4	mA
		VD4=15V	-	0.85	2.4	
High level input voltage	$V_{IN\ H}$	HIN1, 2, 3, LIN1, 2, 3, PFCIN to VSS	2.5	-	-	V
Low level input voltage	$V_{IN\ L}$		-	-	0.8	V
Logic1 input leakage current	I_{IN+}	V_{IN}=+3.3V	-	100	143	μA
Logic0 input leakage current	I_{IN-}	V_{IN}=0V	-	-	2	μA
FLTEN terminal input electric current	IoSD	FAULT:ON / VFLTEN=0.1V	-	2	-	mA
FAULT clearance delay time	FLTCLR	Fault output latch time	1	2	3	ms
FLTEN threshold	V_{EN+}	VEN rising	-	-	2.5	V
	V_{EN-}	VEN falling	0.8	-	-	V
ITRIP threshold voltage	V_{ITRIP}	ITRIP to V_{SS}	0.44	-	0.54	V
PFCTRIP threshold voltage	$V_{PFCTRIP}$	PFCTRIP to V_{SS}	−0.37	-	−0.25	V
ITRIP to shutdown propagation delay	t_{ITRIP}		490	600	850	ns
PFCTRIP to shutdown propagation delay	$t_{PFCTRIP}$		440	550	800	ns
ITRIP and PFCTRIP blanking time	$t_{ITRIPBL}$ $t_{PFCTRIPBL}$		250	350	-	ns
VDD and VBS supply undervoltage protection reset	V_{DDUV+} V_{BSUV+}		10.5	11.1	11.7	V
VDD and VBS supply undervoltage protection set	V_{DDUV-} V_{BSUV-}		10.3	10.9	11.5	V
VDD and VBS supply undervoltage hysteresis	V_{CCUVH} V_{BSUVH}		0.14	0.2	-	V

***7.** Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

***8.** Reference voltage is “VSS” terminal voltage unless otherwise specified.

Notes

1. The pre-drive power supply low voltage protection has approximately 200mV of hysteresis and operates as follows.
   - Upper side : The gate is turned off and will return to regular operation when recovering to the normal voltage, but the latch will continue till the input signal will turn ‘low’.
   - Lower side : The gate is turned off and will automatically reset when recovering to normal voltage. It does not depend on input signal voltage.
2. When assembling the IPM on the heat sink the tightening torque range is 0.6Nm to 0.9Nm.
3. The pre-drive low voltage protection protects the device when the pre-drive supply voltage falls due to an operating malfunction.
4. When use the over-current protection with external shunt resistor, please set the current protection level to be equal to or less than the rating of output peak current.

The characteristic of Thermistor

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	R_{25}	Tc=25°C	99	100	101	kΩ
Resistance	R_{100}	Tc=100°C	5.18	5.38	5.60	kΩ
B-Constant(25-50°C)	B		4208	4250	4293	K
Temperature Range			−40		+125	°C

TYPICAL CHARACTERISTICS

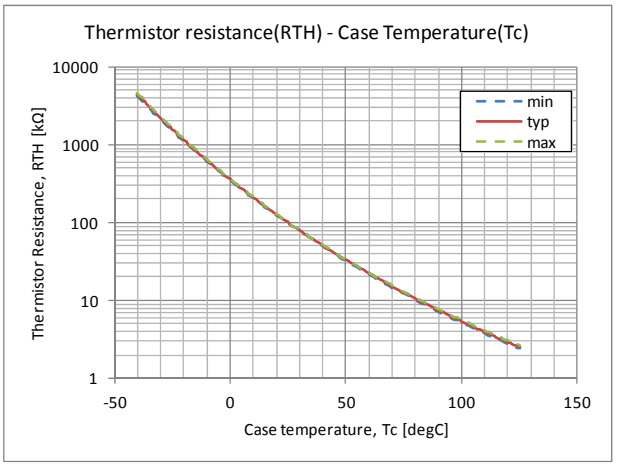


Figure 3. Thermistor resistance – Case temperature

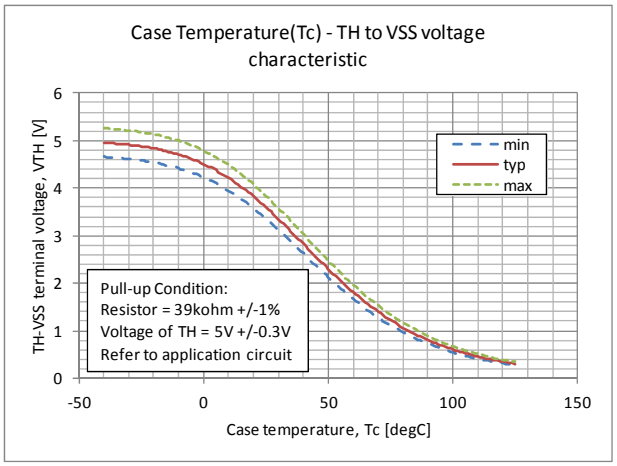


Figure 4. Thermistor voltage – Case temperature (Reference)

Timing Chart

■ UVLO(under Voltage Lockout) protection

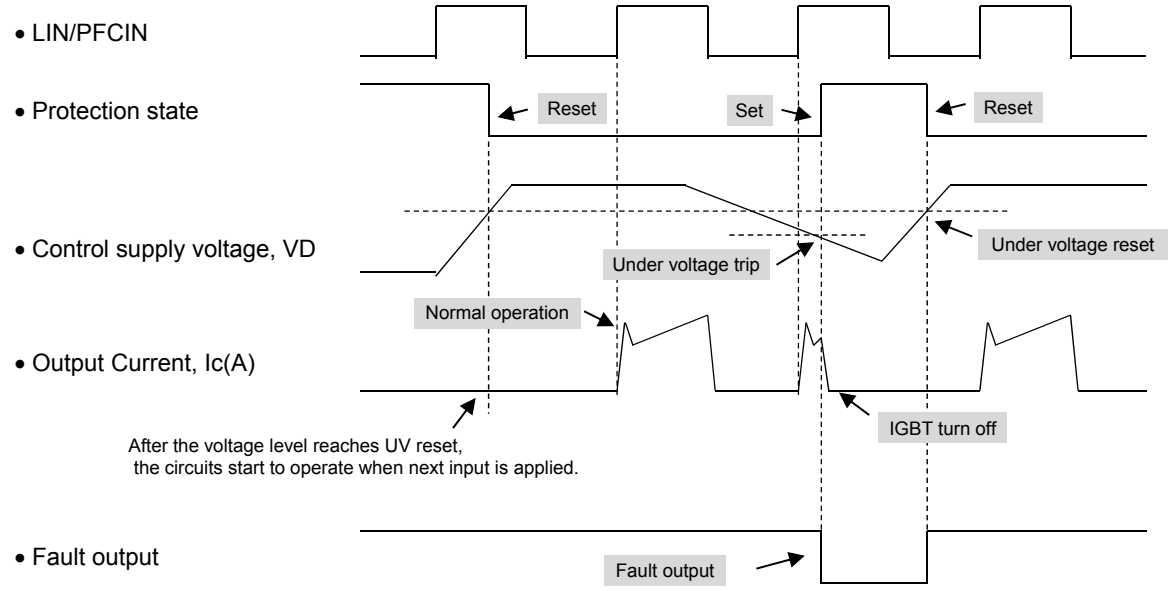


Figure 5. UVLO timing diagram

1. When V_{DD} decreases all gate output signals will go low and cut off all 6 IGBT outputs. When V_{DD} rises the operation will resume immediately.
2. When the upper side voltage at VB1, VB2 and VB3 drops only the corresponding upper side output is turned off. The outputs return to normal operation immediately after the upper side gate voltage rises.

■ Over current protection (ITRIP/PFCTRIP)

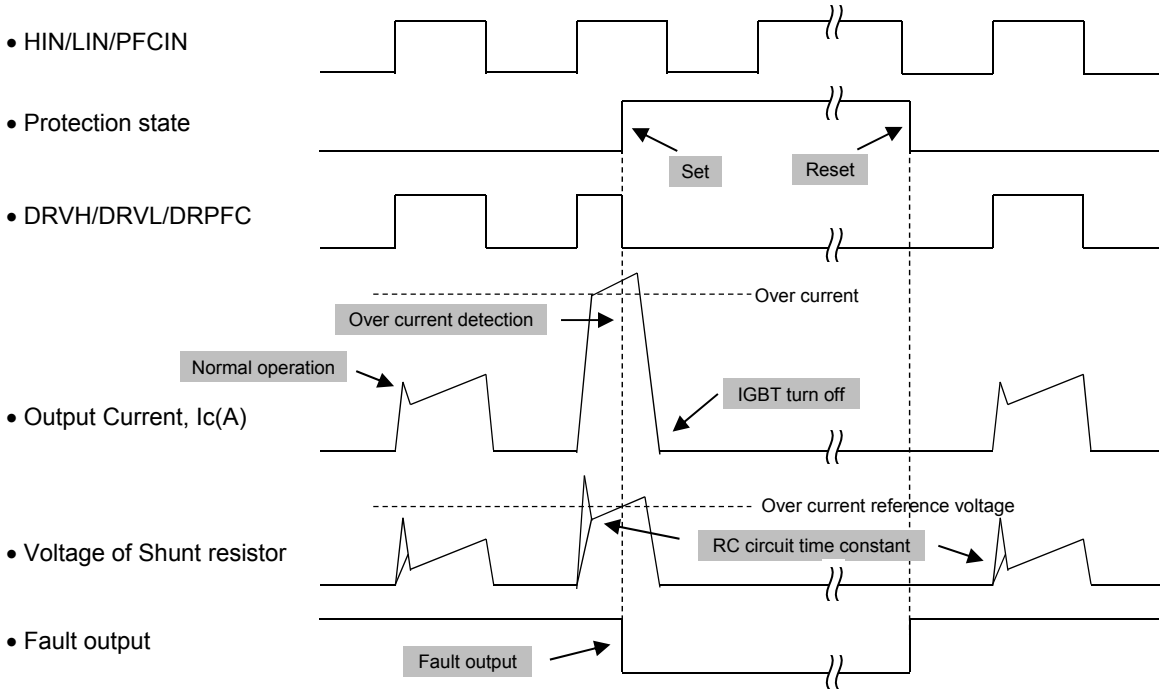


Figure 6. OCP timing diagram

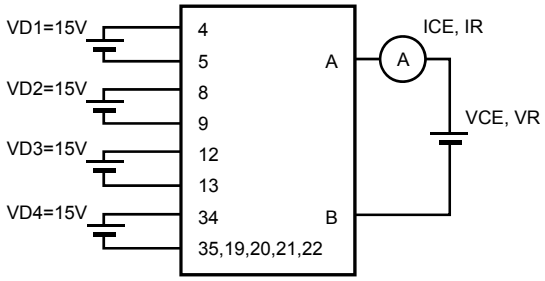
1. When VITRIP exceeds threshold all IGBT's are turned off and normal operation resumes 2ms (typ) after over current condition is removed.

Test Circuit

■ ICES, IR(DB)

	U+	V+	W+	U-	V-	W-	Q1
A	16	16	16	13	9	5	1
B	13	9	5	22	21	20	19

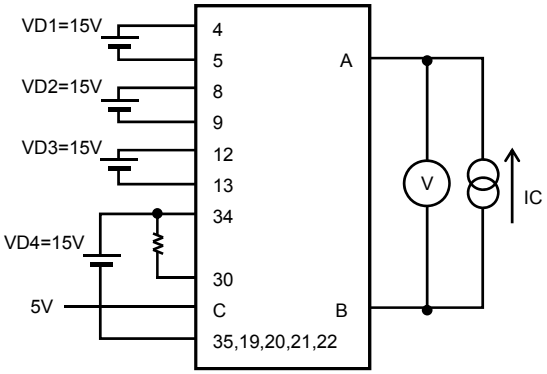
	U(DB)	V(DB)	W(DB)	D1
A	12	8	4	16
B	35	35	35	1



< Figure 7. Test circuit for ICES, IR>

■ V_{CE}(sat) (Test by pulse)

	U+	V+	W+	U-	V-	W-	Q1
A	16	16	16	13	9	5	1
B	13	9	5	22	21	20	19
C	23	24	25	26	27	28	29

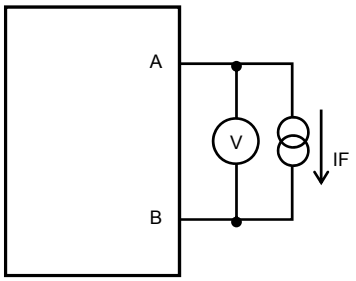


< Figure 8. Test circuit for VCE(sat)>

■ VF (Test by pulse)

	U+	V+	W+	U-	V-	W-
A	16	16	16	13	9	5
B	13	9	5	22	21	20

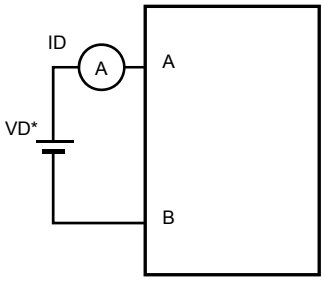
	U(DB)	V(DB)	W(DB)	D1	D2
A	12	8	4	16	1
B	34	34	34	1	19



< Figure 9. Test circuit for VF>

■ ID

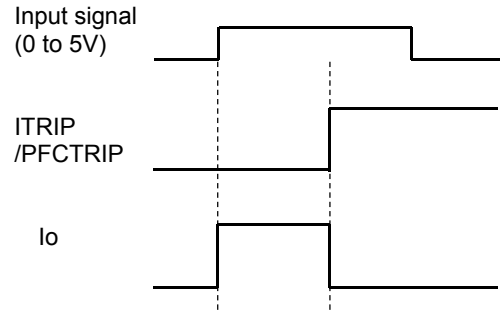
	VD1	VD2	VD3	VD4
A	12	8	4	34
B	13	9	5	35

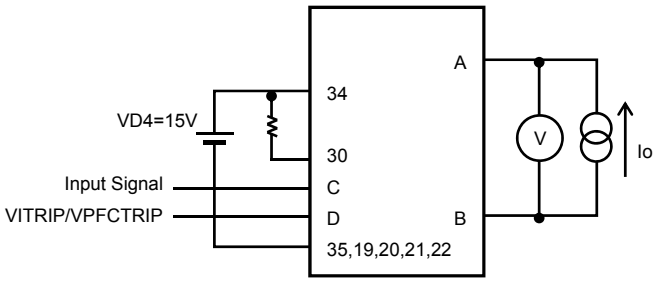


< Figure 10. Test circuit for ID>

■ VITRIP, VPFCTRIP

	VITRIP(U-)	VPFCTRIP
A	13	1
B	22	19
C	26	29
D	32	31

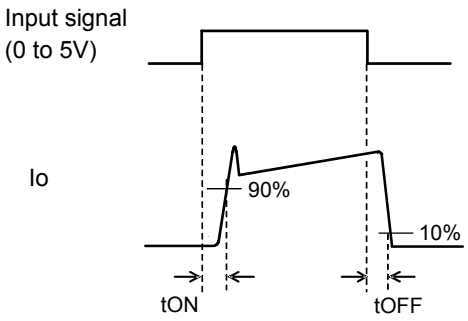


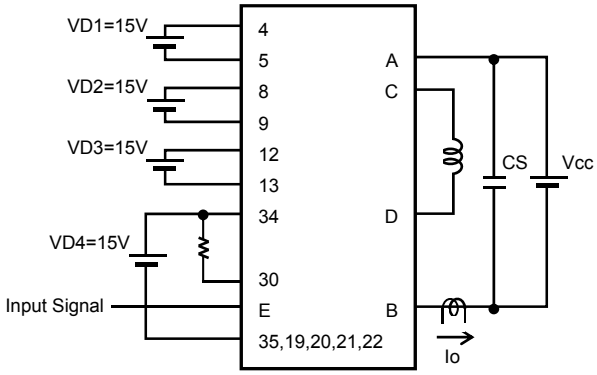


< Figure 11. Test circuit for VITRIP, VPFCTRIP>

■ Switching time

	U+	V+	W+	U-	V-	W-	Q1
A	16	16	16	16	16	16	16
B	22	21	20	22	21	20	19
C	13	9	5	13	9	5	1
D	22	21	20	16	16	16	16
E	23	24	25	26	27	28	29





< Figure 12. Test circuit for Switching time>

Usage Precaution

1. This IPM includes internal bootstrap circuit. By adding a bootstrap capacitor “CB”, a high side drive voltage is generated; each phase requires an individual bootstrap capacitor. The recommended value of CB is in the range of 1 to 47μF, however, this value needs to be verified prior to production. When not using the bootstrap circuit, each high side pre-drive power supply requires an external independent power supply.

2. It is essential that wirning length between terminals in the snubber circuit be kept as short as possible to reduce the effect of surge voltages. Recommended value of “CS” is in the range of 0.1 to 10μF.

3. The “FLTEN” terminal is open Drain (It is operating as “FLTEN” when becoming Low). This terminal serves as the shut down function of the built-in pre-driver (When the terminal voltage is above 2.5V, normalcy works, and it is shut down when it is equal to or less than 0.8V). Please make pulling up outside so that “FLTEN” terminal voltages become more than 2.5V. When the pull up voltage (VP) is at 5V, pull up resistor (RP) connects above 6.8kΩ, and in case of VP=15V, RP connects above 20kΩ.

4. Inside the IPM, a thermistor used as the temperature monitor for internal substrate is connected between TH terminal and V_{SS} terminal, therefore, an external pull up resistor connected between the TH terminal and an external power supply should be used.

5. The pull-down resistor (:33kΩ(typ)) is connected with the inside of the signal input terminal, but please connect the pull-down resistor(about 2.2 to 3.3kΩ) outside to decrease the influence of the noise by wiring etc.

6. As protection of IPM to the unusual current by a short circuit etc, it recommends installing shunt resistors and an over-current protection circuit outside. Moreover, for safety, installation of a fuse in V_{CC} line, etc. is recommended.

7. Disconnection of terminals U, V, or W during normal motor operation will cause damage to IPM, use caution with this connection.

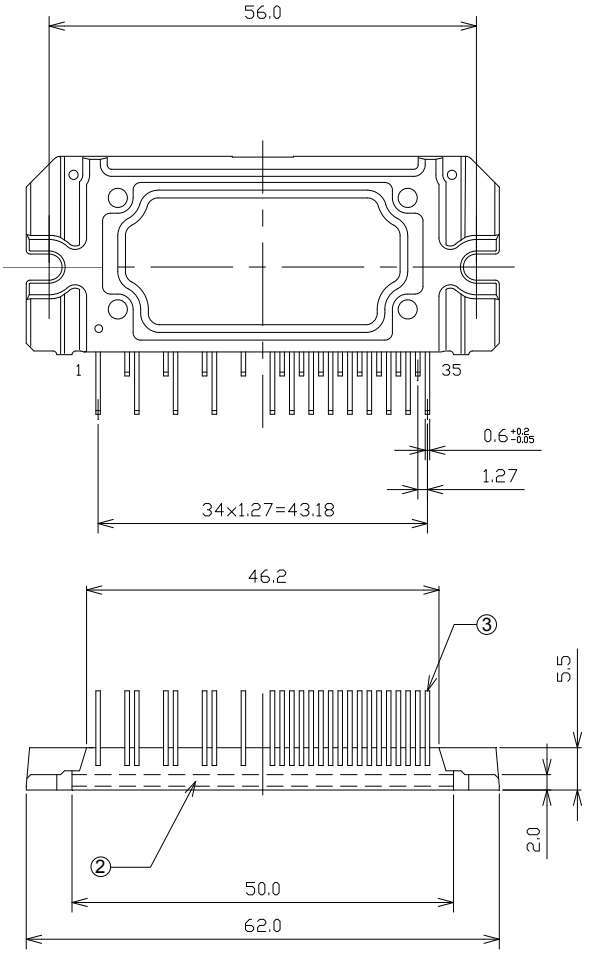
8. The “ITRIP” terminal and the “PFCTRIP” terminal are the input terminal of the built-in comparator. It can stop movement by inputting the voltage more than reference voltage. (At the time of movement, usually those terminals give it for the voltage less than reference voltage). Please use it as various protections such as the over-current protection (feedback from external shunt resistance). In addition, the protection movement is not done a latch of. After the protection movement end, It becomes the movement return state after 2ms (typ.). So, please do the protection movement detection of all input signals in OFF (LOW) promptly afterward.

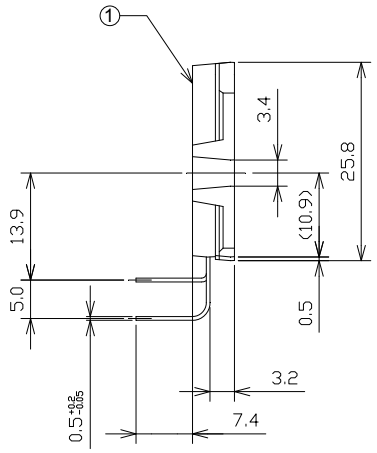
9. When input pulse width is less than 1μs, an output may not react to the pulse. (Both ON signal and OFF signal)

PACKAGE DIMENSIONS
unit : mm

The tolerances of length are +/– 0.5mm unless otherwise specified.

Missing Pin : 2, 3, 6, 7, 10, 11, 14, 15, 17, 18





note1 : Mark of No.1 pin identification.
note2 : The form of a character in this drawing differs from that of IPM.
note3 : This indicates the Lot code.
The form of a character in this drawing differs from that of IPM.

No.	Part Name	Material	Treatment
①	Case	EPOXY	-
②	Substrate	IMST Substrate	-
③	Lead Frame	Cu	Sn

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK57FU394A-E	SIP35 56x25.8 / SIP2A (Pb-Free)	8 / Tube