# CY74FCT2543T
## 8-BIT LATCHED TRANSCEIVER
## WITH 3-STATE OUTPUTS

- **Function and Pinout Compatible With FCT and F Logic**
- **25-$\Omega$ Output Series Resistors to Reduce Transmission-Line Reflection Noise**
- **Reduced $V_{OH}$ (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **$I_{off}$ Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **12-mA Output Sink Current 15-mA Output Source Current**
- **Separation Controls for Data Flow in Each Direction**
- **Back-to-Back Latches for Storage**
- **ESD Protection Exceeds JESD 22**
    - **2000-V Human-Body Model (A114-A)**
    - **200-V Machine Model (A115-A)**
    - **1000-V Charged-Device Model (C101)**
- **3-State Outputs**

**Q OR SO PACKAGE**
**(TOP VIEW)**

| | | | |
|---|---|---|---|
| $\overline{LEBA}$ | 1 | 24 | $V_{CC}$ |
| $\overline{OEBA}$ | 2 | 23 | $\overline{CEBA}$ |
| $A_0$ | 3 | 22 | $B_0$ |
| $A_1$ | 4 | 21 | $B_1$ |
| $A_2$ | 5 | 20 | $B_2$ |
| $A_3$ | 6 | 19 | $B_3$ |
| $A_4$ | 7 | 18 | $B_4$ |
| $A_5$ | 8 | 17 | $B_5$ |
| $A_6$ | 9 | 16 | $B_6$ |
| $A_7$ | 10 | 15 | $B_7$ |
| $\overline{CEAB}$ | 11 | 14 | $\overline{LEAB}$ |
| GND | 12 | 13 | $\overline{OEAB}$ |
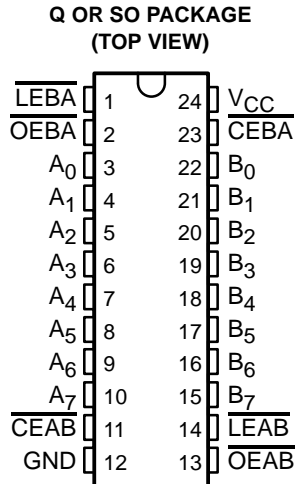
## description

The CY74FCT2543T octal latched transceiver contains two sets of eight D-type latches. Separate latch enable ($\overline{LEAB}$, $\overline{LEBA}$) and output enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs permit each latch set to have independent control of inputting and outputting in either direction of data flow. For example, for data flow from A to B, the A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to take data from B, as indicated in the function table. With $\overline{CEAB}$ low, a low signal on the A-to-B latch enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B output buffers are active and reflect data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs. On-chip termination resistors at the outputs reduce system noise caused by reflections. The CY74FCT2543T can replace the CY74FCT543T to reduce noise in an existing design.

This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

# CY74FCT2543T
## 8-BIT LATCHED TRANSCEIVER
## WITH 3-STATE OUTPUTS

**PIN DESCRIPTION**

| NAME | DESCRIPTION |
|------|-------------|
| $\overline{\text{OEAB}}$ | A-to-B output-enable input (active low) |
| $\overline{\text{OEBA}}$ | B-to-A output-enable input (active low) |
| $\overline{\text{CEAB}}$ | A-to-B enable input (active low) |
| $\overline{\text{CEBA}}$ | B-to-A enable input (active low) |
| $\overline{\text{LEAB}}$ | A-to-B latch-enable input (active low) |
| $\overline{\text{LEBA}}$ | B-to-A latch-enable input (active low) |
| A | A-to-B data inputs or B-to-A 3-state outputs |
| B | B-to-A data inputs or A-to-B 3-state outputs |

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | SPEED (ns) | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|-------|----------|--|------------|-----------------------|------------------|
| −40°C to 85°C | QSOP – Q | Tape and reel | 5.3 | CY74FCT2543CTQCT | FCT2543C |
| | SOIC – SO | Tube | 5.3 | CY74FCT2543CTSOC | FCT2543C |
| | | Tape and reel | 5.3 | CY74FCT2543CTSOCT | |
| | QSOP – Q | Tape and reel | 6.5 | CY74FCT2543ATQCT | FCT2543A |
| | SOIC – SO | Tube | 6.5 | CY74FCT2543ATSOC | FCT2543A |
| | | Tape and reel | 6.5 | CY74FCT2543ATSOCT | |
| | QSOP – Q | Tape and reel | 8.5 | CY74FCT2543TQCT | FCT2543 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

**FUNCTION TABLE**

| INPUTS | | | LATCH A-TO-B‡ | OUTPUT B |
|--------|--|--|----------------|----------|
| $\overline{\text{CEAB}}$ | $\overline{\text{LEAB}}$ | $\overline{\text{OEAB}}$ | | |
| H | X | X | Storing | Z |
| X | H | X | Storing | X |
| X | X | H | X | Z |
| L | L | L | Transparent | Current A inputs |
| L | H | L | Storing | Previous A inputs |

‡ Before $\overline{\text{LEAB}}$ low-to-high transition
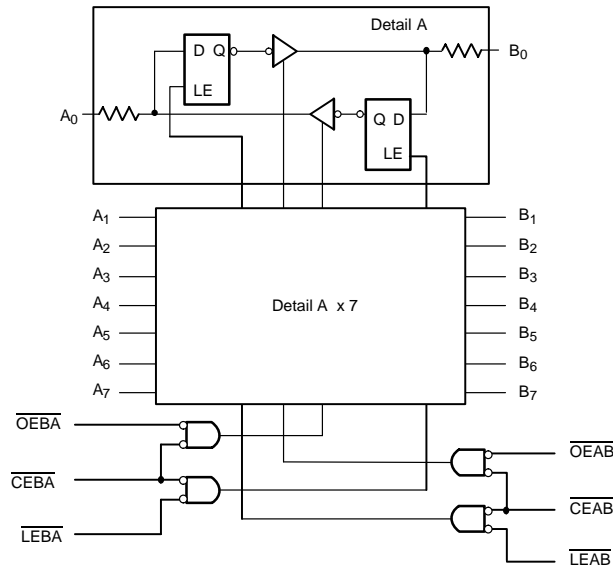H = High logic level, L = Low logic level, X = Don't care,
Z = High-impedance state
A-to-B data flow shown; B-to-A is the same, except using $\overline{\text{CEBA}}$, $\overline{\text{LEBA}}$, and $\overline{\text{OEBA}}$.

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## functional block diagram



## absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

| | |
|---|---|
| Supply voltage range to ground potential | −0.5 V to 7 V |
| DC input voltage range | −0.5 V to 7 V |
| DC output voltage range | −0.5 V to 7 V |
| DC output current (maximum sink current/pin) | 120 mA |
| Package thermal impedance, $\theta_{JA}$ (see Note 1): Q package | 61°C/W |
| SO package | 46°C/W |
| Ambient temperature range with power applied, $T_A$ | −65°C to 135°C |
| Storage temperature range, $T_{stg}$ | −65°C to 150°C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 2)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −15 | mA |
| $I_{OL}$ | Low-level output current | | | 12 | mA |
| $T_A$ | Operating free-air temperature | −40 | | 85 | °C |

NOTE 2: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation.

# CY74FCT2543T
## 8-BIT LATCHED TRANSCEIVER
## WITH 3-STATE OUTPUTS
SCCS042C – SEPTEMBER 1994 – REVISED NOVEMBER 2001

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | | MIN | TYP[†] | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = 4.75 V, | $I_{IN}$ = −18 mA | | | −0.7 | −1.2 | V |
| $V_{OH}$ | $V_{CC}$ = 4.75 V, | $I_{OH}$ = −15 mA | | 2.4 | 3.3 | | V |
| $V_{OL}$ | $V_{CC}$ = 4.75 V, | $I_{OL}$ = 12 mA | | | 0.3 | 0.55 | V |
| $R_{out}$ | $V_{CC}$ = 4.75 V, | $I_{OL}$ = 12 mA | | 20 | 25 | 40 | Ω |
| $V_{hys}$ | All inputs | | | | 0.2 | | V |
| $I_{IH}$ | $V_{CC}$ = 5.25 V | $V_{IN} = V_{CC}$ | | | | 5 | μA |
| | | $V_{IN}$ = 2.7 V | | | | ±1 | |
| $I_{IL}$ | $V_{CC}$ = 5.25 V, | $V_{IN}$ = 0.5 V | | | | ±1 | μA |
| $I_{OZH}$ | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 2.7 V | | | | 15 | μA |
| $I_{OZL}$ | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 0.5 V | | | | −15 | μA |
| $I_{OS}$[‡] | $V_{CC}$ = 5.25 V, | $V_{OUT}$ = 0 V | | −60 | −120 | −225 | mA |
| $I_{off}$ | $V_{CC}$ = 0 V, | $V_{OUT}$ = 4.5 V | | | | ±1 | μA |
| $I_{CC}$ | $V_{CC}$ = 5.25 V, | $V_{IN}$ ≤ 0.2V, | $V_{IN} \geq V_{CC}$ − 0.2 V | | 0.1 | 0.2 | mA |
| $\Delta I_{CC}$ | $V_{CC}$ = 5.25 V, $V_{IN}$ = 3.4 V[§], $f_1$ = 0, Outputs open | | | | 0.5 | 2 | mA |
| $I_{CCD}$[¶] | $V_{CC}$ = 5.25 V, One input switching at 50% duty cycle, Outputs open, $\overline{CEAB}$ and $\overline{OEAB}$ = LOW, CEBA = HIGH, $V_{IN}$ ≤ 0.2 V or $V_{IN} \geq V_{CC}$ − 0.2 V | | | | 0.06 | 1.2 | mA/MHz |
| $I_C$[#] | $V_{CC}$ = 5.25 V, $f_0$ = 10 MHz, Outputs open, $\overline{CEAB}$ and $\overline{OEAB}$ = LOW, CEBA = HIGH, $f_0 = \overline{LEAB}$ = 10 MHz | One bit switching at $f_1$ = 5 MHz at 50% duty cycle | $V_{IN}$ ≤ 0.2 V or $V_{IN} \geq V_{CC}$ − 0.2 V | | 0.7 | 1.4 | mA |
| | | | $V_{IN}$ = 3.4 V or GND | | 1.2 | 3.4 | |
| | | Eight bits switching at $f_1$ = 5 MHz at 50% duty cycle | $V_{IN}$ ≤ 0.2 V or $V_{IN} \geq V_{CC}$ − 0.2 V | | 2.8 | 5.6[‖] | |
| | | | $V_{IN}$ = 3.4 V or GND | | 5.1 | 14.6[‖] | |
| $C_i$ | | | | | 5 | 10 | pF |
| $C_o$ | | | | | 9 | 12 | pF |

† Typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, $I_{OS}$ tests should be performed last.

§ Per TTL-driven input ($V_{IN}$ = 3.4 V); all other inputs at $V_{CC}$ or GND

¶ This parameter is derived for use in total power-supply calculations.

# $I_C$ = $I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

$I_C$ = Total supply current

$I_{CC}$ = Power-supply current with CMOS input levels

$\Delta I_{CC}$ = Power-supply current for a TTL high input ($V_{IN}$ = 3.4 V)

$D_H$ = Duty cycle for TTL inputs high

$N_T$ = Number of TTL inputs at $D_H$

$I_{CCD}$ = Dynamic current caused by an input transition pair (HLH or LHL)

$f_0$ = Clock frequency for registered devices, otherwise zero

$f_1$ = Input signal frequency

$N_1$ = Number of inputs changing at $f_1$

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the $I_{CC}$ formula.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

| PARAMETER | | CY74FCT2543T | | CY74FCT2543AT | | CY74FCT2543CT | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, $\overline{LEBA}$ or $\overline{LEAB}$ low | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, high or low | A or B before $\overline{LEBA}{\downarrow}$ or $\overline{LEAB}{\downarrow}$ | 2 | | 2 | | 2 | | ns |
| $t_h$ | Hold time, high or low | A or B after $\overline{LEBA}{\downarrow}$ or $\overline{LEAB}{\downarrow}$ | 2 | | 2 | | 2 | | ns |

**switching characteristics over operating free-air temperature range (see Figure 1)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | CY74FCT2543T | | CY74FCT2543AT | | CY74FCT2543CT | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | A or B | B or A | 2.5 | 8.5 | 2.5 | 6.5 | 2.5 | 5.5 | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PLH}$ | $\overline{LEBA}$ or $\overline{LEAB}$ | A or B | 2.5 | 12.5 | 2.5 | 8 | 2.5 | 7 | ns |
| $t_{PHL}$ | | | | | | | | | |
| $t_{PZH}$ | $\overline{OEBA}$ or $\overline{OEAB}$ | A or B | 2 | 12 | 2 | 9 | 2 | 8 | ns |
| $t_{PZL}$ | | | 2 | 12 | 2 | 9 | 2 | 8 | |
| $t_{PZH}$ | $\overline{CEBA}$ or $\overline{CEAB}$ | A or B | 2 | 12 | 2 | 9 | 2 | 8 | ns |
| $t_{PZL}$ | | | 2 | 12 | 2 | 9 | 2 | 8 | |
| $t_{PHZ}$ | $\overline{OEBA}$ or $\overline{OEAB}$ | A or B | 2 | 9 | 2 | 7.5 | 2 | 6.5 | ns |
| $t_{PLZ}$ | | | 2 | 9 | 2 | 7.5 | 2 | 6.5 | |
| $t_{PHZ}$ | $\overline{CEBA}$ or $\overline{CEAB}$ | A or B | 2 | 9 | 2 | 7.5 | 2 | 6.5 | ns |
| $t_{PLZ}$ | | | 2 | 9 | 2 | 7.5 | 2 | 6.5 | |

TEXAS
INSTRUMENTS

## PARAMETER MEASUREMENT INFORMATION

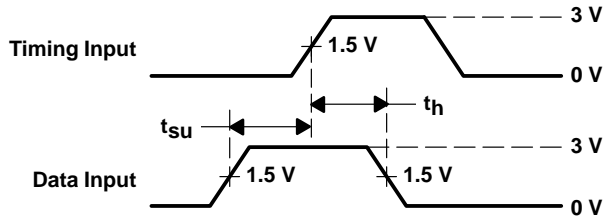| TEST | S1 |
|------|-----|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V |
| $t_{PHZ}/t_{PZH}$ | Open |

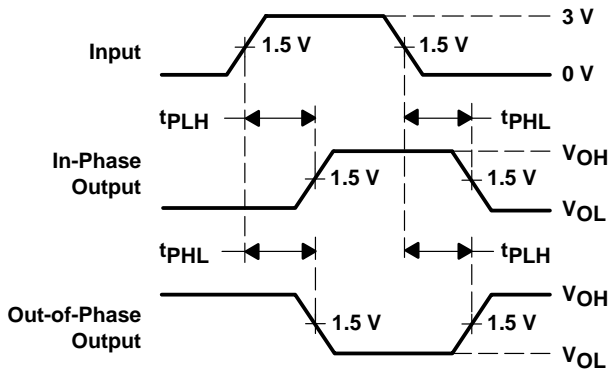**LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS**
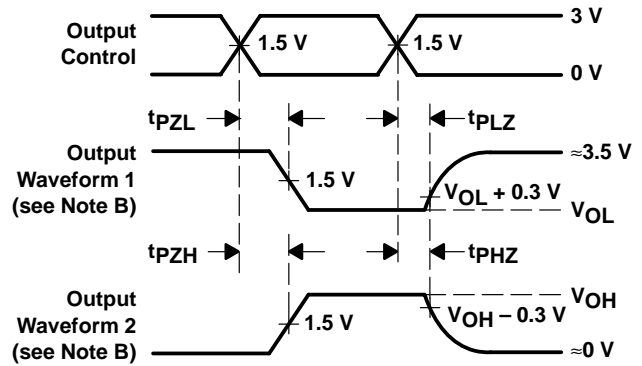
**LOAD CIRCUIT FOR
3-STATE OUTPUTS**

**VOLTAGE WAVEFORMS
PULSE DURATION**

**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

NOTES: A. $C_L$ includes probe and jig capacitance.
        B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
           Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
        C. The outputs are measured one at a time with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CY74FCT2543ATQCT | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2543A | Samples |
| CY74FCT2543ATSOC | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2543A | Samples |
| CY74FCT2543CTQCT | ACTIVE | SSOP | DBQ | 24 | 2500 | Green (RoHS & no Sb/Br) | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | FCT2543C | Samples |
| CY74FCT2543CTSOC | ACTIVE | SOIC | DW | 24 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | FCT2543C | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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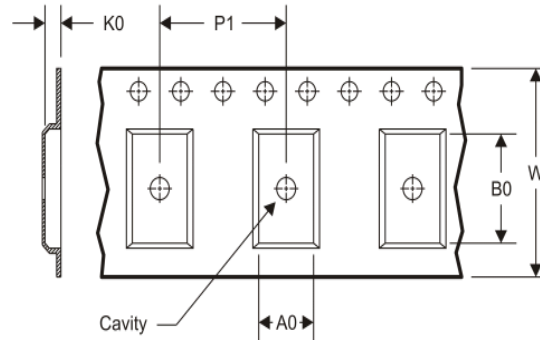
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**
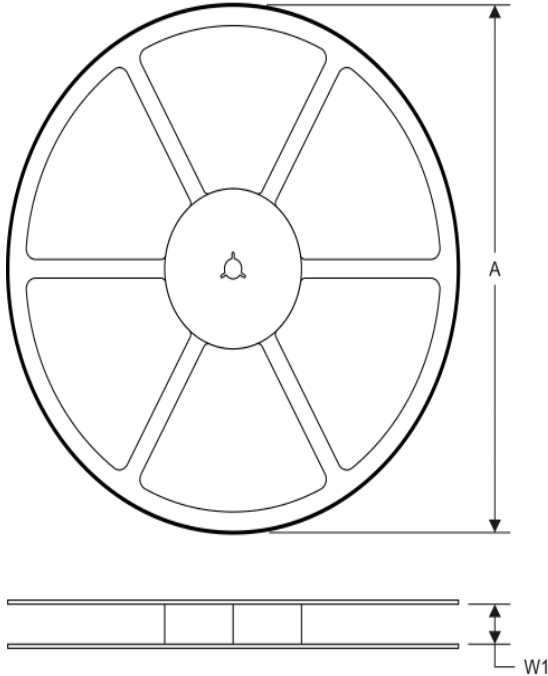
**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CY74FCT2543ATQCT | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| CY74FCT2543CTQCT | SSOP | DBQ | 24 | 2500 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

**TAPE AND REEL BOX  DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CY74FCT2543ATQCT | SSOP | DBQ | 24 | 2500 | 367.0 | 367.0 | 38.0 |
| CY74FCT2543CTQCT | SSOP | DBQ | 24 | 2500 | 367.0 | 367.0 | 38.0 |

DBQ (R−PDSO−G24)  PLASTIC SMALL−OUTLINE PACKAGE

0.344 (8,75)
0.337 (8,55)

24  13

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)

1  12

Pin 1
Index Area

0.025 (0,635)

0.012 (0,30)
0.008 (0,20)

⊕ 0.005 (0,13) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

0.035 (0,89)
0.016 (0,40)

4073301−4/H  10/2008
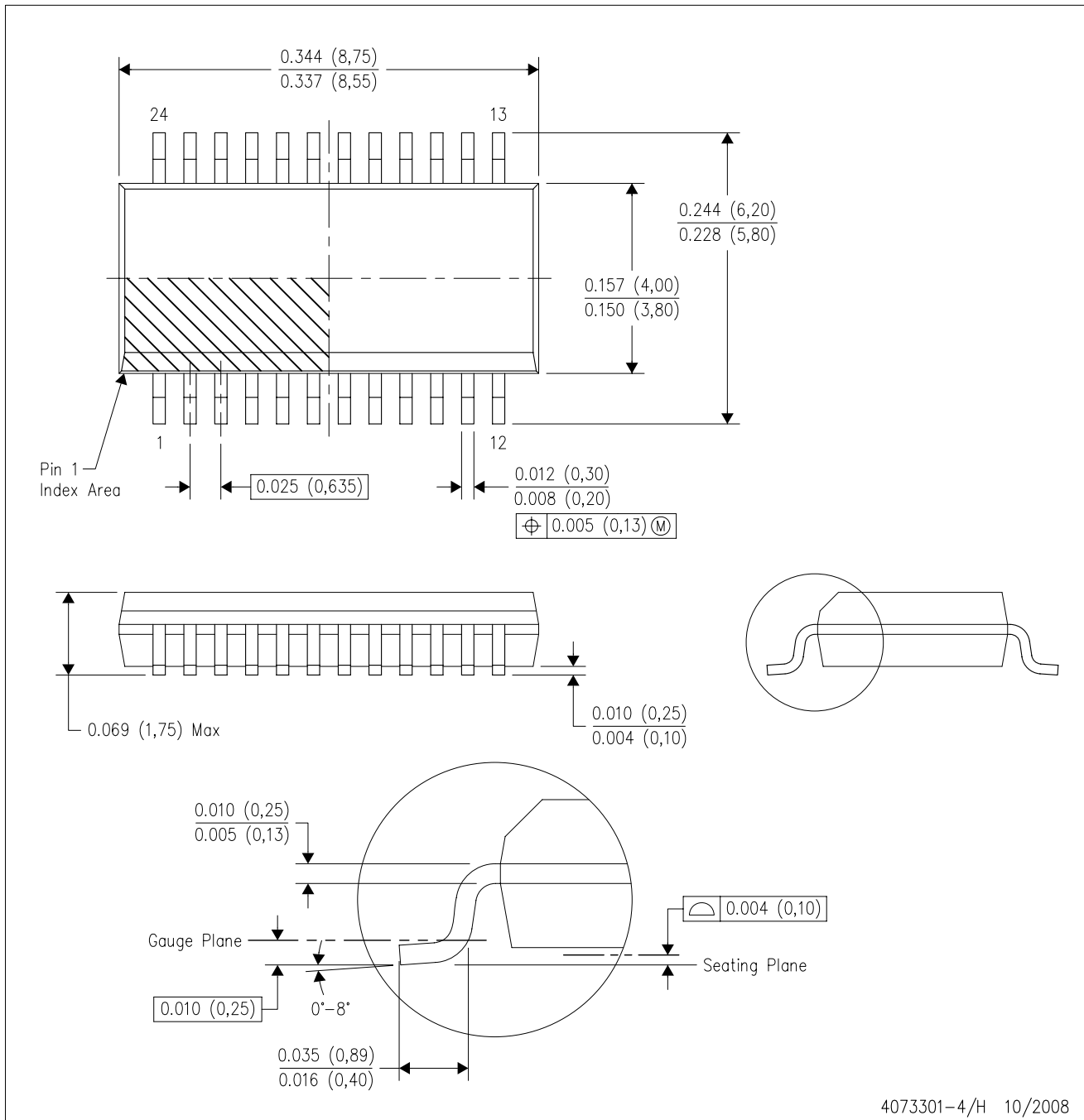
NOTES:  A.  All linear dimensions are in inches (millimeters).
B.  This drawing is subject to change without notice.
C.  Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D.  Falls within JEDEC MO−137 variation AE.

## DBQ (R−PDSO−G24)      PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

24X 0,4

22X 0,635

24X 1,6

5,4

24X 0,4

22X 0,635

24X 1,6

5,4

0,4

Solder Mask Opening

1,7    1,6

Pad Geometry

0,05

0,5

4210335−4/D 03/14
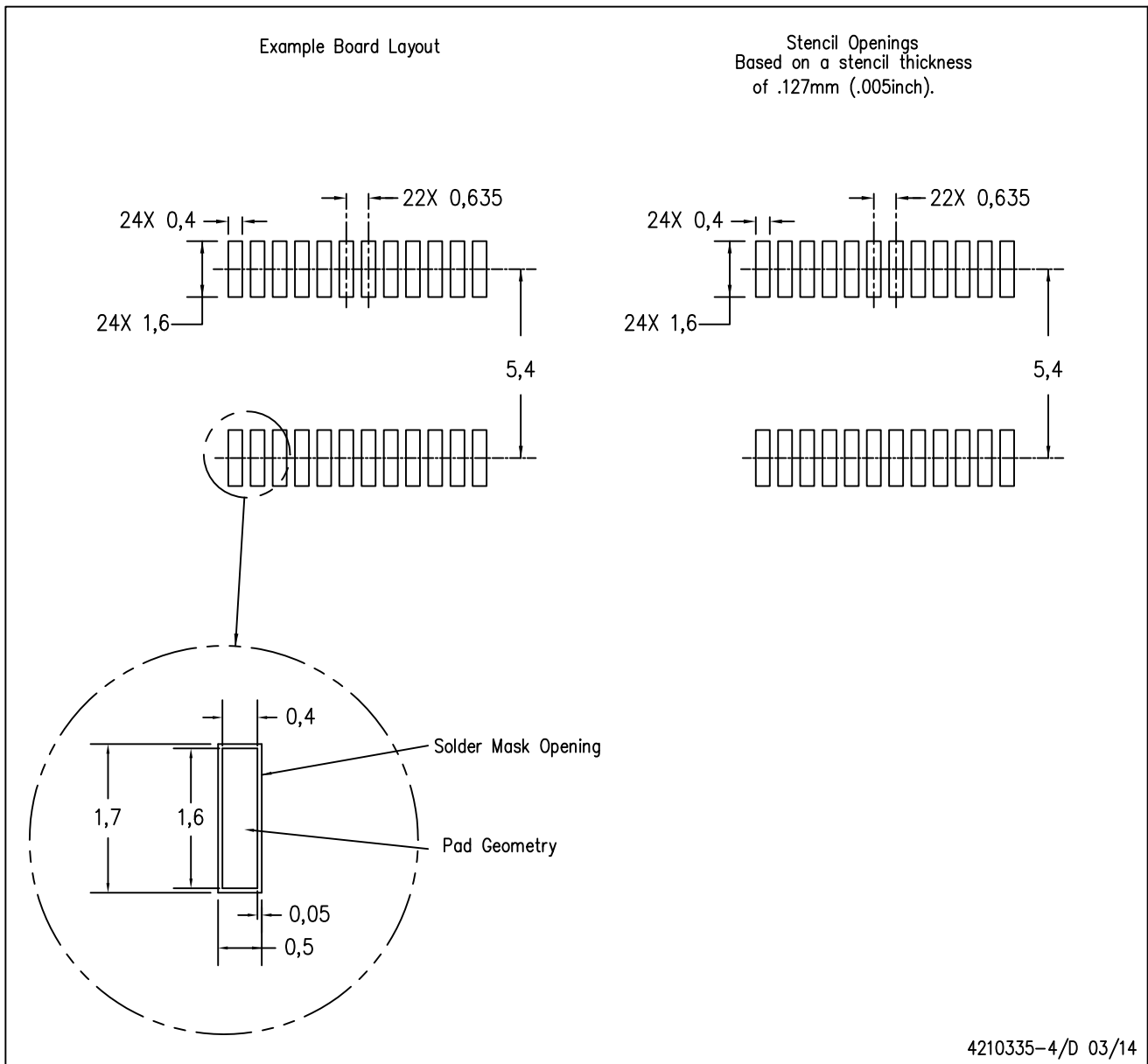
NOTES:    A.   All linear dimensions are in millimeters.
            B.   This drawing is subject to change without notice.
            C.   Publication IPC−7351 is recommended for alternate designs.
            D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC−7525 for other stencil recommendations.

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DW (R−PDSO−G24)                                        PLASTIC SMALL OUTLINE

$\frac{0.614\ (15,60)}{0.598\ (15,20)}$

24                                    13

$\frac{0.419\ (10,63)}{0.393\ (9,97)}$

$\frac{0.299\ (7,60)}{0.291\ (7,40)}$

1                                      12

Pin 1
Index Area

0.050 (1,27)

$\frac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ | 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\frac{0.012\ (0,30)}{0.004\ (0,10)}$

$\frac{0.013\ (0,33)}{0.008\ (0,20)}$

⌂ | 0.004 (0,10)

Seating Plane

Gauge Plane

0.010 (0,25)          0°−8°

$\frac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−5/G 01/11
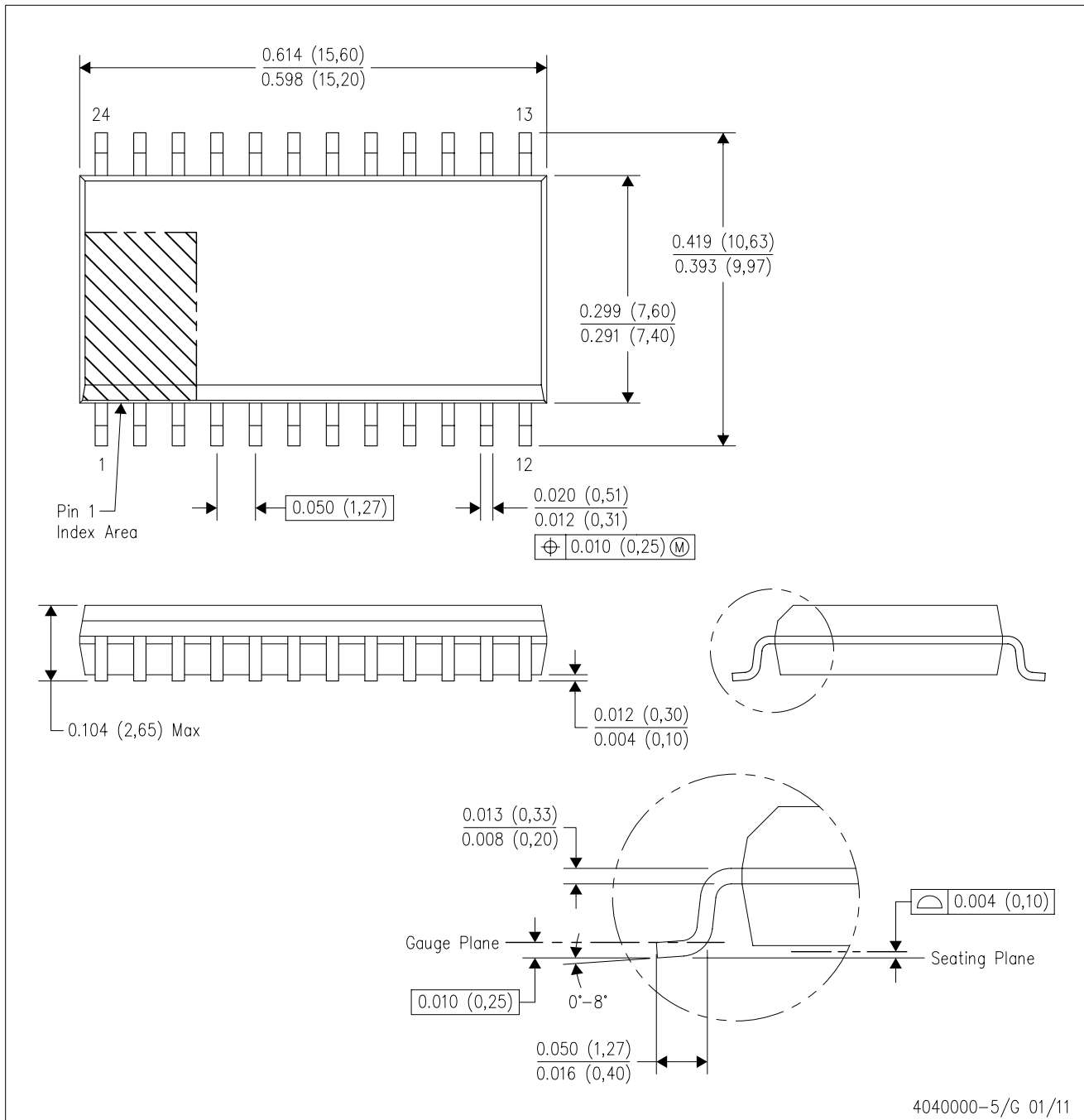
NOTES:   A.  All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.  This drawing is subject to change without notice.
         C.  Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.  Falls within JEDEC MS−013 variation AD.

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