

32-Bit

Microcontroller

TC33x/TC32x

32-Bit Single-Chip Microcontroller
AA-Step

32-Bit Single-Chip Microcontroller

Data Sheet

V 1.1, 2021-03

Microcontrollers

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Table of Contents

1	Summary of Features	6
2	TC33x/TC32x Pin Definition and Functions:	10
2.1	LFBGA-292 Package Variant Pin Configuration of TC33x/TC32x for feature package LP	16
2.2	LFBGA-180 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP	76
2.3	TQFP-144 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP	130
2.4	TQFP-100 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP	182
2.5	TQFP-80 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP	217
2.6	Sequence of Pads in Pad Frame for feature package L and LP	245
2.7	Legend	256
3	Electrical Specification	258
3.1	Parameter Interpretation	258
3.2	Absolute Maximum Ratings	259
3.3	Pin Reliability in Overload	260
3.4	Operating Conditions	262
3.5	5 V / 3.3 V switchable Pads	265
3.6	VADC Parameters	278
3.7	MHz Oscillator	282
3.8	Back-up Clock	284
3.9	Temperature Sensor	285
3.10	Power Supply Current	286
3.10.1	Calculating the 1.25 V Current Consumption	291
3.11	Power Supply Infrastructure and Supply Start-up	291
3.11.1	Supply Ramp-up and Ramp-down Behavior	292
3.11.1.1	Single Supply mode (a)	292
3.11.1.2	Single Supply mode (e)	295
3.11.1.3	External Supply mode (d)	297
3.11.1.4	External Supply mode (h)	299
3.12	Reset Timing	301
3.13	EVR	304
3.14	System Phase Locked Loop (SYS_PLL)	313
3.15	Peripheral Phase Locked Loop (PER_PLL)	314
3.16	AC Specifications	315
3.17	JTAG Parameters	316
3.18	DAP Parameters	318
3.19	ASCLIN SPI Master Timing	320
3.20	QSPI Timings, Master and Slave Mode	322
3.21	E-Ray Parameters	326
3.22	FSP Parameter	328
3.23	Flash Target Parameters	329
3.24	Quality Declarations	334
3.25	Package Outline	336
3.25.1	Package Parameters	338
4	History	340
4.1	Changes from Version 0.4 to Version 0.6	340
4.2	Changes from Version 0.6 to Version 0.7	342
4.3	Changes from Version 0.7 to Version 1.0	346
4.4	Changes from Version 1.0 to Version 1.1	347

1 Summary of Features

The TC33x/TC32x product family has the following features:

- High Performance Microcontroller with one CPU core
- One 32-bit super-scalar TriCore CPU (TC1.6.2P) with the following features:
 - Superior real-time performance
 - Strong bit handling
 - Fully integrated DSP capabilities
 - Multiply-accumulate unit able to sustain 2 MAC operations per cycle
 - Fully pipelined Floating point unit (FPU)
 - up to 300 MHz operation at full temperature range
 - up to 192 Kbyte Data Scratch-Pad RAM (DSPR)
 - up to 8 Kbyte Instruction Scratch-Pad RAM (PSPR)
 - up to 8 Kbyte Data RAM (DLMU)
 - 32 Kbyte Instruction Cache (ICACHE)
 - 16 Kbyte Data Cache (DCACHE)
- Lockstepped shadow core for one TC1.6.2P
- Multiple on-chip memories
 - All embedded NVM and SRAM are ECC protected
 - up to 2 Mbyte Program Flash Memory (PFLASH)
 - up to 128 Kbyte Data Flash Memory (DFLASH 0) usable for EEPROM emulation
 - BootROM (BROM)
- 64 Channel DMA Controller with safe data transfer
- Sophisticated interrupt system (ECC protected)
- High performance on-chip bus structure
 - 64-bit Cross Bar Interconnect (SRI) giving fast parallel access between bus masters, CPUs and memories
 - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
 - SRI to SPB bus bridges (SFI Bridge)
- Optional Hardware Security Module (HSM) on some variants
- Safety Management Unit (SMU) handling safety monitor alarms
- Memory Test Unit with ECC, Memory Initialization and MBIST functions (MTU)
- Hardware I/O Monitor (IOM) for checking of digital I/O
- Versatile On-chip Peripheral Units
 - 12 Asynchronous/Synchronous Serial Channels (ASCLIN) with hardware LIN support (V1.3, V2.0, V2.1 and J2602) up to 50 MBaud
 - 4 Queued SPI Interface Channels (QSPI) with master and slave capability up to 50 Mbit/s
 - 2 MCMCAN Modules with 4 CAN nodes for high efficiency data handling via FIFO buffering
 - 6 Single Edge Nibble Transmission (SENT) channels for connection to sensors
 - 1 FlexRay™ module with 2 channels (E-Ray) supporting V2.1
 - 2 Generic Timer Module (GTM) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
 - One Capture / Compare 6 module (Two kernels CCU60 and CCU61)
 - One General Purpose 12 Timer Unit (GPT12)

- Versatile Successive Approximation ADC (VADC)
 - Cluster of 2 independent ADC kernels
 - Input voltage range from 0 V to 5.5V (ADC supply)
- Digital programmable I/O ports
- On-chip debug support for OCDS Level 1 (CPUs, DMA, On Chip Buses)
- Multi-core debugging, real time tracing, and calibration
- Four/five wire JTAG (IEEE 1149.1) or DAP (Device Access Port) interface
- Power Management System and on-chip regulators
- Clock Generation Unit with System PLL and Peripheral PLL
- Embedded Voltage Regulator
- Qualified for automotive application according to AEC-Q100 (only applicable after delivery release of the corresponding sales codes)
- ISO 26262 Safety Element out of Context for safety requirements up to ASIL D (only applicable for sales codes listed within a released Safety Package Release Note from IFX)

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

Table 1-1 Platform Feature Overview

Feature		TC33x/TC32x
CPUs	Type	TC1.6.2
	Cores / Checker Cores	1 / 1
	Max. Freq.	300 MHz
Cache per CPU	Program	32 KB
	Data	16 KB
SRAM per CPU	PSPR	8 KB
	DSPR	192 KB
	DLMU	8 KB
Extension Memory	TCM	-
	XCM	-
	XTM	-
Program Flash	Size	2 MB
	Banks	1 x 2 MB
Data Flash	Size (single-ended)	128 KB (DF0) + 128 KB (DF1)
DMA	Channels	64
CONVCTRL	Modules	1
EVADC	Primary Groups/Channels	2 / 16
	Secondary Groups/Channels	2 / 28
	Fast Compare Channels	-
EDSADC	Channels	-
GTM	Cluster	2 @ 200MHz
	TIM (8 ch)	2
	TOM (16 ch)	2
	ATOM (8 ch)	1
	MCS (8 ch)	0
	CMU / ICM	1 / 1
	PSM	0
	TBU channels	3 (TBU0-2)
	SPE	2
	CMP / MON	1 / 1
	BRC / DPLL	1 / 0
	CDTM modules	2
	DTM modules	6 (4 on TOM, 2 on ATOM)

Table 1-1 Platform Feature Overview (cont'd)

Feature		TC33x/TC32x
Timer	GPT12	1
	CCU6 (2 kernels CCU60 / CCU61)	1
STM	Modules	1
FlexRay	Modules	1
	Channels	2
CAN	Modules	2
	Nodes	2 x 4
	of which support TT-CAN	-
QSPI	Modules	4
	HSIC Channels	2
ASCLIN	Modules	12
I2C	Interfaces	-
SENT	Channels	6
PSI5	Modules	-
PSI5-S	Modules	-
HSSL	Channels	-
MSC	Channels	-
EBU	External Bus	-
SDMMC	eMMC/SD Interface	-
FCE	Modules	1
Safety Support	SMU	yes
	IOM	yes
SPU	Modules	-
RIF	Modules	-
HSPDM	Modules	-
Security	HSM+	1
Debug	OCDS	yes
	MCDS	no
	miniMCDS	no
	miniMCDS TRAM	no
	MCDS light	no
	AGBT	no
Low Power Features	Standby RAM	1
	SCR	yes
Packages	Type	LFBGA-292 / LFBGA-180 / TQFP-144 / TQFP-100 / TQFP-80
I/O	Type	5 V CMOS / 3.3 V CMOS
T _{ambient}	Range	-40 ... +150°C

2 TC33x/TC32x Pin Definition and Functions:

The following figures are showing the TC33x/TC32x Logic Symbols for the package variants:

- LFBGA-292 for feature package LP ([Figure 2-1](#))
- LFBGA-180 for feature package L and LP ([Figure 2-2](#))
- TQFP-144 for feature package L and LP ([Figure 2-3](#))
- TQFP-100 for feature package L and LP ([Figure 2-4](#))
- TQFP-80 for feature package L and LP ([Figure 2-5](#))

TC33x/TC32x Pin Definition and Functions:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		
A	NC1	VEXT	P10.7	P10.6	P10.2	P10.3	P10.0	P11.11	P11.9	P11.2	P13.3	P13.1	P14.8	P14.5	P14.1	P15.6	P15.4	P15.1	VDDP3	VSS	A	
B	P02.0	VSS	VEXT	P10.8	P10.5	P10.4	P10.1	P11.12	P11.10	P11.3	P13.2	P13.0	P14.6	P14.3	P14.4	P14.0	P15.3	VDDP3	VSS	P15.0	B	
C	P02.2	P02.1																	P15.2	P20.14	C	
D	P02.4	P02.3	VSS	VFLEX	NC	NC	NC	NC	P11.6	NC	P14.10	P14.9	P14.7	P15.8	P15.7	VDD	VSS		P20.12	P20.13	D	
E	P02.6	P02.5	NC	VSS	NC	P11.8	NC	NC	NC	NC	NC	NC	P14.2	P15.5	VDD	VSS	P20.9		P20.10	P20.11	E	
F	P02.8	P02.7	NC	NC												ESR0	P20.6		P20.7	P20.8	F	
G	P00.0	P00.1	NC	NC				VDD	VSS	VSS	VSS	VSS	VSS	VDD		ESR1	PORST		P20.1	P20.3	G	
H	P00.2	P00.3	NC	NC			VDD		VSS	VSS	VSS	VSS		VDD		P21.7 / TDO	P21.6 / TDI		P20.2	P20.0	H	
J	P00.4	P00.5	P00.6	NC			VSS	VSS		VSS	VSS		VSS	VSS		TCK	P21.1		P21.3	P21.5	J	
K	P00.7	P00.9	P00.8	P00.10			VSS	VSS	VSS	VSS	VSS	VSS	VSS	NC		TMS	P21.0		P21.2	P21.4	K	
L	P00.11	P00.12	NC	NC			VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		NC	NC		TRST	VSS	L	
M	NC	NC	NC	NC			VSS	VSS		VSS	VSS		VSS	VSS		NC	NC		XTAL2	XTAL1	M	
N	NC	NC	AN36 / P40.6	AN38 / P40.8			VDD		VSS	VSS	VSS	VSS		VDDO		NC	NC		VDD	VEXT	N	
P	AN39 / P40.9	AN37 / P40.7	AN32 / P40.4	AN34			VDD	VSS	VSS	VSS	VSS	VSS	VDDO			P22.4	NC		P22.1	P22.0	P	
R	AN33 / P40.5	AN35	NC	NC												NC	NC		P22.3	P22.2	R	
T	NC	NC	NC	NC	AN15	AN12	AN6	AN4	AN0	VEVRS B	P34.2	NC	NC	NC	VSS	P23.5			NC	NC	T	
U	NC	NC	NC1	NC	AN14	AN9	AN7	AN3	AN1	P34.1	P34.3	NC	NC	NC	NC	VSS			P23.1	NC	U	
V	NC	NC																	VEXT	NC	V	
W	NC	NC	NC	NC	NC	AN13	AN11	AN8	AN2	P33.0	P33.2	P33.4	P33.6	P33.8	P33.10	P33.12	VCAP1	P32.4	VSS	VEXT	W	
Y	NC1	NC	NC	VSSM	VDDM	VAREF 1	VAGND 1	AN10	AN5	P33.1	P33.3	P33.5	P33.7	P33.9	P33.11	NC	VCAP0	NC	NC	NC	VSS	Y

Figure 2-1 TC33x/TC32x Logic Symbol for the package variant LFBGA-292 for feature package LP

TC33x/TC32x Pin Definition and Functions:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14					
A	NC	P10.3	P10.2	P11.12	P11.9	P11.2	P13.0	P13.2	P14.0	P15.3	P15.6	P15.1	P15.0	NC	A				
B	P02.0	VSS	P10.1	P10.4	P11.10	P11.3	P13.1	P13.3	P14.5	P14.1	P15.4	P15.2	VSS	P20.14	B				
C	P02.1	P02.2	VSS	NC	P11.11	P11.6	NC	NC	P14.6	P14.4	P14.3	VSS	P20.13	P20.10	C				
D	P02.5	P02.4	P02.3	VSS	VFLEX	P11.8	P15.8	P15.7	P14.2	P15.5	VSS	P20.9	P20.12	P20.11	D				
E	P02.6	P02.7	P02.8	P10.6	VSS					VSS	$\overline{\text{ESR1}}$	P20.7	$\overline{\text{PORST}}$	$\overline{\text{ESR0}}$	E				
F	P00.4	P00.3	P00.2	P10.5					VEXT	VDDP3	VEXT	VDD			P20.6	P20.8	P21.6 / TDI	P21.7 / TDO	F
G	P00.8	P00.7	P00.6	P00.0					VEXT	VSS	VSS	VDD			TMS	P20.3	P20.2	TCK	G
H	P00.12	P00.9	P00.5	P00.1					VDD	VSS	VSS	VEVRS B			P22.2	P21.0	P20.0	P21.5	H
J	AN36 / P40.6	AN37 / P40.7	AN38 / P40.8	AN39 / P40.9					VSS	VDD	VDDO	VEXT			P22.0	P22.3	P21.4	P21.3	J
K	AN32 / P40.4	AN33 / P40.5	AN34	AN35	VSS					VSS	NC	$\overline{\text{TRST}}$	P21.2	VSS	K				
L	NC	NC	NC	AN14	AN5	AN2	AN0	P33.4	P33.8	P33.7	VSS	P22.1	XTAL2	XTAL1	L				
M	NC	NC	AN12	AN10	AN6	AN3	P34.1	P33.1	P33.0	P33.12	NC	VSS	VDD	VEXT	M				
N	AN15	AN13	AN9	AN11	AN8	AN4	P34.2	P33.3	P33.5	P33.11	P33.10	VCAP1	VSS	P23.1	N				
P	NC	VSSM / VAGND 1	VDDM	VAREF 1	AN7	AN1	P34.3	P33.2	P33.6	P33.9	VEXT	VCAP0	NC	NC	P				

Figure 2-2 TC33x/TC32x Logic Symbol for the package variant LFBGA-180 for feature package L and LP

TC33x/TC32x Pin Definition and Functions:

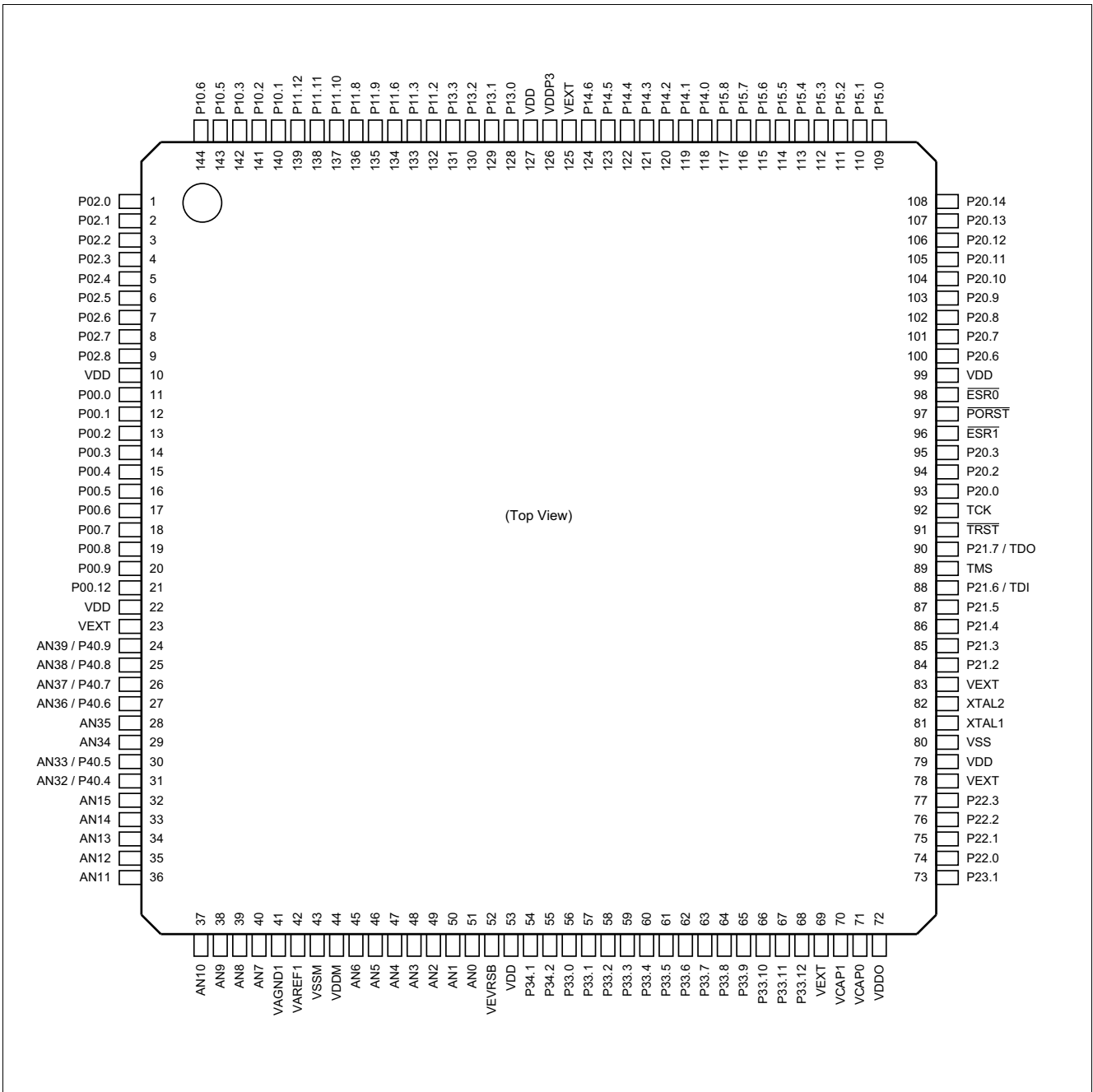


Figure 2-3 TC33x/TC32x Logic Symbol for the package variant TQFP-144 for feature package L and LP

TC33x/TC32x Pin Definition and Functions:

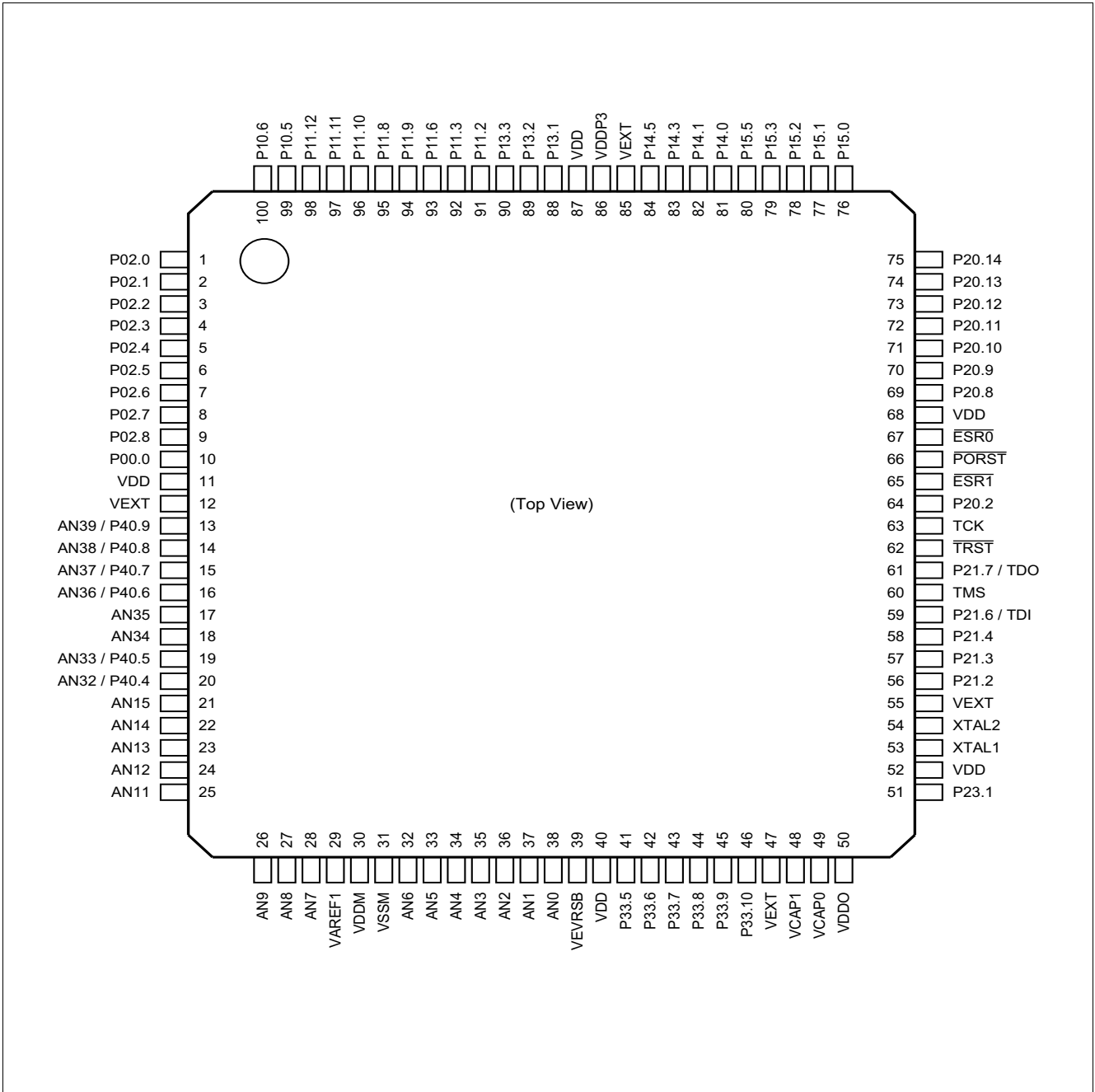


Figure 2-4 TC33x/TC32x Logic Symbol for the package variant TQFP-100 for feature package L and LP

TC33x/TC32x Pin Definition and Functions:

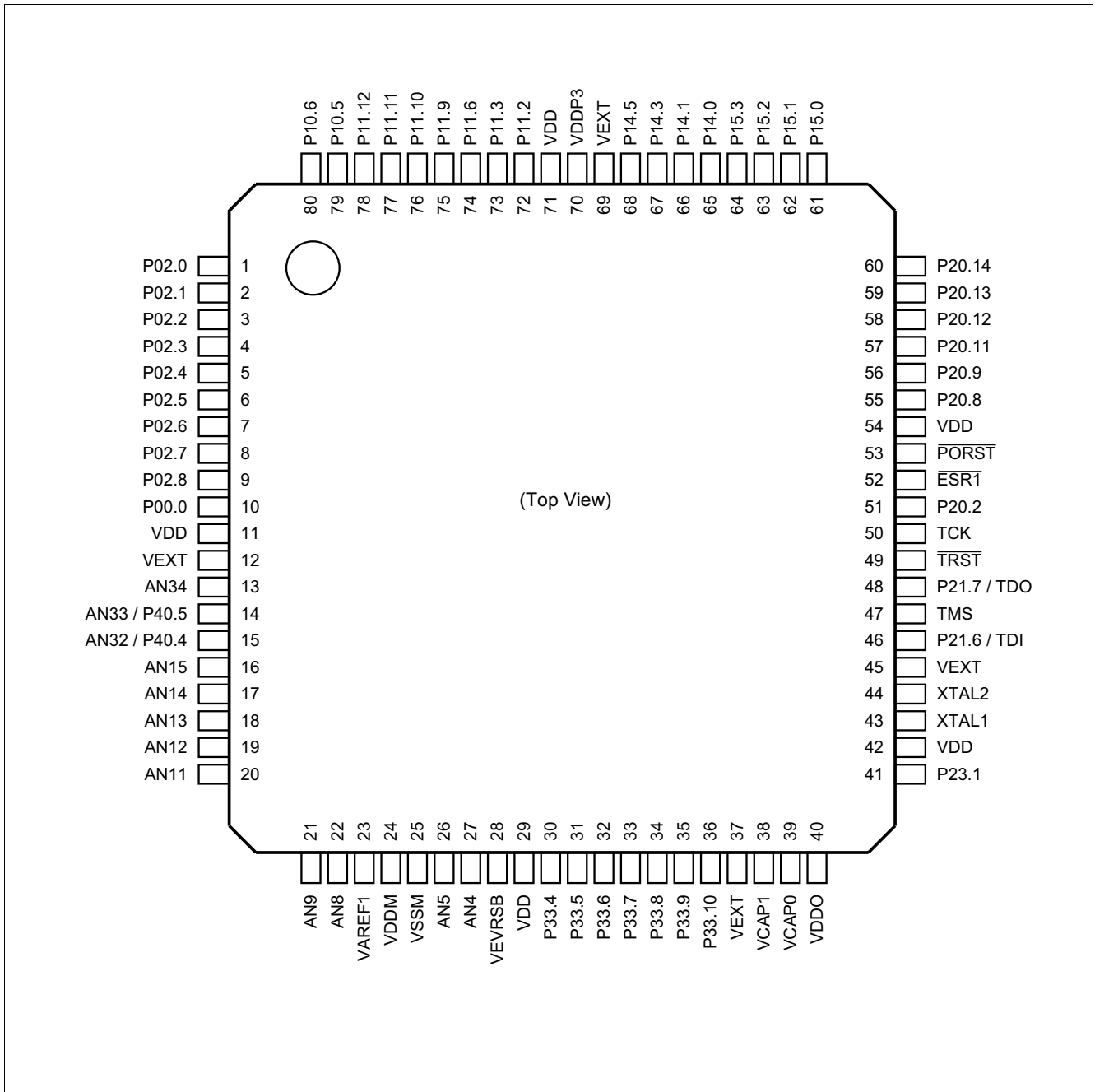


Figure 2-5 TC33x/TC32x Logic Symbol for the package variant TQFP-80 for feature package L and LP

2.1 LFBGA-292 Package Variant Pin Configuration of TC33x/TC32x for feature package LP

Table 2-1 Port 00 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G1	P00.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	CCU61_CTRAPA			Trap input capture
	CCU60_T12HRE			External timer start 12
	P00.0	O0		General-purpose output
	GTM_TOUT9	O1		GTM muxed output
	IOM_REF0_9			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CCU60_CC60INB			T12 capture input 60
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	CCU61_CC60INA			T12 capture input 60
	SENT_SENT0B			Receive input channel 0
	EVADC_G9CH11	AI		Analog input channel 11, group 9
	P00.1	O0		General-purpose output
	GTM_TOUT10	O1		GTM muxed output
	IOM_REF0_10			Reference input 0
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC0	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
IOM_REF1_13			Reference input 1	
H1	P00.2	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SENT_SENT1B			Receive input channel 1
	EVADC_G9CH10	AI		Analog input channel 10, group 9
	P00.2	O0		General-purpose output
	GTM_TOUT11	O1		GTM muxed output
	IOM_REF0_11			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	QSPI3_SL5O4	O6		Master slave select output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H2	P00.3	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU60_CC61INB			T12 capture input 61
	CAN03_RXDA			CAN receive input node 3
	SENT_SENT2B			Receive input channel 2
	CCU61_CC61INA			T12 capture input 61
	EVADC_G9CH9	AI		Analog input channel 9, group 9
	P00.3	O0		General-purpose output
	GTM_TOUT12	O1		GTM muxed output
	IOM_REF0_12			Reference input 0
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC2	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
IOM_REF1_12		Reference input 1		
J1	P00.4	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SCU_E_REQ2_2			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT3B			Receive input channel 3
	ASCLIN10_ARXA			Receive input
	EVADC_G9CH8	AI		Analog input channel 8, group 9
	P00.4	O0		General-purpose output
	GTM_TOUT13	O1		GTM muxed output
	IOM_REF0_13			Reference input 0
	—	O2		Reserved
	CAN11_TXD	O3		CAN transmit output node 1
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC3	O6		Transmit output
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
	IOM_REF1_9			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J2	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU60_CC62INB			T12 capture input 62
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7			AI
	P00.5	O0	General-purpose output	
	GTM_TOUT14	O1	GTM muxed output	
	IOM_REF0_14	O2	Reference input 0	
	—		Reserved	
	QSPI3_SLSO3		O3	Master slave select output
	—		O4	Reserved
	—		O5	Reserved
	SENT_SPC4		O6	Transmit output
	CCU61_CC62		O7	T12 PWM channel 62
	IOM_MON1_10	O7	Monitor input 1	
IOM_REF1_11	Reference input 1			
J4	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI	Analog input channel 6, group 9	
	P00.6	O0	General-purpose output	
	GTM_TOUT15	O1	GTM muxed output	
	IOM_REF0_15	O2	Reference input 0	
	—		Reserved	
	—		Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	EVADC_EMUX10	O5	Control of external analog multiplexer interface 1	
	SENT_SPC5	O6	Transmit output	
	CCU61_COUT62	O7	T12 PWM channel 62	
	IOM_MON1_13	O7	Monitor input 1	
IOM_REF1_8	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K1	P00.7	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU61_CC60INC			T12 capture input 60
	GPT120_T2INA			Trigger/gate input of timer T2
	CCU61_CCPOS0A			Hall capture input 0
	CCU60_T12HRB			External timer start 12
	GTM_DTMT0_2			CDTM0_DTM0
	EVADC_G9CH5			AI
	P00.7	O0	General-purpose output	
	GTM_TOUT16	O1	GTM muxed output	
	ASCLIN5_ATX	O2	Transmit output	
	—	O3	Reserved	
	—	O4	Reserved	
	EVADC_EMUX11	O5	Control of external analog multiplexer interface 1	
	—	O6	Reserved	
	CCU61_CC60	O7	T12 PWM channel 60	
	IOM_MON1_8		Monitor input 1	
IOM_REF1_13		Reference input 1		
K4	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU61_CC61INC			T12 capture input 61
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4			AI
	P00.8	O0	General-purpose output	
	GTM_TOUT17	O1	GTM muxed output	
	QSPI3_SLSO6	O2	Master slave select output	
	ASCLIN10_ATX	O3	Transmit output	
	—	O4	Reserved	
	EVADC_EMUX12	O5	Control of external analog multiplexer interface 1	
	—	O6	Reserved	
	CCU61_CC61	O7	T12 PWM channel 61	
	IOM_MON1_9		Monitor input 1	
IOM_REF1_12		Reference input 1		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	CCU61_CCPOS2A			Hall capture input 2
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3			AI
	P00.9	O0	General-purpose output	
	GTM_TOUT18	O1	GTM muxed output	
	QSPI3_SLSO7	O2	Master slave select output	
	ASCLIN3_ARTS	O3	Ready to send output	
	—	O4	Reserved	
	ASCLIN4_ATX	O5	Transmit output	
	—	O6	Reserved	
	CCU61_CC62	O7	T12 PWM channel 62	
	IOM_MON1_10		Monitor input 1	
IOM_REF1_11	Reference input 1			
K5	P00.10	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN1_1			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_1			Mux input channel 1 of TIM module 0
	EVADC_G9CH2	AI	Analog input channel 2, group 9	
	P00.10	O0	General-purpose output	
	GTM_TOUT19	O1	GTM muxed output	
	ASCLIN4_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_7		Monitor input 1	
	IOM_REF1_7		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-1 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L1	P00.11	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN2_1			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_1			Mux input channel 2 of TIM module 0
	CCU60_CTRAPA			Trap input capture
	CCU61_T12HRE			External timer start 12
	EVADC_G9CH1			Analog input channel 1, group 9
	P00.11	O0		General-purpose output
	GTM_TOUT20	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
L2	P00.12	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	ASCLIN3_ACTSA			Clear to send input
	ASCLIN4_ARXA			Receive input
	EVADC_G9CH0	AI		Analog input channel 0, group 9
	P00.12	O0		General-purpose output
	GTM_TOUT21	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
IOM_MON1_7	Monitor input 1			
IOM_REF1_7	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-2 Port 02 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.0	O0	General-purpose output	
	GTM_TOUT0	O1	GTM muxed output	
	IOM_REF0_0		Reference input 0	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI3_SLSO1	O3	Master slave select output	
	—	O4	Reserved	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5		Monitor input 2	
	IOM_REF2_5		Reference input 2	
	ERAY0_TXDA	O6	Transmit Channel A	
	CCU60_CC60	O7	T12 PWM channel 60	
	IOM_MON1_2		Monitor input 1	
	IOM_REF1_6		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C2	P02.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2_1			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.1	O0	General-purpose output	
	GTM_TOUT1	O1	GTM muxed output	
	IOM_REF0_1		Reference input 0	
	—	O2	Reserved	
	QSPI3_SLSO2	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT60	O7	T12 PWM channel 60	
	IOM_MON1_3		Monitor input 1	
	IOM_REF1_3		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
C1	P02.2	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1	
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0	
	CCU61_CC61INB			T12 capture input 61	
	CCU60_CC61INA			T12 capture input 61	
	P02.2			O0	General-purpose output
	GTM_TOUT2			O1	GTM muxed output
	IOM_REF0_2				Reference input 0
	ASCLIN1_ATX			O2	Transmit output
	IOM_MON2_13				Monitor input 2
	IOM_REF2_13				Reference input 2
	QSPI3_SLSO3			O3	Master slave select output
	—	O4	Reserved		
	CAN02_TXD	O5	CAN transmit output node 2		
	IOM_MON2_7		Monitor input 2		
	IOM_REF2_7		Reference input 2		
	ERAY0_TXDB	O6	Transmit Channel B		
	CCU60_CC61	O7	T12 PWM channel 61		
	IOM_MON1_1		Monitor input 1		
IOM_REF1_5		Reference input 1			
D2	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0	
	ERAY0_RXDB2			Receive Channel B2	
	CAN02_RXDB			CAN receive input node 2	
	ASCLIN1_ARXG			Receive input	
	P02.3			O0	General-purpose output
	GTM_TOUT3			O1	GTM muxed output
	IOM_REF0_3				Reference input 0
	ASCLIN2_ASLSO			O2	Slave select signal output
	QSPI3_SLSO4			O3	Master slave select output
	—			O4	Reserved
	—	O5	Reserved		
	—	O6	Reserved		
	CCU60_COUT61	O7	T12 PWM channel 61		
	IOM_MON1_4		Monitor input 1		
	IOM_REF1_2		Reference input 1		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
D1	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1	
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0	
	CCU61_CC62INB			T12 capture input 62	
	QSPI3_SLSIA			Slave select input	
	CCU60_CC62INA			T12 capture input 62	
	CAN11_RXDA			CAN receive input node 1	
	P02.4			O0	General-purpose output
	GTM_TOUT4			O1	GTM muxed output
	IOM_REF0_4				Reference input 0
	ASCLIN2_ASCLK	O2	Shift clock output		
	QSPI3_SLSO0	O3	Master slave select output		
	—	O4	Reserved		
	—	O5	Reserved		
	ERAY0_TXENA	O6	Transmit Enable Channel A		
	CCU60_CC62	O7	T12 PWM channel 62		
	IOM_MON1_0		Monitor input 1		
IOM_REF1_4		Reference input 1			
E2	P02.5	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1	
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0	
	QSPI3_MRSTA			Master SPI data input	
	SENT_SENT3C			Receive input channel 3	
	P02.5			O0	General-purpose output
	GTM_TOUT5			O1	GTM muxed output
	IOM_REF0_5				Reference input 0
	CAN11_TXD			O2	CAN transmit output node 1
	QSPI3_MRST			O3	Slave SPI data output
	IOM_MON2_3		Monitor input 2		
	IOM_REF2_3		Reference input 2		
	—	O4	Reserved		
	—	O5	Reserved		
	ERAY0_TXENB	O6	Transmit Enable Channel B		
	CCU60_COUT62	O7	T12 PWM channel 62		
	IOM_MON1_5		Monitor input 1		
IOM_REF1_1		Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	CCU60_CC60INC			T12 capture input 60
	SENT_SENT2C			Receive input channel 2
	GPT120_T3INA			Trigger/gate input of core timer T3
	CCU60_CCPOS0A			Hall capture input 0
	CCU61_T12HRB			External timer start 12
	QSPI3_MTSRA			Slave SPI data input
	P02.6			O0
	GTM_TOUT6	O1	GTM muxed output	
	IOM_REF0_6		Reference input 0	
	—	O2	Reserved	
	QSPI3_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	EVADC_EMUX00	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC60	O7	T12 PWM channel 60	
	IOM_MON1_2		Monitor input 1	
	IOM_REF1_6		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-2 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P02.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	CCU60_CC61INC			T12 capture input 61
	SENT_SENT1C			Receive input channel 1
	GPT120_T3EUDA			Count direction control input of core timer T3
	CCU60_CCPOS1A			Hall capture input 1
	QSPI3_SCLKA			Slave SPI clock inputs
	CCU61_T13HRB			External timer start 13
	P02.7			O0
	GTM_TOUT7	O1	GTM muxed output	
	IOM_REF0_7	O2	Reference input 0	
	—		Reserved	
	QSPI3_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	EVADC_EMUX01	O5	Control of external analog multiplexer interface 0	
	SENT_SPC1	O6	Transmit output	
	CCU60_CC61	O7	T12 PWM channel 61	
	IOM_MON1_1		Monitor input 1	
	IOM_REF1_5		Reference input 1	
F1	P02.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CCU60_CC62INC			T12 capture input 62
	SENT_SENT0C			Receive input channel 0
	CCU60_CCPOS2A			Hall capture input 2
	GPT120_T4INA			Trigger/gate input of timer T4
	CCU61_T12HRC			External timer start 12
	CCU61_T13HRC			External timer start 13
	P02.8	O0	General-purpose output	
	GTM_TOUT8	O1	GTM muxed output	
	IOM_REF0_8	O2	Reference input 0	
	QSPI3_SLSO5		Master slave select output	
	ASCLIN8_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	EVADC_EMUX02	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC62	O7	T12 PWM channel 62	
	IOM_MON1_0		Monitor input 1	
IOM_REF1_4	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-3 Port 10 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P10.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN4_2			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_2			Mux input channel 4 of TIM module 0
	GPT120_T6EUDB			Count direction control input of core timer T6
	ASCLIN11_ARXA			Receive input
	P10.0	O0		General-purpose output
	GTM_TOUT102	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	QSPI1_SLSO10	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
B7	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	—			O4
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-3 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A5	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P10.2	O0	General-purpose output	
	GTM_TOUT104	O1	GTM muxed output	
	IOM_MON2_9		Monitor input 2	
	—	O2	Reserved	
	QSPI1_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
—	O6	Reserved		
—	O7	Reserved		
A6	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0	General-purpose output	
	GTM_TOUT105	O1	GTM muxed output	
	IOM_MON2_10		Monitor input 2	
	—	O2	Reserved	
	QSPI1_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	—	O5	Reserved	
	CAN02_TXD	O6	CAN transmit output node 2	
IOM_MON2_7		Monitor input 2		
IOM_REF2_7		Reference input 2		
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-3 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B6	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB			Receive input
	P10.4	O0	General-purpose output	
	GTM_TOUT106	O1	GTM muxed output	
	IOM_MON2_11	O2	Monitor input 2	
	—		Reserved	
	QSPI1_SLSO8	O3	Master slave select output	
	QSPI1_MTSR	O4	Master SPI data output	
	—	O5	Reserved	
—	O6	Reserved		
—	O7	Reserved		
B5	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0	General-purpose output	
	GTM_TOUT107	O1	GTM muxed output	
	IOM_REF2_9	O2	Reference input 2	
	ASCLIN2_ATX		Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14	O3	Reference input 2	
	QSPI3_SLSO8		Master slave select output	
	QSPI1_SLSO9	O4	Master slave select output	
	GPT120_T6OUT	O5	External output for overflow/underflow detection of core timer T6	
	ASCLIN2_ASLSO	O6	Slave select signal output	
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-3 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A4	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6			O0
	GTM_TOUT108	O1	GTM muxed output	
	IOM_REF2_10		Reference input 2	
	ASCLIN2_ASCLK	O2	Shift clock output	
	QSPI3_MTSR	O3	Master SPI data output	
	GPT120_T3OUT	O4	External output for overflow/underflow detection of core timer T3	
	—	O5	Reserved	
	QSPI1_MRST	O6	Slave SPI data output	
	IOM_MON2_1		Monitor input 2	
IOM_REF2_1		Reference input 2		
—	O7	Reserved		
A3	P10.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_3			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_3			Mux input channel 0 of TIM module 0
	GPT120_T3EUDB			Count direction control input of core timer T3
	ASCLIN2_ACTSA			Clear to send input
	QSPI3_MRSTB			Master SPI data input
	SCU_E_REQ0_2			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	CCU60_CCPOS1C			Hall capture input 1
	P10.7			O0
	GTM_TOUT109	O1	GTM muxed output	
	IOM_REF2_11		Reference input 2	
	—	O2	Reserved	
	QSPI3_MRST	O3	Slave SPI data output	
	IOM_MON2_3		Monitor input 2	
	IOM_REF2_3		Reference input 2	
	—	O4	Reserved	
	—	O5	Reserved	
	CAN12_TXD	O6	CAN transmit output node 2	
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-3 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B4	P10.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_2			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_2			Mux input channel 5 of TIM module 0
	CAN12_RXDB			CAN receive input node 2
	GPT120_T4INB			Trigger/gate input of timer T4
	QSPI3_SCLKB			Slave SPI clock inputs
	SCU_E_REQ1_2			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	CCU60_CCPOS2C			Hall capture input 2
	P10.8			O0
	GTM_TOUT110	O1	GTM muxed output	
	ASCLIN2_ARTS	O2	Ready to send output	
	QSPI3_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
—	O7	Reserved		

Table 2-4 Port 11 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A10	P11.2	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B10	P11.3	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
D9	P11.6	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1
E7	P11.8	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	CAN12_RXDD			CAN receive input node 2
	P11.8	O0		General-purpose output
	GTM_TOUT124	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P11.9	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
B9	P11.10	I	FAST / PU1 / VFLEX / ES	General-purpose input
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	QSPI1_SLSIA			Slave select input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
IOM_REF1_4	Reference input 1			

TC33x/TC32x Pin Definition and Functions: LFBGA-292 Package Variant Pin

Table 2-4 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A8	P11.11	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPIO_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
B8	P11.12	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

Table 2-5 Port 13 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B12	P13.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0
A12	P13.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
B11	P13.2	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-5 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P13.3	I	FAST / PU1 / VEXT / ES6	General-purpose input
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

Table 2-6 Port 14 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B16	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA			O3
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6	O6		Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK			Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5	O7		Monitor input 1
	IOM_REF1_1			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-6 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A15	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1			O0
	GTM_TOUT81	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_6		Monitor input 1	
IOM_REF1_0	Reference input 1			
E13	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0	General-purpose output	
	GTM_TOUT82	O1	GTM muxed output	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI2_SLSO1	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	ASCLIN2_ASCLK	O6	Shift clock output	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-6 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B14	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0		General-purpose output
	GTM_TOUT83	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
B15	P14.4	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	PMS_HWCFG6IN			HWCFG6 pin input
	GTM_DTMT0_0			CDTM0_DTM0
	P14.4	O0		General-purpose output
	GTM_TOUT84	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-6 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A14	P14.5	I	FAST / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0		General-purpose output
	GTM_TOUT85	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
—	O7	Reserved		
B13	P14.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	P14.6			O0
	GTM_TOUT86	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SLSO2	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved
D13	P14.7	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_5			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_5			Mux input channel 0 of TIM module 0
	ERAY0_RXDB0			Receive Channel B0
	CAN10_RXDB			CAN receive input node 0
	CAN13_RXDA			CAN receive input node 3
	ASCLIN9_ARXC			Receive input
	P14.7			O0
	GTM_TOUT87	O1		GTM muxed output
	ASCLIN0_ARTS	O2		Ready to send output
	QSPI2_SLSO4	O3		Master slave select output
	ASCLIN9_ATX	O4		Transmit output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-6 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A13	P14.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	ERAY0_RXDA0			Receive Channel A0
	CAN02_RXDD			CAN receive input node 2
	ASCLIN1_ARXD			Receive input
	P14.8	O0		General-purpose output
	GTM_TOUT88	O1		GTM muxed output
	ASCLIN5_ASLSO	O2		Slave select signal output
	ASCLIN7_ASLSO	O3		Slave select signal output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
D12	P14.9	I	FAST / PU1 / VEXT / ES	General-purpose input
	ASCLIN0_ACTSA			Clear to send input
	ASCLIN9_ARXD			Receive input
	P14.9	O0		General-purpose output
	GTM_TOUT89	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	CAN10_TXD	O4		CAN transmit output node 0
	ERAY0_TXENB	O5		Transmit Enable Channel B
	ERAY0_TXENA	O6		Transmit Enable Channel A
	—	O7		Reserved
	D11	P14.10		I
P14.10		O0	General-purpose output	
GTM_TOUT90		O1	GTM muxed output	
—		O2	Reserved	
—		O3	Reserved	
ASCLIN1_ATX		O4	Transmit output	
IOM_MON2_13			Monitor input 2	
IOM_REF2_13			Reference input 2	
CAN02_TXD		O5	CAN transmit output node 2	
IOM_MON2_7		O6	Monitor input 2	
IOM_REF2_7			Reference input 2	
ERAY0_TXDA		O6	Transmit Channel A	
—		O7	Reserved	

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-7 Port 15 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B20	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI0_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
	A18	P15.1		I
CAN02_RXDA		CAN receive input node 2		
ASCLIN1_ARXA		Receive input		
QSPI2_SLSIB		Slave select input		
SCU_E_REQ7_2		ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)		
P15.1		O0	General-purpose output	
GTM_TOUT72		O1	GTM muxed output	
ASCLIN1_ATX		O2	Transmit output	
IOM_MON2_13			Monitor input 2	
IOM_REF2_13			Reference input 2	
QSPI2_SLSO5		O3	Master slave select output	
—		O4	Reserved	
—		O5	Reserved	
—		O6	Reserved	
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-7 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C19	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	QSPI2_HSICINA			Highspeed capture channel
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12	O3		Reference input 2
	QSPI2_SLSO0			Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved
B17	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	QSPI2_HSICINB			Highspeed capture channel
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12	O3		Reference input 2
	QSPI2_SCLK			Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: LFBGA-292 Package Variant Pin

Table 2-7 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function		
A17	P15.4	I	FAST / PU1 / VEXT / ES	General-purpose input		
	QSPI2_MRSTA			Master SPI data input		
	SCU_E_REQ0_0			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)		
	P15.4			O0	General-purpose output	
	GTM_TOUT75			O1	GTM muxed output	
	ASCLIN1_ATX			O2	Transmit output	
	IOM_MON2_13				Monitor input 2	
	IOM_REF2_13				Reference input 2	
	QSPI2_MRST			O3	Slave SPI data output	
	IOM_MON2_2				Monitor input 2	
	IOM_REF2_2				Reference input 2	
	—			O4	Reserved	
	—			O5	Reserved	
	—			O6	Reserved	
	CCU60_CC62			O7	T12 PWM channel 62	
IOM_MON1_0	Monitor input 1					
IOM_REF1_4	Reference input 1					
E14	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input		
	ASCLIN1_ARXB			Receive input		
	QSPI2_MTSRA			Slave SPI data input		
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)		
	P15.5			O0	General-purpose output	
	GTM_TOUT76			O1	GTM muxed output	
	ASCLIN1_ATX			O2	Transmit output	
	IOM_MON2_13				Monitor input 2	
	IOM_REF2_13				Reference input 2	
	QSPI2_MTSR			O3	Master SPI data output	
	—				O4	Reserved
	—				O5	Reserved
	—			O6	Reserved	
	CCU60_CC61			O7	T12 PWM channel 61	
	IOM_MON1_1				Monitor input 1	
IOM_REF1_5	Reference input 1					

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-7 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A16	P15.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	QSPI2_MTSRB			Slave SPI data input
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15	O3		Reference input 2
	QSPI2_MTSR			Master SPI data output
	—	O4		Reserved
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1
D15	P15.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB	Master SPI data input		
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15	O3		Reference input 2
	QSPI2_MRST			Slave SPI data output
	IOM_MON2_2	O4		Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
CCU60_COUT60	T12 PWM channel 60			
IOM_MON1_3	Monitor input 1			
IOM_REF1_3		Reference input 1		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-7 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D14	P15.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5_0			ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.8	O0	General-purpose output	
	GTM_TOUT79	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI2_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	ASCLIN3_ASCLK	O6	Shift clock output	
	CCU60_COUT61	O7	T12 PWM channel 61	
	IOM_MON1_4		Monitor input 1	
IOM_REF1_2	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-8 Port 20 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H20	P20.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	GTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	CAN03_RXDC			CAN receive input node 3
	CCU_PAD_SYSCCLK			Sysclk input
	CBS_TGI0			Trigger input
	SCU_E_REQ6_0			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T6EUDA			Count direction control input of core timer T6
	P20.0	O0		General-purpose output
	GTM_TOUT59	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	ASCLIN3_ASCLK	O3		Shift clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
CBS_TGO0	O	Trigger output		
G19	P20.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CBS_TGI1			Trigger input
	P20.1	O0		General-purpose output
	GTM_TOUT60	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	CBS_TGO1	O		Trigger output
H19	P20.2	I	S / PU / VEXT	General-purpose input This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			Testmode Enable Input

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G20	P20.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	ASCLIN3_ARXC			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	P20.3	O0		General-purpose output
	GTM_TOUT61	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI0_SLSO9	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
F17	P20.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	P20.6	O0		General-purpose output
	GTM_TOUT62	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F19	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
F20	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5	O6		Monitor input 2
	IOM_REF2_5			Reference input 2
	—			Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8	O7		Monitor input 1
IOM_REF1_13	Reference input 1			

TC33x/TC32x Pin Definition and Functions: LFBGA-292 Package Variant Pin

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
E17	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input	
	CAN03_RXDE			CAN receive input node 3	
	ASCLIN1_ARXC			Receive input	
	QSPIO_SLSIB			Slave select input	
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	P20.9	O0		General-purpose output	
	GTM_TOUT65	O1		GTM muxed output	
	—	O2		Reserved	
	QSPIO_SLSO1	O3		Master slave select output	
	QSPI1_SLSO1	O4		Master slave select output	
	—	O5		Reserved	
	—	O6		Reserved	
	CCU61_CC61	O7		T12 PWM channel 61	
	IOM_MON1_9			Monitor input 1	
IOM_REF1_12	Reference input 1				
E19	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input	
	P20.10			O0	General-purpose output
	GTM_TOUT66			O1	GTM muxed output
	ASCLIN1_ATX			O2	Transmit output
	IOM_MON2_13				Monitor input 2
	IOM_REF2_13				Reference input 2
	QSPIO_SLSO6			O3	Master slave select output
	QSPI2_SLSO7			O4	Master slave select output
	CAN03_TXD			O5	CAN transmit output node 3
	IOM_MON2_8			O6	Monitor input 2
	IOM_REF2_8				Reference input 2
	ASCLIN1_ASCLK			O6	Shift clock output
	CCU61_CC62			O7	T12 PWM channel 62
	IOM_MON1_10				Monitor input 1
IOM_REF1_11	Reference input 1				

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E20	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI0_SCLKA			Slave SPI clock inputs
	P20.11			O0
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
D19	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI0_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13	O2		Monitor input 0
	—			Reserved
	QSPI0_MRST			O3
	IOM_MON2_0	O4		Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR			O4
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-8 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D20	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPIO_SLSO2	O3		Master slave select output
	QSPIO_SLSO2	O4		Master slave select output
	QSPIO_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
C20	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	DMU_FDEST			Enter destructive debug mode
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15			Monitor input 0
	—	O2		Reserved
	QSPIO_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-9 Port 21 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
K17	P21.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	ASCLIN11_ARXC			Receive input
	P21.0	O0		General-purpose output
	GTM_TOUT51	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSM_HSM1	O		Pin Output Value
J17	P21.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	ASCLIN11_ARXD			Receive input
	P21.1	O0		General-purpose output
	GTM_TOUT52	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSM_HSM2	O		Pin Output Value
K19	P21.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	SCU_EMGSTOP_POR T_B			Emergency stop Port Pin B input request
	ASCLIN11_ARXE			Receive input
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-9 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J19	P21.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
K20	P21.4	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	P21.4	O0		General-purpose output
	GTM_TOUT55	O1		GTM muxed output
	ASCLIN11_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
J20	P21.5	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	ASCLIN11_ARXF	O0		Receive input
	P21.5			General-purpose output
	GTM_TOUT56			O1
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN11_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
—	O6	Reserved		
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-9 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H17	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	General-purpose input PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input
	P21.6	O0	General-purpose output	
	GTM_TOUT57	O1	GTM muxed output	
	ASCLIN3_ASLSO	O2	Slave select signal output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T3OUT	O7	External output for overflow/underflow detection of core timer T3	
	CBS_TGO2	O	Trigger output	
DAP3	I/O	DAP: DAP3 Data I/O		

TC33x/TC32x Pin Definition and Functions: LFBGA-292 Package Variant Pin

Table 2-9 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H16	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	P21.7	O0	General-purpose output	
	GTM_TOUT58	O1	GTM muxed output	
	ASCLIN3_ATX	O2	Transmit output	
	IOM_MON2_15		Monitor input 2	
	IOM_REF2_15		Reference input 2	
	ASCLIN3_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T6OUT	O7	External output for overflow/underflow detection of core timer T6	
	CBS_TGO3	O	Trigger output	
	DAP2	I/O	DAP: DAP2 Data I/O	
TDO	O	JTAG Module Data Output		

Table 2-10 Port 22 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
P20	P22.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	ASCLIN6_ARXE			Receive input
	QSPI3_MTSRD			Slave SPI data input
	P22.0	O0	General-purpose output	
	GTM_TOUT47	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI3_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	ASCLIN6_ATX	O7	Transmit output	

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-10 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
P19	P22.1	I	FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1	
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0	
	ASCLIN7_ARXE			Receive input	
	QSPI3_MRSTD			Master SPI data input	
	P22.1			O0	General-purpose output
	GTM_TOUT48			O1	GTM muxed output
	—			O2	Reserved
	QSPI3_MRST			O3	Slave SPI data output
	IOM_MON2_3				Monitor input 2
	IOM_REF2_3	Reference input 2			
	—	O4	Reserved		
	—	O5	Reserved		
	—	O6	Reserved		
ASCLIN7_ATX	O7	Transmit output			
R20	P22.2	I	FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0	
	P22.2			O0	General-purpose output
	GTM_TOUT49			O1	GTM muxed output
	ASCLIN5_ATX			O2	Transmit output
	QSPI3_SLSO12			O3	Master slave select output
	—			O4	Reserved
	—			O5	Reserved
	—			O6	Reserved
	—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-10 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R19	P22.3	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	ASCLIN5_ARXC			Receive input
	QSPI3_SCLKD			Slave SPI clock inputs
	P22.3	O0		General-purpose output
	GTM_TOUT50	O1		GTM muxed output
	—	O2		Reserved
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
P16	P22.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	ASCLIN7_ARXF			Receive input
	P22.4	O0		General-purpose output
	GTM_TOUT130	O1		GTM muxed output
	ASCLIN4_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	QSPI0_SLSO12	O4		Master slave select output
	—	O5		Reserved
	CAN13_TXD	O6		CAN transmit output node 3
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-11 Port 23 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
U19	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	ASCLIN6_ARXF			Receive input
	P23.1	O0		General-purpose output
	GTM_TOUT42	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	—	O3		Reserved
	GTM_CLK0	O4		CGM generated clock
	CAN10_TXD	O5		CAN transmit output node 0
	CCU_EXTCLK0	O6		External Clock 0
ASCLIN6_ASCLK	O7	Shift clock output		
T17	P23.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_7			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_7			Mux input channel 2 of TIM module 0
	P23.5	O0		General-purpose output
	GTM_TOUT46	O1		GTM muxed output
	ASCLIN6_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-12 Port 32 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
W18	P32.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_5			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_5			Mux input channel 5 of TIM module 0
	ASCLIN1_ACTSB			Clear to send input
	P32.4	O0		General-purpose output
	GTM_TOUT40	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	GTM_CLK1	O4		CGM generated clock
	—	O5		Reserved
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
	PMS_DCDCSYNCO	O		DC-DC synchronization output

Table 2-13 Port 33 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
W10	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	IOM_PIN_0			GPIO pad input to FPC
	GTM_DTMT1_2			CDTM1_DTM0
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	IOM_MON0_0			Monitor input 0
	IOM_GTM_0			GTM-provided inputs to EXOR combiner
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y10	P33.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	ASCLIN8_ARXC			Receive input
	IOM_PIN_1			GPIO pad input to FPC
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	IOM_MON0_1			Monitor input 0
	IOM_GTM_1			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASLSO			O2
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
—	O7	Reserved		
W11	P33.2	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	IOM_PIN_2			GPIO pad input to FPC
	P33.2			O0
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK			O2
	QSPI2_SLSO10	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y11	P33.3	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	IOM_PIN_3			GPIO pad input to FPC
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved
W12	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0		General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	IOM_MON0_4			Monitor input 0
	IOM_GTM_4			GTM-provided inputs to EXOR combiner
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
—	O6	Reserved		
CAN13_TXD	O7	CAN transmit output node 3		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
Y12	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input	
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1	
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0	
	GPT120_T4EUDB			Count direction control input of timer T4	
	ASCLIN2_ACTSB			Clear to send input	
	CCU61_CCPOS2C			Hall capture input 2	
	SENT_SENT5C			Receive input channel 5	
	CAN13_RXDB			CAN receive input node 3	
	IOM_PIN_5			GPIO pad input to FPC	
	P33.5			O0	General-purpose output
	GTM_TOUT27	O1	GTM muxed output		
	IOM_MON0_5		Monitor input 0		
	IOM_GTM_5		GTM-provided inputs to EXOR combiner		
	QSPI0_SLSO7	O2	Master slave select output		
	QSPI1_SLSO7	O3	Master slave select output		
	—	O4	Reserved		
	EVADC_EMUX11	O5	Control of external analog multiplexer interface 1		
	—	O6	Reserved		
ASCLIN5_ASLSO	O7	Slave select signal output			
W13	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input	
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1	
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0	
	GPT120_T2EUDB			Count direction control input of timer T2	
	SENT_SENT4C			Receive input channel 4	
	CCU61_CCPOS1C			Hall capture input 1	
	ASCLIN8_ARXD			Receive input	
	IOM_PIN_6			GPIO pad input to FPC	
	P33.6			O0	General-purpose output
	GTM_TOUT28			O1	GTM muxed output
	IOM_MON0_6		Monitor input 0		
	IOM_GTM_6		GTM-provided inputs to EXOR combiner		
	ASCLIN2_ASLSO	O2	Slave select signal output		
	QSPI2_SLSO11	O3	Master slave select output		
	—	O4	Reserved		
	EVADC_EMUX10	O5	Control of external analog multiplexer interface 1		
	—	O6	Reserved		
	—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y13	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7			O0
	GTM_TOUT29	O1	GTM muxed output	
	IOM_MON0_7		Monitor input 0	
	IOM_GTM_7		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	ASCLIN8_ATX	O4	Transmit output	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W14	P33.8	I	FAST / HighZ / VEVR SB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_PORT_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0	General-purpose output	
	GTM_TOUT30	O1	GTM muxed output	
	IOM_MON0_8	O2	Monitor input 0	
	ASCLIN2_ATX		Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14	Reference input 2		
	—	O3	Reserved	
	—	O4	Reserved	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5	O6	Monitor input 2	
	IOM_REF2_5		Reference input 2	
	—		Reserved	
	CCU61_COUT62	O7	T12 PWM channel 62	
	IOM_MON1_13	O	Monitor input 1	
IOM_REF1_8	Reference input 1			
SMU_FSP0		FSP[1..0] Output Signals - Generated by SMU_core		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
Y14	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	QSPI3_HUSICINA			Highspeed capture channel
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0	General-purpose output	
	GTM_TOUT31	O1	GTM muxed output	
	IOM_MON0_9		Monitor input 0	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	—	O3	Reserved	
	ASCLIN2_ASCLK	O4	Shift clock output	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ATX	O6	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	CCU61_CC62	O7	T12 PWM channel 62	
IOM_MON1_10	Monitor input 1			
IOM_REF1_11	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W15	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI3_HSICINB			Highspeed capture channel
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	—	O3		Reserved
	ASCLIN1_ASLSO	O4		Slave select signal output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9		Reference input 1		
SMU_FSP1	O	FSP[1..0] Output Signals - Generated by SMU_core		
Y15	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
IOM_REF1_12		Reference input 1		

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-13 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
W16	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12	O2		Monitor input 0
	ASCLIN1_ATX			Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13	O3		Reference input 2
	—			Reserved
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
IOM_REF1_10	Reference input 1			

Table 2-14 Port 34 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
U11	P34.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	P34.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	CAN00_TXD	O4		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-14 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T12	P34.2	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	P34.2	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1
U12	P34.3	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	P34.3			General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI2_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

Table 2-15 Analog Inputs

Ball	Symbol	Ctrl.	Buffer Type	Function
T10	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
U10	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
W9	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
U9	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-15 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
T9	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G0CH4			Analog input channel 4, group 0
	EVADC_G8CH8			Analog input channel 8, group 8
Y9	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G0CH5			Analog input channel 5, group 0
	EVADC_G8CH9			Analog input channel 9, group 8
T8	AN6	I	D / HighZ / VDDM	Analog Input 6
	EVADC_G0CH6			Analog input channel 6, group 0
	EVADC_G8CH10			Analog input channel 10, group 8
U8	AN7	I	D / HighZ / VDDM	Analog Input 7
	EVADC_G0CH7			Analog input channel 7, group 0
	EVADC_G8CH11			Analog input channel 11, group 8
W8	AN8	I	D / HighZ / VDDM	Analog Input 8
	EVADC_G1CH0			Analog input channel 0, group 1
	EVADC_G8CH12			Analog input channel 12, group 8
U7	AN9	I	D / HighZ / VDDM	Analog Input 9
	EVADC_G1CH1			Analog input channel 1, group 1
	EVADC_G8CH13			Analog input channel 13, group 8
Y8	AN10	I	D / HighZ / VDDM	Analog Input 10
	EVADC_G1CH2			Analog input channel 2, group 1
	EVADC_G8CH14			Analog input channel 14, group 8
W7	AN11	I	D / HighZ / VDDM	Analog Input 11
	EVADC_G1CH3			Analog input channel 3, group 1
	EVADC_G8CH15			Analog input channel 15, group 8
T7	AN12	I	D / HighZ / VDDM	Analog Input 12
	EVADC_G1CH4			Analog input channel 4, group 1
W6	AN13	I	D / HighZ / VDDM	Analog Input 13
	EVADC_G1CH5			Analog input channel 5, group 1
U6	AN14	I	D / HighZ / VDDM	Analog Input 14
	EVADC_G1CH6			Analog input channel 6, group 1
T6	AN15	I	D / HighZ / VDDM	Analog Input 15
	EVADC_G1CH7			Analog input channel 7, group 1
P4	AN32/P40.4	I	S / HighZ / VDDM	Analog Input 32
	SENT_SENT4A			Receive input channel 4
	EVADC_G8CH0			Analog input channel 0, group 8
	CCU60_CCPOS2D			Hall capture input 2

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-15 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
R1	AN33/P40.5	I	S / HighZ / VDDM	Analog Input 33
	SENT_SENT5A			Receive input channel 5
	EVADC_G8CH1			Analog input channel 1, group 8
	CCU61_CCPOS0D			Hall capture input 0
P5	AN34	I	D / HighZ / VDDM	Analog Input 34
	EVADC_G8CH2			Analog input channel 2, group 8
R2	AN35	I	D / HighZ / VDDM	Analog Input 35
	EVADC_G8CH3			Analog input channel 3, group 8
N4	AN36/P40.6	I	S / HighZ / VDDM	Analog Input 36
	SENT_SENT0A			Receive input channel 0
	EVADC_G8CH4			Analog input channel 4, group 8
	CCU61_CCPOS1B			Hall capture input 1
P2	AN37/P40.7	I	S / HighZ / VDDM	Analog Input 37
	SENT_SENT1A			Receive input channel 1
	EVADC_G8CH5			Analog input channel 5, group 8
	CCU61_CCPOS1D			Hall capture input 1
N5	AN38/P40.8	I	S / HighZ / VDDM	Analog Input 38
	SENT_SENT2A			Receive input channel 2
	EVADC_G8CH6			Analog input channel 6, group 8
	CCU61_CCPOS2B			Hall capture input 2
P1	AN39/P40.9	I	S / HighZ / VDDM	Analog Input 39
	SENT_SENT3A			Receive input channel 3
	EVADC_G8CH7			Analog input channel 7, group 8
	CCU61_CCPOS2D			Hall capture input 2

Table 2-16 System I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
W17	VCAP1	I/O	—	External Switch Capacitor
W17	VCAP1	I/O	—	External Switch Capacitor
Y17	VCAP0	I/O	—	External Switch Capacitor
Y17	VCAP0	I/O	—	External Switch Capacitor
M20	XTAL1	I	XTAL / VEXT	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
M19	XTAL2	O	XTAL / VEXT	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
K16	TMS	I	FAST /	JTAG Module State Machine Control Input
	DAP1	I/O	PD2 / VEXT	DAP: DAP1 Data I/O

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-16 System I/O (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L19	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	JTAG Module Reset/Enable Input
J16	TCK	I	FAST /	JTAG Module Clock Input
	DAP0	I	PD2 / VEXT	DAP: DAP0 Clock Input
G16	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		ESR1 pin input
G17	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
F16	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		ESR0 pin input

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-17 Supply

Ball	Symbol	Ctrl.	Buffer Type	Function
Y5	VDDM	I	—	ADC Analog Power Supply (5V / 3.3V)
G9, G10, G11, G12, H9, H10, H11, H12, J7, J8, J10, J11, J13, J14, K7, K8, K9, K10, K11, K12, K13, L7, L8, L9, L10, L11, L12, L13, L14, M7, M8, M10, M11, M13, M14, N9, N10, N11, P9, P10, P11	VSS	I	—	Digital Ground
D16, E15, G8, G13, H7, H14, N7, P8	VDD	I	—	Digital Core Power Supply (1.25V)
A2, B3, V19, W20	VEXT	I	—	External Power Supply (5V / 3.3V)
D5	VFLEX	I	—	Digital Power Supply for Flex Port Pads (5V / 3.3V)
A19, B18	VDDP3	I	—	Flash Power Supply (3.3V)
A20, B2, B19, D4, D17, E5, E16, T16, U17, W19, Y20	VSS	I	—	Digital Ground
Y4	VSSM	I	—	Analog Ground for VDDM
L20	VSS	I	—	Oscillator Ground, VSS(OSC)
N12, P12	VSS	I	—	Digital Ground
Y6	VAREF1	I	—	Positive Analog Reference Voltage 1
Y7	VAGND1	I	—	Negative Analog Reference Voltage 1

TC33x/TC32x Pin Definition and Functions:LFBGA-292 Package Variant Pin

Table 2-17 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6, D7, D8, D10, E4, E6, E8, E9, E10, E11, E12, F4, F5, G4, G5, H4, H5, J5, K14, L4, L5, L16, L17, M1, M2, M4, M5, M16, M17, N1, N2, N16, N17, P17, R4, R5, R16, R17, T1, T2, T4, T5, T13, T14, T15, T19, T20, U1, U2, U5, U13, U14, U15, U16, U20, V1, V2, V20, W1, W2, W3, W4, W5, Y2, Y3, Y16, Y18, Y19	NC	I	—	Not connected. These pins are reserved for future extensions and shall not be connected externally
A1, Y1, U4	NC1	I	—	Not connected. These pins are not connected on package level and will not be used for future extensions
T11	VEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
N19	VDD	I	—	Digital Power Supply for Oscillator (1.25V), VDD(OSC)
N20	VEXT	I	—	Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)
N14, P13	VDDO	I	—	Switch capacitor EVRC Core regulator VDD supply output which shall be connected to other VDD pins externally on PCB level

2.2 LFBGA-180 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP

Table 2-18 Port 00 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
G4	P00.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	CCU61_CTRAPA			Trap input capture
	CCU60_T12HRE			External timer start 12
	P00.0	O0		General-purpose output
	GTM_TOUT9	O1		GTM muxed output
	IOM_REF0_9			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-18 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H4	P00.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CCU60_CC60INB			T12 capture input 60
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	CCU61_CC60INA			T12 capture input 60
	SENT_SENT0B			Receive input channel 0
	EVADC_G9CH11	AI		Analog input channel 11, group 9
	P00.1	O0		General-purpose output
	GTM_TOUT10	O1		GTM muxed output
	IOM_REF0_10			Reference input 0
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC0	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
IOM_MON1_8			Monitor input 1	
IOM_REF1_13			Reference input 1	
F3	P00.2	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SENT_SENT1B			Receive input channel 1
	EVADC_G9CH10	AI		Analog input channel 10, group 9
	P00.2	O0		General-purpose output
	GTM_TOUT11	O1		GTM muxed output
	IOM_REF0_11			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	QSPI3_SL5O4	O6		Master slave select output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-18 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F2	P00.3	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU60_CC61INB			T12 capture input 61
	CAN03_RXDA			CAN receive input node 3
	SENT_SENT2B			Receive input channel 2
	CCU61_CC61INA			T12 capture input 61
	EVADC_G9CH9			Analog input channel 9, group 9
	P00.3	O0	General-purpose output	
	GTM_TOUT12	O1	GTM muxed output	
	IOM_REF0_12		Reference input 0	
	ASCLIN3_ASLSO	O2	Slave select signal output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	SENT_SPC2	O6	Transmit output	
	CCU61_CC61	O7	T12 PWM channel 61	
	IOM_MON1_9		Monitor input 1	
IOM_REF1_12	Reference input 1			
F1	P00.4	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SCU_E_REQ2_2			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT3B			Receive input channel 3
	ASCLIN10_ARXA			Receive input
	EVADC_G9CH8	AI	Analog input channel 8, group 9	
	P00.4	O0	General-purpose output	
	GTM_TOUT13	O1	GTM muxed output	
	IOM_REF0_13		Reference input 0	
	—	O2	Reserved	
	CAN11_TXD	O3	CAN transmit output node 1	
	—	O4	Reserved	
	—	O5	Reserved	
	SENT_SPC3	O6	Transmit output	
	CCU61_COUT61	O7	T12 PWM channel 61	
	IOM_MON1_12		Monitor input 1	
	IOM_REF1_9		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-18 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H3	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU60_CC62INB			T12 capture input 62
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7			AI
	P00.5	O0	General-purpose output	
	GTM_TOUT14	O1	GTM muxed output	
	IOM_REF0_14	O2	Reference input 0	
	—		Reserved	
	QSPI3_SLSO3		O3	Master slave select output
	—		O4	Reserved
	—		O5	Reserved
	SENT_SPC4		O6	Transmit output
	CCU61_CC62		O7	T12 PWM channel 62
	IOM_MON1_10	O7	Monitor input 1	
IOM_REF1_11	Reference input 1			
G3	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI	Analog input channel 6, group 9	
	P00.6	O0	General-purpose output	
	GTM_TOUT15	O1	GTM muxed output	
	IOM_REF0_15	O2	Reference input 0	
	—		Reserved	
	—		Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	EVADC_EMUX10	O5	Control of external analog multiplexer interface 1	
	SENT_SPC5	O6	Transmit output	
	CCU61_COUT62	O7	T12 PWM channel 62	
	IOM_MON1_13	O7	Monitor input 1	
IOM_REF1_8	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-18 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G2	P00.7	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU61_CC60INC			T12 capture input 60
	GPT120_T2INA			Trigger/gate input of timer T2
	CCU61_CCPOS0A			Hall capture input 0
	CCU60_T12HRB			External timer start 12
	GTM_DTMT0_2			CDTM0_DTM0
	EVADC_G9CH5	AI		Analog input channel 5, group 9
	P00.7	O0		General-purpose output
	GTM_TOUT16	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8		Monitor input 1	
IOM_REF1_13	Reference input 1			
G1	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU61_CC61INC			T12 capture input 61
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4	AI		Analog input channel 4, group 9
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9		Monitor input 1	
IOM_REF1_12	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-18 Port 00 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
H2	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	CCU61_CCPOS2A			Hall capture input 2
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3			AI
	P00.9	O0	General-purpose output	
	GTM_TOUT18	O1	GTM muxed output	
	QSPI3_SLSO7	O2	Master slave select output	
	ASCLIN3_ARTS	O3	Ready to send output	
	—	O4	Reserved	
	ASCLIN4_ATX	O5	Transmit output	
	—	O6	Reserved	
	CCU61_CC62	O7	T12 PWM channel 62	
	IOM_MON1_10		Monitor input 1	
	IOM_REF1_11		Reference input 1	
H1	P00.12	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	ASCLIN3_ACTSA			Clear to send input
	ASCLIN4_ARXA			Receive input
	EVADC_G9CH0	AI	Analog input channel 0, group 9	
	P00.12	O0	General-purpose output	
	GTM_TOUT21	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_7		Monitor input 1	
	IOM_REF1_7		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-19 Port 02 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.0	O0	General-purpose output	
	GTM_TOUT0	O1	GTM muxed output	
	IOM_REF0_0		Reference input 0	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI3_SLSO1	O3	Master slave select output	
	—	O4	Reserved	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5		Monitor input 2	
	IOM_REF2_5		Reference input 2	
	ERAY0_TXDA	O6	Transmit Channel A	
	CCU60_CC60	O7	T12 PWM channel 60	
IOM_MON1_2		Monitor input 1		
IOM_REF1_6		Reference input 1		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-19 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C1	P02.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2_1			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.1	O0	General-purpose output	
	GTM_TOUT1	O1	GTM muxed output	
	IOM_REF0_1		Reference input 0	
	—	O2	Reserved	
	QSPI3_SLSO2	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT60	O7	T12 PWM channel 60	
	IOM_MON1_3		Monitor input 1	
	IOM_REF1_3		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-19 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
C2	P02.2	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1	
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0	
	CCU61_CC61INB			T12 capture input 61	
	CCU60_CC61INA			T12 capture input 61	
	P02.2			O0	General-purpose output
	GTM_TOUT2			O1	GTM muxed output
	IOM_REF0_2				Reference input 0
	ASCLIN1_ATX			O2	Transmit output
	IOM_MON2_13				Monitor input 2
	IOM_REF2_13				Reference input 2
	QSPI3_SLSO3			O3	Master slave select output
	—	O4	Reserved		
	CAN02_TXD	O5	CAN transmit output node 2		
	IOM_MON2_7		Monitor input 2		
	IOM_REF2_7		Reference input 2		
	ERAY0_TXDB	O6	Transmit Channel B		
	CCU60_CC61	O7	T12 PWM channel 61		
	IOM_MON1_1		Monitor input 1		
IOM_REF1_5		Reference input 1			
D3	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0	
	ERAY0_RXDB2			Receive Channel B2	
	CAN02_RXDB			CAN receive input node 2	
	ASCLIN1_ARXG			Receive input	
	P02.3			O0	General-purpose output
	GTM_TOUT3			O1	GTM muxed output
	IOM_REF0_3				Reference input 0
	ASCLIN2_ASLSO			O2	Slave select signal output
	QSPI3_SLSO4			O3	Master slave select output
	—			O4	Reserved
	—	O5	Reserved		
	—	O6	Reserved		
	CCU60_COUT61	O7	T12 PWM channel 61		
	IOM_MON1_4		Monitor input 1		
	IOM_REF1_2		Reference input 1		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-19 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
D2	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1	
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0	
	CCU61_CC62INB			T12 capture input 62	
	QSPI3_SLSIA			Slave select input	
	CCU60_CC62INA			T12 capture input 62	
	CAN11_RXDA			CAN receive input node 1	
	P02.4	O0	General-purpose output		
	GTM_TOUT4	O1	GTM muxed output		
	IOM_REF0_4		Reference input 0		
	ASCLIN2_ASCLK	O2	Shift clock output		
	QSPI3_SLSO0	O3	Master slave select output		
	—	O4	Reserved		
	—	O5	Reserved		
	ERAY0_TXENA	O6	Transmit Enable Channel A		
	CCU60_CC62	O7	T12 PWM channel 62		
	IOM_MON1_0		Monitor input 1		
IOM_REF1_4	Reference input 1				
D1	P02.5	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1	
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0	
	QSPI3_MRSTA			Master SPI data input	
	SENT_SENT3C			Receive input channel 3	
	P02.5			O0	General-purpose output
	GTM_TOUT5			O1	GTM muxed output
	IOM_REF0_5		Reference input 0		
	CAN11_TXD	O2	CAN transmit output node 1		
	QSPI3_MRST	O3	Slave SPI data output		
	IOM_MON2_3		Monitor input 2		
	IOM_REF2_3		Reference input 2		
	—	O4	Reserved		
	—	O5	Reserved		
	ERAY0_TXENB	O6	Transmit Enable Channel B		
	CCU60_COUT62	O7	T12 PWM channel 62		
	IOM_MON1_5		Monitor input 1		
IOM_REF1_1	Reference input 1				

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-19 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E1	P02.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	CCU60_CC60INC			T12 capture input 60
	SENT_SENT2C			Receive input channel 2
	GPT120_T3INA			Trigger/gate input of core timer T3
	CCU60_CCPOS0A			Hall capture input 0
	CCU61_T12HRB			External timer start 12
	QSPI3_MTSRA			Slave SPI data input
	P02.6			O0
	GTM_TOUT6	O1	GTM muxed output	
	IOM_REF0_6		Reference input 0	
	—	O2	Reserved	
	QSPI3_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	EVADC_EMUX00	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC60	O7	T12 PWM channel 60	
	IOM_MON1_2		Monitor input 1	
	IOM_REF1_6		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-19 Port 02 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E2	P02.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	CCU60_CC61INC			T12 capture input 61
	SENT_SENT1C			Receive input channel 1
	GPT120_T3EUDA			Count direction control input of core timer T3
	CCU60_CCPOS1A			Hall capture input 1
	QSPI3_SCLKA			Slave SPI clock inputs
	CCU61_T13HRB			External timer start 13
	P02.7			O0
	GTM_TOUT7	O1	GTM muxed output	
	IOM_REF0_7	O2	Reference input 0	
	—		Reserved	
	QSPI3_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	EVADC_EMUX01	O5	Control of external analog multiplexer interface 0	
	SENT_SPC1	O6	Transmit output	
	CCU60_CC61	O7	T12 PWM channel 61	
	IOM_MON1_1		Monitor input 1	
	IOM_REF1_5		Reference input 1	
E3	P02.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CCU60_CC62INC			T12 capture input 62
	SENT_SENT0C			Receive input channel 0
	CCU60_CCPOS2A			Hall capture input 2
	GPT120_T4INA			Trigger/gate input of timer T4
	CCU61_T12HRC			External timer start 12
	CCU61_T13HRC			External timer start 13
	P02.8	O0	General-purpose output	
	GTM_TOUT8	O1	GTM muxed output	
	IOM_REF0_8	O2	Reference input 0	
	QSPI3_SLSO5		Master slave select output	
	ASCLIN8_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	EVADC_EMUX02	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC62	O7	T12 PWM channel 62	
	IOM_MON1_0		Monitor input 1	
IOM_REF1_4	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-20 Port 10 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
B3	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
—	O6		Reserved	
—	O7		Reserved	
A3	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—		O2	
	QSPI1_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
—	O6		Reserved	
—	O7		Reserved	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-20 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A2	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3			O0
	GTM_TOUT105	O1	GTM muxed output	
	IOM_MON2_10	O2	Monitor input 2	
	—		Reserved	
	QSPI1_MTSR		O3	Master SPI data output
	—	O4	Reserved	
	—	O5	Reserved	
	CAN02_TXD	O6	CAN transmit output node 2	
	IOM_MON2_7	O7	Monitor input 2	
	IOM_REF2_7		Reference input 2	
—	Reserved			
B4	P10.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_2			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_2			Mux input channel 6 of TIM module 0
	QSPI1_MTSRC			Slave SPI data input
	CCU60_CCPOS0C			Hall capture input 0
	GPT120_T3INB			Trigger/gate input of core timer T3
	ASCLIN11_ARXB			Receive input
	P10.4	O0	General-purpose output	
	GTM_TOUT106	O1	GTM muxed output	
	IOM_MON2_11	O2	Monitor input 2	
	—		Reserved	
	QSPI1_SLSO8		O3	Master slave select output
	QSPI1_MTSR	O4	Master SPI data output	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-20 Port 10 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F4	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	IOM_REF2_9			Reference input 2
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	ASCLIN2_ASLSO	O6		Slave select signal output
—	O7	Reserved		
E4	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
IOM_MON2_1	Monitor input 2			
IOM_REF2_1	Reference input 2			
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-21 Port 11 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A6	P11.2	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
B6	P11.3	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
C6	P11.6	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-21 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D6	P11.8	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	CAN12_RXDD			CAN receive input node 2
	P11.8	O0		General-purpose output
	GTM_TOUT124	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
A5	P11.9	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-21 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B5	P11.10	I	FAST / PU1 / VFLEX / ES	General-purpose input
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	QSPI1_SLSIA			Slave select input
	P11.10	O0	FAST / PU1 / VFLEX / ES	General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
IOM_REF1_4		Reference input 1		
C5	P11.11	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.11			O0
	GTM_TOUT100	O1	FAST / PU1 / VFLEX / ES	GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-21 Port 11 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A4	P11.12	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13	O3		Reference input 2
	GTM_CLK2			CGM generated clock
	ERAY0_TXDB			Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8	O6		Reference input 2
	CCU_EXTCLK1			External Clock 1
	CCU60_CC60			T12 PWM channel 60
	IOM_MON1_2	O7		Monitor input 1
	IOM_REF1_6			Reference input 1

Table 2-22 Port 13 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A7	P13.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CAN10_TXD	O7		CAN transmit output node 0

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-22 Port 13 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B7	P13.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
A8	P13.2	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	P13.2			O0
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	B8	P13.3		I
P13.3		O0	General-purpose output	
GTM_TOUT94		O1	GTM muxed output	
ASCLIN10_ASLSO		O2	Slave select signal output	
—		O3	Reserved	
—		O4	Reserved	
—		O5	Reserved	
—		O6	Reserved	
—		O7	Reserved	

Table 2-23 Port 14 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A9	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ASCLK	O6		Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5		Monitor input 1	
	IOM_REF1_1		Reference input 1	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-23 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B10	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1			O0
	GTM_TOUT81	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_6		Monitor input 1	
IOM_REF1_0	Reference input 1			
D9	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2			O0
	GTM_TOUT82	O1	GTM muxed output	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI2_SLSO1	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	ASCLIN2_ASCLK	O6	Shift clock output	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-23 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C11	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0		General-purpose output
	GTM_TOUT83	O1		GTM muxed output
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI2_SLSO3	O3		Master slave select output
	ASCLIN1_ASLSO	O4		Slave select signal output
	ASCLIN3_ASLSO	O5		Slave select signal output
	—	O6		Reserved
	—	O7		Reserved
C10	P14.4	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	PMS_HWCFG6IN			HWCFG6 pin input
	GTM_DTMT0_0			CDTM0_DTM0
	P14.4	O0		General-purpose output
	GTM_TOUT84	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-23 Port 14 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B9	P14.5	I	FAST / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0		General-purpose output
	GTM_TOUT85	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	—	O7		Reserved
C9	P14.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	P14.6			O0
	GTM_TOUT86	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SLSO2	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-24 Port 15 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
A13	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13	O3		Reference input 2
	QSPI0_SLSO13			Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7	O6		Reference input 2
	ASCLIN1_ASCLK			Shift clock output
	—	O7		Reserved
	A12	P15.1		I
CAN02_RXDA		CAN receive input node 2		
ASCLIN1_ARXA		Receive input		
QSPI2_SLSIB		Slave select input		
SCU_E_REQ7_2		ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)		
P15.1		O0	General-purpose output	
GTM_TOUT72		O1	GTM muxed output	
ASCLIN1_ATX		O2	Transmit output	
IOM_MON2_13			Monitor input 2	
IOM_REF2_13		O3	Reference input 2	
QSPI2_SLSO5			Master slave select output	
—		O4	Reserved	
—		O5	Reserved	
—		O6	Reserved	
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-24 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B12	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	QSPI2_HSICINA			Highspeed capture channel
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12	O3		Reference input 2
	QSPI2_SLSO0			Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved
A10	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	QSPI2_HSICINB			Highspeed capture channel
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12	O3		Reference input 2
	QSPI2_SCLK			Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-24 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B11	P15.4	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI2_MRSTA			Master SPI data input
	SCU_E_REQ0_0			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.4	O0		General-purpose output
	GTM_TOUT75	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
IOM_MON1_0	Monitor input 1			
IOM_REF1_4	Reference input 1			
D10	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	ASCLIN1_ARXB			Receive input
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
IOM_REF1_5	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-24 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
A11	P15.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0
	QSPI2_MTSRB			Slave SPI data input
	P15.6	O0		General-purpose output
	GTM_TOUT77	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	QSPI2_SCLK	O5		Master SPI clock output
	ASCLIN3_ASCLK	O6		Shift clock output
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
IOM_REF1_6	Reference input 1			
D8	P15.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_5			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_5			Mux input channel 1 of TIM module 0
	ASCLIN3_ARXA			Receive input
	QSPI2_MRSTB	Master SPI data input		
	P15.7	O0		General-purpose output
	GTM_TOUT78	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI2_MRST	O3		Slave SPI data output
	IOM_MON2_2			Monitor input 2
	IOM_REF2_2			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
IOM_MON1_3	Monitor input 1			
IOM_REF1_3	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-24 Port 15 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D7	P15.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5_0			ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.8	O0	General-purpose output	
	GTM_TOUT79	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI2_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	ASCLIN3_ASCLK	O6	Shift clock output	
	CCU60_COUT61	O7	T12 PWM channel 61	
	IOM_MON1_4		Monitor input 1	
IOM_REF1_2	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-25 Port 20 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H13	P20.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	GTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	CAN03_RXDC			CAN receive input node 3
	CCU_PAD_SYSClk			Sysclk input
	CBS_TGI0			Trigger input
	SCU_E_REQ6_0			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T6EUDA			Count direction control input of core timer T6
	P20.0			O0
	GTM_TOUT59	O1	GTM muxed output	
	ASCLIN3_ATX	O2	Transmit output	
	IOM_MON2_15		Monitor input 2	
	IOM_REF2_15	O3	Reference input 2	
	ASCLIN3_ASCLK		Shift clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	
CBS_TGO0	O	Trigger output		
G13	P20.2	I	S / PU / VEXT	General-purpose input This pin is latched at power on reset release to enter test mode.
	TESTMODE			Testmode Enable Input

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-25 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
G12	P20.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	ASCLIN3_ARXC			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	P20.3	O0		General-purpose output
	GTM_TOUT61	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI0_SLSO9	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
	—	O7		Reserved
F11	P20.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	P20.6	O0		General-purpose output
	GTM_TOUT62	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-25 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
E12	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
F12	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
IOM_REF1_13	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-25 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
D12	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input	
	CAN03_RXDE			CAN receive input node 3	
	ASCLIN1_ARXC			Receive input	
	QSPIO_SLSIB			Slave select input	
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	P20.9	O0		General-purpose output	
	GTM_TOUT65	O1		GTM muxed output	
	—	O2		Reserved	
	QSPIO_SLSO1	O3		Master slave select output	
	QSPI1_SLSO1	O4		Master slave select output	
	—	O5		Reserved	
	—	O6		Reserved	
	CCU61_CC61	O7		T12 PWM channel 61	
	IOM_MON1_9			Monitor input 1	
IOM_REF1_12	Reference input 1				
C14	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input	
	P20.10			O0	General-purpose output
	GTM_TOUT66			O1	GTM muxed output
	ASCLIN1_ATX			O2	Transmit output
	IOM_MON2_13				Monitor input 2
	IOM_REF2_13				Reference input 2
	QSPIO_SLSO6			O3	Master slave select output
	QSPI2_SLSO7			O4	Master slave select output
	CAN03_TXD			O5	CAN transmit output node 3
	IOM_MON2_8			O6	Monitor input 2
	IOM_REF2_8				Reference input 2
	ASCLIN1_ASCLK			O6	Shift clock output
	CCU61_CC62			O7	T12 PWM channel 62
	IOM_MON1_10				Monitor input 1
IOM_REF1_11	Reference input 1				

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-25 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
D14	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI0_SCLKA			Slave SPI clock inputs
	P20.11			O0
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
D13	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI0_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13	O2		Monitor input 0
	—			Reserved
	QSPI0_MRST			O3
	IOM_MON2_0	O4		Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR			O4
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-25 Port 20 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
C13	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPIO_SLSO2	O3		Master slave select output
	QSPIO_SLSO2	O4		Master slave select output
	QSPIO_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
B14	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	DMU_FDEST			Enter destructive debug mode
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15			Monitor input 0
	—	O2		Reserved
	QSPIO_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-26 Port 21 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
H12	P21.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	ASCLIN11_ARXC			Receive input
	P21.0	O0		General-purpose output
	GTM_TOUT51	O1		GTM muxed output
	ASCLIN11_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
	HSM_HSM1	O		Pin Output Value
K13	P21.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	SCU_EMGSTOP_POR T_B			Emergency stop Port Pin B input request
	ASCLIN11_ARXE			Receive input
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
—	O5	Reserved		
—	O6	Reserved		
—	O7	Reserved		
J14	P21.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-26 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J13	P21.4	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	P21.4	O0		General-purpose output
	GTM_TOUT55	O1		GTM muxed output
	ASCLIN11_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
H14	P21.5	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0
	ASCLIN11_ARXF			Receive input
	P21.5	O0		General-purpose output
	GTM_TOUT56	O1		GTM muxed output
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN11_ATX	O3		Transmit output
	—	O4		Reserved
	—	O5		Reserved
—	O6	Reserved		
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-26 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F13	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	General-purpose input PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input
	P21.6	O0	General-purpose output	
	GTM_TOUT57	O1	GTM muxed output	
	ASCLIN3_ASLSO	O2	Slave select signal output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T3OUT	O7	External output for overflow/underflow detection of core timer T3	
	CBS_TGO2	O	Trigger output	
DAP3	I/O	DAP: DAP3 Data I/O		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-26 Port 21 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
F14	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	P21.7	O0	General-purpose output	
	GTM_TOUT58	O1	GTM muxed output	
	ASCLIN3_ATX	O2	Transmit output	
	IOM_MON2_15		Monitor input 2	
	IOM_REF2_15		Reference input 2	
	ASCLIN3_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T6OUT	O7	External output for overflow/underflow detection of core timer T6	
	CBS_TGO3	O	Trigger output	
	DAP2	I/O	DAP: DAP2 Data I/O	
TDO	O	JTAG Module Data Output		

Table 2-27 Port 22 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
J11	P22.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	ASCLIN6_ARXE			Receive input
	QSPI3_MTSRD			Slave SPI data input
	P22.0	O0	General-purpose output	
	GTM_TOUT47	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI3_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	ASCLIN6_ATX	O7	Transmit output	

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-27 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function	
L12	P22.1	I	FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1	
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0	
	ASCLIN7_ARXE			Receive input	
	QSPI3_MRSTD			Master SPI data input	
	P22.1			O0	General-purpose output
	GTM_TOUT48			O1	GTM muxed output
	—			O2	Reserved
	QSPI3_MRST			O3	Slave SPI data output
	IOM_MON2_3				Monitor input 2
	IOM_REF2_3				Reference input 2
	—			O4	Reserved
	—			O5	Reserved
	—			O6	Reserved
ASCLIN7_ATX	O7	Transmit output			
H11	P22.2	I	FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0	
	P22.2			O0	General-purpose output
	GTM_TOUT49			O1	GTM muxed output
	ASCLIN5_ATX			O2	Transmit output
	QSPI3_SLSO12			O3	Master slave select output
	—			O4	Reserved
	—			O5	Reserved
	—			O6	Reserved
	—			O7	Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-27 Port 22 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
J12	P22.3	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	ASCLIN5_ARXC			Receive input
	QSPI3_SCLKD			Slave SPI clock inputs
	P22.3	O0		General-purpose output
	GTM_TOUT50	O1		GTM muxed output
	—	O2		Reserved
	QSPI3_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

Table 2-28 Port 23 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
N14	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	ASCLIN6_ARXF			Receive input
	P23.1	O0		General-purpose output
	GTM_TOUT42	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	—	O3		Reserved
	GTM_CLK0	O4		CGM generated clock
	CAN10_TXD	O5		CAN transmit output node 0
	CCU_EXTCLK0	O6		External Clock 0
	ASCLIN6_ASCLK	O7		Shift clock output

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-29 Port 33 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function	
M9	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input	
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1	
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0	
	IOM_PIN_0			GPIO pad input to FPC	
	GTM_DTMT1_2			CDTM1_DTM0	
	P33.0			O0	General-purpose output
	GTM_TOUT22			O1	GTM muxed output
	IOM_MON0_0				Monitor input 0
	IOM_GTM_0				GTM-provided inputs to EXOR combiner
	ASCLIN5_ATX			O2	Transmit output
	—	O3	Reserved		
	—	O4	Reserved		
	—	O5	Reserved		
	—	O6	Reserved		
—	O7	Reserved			
M8	P33.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input	
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1	
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0	
	ASCLIN8_ARXC			Receive input	
	IOM_PIN_1			GPIO pad input to FPC	
	P33.1			O0	General-purpose output
	GTM_TOUT23			O1	GTM muxed output
	IOM_MON0_1				Monitor input 0
	IOM_GTM_1				GTM-provided inputs to EXOR combiner
	ASCLIN3_ASLSO			O2	Slave select signal output
	QSPI2_SCLK	O3	Master SPI clock output		
	—	O4	Reserved		
	EVADC_EMUX02	O5	Control of external analog multiplexer interface 0		
	—	O6	Reserved		
—	O7	Reserved			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-29 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P8	P33.2	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	IOM_PIN_2			GPIO pad input to FPC
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved
N8	P33.3	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	IOM_PIN_3			GPIO pad input to FPC
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-29 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L8	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0	General-purpose output	
	GTM_TOUT26	O1	GTM muxed output	
	IOM_MON0_4		Monitor input 0	
	IOM_GTM_4		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ARTS		O2	Ready to send output
	QSPI2_SLSO12	O3	Master slave select output	
	—	O4	Reserved	
	EVADC_EMUX12	O5	Control of external analog multiplexer interface 1	
	—	O6	Reserved	
	CAN13_TXD	O7	CAN transmit output node 3	
N9	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	GPT120_T4EUDB			Count direction control input of timer T4
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	P33.5	O0	General-purpose output	
	GTM_TOUT27	O1	GTM muxed output	
	IOM_MON0_5		Monitor input 0	
	IOM_GTM_5		GTM-provided inputs to EXOR combiner	
	QSPI0_SLSO7		O2	Master slave select output
	QSPI1_SLSO7	O3	Master slave select output	
	—	O4	Reserved	
EVADC_EMUX11	O5	Control of external analog multiplexer interface 1		
—	O6	Reserved		
ASCLIN5_ASLSO	O7	Slave select signal output		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-29 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P9	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	GPT120_T2EUDB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	P33.6	O0	General-purpose output	
	GTM_TOUT28	O1	GTM muxed output	
	IOM_MON0_6		Monitor input 0	
	IOM_GTM_6		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ASLSO	O2	Slave select signal output	
	QSPI2_SLSO11	O3	Master slave select output	
	—	O4	Reserved	
	EVADC_EMUX10	O5	Control of external analog multiplexer interface 1	
	—	O6	Reserved	
—	O7	Reserved		
L10	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7	O0	General-purpose output	
	GTM_TOUT29	O1	GTM muxed output	
	IOM_MON0_7		Monitor input 0	
	IOM_GTM_7		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	ASCLIN8_ATX	O4	Transmit output	
	—	O5	Reserved	
	—	O6	Reserved	
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-29 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
L9	P33.8	I	FAST / HighZ / VEVR SB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_PORT_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0	General-purpose output	
	GTM_TOUT30	O1	GTM muxed output	
	IOM_MON0_8	O2	Monitor input 0	
	ASCLIN2_ATX		Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14	Reference input 2		
	—	O3	Reserved	
	—	O4	Reserved	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5	O6	Monitor input 2	
	IOM_REF2_5		Reference input 2	
	—		Reserved	
	CCU61_COUT62	O7	T12 PWM channel 62	
	IOM_MON1_13	O	Monitor input 1	
IOM_REF1_8	Reference input 1			
SMU_FSP0	O	FSP[1..0] Output Signals - Generated by SMU_core		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-29 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
P10	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	QSPI3_HUSICINA			Highspeed capture channel
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0	General-purpose output	
	GTM_TOUT31	O1	GTM muxed output	
	IOM_MON0_9		Monitor input 0	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	—	O3	Reserved	
	ASCLIN2_ASCLK	O4	Shift clock output	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ATX	O6	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	CCU61_CC62	O7	T12 PWM channel 62	
IOM_MON1_10	Monitor input 1			
IOM_REF1_11	Reference input 1			

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-29 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N11	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI3_HSICINB			Highspeed capture channel
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0		General-purpose output
	GTM_TOUT32	O1		GTM muxed output
	IOM_MON0_10			Monitor input 0
	QSPI1_SLSO6	O2		Master slave select output
	—	O3		Reserved
	ASCLIN1_ASLSO	O4		Slave select signal output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9		Reference input 1		
SMU_FSP1	O	FSP[1..0] Output Signals - Generated by SMU_core		
N10	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0		General-purpose output
	GTM_TOUT33	O1		GTM muxed output
	IOM_MON0_11			Monitor input 0
	ASCLIN1_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
IOM_REF1_12		Reference input 1		

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-29 Port 33 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
M10	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12	O2		Monitor input 0
	ASCLIN1_ATX			Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13	O3		Reference input 2
	—			Reserved
	ASCLIN1_ASCLK			O4
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
IOM_MON1_11	Monitor input 1			
IOM_REF1_10	Reference input 1			

Table 2-30 Port 34 Functions

Ball	Symbol	Ctrl.	Buffer Type	Function
M7	P34.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	P34.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	CAN00_TXD	O4		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-30 Port 34 Functions (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N7	P34.2	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	P34.2	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1
P7	P34.3	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	P34.3			General-purpose output
	—	O1		Reserved
	ASCLIN4_ASCLK	O2		Shift clock output
	—	O3		Reserved
	QSPI2_SLSO10	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

Table 2-31 Analog Inputs

Ball	Symbol	Ctrl.	Buffer Type	Function
L7	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
P6	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
L6	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
M6	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-31 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
N6	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G0CH4			Analog input channel 4, group 0
	EVADC_G8CH8			Analog input channel 8, group 8
L5	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G0CH5			Analog input channel 5, group 0
	EVADC_G8CH9			Analog input channel 9, group 8
M5	AN6	I	D / HighZ / VDDM	Analog Input 6
	EVADC_G0CH6			Analog input channel 6, group 0
	EVADC_G8CH10			Analog input channel 10, group 8
P5	AN7	I	D / HighZ / VDDM	Analog Input 7
	EVADC_G0CH7			Analog input channel 7, group 0
	EVADC_G8CH11			Analog input channel 11, group 8
N5	AN8	I	D / HighZ / VDDM	Analog Input 8
	EVADC_G1CH0			Analog input channel 0, group 1
	EVADC_G8CH12			Analog input channel 12, group 8
N3	AN9	I	D / HighZ / VDDM	Analog Input 9
	EVADC_G1CH1			Analog input channel 1, group 1
	EVADC_G8CH13			Analog input channel 13, group 8
M4	AN10	I	D / HighZ / VDDM	Analog Input 10
	EVADC_G1CH2			Analog input channel 2, group 1
	EVADC_G8CH14			Analog input channel 14, group 8
N4	AN11	I	D / HighZ / VDDM	Analog Input 11
	EVADC_G1CH3			Analog input channel 3, group 1
	EVADC_G8CH15			Analog input channel 15, group 8
M3	AN12	I	D / HighZ / VDDM	Analog Input 12
	EVADC_G1CH4			Analog input channel 4, group 1
N2	AN13	I	D / HighZ / VDDM	Analog Input 13
	EVADC_G1CH5			Analog input channel 5, group 1
L4	AN14	I	D / HighZ / VDDM	Analog Input 14
	EVADC_G1CH6			Analog input channel 6, group 1
N1	AN15	I	D / HighZ / VDDM	Analog Input 15
	EVADC_G1CH7			Analog input channel 7, group 1
K1	AN32/P40.4	I	S / HighZ / VDDM	Analog Input 32
	SENT_SENT4A			Receive input channel 4
	EVADC_G8CH0			Analog input channel 0, group 8
	CCU60_CCPOS2D			Hall capture input 2

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-31 Analog Inputs (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K2	AN33/P40.5	I	S / HighZ / VDDM	Analog Input 33
	SENT_SENT5A			Receive input channel 5
	EVADC_G8CH1			Analog input channel 1, group 8
	CCU61_CCPOS0D			Hall capture input 0
K3	AN34	I	D / HighZ / VDDM	Analog Input 34
	EVADC_G8CH2			Analog input channel 2, group 8
K4	AN35	I	D / HighZ / VDDM	Analog Input 35
	EVADC_G8CH3			Analog input channel 3, group 8
J1	AN36/P40.6	I	S / HighZ / VDDM	Analog Input 36
	SENT_SENT0A			Receive input channel 0
	EVADC_G8CH4			Analog input channel 4, group 8
	CCU61_CCPOS1B			Hall capture input 1
J2	AN37/P40.7	I	S / HighZ / VDDM	Analog Input 37
	SENT_SENT1A			Receive input channel 1
	EVADC_G8CH5			Analog input channel 5, group 8
	CCU61_CCPOS1D			Hall capture input 1
J3	AN38/P40.8	I	S / HighZ / VDDM	Analog Input 38
	SENT_SENT2A			Receive input channel 2
	EVADC_G8CH6			Analog input channel 6, group 8
	CCU61_CCPOS2B			Hall capture input 2
J4	AN39/P40.9	I	S / HighZ / VDDM	Analog Input 39
	SENT_SENT3A			Receive input channel 3
	EVADC_G8CH7			Analog input channel 7, group 8
	CCU61_CCPOS2D			Hall capture input 2

Table 2-32 System I/O

Ball	Symbol	Ctrl.	Buffer Type	Function
N12	VCAP1	I/O	—	External Switch Capacitor
N12	VCAP1	I/O	—	External Switch Capacitor
P12	VCAP0	I/O	—	External Switch Capacitor
P12	VCAP0	I/O	—	External Switch Capacitor
L14	XTAL1	I	XTAL / VEXT	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
L13	XTAL2	O	XTAL / VEXT	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
G11	TMS	I	FAST /	JTAG Module State Machine Control Input
	DAP1	I/O	PD2 / VEXT	DAP: DAP1 Data I/O

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-32 System I/O (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
K12	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	JTAG Module Reset/Enable Input
G14	TCK	I	FAST /	JTAG Module Clock Input
	DAP0	I	PD2 / VEXT	DAP: DAP0 Clock Input
E11	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		ESR1 pin input
E13	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
E14	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		ESR0 pin input

Table 2-33 Supply

Ball	Symbol	Ctrl.	Buffer Type	Function
P3	VDDM	I	—	ADC Analog Power Supply (5V / 3.3V)
B13, C12, D11, E10, G7, G8, H7, H8, J6, K5	VSS	I	—	Digital Ground
F9, G9, H6, J7	VDD	I	—	Digital Core Power Supply (1.25V)
F6, F8, G6, J9, P11	VEXT	I	—	External Power Supply (5V / 3.3V)
D5	VFLEX	I	—	Digital Power Supply for Flex Port Pads (5V / 3.3V)
F7	VDDP3	I	—	Flash Power Supply (3.3V)

TC33x/TC32x Pin Definition and Functions:LFBGA-180 Package Variant Pin

Table 2-33 Supply (cont'd)

Ball	Symbol	Ctrl.	Buffer Type	Function
B2, C3, D4, E5, K10, L11, M12	VSS	I	—	Digital Ground
K14	VSS	I	—	Oscillator Ground, VSS(OSC)
N13	VSS	I	—	Digital Ground
P4	VAREF1	I	—	Positive Analog Reference Voltage 1
A1, A14, C4, C7, C8, K11, L1, L2, L3, M1, M2, M11, P1, P13, P14	NC	I	—	Not connected. These pins are reserved for future extensions and shall not be connected externally
H9	VEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
M13	VDD	I	—	Digital Power Supply for Oscillator (1.25V), VDD(OSC)
M14	VEXT	I	—	Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)
J8	VDDO	I	—	Switch capacitor EVRC Core regulator VDD supply output which shall be connected to other VDD pins externally on PCB level
P2	VSSM/VAGND1	I	—	Analog Ground for VDDM / Negative Analog Reference Voltage 1

2.3 TQFP-144 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP

Note: In the following QFP package the VFLEX supply is internally connected to VEXT supply and thus does not show up in the corresponding package drawings neither supply tables as a dedicated pin.

Table 2-34 Port 00 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function	
11	P00.0	I	FAST / PU1 / VEXT / ES	General-purpose input	
	CCU61_CTRAPA			Trap input capture	
	CCU60_T12HRE			External timer start 12	
	P00.0	O0		General-purpose output	
	GTM_TOUT9	O1		GTM muxed output	
	IOM_REF0_9			Reference input 0	
	ASCLIN3_ASCLK			O2	Shift clock output
	ASCLIN3_ATX			O3	Transmit output
	IOM_MON2_15			Monitor input 2	
	IOM_REF2_15			Reference input 2	
	—	O4		Reserved	
	CAN10_TXD	O5		CAN transmit output node 0	
	—	O6		Reserved	
	CCU60_COUT63	O7		T13 PWM channel 63	
	IOM_MON1_6			Monitor input 1	
IOM_REF1_0	Reference input 1				

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-34 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
12	P00.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CCU60_CC60INB			T12 capture input 60
	ASCLIN3_ARXE			Receive input
	CAN10_RXDA			CAN receive input node 0
	CCU61_CC60INA			T12 capture input 60
	SENT_SENT0B			Receive input channel 0
	EVADC_G9CH11	AI		Analog input channel 11, group 9
	P00.1	O0		General-purpose output
	GTM_TOUT10	O1		GTM muxed output
	IOM_REF0_10			Reference input 0
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC0	O6		Transmit output
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
IOM_REF1_13			Reference input 1	
13	P00.2	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SENT_SENT1B			Receive input channel 1
	EVADC_G9CH10	AI		Analog input channel 10, group 9
	P00.2	O0		General-purpose output
	GTM_TOUT11	O1		GTM muxed output
	IOM_REF0_11			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	QSPI3_SL5O4	O6		Master slave select output
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-34 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
14	P00.3	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU60_CC61INB			T12 capture input 61
	CAN03_RXDA			CAN receive input node 3
	SENT_SENT2B			Receive input channel 2
	CCU61_CC61INA			T12 capture input 61
	EVADC_G9CH9	AI		Analog input channel 9, group 9
	P00.3	O0		General-purpose output
	GTM_TOUT12	O1		GTM muxed output
	IOM_REF0_12			Reference input 0
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC2	O6		Transmit output
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9		Monitor input 1	
IOM_REF1_12	Reference input 1			
15	P00.4	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SCU_E_REQ2_2			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	SENT_SENT3B			Receive input channel 3
	ASCLIN10_ARXA			Receive input
	EVADC_G9CH8	AI		Analog input channel 8, group 9
	P00.4	O0		General-purpose output
	GTM_TOUT13	O1		GTM muxed output
	IOM_REF0_13			Reference input 0
	—	O2		Reserved
	CAN11_TXD	O3		CAN transmit output node 1
	—	O4		Reserved
	—	O5		Reserved
	SENT_SPC3	O6		Transmit output
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12		Monitor input 1	
	IOM_REF1_9		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-34 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
16	P00.5	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU60_CC62INB			T12 capture input 62
	CCU61_CC62INA			T12 capture input 62
	SENT_SENT4B			Receive input channel 4
	CAN11_RXDB			CAN receive input node 1
	GTM_DTMT1_1			CDTM1_DTM0
	EVADC_G9CH7	AI	Analog input channel 7, group 9	
	P00.5	O0	General-purpose output	
	GTM_TOUT14	O1	GTM muxed output	
	IOM_REF0_14	O2	Reference input 0	
	—		Reserved	
	QSPI3_SLSO3	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	SENT_SPC4	O6	Transmit output	
	CCU61_CC62	O7	T12 PWM channel 62	
	IOM_MON1_10		Monitor input 1	
IOM_REF1_11	Reference input 1			
17	P00.6	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	SENT_SENT5B			Receive input channel 5
	ASCLIN5_ARXA			Receive input
	EVADC_G9CH6	AI	Analog input channel 6, group 9	
	P00.6	O0	General-purpose output	
	GTM_TOUT15	O1	GTM muxed output	
	IOM_REF0_15	O2	Reference input 0	
	—		Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	EVADC_EMUX10	O5	Control of external analog multiplexer interface 1	
	SENT_SPC5	O6	Transmit output	
	CCU61_COUT62	O7	T12 PWM channel 62	
	IOM_MON1_13		Monitor input 1	
IOM_REF1_8	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-34 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
18	P00.7	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU61_CC60INC			T12 capture input 60
	GPT120_T2INA			Trigger/gate input of timer T2
	CCU61_CCPOS0A			Hall capture input 0
	CCU60_T12HRB			External timer start 12
	GTM_DTMT0_2			CDTM0_DTM0
	EVADC_G9CH5	AI		Analog input channel 5, group 9
	P00.7	O0		General-purpose output
	GTM_TOUT16	O1		GTM muxed output
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8		Monitor input 1	
IOM_REF1_13	Reference input 1			
19	P00.8	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	CCU61_CC61INC			T12 capture input 61
	GPT120_T2EUDA			Count direction control input of timer T2
	CCU61_CCPOS1A			Hall capture input 1
	CCU60_T13HRB			External timer start 13
	ASCLIN10_ARXB			Receive input
	EVADC_G9CH4	AI		Analog input channel 4, group 9
	P00.8	O0		General-purpose output
	GTM_TOUT17	O1		GTM muxed output
	QSPI3_SLSO6	O2		Master slave select output
	ASCLIN10_ATX	O3		Transmit output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9		Monitor input 1	
IOM_REF1_12	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-34 Port 00 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
20	P00.9	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN0_1			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_1			Mux input channel 0 of TIM module 0
	CCU61_CC62INC			T12 capture input 62
	CCU61_CCPOS2A			Hall capture input 2
	GPT120_T4EUDA			Count direction control input of timer T4
	CCU60_T13HRC			External timer start 13
	CCU60_T12HRC			External timer start 12
	EVADC_G9CH3			AI
	P00.9	O0	General-purpose output	
	GTM_TOUT18	O1	GTM muxed output	
	QSPI3_SLSO7	O2	Master slave select output	
	ASCLIN3_ARTS	O3	Ready to send output	
	—	O4	Reserved	
	ASCLIN4_ATX	O5	Transmit output	
	—	O6	Reserved	
	CCU61_CC62	O7	T12 PWM channel 62	
	IOM_MON1_10		Monitor input 1	
	IOM_REF1_11		Reference input 1	
21	P00.12	I	SLOW / PU1 / VEXT / ES1	General-purpose input
	GTM_TIM1_IN3_1			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_1			Mux input channel 3 of TIM module 0
	ASCLIN3_ACTSA			Clear to send input
	ASCLIN4_ARXA			Receive input
	EVADC_G9CH0	AI	Analog input channel 0, group 9	
	P00.12	O0	General-purpose output	
	GTM_TOUT21	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_7		Monitor input 1	
	IOM_REF1_7		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-35 Port 02 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.0	O0	General-purpose output	
	GTM_TOUT0	O1	GTM muxed output	
	IOM_REF0_0		Reference input 0	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI3_SLSO1	O3	Master slave select output	
	—	O4	Reserved	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5		Monitor input 2	
	IOM_REF2_5		Reference input 2	
	ERAY0_TXDA	O6	Transmit Channel A	
	CCU60_CC60	O7	T12 PWM channel 60	
	IOM_MON1_2		Monitor input 1	
IOM_REF1_6		Reference input 1		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-35 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2_1			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.1	O0	General-purpose output	
	GTM_TOUT1	O1	GTM muxed output	
	IOM_REF0_1		Reference input 0	
	—	O2	Reserved	
	QSPI3_SLSO2	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT60	O7	T12 PWM channel 60	
IOM_MON1_3		Monitor input 1		
IOM_REF1_3		Reference input 1		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-35 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
3	P02.2	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1	
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0	
	CCU61_CC61INB			T12 capture input 61	
	CCU60_CC61INA			T12 capture input 61	
	P02.2			O0	General-purpose output
	GTM_TOUT2			O1	GTM muxed output
	IOM_REF0_2				Reference input 0
	ASCLIN1_ATX			O2	Transmit output
	IOM_MON2_13				Monitor input 2
	IOM_REF2_13				Reference input 2
	QSPI3_SLSO3			O3	Master slave select output
	—	O4	Reserved		
	CAN02_TXD	O5	CAN transmit output node 2		
	IOM_MON2_7		Monitor input 2		
	IOM_REF2_7		Reference input 2		
	ERAY0_TXDB	O6	Transmit Channel B		
	CCU60_CC61	O7	T12 PWM channel 61		
	IOM_MON1_1		Monitor input 1		
IOM_REF1_5		Reference input 1			
4	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0	
	ERAY0_RXDB2			Receive Channel B2	
	CAN02_RXDB			CAN receive input node 2	
	ASCLIN1_ARXG				Receive input
	P02.3			O0	General-purpose output
	GTM_TOUT3			O1	GTM muxed output
	IOM_REF0_3				Reference input 0
	ASCLIN2_ASLSO			O2	Slave select signal output
	QSPI3_SLSO4			O3	Master slave select output
	—			O4	Reserved
	—	O5	Reserved		
	—	O6	Reserved		
	CCU60_COUT61	O7	T12 PWM channel 61		
	IOM_MON1_4		Monitor input 1		
	IOM_REF1_2		Reference input 1		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-35 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
5	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1	
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0	
	CCU61_CC62INB			T12 capture input 62	
	QSPI3_SLSIA			Slave select input	
	CCU60_CC62INA			T12 capture input 62	
	CAN11_RXDA			CAN receive input node 1	
	P02.4			O0	General-purpose output
	GTM_TOUT4			O1	GTM muxed output
	IOM_REF0_4				Reference input 0
	ASCLIN2_ASCLK	O2	Shift clock output		
	QSPI3_SLSO0	O3	Master slave select output		
	—	O4	Reserved		
	—	O5	Reserved		
	ERAY0_TXENA	O6	Transmit Enable Channel A		
	CCU60_CC62	O7	T12 PWM channel 62		
	IOM_MON1_0		Monitor input 1		
IOM_REF1_4		Reference input 1			
6	P02.5	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1	
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0	
	QSPI3_MRSTA			Master SPI data input	
	SENT_SENT3C			Receive input channel 3	
	P02.5			O0	General-purpose output
	GTM_TOUT5			O1	GTM muxed output
	IOM_REF0_5				Reference input 0
	CAN11_TXD			O2	CAN transmit output node 1
	QSPI3_MRST			O3	Slave SPI data output
	IOM_MON2_3		Monitor input 2		
	IOM_REF2_3		Reference input 2		
	—	O4	Reserved		
	—	O5	Reserved		
	ERAY0_TXENB	O6	Transmit Enable Channel B		
	CCU60_COUT62	O7	T12 PWM channel 62		
	IOM_MON1_5		Monitor input 1		
IOM_REF1_1		Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-35 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	CCU60_CC60INC			T12 capture input 60
	SENT_SENT2C			Receive input channel 2
	GPT120_T3INA			Trigger/gate input of core timer T3
	CCU60_CCPOS0A			Hall capture input 0
	CCU61_T12HRB			External timer start 12
	QSPI3_MTSRA			Slave SPI data input
	P02.6			O0
	GTM_TOUT6	O1	GTM muxed output	
	IOM_REF0_6		Reference input 0	
	—	O2	Reserved	
	QSPI3_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	EVADC_EMUX00	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC60	O7	T12 PWM channel 60	
	IOM_MON1_2		Monitor input 1	
	IOM_REF1_6		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-35 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	CCU60_CC61INC			T12 capture input 61
	SENT_SENT1C			Receive input channel 1
	GPT120_T3EUDA			Count direction control input of core timer T3
	CCU60_CCPOS1A			Hall capture input 1
	QSPI3_SCLKA			Slave SPI clock inputs
	CCU61_T13HRB			External timer start 13
	P02.7			O0
	GTM_TOUT7	O1	GTM muxed output	
	IOM_REF0_7	O2	Reference input 0	
	—		Reserved	
	QSPI3_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	EVADC_EMUX01	O5	Control of external analog multiplexer interface 0	
	SENT_SPC1	O6	Transmit output	
	CCU60_CC61	O7	T12 PWM channel 61	
	IOM_MON1_1	O7	Monitor input 1	
	IOM_REF1_5		Reference input 1	
9	P02.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CCU60_CC62INC			T12 capture input 62
	SENT_SENT0C			Receive input channel 0
	CCU60_CCPOS2A			Hall capture input 2
	GPT120_T4INA			Trigger/gate input of timer T4
	CCU61_T12HRC			External timer start 12
	CCU61_T13HRC			External timer start 13
	P02.8	O0	General-purpose output	
	GTM_TOUT8	O1	GTM muxed output	
	IOM_REF0_8	O2	Reference input 0	
	QSPI3_SLSO5		Master slave select output	
	ASCLIN8_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	EVADC_EMUX02	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC62	O7	T12 PWM channel 62	
	IOM_MON1_0	O7	Monitor input 1	
IOM_REF1_4	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-36 Port 10 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
140	P10.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_3			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_3			Mux input channel 1 of TIM module 0
	GPT120_T5EUDB			Count direction control input of timer T5
	QSPI1_MRSTA			Master SPI data input
	GTM_DTMT0_1			CDTM0_DTM0
	P10.1	O0		General-purpose output
	GTM_TOUT103	O1		GTM muxed output
	QSPI1_MTSR	O2		Master SPI data output
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	—	O4		Reserved
	—	O5		Reserved
—	O6		Reserved	
—	O7		Reserved	
141	P10.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_3			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_3			Mux input channel 2 of TIM module 0
	CAN02_RXDE			CAN receive input node 2
	QSPI1_SCLKA			Slave SPI clock inputs
	GPT120_T6INB			Trigger/gate input of core timer T6
	SCU_E_REQ2_0			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P10.2	O0		General-purpose output
	GTM_TOUT104	O1		GTM muxed output
	IOM_MON2_9			Monitor input 2
	—		O2	
	QSPI1_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
—	O6		Reserved	
—	O7		Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-36 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
142	P10.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_3			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_3			Mux input channel 3 of TIM module 0
	QSPI1_MTSRA			Slave SPI data input
	SCU_E_REQ3_0			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T5INB			Trigger/gate input of timer T5
	P10.3	O0	General-purpose output	
	GTM_TOUT105	O1	GTM muxed output	
	IOM_MON2_10	O2	Monitor input 2	
	—		Reserved	
	QSPI1_MTSR		Master SPI data output	
	—	O4	Reserved	
	—	O5	Reserved	
	CAN02_TXD	O6	CAN transmit output node 2	
	IOM_MON2_7	O7	Monitor input 2	
IOM_REF2_7	Reference input 2			
—	Reserved			
143	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0	General-purpose output	
	GTM_TOUT107	O1	GTM muxed output	
	IOM_REF2_9	O2	Reference input 2	
	ASCLIN2_ATX		Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14	O3	Reference input 2	
	QSPI3_SLSO8		Master slave select output	
	QSPI1_SLSO9		Master slave select output	
	GPT120_T6OUT	O5	External output for overflow/underflow detection of core timer T6	
	ASCLIN2_ASLSO	O6	Slave select signal output	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-36 Port 10 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
144	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0	SLOW / PU2 / VEXT / ES	General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
	IOM_MON2_1			Monitor input 2
IOM_REF2_1		Reference input 2		
—	O7	Reserved		

Table 2-37 Port 11 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
132	P11.2	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-37 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
133	P11.3	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
134	P11.6	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1
136	P11.8	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	CAN12_RXDD			CAN receive input node 2
	P11.8	O0		General-purpose output
	GTM_TOUT124	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-37 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
135	P11.9	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
137	P11.10	I	FAST / PU1 / VFLEX / ES	General-purpose input
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	QSPI1_SLSIA			Slave select input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
IOM_REF1_4	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-37 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
138	P11.11	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPIO_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
IOM_REF1_5	Reference input 1			
139	P11.12	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-38 Port 13 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
128	P13.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	ASCLIN10_ARXC			Receive input
	P13.0	O0		General-purpose output
	GTM_TOUT91	O1		GTM muxed output
	ASCLIN10_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CAN10_TXD	O7	CAN transmit output node 0	
129	P13.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7	Reserved	
130	P13.2	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-38 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
131	P13.3	I	FAST / PU1 / VEXT / ES6	General-purpose input
	P13.3	O0		General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

Table 2-39 Port 14 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
118	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6	O6		Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK			Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5	O7		Monitor input 1
	IOM_REF1_1			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-39 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
119	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1			O0
	GTM_TOUT81	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_6		Monitor input 1	
IOM_REF1_0	Reference input 1			
120	P14.2	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN5_3			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_3			Mux input channel 5 of TIM module 0
	PMS_HWCFG2IN			HWCFG2 pin input
	P14.2	O0	General-purpose output	
	GTM_TOUT82	O1	GTM muxed output	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI2_SLSO1	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	ASCLIN2_ASCLK	O6	Shift clock output	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-39 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
121	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0	General-purpose output	
	GTM_TOUT83	O1	GTM muxed output	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI2_SLSO3	O3	Master slave select output	
	ASCLIN1_ASLSO	O4	Slave select signal output	
	ASCLIN3_ASLSO	O5	Slave select signal output	
	—	O6	Reserved	
	—	O7	Reserved	
122	P14.4	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_2			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_2			Mux input channel 7 of TIM module 0
	PMS_HWCFG6IN			HWCFG6 pin input
	GTM_DTMT0_0			CDTM0_DTM0
	P14.4	O0	General-purpose output	
	GTM_TOUT84	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-39 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
123	P14.5	I	FAST / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0		General-purpose output
	GTM_TOUT85	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	ERAY0_TXDB	O6		Transmit Channel B
	—	O7		Reserved
124	P14.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_4			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_4			Mux input channel 1 of TIM module 0
	P14.6			O0
	GTM_TOUT86	O1		GTM muxed output
	—	O2		Reserved
	QSPI2_SLSO2	O3		Master slave select output
	CAN13_TXD	O4		CAN transmit output node 3
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-40 Port 15 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
109	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPIO_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7	O6		Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
110	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13	O3		Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-40 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
111	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	QSPI2_HSICINA			Highspeed capture channel
	P15.2	O0	General-purpose output	
	GTM_TOUT73	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12	O3	Reference input 2	
	QSPI2_SLSO0		Master slave select output	
	—	O4	Reserved	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6	O6	Reference input 2	
	ASCLIN0_ASCLK		Shift clock output	
	—	O7	Reserved	
112	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	QSPI2_HSICINB			Highspeed capture channel
	P15.3	O0	General-purpose output	
	GTM_TOUT74	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12	O3	Reference input 2	
	QSPI2_SCLK		Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-40 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
113	P15.4	I	FAST / PU1 / VEXT / ES	General-purpose input	
	QSPI2_MRSTA			Master SPI data input	
	SCU_E_REQ0_0			ERU Channel 0 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	P15.4			O0	General-purpose output
	GTM_TOUT75	O1		GTM muxed output	
	ASCLIN1_ATX	O2		Transmit output	
	IOM_MON2_13			Monitor input 2	
	IOM_REF2_13			Reference input 2	
	QSPI2_MRST	O3		Slave SPI data output	
	IOM_MON2_2			Monitor input 2	
	IOM_REF2_2			Reference input 2	
	—	O4		Reserved	
	—	O5		Reserved	
	—	O6		Reserved	
	CCU60_CC62	O7		T12 PWM channel 62	
IOM_MON1_0	Monitor input 1				
IOM_REF1_4	Reference input 1				
114	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input	
	ASCLIN1_ARXB			Receive input	
	QSPI2_MTSRA			Slave SPI data input	
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	P15.5	O0		General-purpose output	
	GTM_TOUT76	O1		GTM muxed output	
	ASCLIN1_ATX	O2		Transmit output	
	IOM_MON2_13			Monitor input 2	
	IOM_REF2_13			Reference input 2	
	QSPI2_MTSR	O3		Master SPI data output	
	—			O4	Reserved
	—			O5	Reserved
	—	O6		Reserved	
	CCU60_CC61	O7		T12 PWM channel 61	
	IOM_MON1_1			Monitor input 1	
IOM_REF1_5	Reference input 1				

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-40 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
115	P15.6	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN0_6			Mux input channel 0 of TIM module 1	
	GTM_TIM0_IN0_6			Mux input channel 0 of TIM module 0	
	QSPI2_MTSRB			Slave SPI data input	
	P15.6	O0	FAST / PU1 / VEXT / ES	General-purpose output	
	GTM_TOUT77	O1		GTM muxed output	
	ASCLIN3_ATX	O2		Transmit output	
	IOM_MON2_15			Monitor input 2	
	IOM_REF2_15			Reference input 2	
	QSPI2_MTSR			O3	Master SPI data output
	—	O4		Reserved	
	QSPI2_SCLK	O5		Master SPI clock output	
	ASCLIN3_ASCLK	O6		Shift clock output	
	CCU60_CC60	O7		T12 PWM channel 60	
	IOM_MON1_2			Monitor input 1	
IOM_REF1_6	Reference input 1				
116	P15.7	I		FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_5				Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_5				Mux input channel 1 of TIM module 0
	ASCLIN3_ARXA		Receive input		
	QSPI2_MRSTB		Master SPI data input		
	P15.7	O0	FAST / PU1 / VEXT / ES	General-purpose output	
	GTM_TOUT78	O1		GTM muxed output	
	ASCLIN3_ATX	O2		Transmit output	
	IOM_MON2_15			Monitor input 2	
	IOM_REF2_15			Reference input 2	
	QSPI2_MRST			O3	Slave SPI data output
	IOM_MON2_2			Monitor input 2	
	IOM_REF2_2			Reference input 2	
	—	O4		Reserved	
	—	O5		Reserved	
—	O6	Reserved			
CCU60_COUT60	O7	T12 PWM channel 60			
IOM_MON1_3		Monitor input 1			
IOM_REF1_3		Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-40 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
117	P15.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_5			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_5			Mux input channel 2 of TIM module 0
	QSPI2_SCLKB			Slave SPI clock inputs
	SCU_E_REQ5_0			ERU Channel 5 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.8	O0	General-purpose output	
	GTM_TOUT79	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI2_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	ASCLIN3_ASCLK	O6	Shift clock output	
	CCU60_COUT61	O7	T12 PWM channel 61	
	IOM_MON1_4		Monitor input 1	
	IOM_REF1_2		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-41 Port 20 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
93	P20.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_7			Mux input channel 6 of TIM module 1
	GTM_TIM1_IN4_9			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN6_7			Mux input channel 6 of TIM module 0
	CAN03_RXDC			CAN receive input node 3
	CCU_PAD_SYSCCLK			Sysclk input
	CBS_TGI0			Trigger input
	SCU_E_REQ6_0			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	GPT120_T6EUDA			Count direction control input of core timer T6
	P20.0			O0
	GTM_TOUT59	O1	GTM muxed output	
	ASCLIN3_ATX	O2	Transmit output	
	IOM_MON2_15		Monitor input 2	
	IOM_REF2_15		Reference input 2	
	ASCLIN3_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	
	CBS_TGO0	O	Trigger output	
94	P20.2	I	S / PU / VEXT	General-purpose input This pin is latched at power on reset release to enter test mode.
	TESTMODE			Testmode Enable Input

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-41 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
95	P20.3	I	SLOW / PU1 / VEXT / ES	General-purpose input
	ASCLIN3_ARXC			Receive input
	GPT120_T6INA			Trigger/gate input of core timer T6
	P20.3	O0		General-purpose output
	GTM_TOUT61	O1		GTM muxed output
	ASCLIN3_ATX	O2		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	QSPI0_SLSO9	O3		Master slave select output
	QSPI2_SLSO9	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	—	O6		Reserved
—	O7	Reserved		
100	P20.6	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CAN12_RXDA			CAN receive input node 2
	ASCLIN9_ARXE			Receive input
	P20.6	O0		General-purpose output
	GTM_TOUT62	O1		GTM muxed output
	ASCLIN1_ARTS	O2		Ready to send output
	QSPI0_SLSO8	O3		Master slave select output
	QSPI2_SLSO8	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-41 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
101	P20.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN00_RXDB			CAN receive input node 0
	ASCLIN1_ACTSA			Clear to send input
	ASCLIN9_ARXF			Receive input
	P20.7	O0		General-purpose output
	GTM_TOUT63	O1		GTM muxed output
	ASCLIN9_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	CAN12_TXD	O5		CAN transmit output node 2
	—	O6		Reserved
	CCU61_COUT63	O7		T13 PWM channel 63
	IOM_MON1_7			Monitor input 1
	IOM_REF1_7			Reference input 1
102	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPI0_SLSO0	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
IOM_REF1_13	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-41 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
103	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input	
	CAN03_RXDE			CAN receive input node 3	
	ASCLIN1_ARXC			Receive input	
	QSPIO_SLSIB			Slave select input	
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	P20.9	O0	General-purpose output		
	GTM_TOUT65	O1	GTM muxed output		
	—	O2	Reserved		
	QSPIO_SLSO1	O3	Master slave select output		
	QSPI1_SLSO1	O4	Master slave select output		
	—	O5	Reserved		
	—	O6	Reserved		
	CCU61_CC61	O7	T12 PWM channel 61		
	IOM_MON1_9		Monitor input 1		
IOM_REF1_12	Reference input 1				
104	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input	
	P20.10			O0	General-purpose output
	GTM_TOUT66			O1	GTM muxed output
	ASCLIN1_ATX			O2	Transmit output
	IOM_MON2_13				Monitor input 2
	IOM_REF2_13				Reference input 2
	QSPIO_SLSO6			O3	Master slave select output
	QSPI2_SLSO7			O4	Master slave select output
	CAN03_TXD			O5	CAN transmit output node 3
	IOM_MON2_8			O6	Monitor input 2
	IOM_REF2_8				Reference input 2
	ASCLIN1_ASCLK			O6	Shift clock output
	CCU61_CC62			O7	T12 PWM channel 62
	IOM_MON1_10				Monitor input 1
	IOM_REF1_11				Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-41 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
105	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI0_SCLKA			Slave SPI clock inputs
	P20.11			O0
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
106	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI0_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13	O2		Monitor input 0
	—			Reserved
	QSPI0_MRST			O3
	IOM_MON2_0	O4		Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR			O4
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-41 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
107	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPIO_SLSO2	O3		Master slave select output
	QSPIO_SLSO2	O4		Master slave select output
	QSPIO_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1
108	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	DMU_FDEST			Enter destructive debug mode
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15			Monitor input 0
	—	O2		Reserved
	QSPIO_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-42 Port 21 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function	
84	P21.2	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1	
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0	
	SCU_EMGSTOP_POR T_B			Emergency stop Port Pin B input request	
	ASCLIN11_ARXE			Receive input	
	P21.2	O0	General-purpose output		
	GTM_TOUT53	O1	GTM muxed output		
	ASCLIN3_ASLSO	O2	Slave select signal output		
	—	O3	Reserved		
	—	O4	Reserved		
	—	O5	Reserved		
	—	O6	Reserved		
—	O7	Reserved			
85	P21.3	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1	
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0	
	P21.3			O0	General-purpose output
	GTM_TOUT54			O1	GTM muxed output
	ASCLIN11_ASCLK	O2	Shift clock output		
	—	O3	Reserved		
	—	O4	Reserved		
	—	O5	Reserved		
	—	O6	Reserved		
	—	O7	Reserved		
	86	P21.4	I	FAST / PU1 / VEXT / ES6	General-purpose input
GTM_TIM1_IN2_6		Mux input channel 2 of TIM module 1			
GTM_TIM0_IN2_6		Mux input channel 2 of TIM module 0			
P21.4		O0			General-purpose output
GTM_TOUT55		O1			GTM muxed output
ASCLIN11_ASLSO		O2	Slave select signal output		
—		O3	Reserved		
—		O4	Reserved		
—		O5	Reserved		
—		O6	Reserved		
—		O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-42 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
87	P21.5	I	FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM1_IN3_6			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_6			Mux input channel 3 of TIM module 0	
	ASCLIN11_ARXF			Receive input	
	P21.5	O0		General-purpose output	
	GTM_TOUT56	O1		GTM muxed output	
	ASCLIN3_ASCLK	O2		Shift clock output	
	ASCLIN11_ATX	O3		Transmit output	
	—	O4		Reserved	
	—	O5		Reserved	
	—	O6		Reserved	
	—	O7		Reserved	
88	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	General-purpose input PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.	
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1	
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0	
	GPT120_T5EUDA			Count direction control input of timer T5	
	ASCLIN3_ARXF			Receive input	
	CBS_TGI2			Trigger input	
	TDI			JTAG Module Data Input	
	P21.6			O0	General-purpose output
	GTM_TOUT57			O1	GTM muxed output
	ASCLIN3_ASLSO			O2	Slave select signal output
	—			O3	Reserved
	—			O4	Reserved
	—			O5	Reserved
	—			O6	Reserved
	GPT120_T3OUT			O7	External output for overflow/underflow detection of core timer T3
	CBS_TGO2			O	Trigger output
DAP3	I/O	DAP: DAP3 Data I/O			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-42 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
90	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	P21.7	O0	General-purpose output	
	GTM_TOUT58	O1	GTM muxed output	
	ASCLIN3_ATX	O2	Transmit output	
	IOM_MON2_15		Monitor input 2	
	IOM_REF2_15		Reference input 2	
	ASCLIN3_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T6OUT	O7	External output for overflow/underflow detection of core timer T6	
	CBS_TGO3	O	Trigger output	
	DAP2	I/O	DAP: DAP2 Data I/O	
TDO	O	JTAG Module Data Output		

Table 2-43 Port 22 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
74	P22.0	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN1_7			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_7			Mux input channel 1 of TIM module 0
	ASCLIN6_ARXE			Receive input
	QSPI3_MTSRD			Slave SPI data input
	P22.0	O0	General-purpose output	
	GTM_TOUT47	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI3_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	ASCLIN6_ATX	O7	Transmit output	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-43 Port 22 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
75	P22.1	I	FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM1_IN0_8			Mux input channel 0 of TIM module 1	
	GTM_TIM0_IN0_8			Mux input channel 0 of TIM module 0	
	ASCLIN7_ARXE			Receive input	
	QSPI3_MRSTD			Master SPI data input	
	P22.1			O0	General-purpose output
	GTM_TOUT48			O1	GTM muxed output
	—			O2	Reserved
	QSPI3_MRST			O3	Slave SPI data output
	IOM_MON2_3				Monitor input 2
	IOM_REF2_3				Reference input 2
	—			O4	Reserved
	—			O5	Reserved
	—			O6	Reserved
ASCLIN7_ATX	O7	Transmit output			
76	P22.2	I	FAST / PU1 / VEXT / ES6	General-purpose input	
	GTM_TIM1_IN3_7			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_7			Mux input channel 3 of TIM module 0	
	P22.2			O0	General-purpose output
	GTM_TOUT49			O1	GTM muxed output
	ASCLIN5_ATX			O2	Transmit output
	QSPI3_SLSO12			O3	Master slave select output
	—			O4	Reserved
	—			O5	Reserved
	—			O6	Reserved
	—			O7	Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-43 Port 22 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
77	P22.3	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN4_4			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_4			Mux input channel 4 of TIM module 0
	ASCLIN5_ARXC			Receive input
	QSPI3_SCLKD			Slave SPI clock inputs
	P22.3	O0	General-purpose output	
	GTM_TOUT50	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI3_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

Table 2-44 Port 23 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	ASCLIN6_ARXF			Receive input
	P23.1	O0	General-purpose output	
	GTM_TOUT42	O1	GTM muxed output	
	ASCLIN1_ARTS	O2	Ready to send output	
	—	O3	Reserved	
	GTM_CLK0	O4	CGM generated clock	
	CAN10_TXD	O5	CAN transmit output node 0	
	CCU_EXTCLK0	O6	External Clock 0	
	ASCLIN6_ASCLK	O7	Shift clock output	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-45 Port 33 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
56	P33.0	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN4_6			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_6			Mux input channel 4 of TIM module 0
	IOM_PIN_0			GPIO pad input to FPC
	GTM_DTMT1_2			CDTM1_DTM0
	P33.0	O0		General-purpose output
	GTM_TOUT22	O1		GTM muxed output
	IOM_MON0_0			Monitor input 0
	IOM_GTM_0	GTM-provided inputs to EXOR combiner		
	ASCLIN5_ATX	O2		Transmit output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
57	P33.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN5_6			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_6			Mux input channel 5 of TIM module 0
	ASCLIN8_ARXC			Receive input
	IOM_PIN_1			GPIO pad input to FPC
	P33.1	O0		General-purpose output
	GTM_TOUT23	O1		GTM muxed output
	IOM_MON0_1			Monitor input 0
	IOM_GTM_1	GTM-provided inputs to EXOR combiner		
	ASCLIN3_ASLSO	O2		Slave select signal output
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	EVADC_EMUX02	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-45 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
58	P33.2	I	SLOW / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM1_IN6_6			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_6			Mux input channel 6 of TIM module 0
	IOM_PIN_2			GPIO pad input to FPC
	P33.2	O0		General-purpose output
	GTM_TOUT24	O1		GTM muxed output
	IOM_MON0_2			Monitor input 0
	IOM_GTM_2			GTM-provided inputs to EXOR combiner
	ASCLIN3_ASCLK	O2		Shift clock output
	QSPI2_SLSO10	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX01	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved
59	P33.3	I	SLOW / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM1_IN7_6			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_6			Mux input channel 7 of TIM module 0
	IOM_PIN_3			GPIO pad input to FPC
	P33.3	O0		General-purpose output
	GTM_TOUT25	O1		GTM muxed output
	IOM_MON0_3			Monitor input 0
	IOM_GTM_3			GTM-provided inputs to EXOR combiner
	ASCLIN5_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	EVADC_EMUX00	O5		Control of external analog multiplexer interface 0
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-45 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
60	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0	SLOW / PU1 / VEVRSB / ES5	General-purpose output
	GTM_TOUT26	O1		GTM muxed output
	IOM_MON0_4			Monitor input 0
	IOM_GTM_4			GTM-provided inputs to EXOR combiner
	ASCLIN2_ARTS	O2		Ready to send output
	QSPI2_SLSO12	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX12	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
	CAN13_TXD	O7		CAN transmit output node 3
61	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	GPT120_T4EUDB			Count direction control input of timer T4
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C			Receive input channel 5
	CAN13_RXDB			CAN receive input node 3
	IOM_PIN_5			GPIO pad input to FPC
	P33.5	O0	SLOW / PU1 / VEVRSB / ES5	General-purpose output
	GTM_TOUT27	O1		GTM muxed output
	IOM_MON0_5			Monitor input 0
	IOM_GTM_5			GTM-provided inputs to EXOR combiner
	QSPI0_SLSO7	O2		Master slave select output
	QSPI1_SLSO7	O3		Master slave select output
	—	O4		Reserved
	EVADC_EMUX11	O5		Control of external analog multiplexer interface 1
	—	O6		Reserved
ASCLIN5_ASLSO	O7	Slave select signal output		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-45 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
62	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	GPT120_T2EADB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	P33.6	O0	General-purpose output	
	GTM_TOUT28	O1	GTM muxed output	
	IOM_MON0_6		Monitor input 0	
	IOM_GTM_6		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ASLSO	O2	Slave select signal output	
	QSPI2_SLSO11	O3	Master slave select output	
	—	O4	Reserved	
	EVADC_EMUX10	O5	Control of external analog multiplexer interface 1	
	—	O6	Reserved	
—	O7	Reserved		
63	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7	O0	General-purpose output	
	GTM_TOUT29	O1	GTM muxed output	
	IOM_MON0_7		Monitor input 0	
	IOM_GTM_7		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	ASCLIN8_ATX	O4	Transmit output	
	—	O5	Reserved	
	—	O6	Reserved	
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-45 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
64	P33.8	I	FAST / HighZ / VEVRSB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_PORT_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0		General-purpose output
	GTM_TOUT30	O1		GTM muxed output
	IOM_MON0_8			Monitor input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5		Monitor input 2	
	IOM_REF2_5		Reference input 2	
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13		Monitor input 1	
IOM_REF1_8	Reference input 1			
SMU_FSP0	O		FSP[1..0] Output Signals - Generated by SMU_core	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-45 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
65	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	QSPI3_HSIICINA			Highspeed capture channel
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0	General-purpose output	
	GTM_TOUT31	O1	GTM muxed output	
	IOM_MON0_9		Monitor input 0	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	—	O3	Reserved	
	ASCLIN2_ASCLK	O4	Shift clock output	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ATX	O6	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	CCU61_CC62	O7	T12 PWM channel 62	
IOM_MON1_10	Monitor input 1			
IOM_REF1_11	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-45 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
66	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI3_HSICINB			Highspeed capture channel
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0	General-purpose output	
	GTM_TOUT32	O1	GTM muxed output	
	IOM_MON0_10		Monitor input 0	
	QSPI1_SLSO6	O2	Master slave select output	
	—	O3	Reserved	
	ASCLIN1_ASLSO	O4	Slave select signal output	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_COUT61	O7	T12 PWM channel 61	
	IOM_MON1_12		Monitor input 1	
IOM_REF1_9		Reference input 1		
SMU_FSP1	O	FSP[1..0] Output Signals - Generated by SMU_core		
67	P33.11	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_8			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_8			Mux input channel 2 of TIM module 0
	IOM_PIN_11			GPIO pad input to FPC
	P33.11	O0	General-purpose output	
	GTM_TOUT33	O1	GTM muxed output	
	IOM_MON0_11		Monitor input 0	
	ASCLIN1_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_CC61	O7	T12 PWM channel 61	
	IOM_MON1_9		Monitor input 1	
	IOM_REF1_12		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-45 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
68	P33.12	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	CAN00_RXDD			CAN receive input node 0
	PMS_PINBWKP			PINB (P33.12) pin input
	IOM_PIN_12			GPIO pad input to FPC
	P33.12	O0		General-purpose output
	GTM_TOUT34	O1		GTM muxed output
	IOM_MON0_12	O2		Monitor input 0
	ASCLIN1_ATX			Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	—	O3		Reserved
	ASCLIN1_ASCLK	O4		Shift clock output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
IOM_REF1_10	Reference input 1			

Table 2-46 Port 34 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
54	P34.1	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	P34.1	O0		General-purpose output
	—	O1		Reserved
	ASCLIN4_ATX	O2		Transmit output
	—	O3		Reserved
	CAN00_TXD	O4		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-46 Port 34 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
55	P34.2	I	SLOW / PU1 / VEVRSB / ES	General-purpose input
	ASCLIN4_ARXB			Receive input
	CAN00_RXDG			CAN receive input node 0
	P34.2	O0		General-purpose output
	—	O1		Reserved
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

Table 2-47 Analog Inputs

Pin	Symbol	Ctrl.	Buffer Type	Function
51	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
50	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
49	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
48	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0
47	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G0CH4			Analog input channel 4, group 0
	EVADC_G8CH8			Analog input channel 8, group 8
46	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G0CH5			Analog input channel 5, group 0
	EVADC_G8CH9			Analog input channel 9, group 8
45	AN6	I	D / HighZ / VDDM	Analog Input 6
	EVADC_G0CH6			Analog input channel 6, group 0
	EVADC_G8CH10			Analog input channel 10, group 8
40	AN7	I	D / HighZ / VDDM	Analog Input 7
	EVADC_G0CH7			Analog input channel 7, group 0
	EVADC_G8CH11			Analog input channel 11, group 8

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-47 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
39	AN8	I	D / HighZ / VDDM	Analog Input 8
	EVADC_G1CH0			Analog input channel 0, group 1
	EVADC_G8CH12			Analog input channel 12, group 8
38	AN9	I	D / HighZ / VDDM	Analog Input 9
	EVADC_G1CH1			Analog input channel 1, group 1
	EVADC_G8CH13			Analog input channel 13, group 8
37	AN10	I	D / HighZ / VDDM	Analog Input 10
	EVADC_G1CH2			Analog input channel 2, group 1
	EVADC_G8CH14			Analog input channel 14, group 8
36	AN11	I	D / HighZ / VDDM	Analog Input 11
	EVADC_G1CH3			Analog input channel 3, group 1
	EVADC_G8CH15			Analog input channel 15, group 8
35	AN12	I	D / HighZ / VDDM	Analog Input 12
	EVADC_G1CH4			Analog input channel 4, group 1
34	AN13	I	D / HighZ / VDDM	Analog Input 13
	EVADC_G1CH5			Analog input channel 5, group 1
33	AN14	I	D / HighZ / VDDM	Analog Input 14
	EVADC_G1CH6			Analog input channel 6, group 1
32	AN15	I	D / HighZ / VDDM	Analog Input 15
	EVADC_G1CH7			Analog input channel 7, group 1
31	AN32/P40.4	I	S / HighZ / VDDM	Analog Input 32
	SENT_SENT4A			Receive input channel 4
	EVADC_G8CH0			Analog input channel 0, group 8
	CCU60_CCPOS2D			Hall capture input 2
30	AN33/P40.5	I	S / HighZ / VDDM	Analog Input 33
	SENT_SENT5A			Receive input channel 5
	EVADC_G8CH1			Analog input channel 1, group 8
	CCU61_CCPOS0D			Hall capture input 0
29	AN34	I	D / HighZ / VDDM	Analog Input 34
	EVADC_G8CH2			Analog input channel 2, group 8
28	AN35	I	D / HighZ / VDDM	Analog Input 35
	EVADC_G8CH3			Analog input channel 3, group 8
27	AN36/P40.6	I	S / HighZ / VDDM	Analog Input 36
	SENT_SENT0A			Receive input channel 0
	EVADC_G8CH4			Analog input channel 4, group 8
	CCU61_CCPOS1B			Hall capture input 1

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-47 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
26	AN37/P40.7	I	S / HighZ / VDDM	Analog Input 37
	SENT_SENT1A			Receive input channel 1
	EVADC_G8CH5			Analog input channel 5, group 8
	CCU61_CCPOS1D			Hall capture input 1
25	AN38/P40.8	I	S / HighZ / VDDM	Analog Input 38
	SENT_SENT2A			Receive input channel 2
	EVADC_G8CH6			Analog input channel 6, group 8
	CCU61_CCPOS2B			Hall capture input 2
24	AN39/P40.9	I	S / HighZ / VDDM	Analog Input 39
	SENT_SENT3A			Receive input channel 3
	EVADC_G8CH7			Analog input channel 7, group 8
	CCU61_CCPOS2D			Hall capture input 2

Table 2-48 System I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
70	VCAP1	I/O	—	External Switch Capacitor
71	VCAP0	I/O	—	External Switch Capacitor
81	XTAL1	I	XTAL / VEXT	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
82	XTAL2	O	XTAL / VEXT	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
89	TMS	I	FAST /	JTAG Module State Machine Control Input
	DAP1	I/O	PD2 / VEXT	DAP: DAP1 Data I/O
91	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	JTAG Module Reset/Enable Input
92	TCK	I	FAST /	JTAG Module Clock Input
	DAP0	I	PD2 / VEXT	DAP: DAP0 Clock Input
96	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		ESR1 pin input

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-48 System I/O (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
97	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
98	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of $\overline{\text{PORST_N}}$ until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOC register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		ESR0 pin input

Table 2-49 Supply

Pin	Symbol	Ctrl.	Buffer Type	Function
44	VDDM	I	—	ADC Analog Power Supply (5V / 3.3V)
126	VDDP3	I	—	Flash Power Supply (3.3V)
42	VAREF1	I	—	Positive Analog Reference Voltage 1
52	VEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
10	VDD	I	—	Digital Core Power Supply (1.25V)
125	VEXT	I	—	External Power Supply (5V / 3.3V)
23	VEXT	I	—	External Power Supply (5V / 3.3V)
69	VEXT	I	—	External Power Supply (5V / 3.3V)
78	VEXT	I	—	External Power Supply (5V / 3.3V)
127	VDD	I	—	Digital Core Power Supply (1.25V)
22	VDD	I	—	Digital Core Power Supply (1.25V)
79	VDD	I	—	Digital Core Power Supply (1.25V)
99	VDD	I	—	Digital Core Power Supply (1.25V)
53	VDD	I	—	Digital Core Power Supply (1.25V)
72	VDDO	I	—	Switch capacitor EVRC Core regulator VDD supply output which shall be connected to other VDD pins externally on PCB level
E-PAD	VSS	I	—	Digital Ground
43	VSSM	I	—	Analog Ground for VDDM
41	VAGND1	I	—	Negative Analog Reference Voltage 1

TC33x/TC32x Pin Definition and Functions: TQFP-144 Package Variant Pin

Table 2-49 Supply (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
80	VSS	I	—	Oscillator Ground, VSS(OSC)
83	VEXT	I	—	Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)

2.4 TQFP-100 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP

Note: In the following QFP package the VFLEX supply is internally connected to VEXT supply and thus does not show up in the corresponding package drawings neither supply tables as a dedicated pin.

Table 2-50 Port 00 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
10	P00.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	CCU61_CTRAPA			Trap input capture
	CCU60_T12HRE			External timer start 12
	P00.0	O0	FAST / PU1 / VEXT / ES	General-purpose output
	GTM_TOUT9	O1		GTM muxed output
	IOM_REF0_9	O2		Reference input 0
	ASCLIN3_ASCLK			Shift clock output
	ASCLIN3_ATX			Transmit output
	IOM_MON2_15	O3		Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
IOM_REF1_0	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-51 Port 02 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.0	O0	General-purpose output	
	GTM_TOUT0	O1	GTM muxed output	
	IOM_REF0_0	O2	Reference input 0	
	ASCLIN2_ATX		Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14	O3	Reference input 2	
	QSPI3_SLSO1		Master slave select output	
	—	O4	Reserved	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5	O6	Monitor input 2	
	IOM_REF2_5		Reference input 2	
	ERAY0_TXDA	O6	Transmit Channel A	
	CCU60_CC60	O7	T12 PWM channel 60	
IOM_MON1_2	Monitor input 1			
IOM_REF1_6	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-51 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2_1			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.1	O0	General-purpose output	
	GTM_TOUT1	O1	GTM muxed output	
	IOM_REF0_1		Reference input 0	
	—	O2	Reserved	
	QSPI3_SLSO2	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT60	O7	T12 PWM channel 60	
	IOM_MON1_3		Monitor input 1	
	IOM_REF1_3		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-51 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
3	P02.2	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1	
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0	
	CCU61_CC61INB			T12 capture input 61	
	CCU60_CC61INA			T12 capture input 61	
	P02.2			O0	General-purpose output
	GTM_TOUT2			O1	GTM muxed output
	IOM_REF0_2				Reference input 0
	ASCLIN1_ATX			O2	Transmit output
	IOM_MON2_13				Monitor input 2
	IOM_REF2_13				Reference input 2
	QSPI3_SLSO3			O3	Master slave select output
	—			O4	Reserved
	CAN02_TXD	O5	CAN transmit output node 2		
	IOM_MON2_7		Monitor input 2		
	IOM_REF2_7		Reference input 2		
	ERAY0_TXDB	O6	Transmit Channel B		
	CCU60_CC61	O7	T12 PWM channel 61		
	IOM_MON1_1		Monitor input 1		
IOM_REF1_5		Reference input 1			
4	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0	
	ERAY0_RXDB2			Receive Channel B2	
	CAN02_RXDB			CAN receive input node 2	
	ASCLIN1_ARXG				Receive input
	P02.3			O0	General-purpose output
	GTM_TOUT3			O1	GTM muxed output
	IOM_REF0_3				Reference input 0
	ASCLIN2_ASLSO			O2	Slave select signal output
	QSPI3_SLSO4			O3	Master slave select output
	—			O4	Reserved
	—			O5	Reserved
	—	O6	Reserved		
	CCU60_COUT61	O7	T12 PWM channel 61		
	IOM_MON1_4		Monitor input 1		
	IOM_REF1_2		Reference input 1		

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-51 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
5	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1	
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0	
	CCU61_CC62INB			T12 capture input 62	
	QSPI3_SLSIA			Slave select input	
	CCU60_CC62INA			T12 capture input 62	
	CAN11_RXDA			CAN receive input node 1	
	P02.4			O0	General-purpose output
	GTM_TOUT4			O1	GTM muxed output
	IOM_REF0_4				Reference input 0
	ASCLIN2_ASCLK			O2	Shift clock output
	QSPI3_SLSO0			O3	Master slave select output
	—			O4	Reserved
	—			O5	Reserved
	ERAY0_TXENA			O6	Transmit Enable Channel A
	CCU60_CC62			O7	T12 PWM channel 62
	IOM_MON1_0				Monitor input 1
IOM_REF1_4		Reference input 1			
6	P02.5	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1	
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0	
	QSPI3_MRSTA			Master SPI data input	
	SENT_SENT3C			Receive input channel 3	
	P02.5			O0	General-purpose output
	GTM_TOUT5			O1	GTM muxed output
	IOM_REF0_5				Reference input 0
	CAN11_TXD			O2	CAN transmit output node 1
	QSPI3_MRST			O3	Slave SPI data output
	IOM_MON2_3				Monitor input 2
	IOM_REF2_3				Reference input 2
	—			O4	Reserved
	—			O5	Reserved
	ERAY0_TXENB			O6	Transmit Enable Channel B
	CCU60_COUT62			O7	T12 PWM channel 62
	IOM_MON1_5				Monitor input 1
IOM_REF1_1		Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-51 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	CCU60_CC60INC			T12 capture input 60
	SENT_SENT2C			Receive input channel 2
	GPT120_T3INA			Trigger/gate input of core timer T3
	CCU60_CCPOS0A			Hall capture input 0
	CCU61_T12HRB			External timer start 12
	QSPI3_MTSRA			Slave SPI data input
	P02.6			O0
	GTM_TOUT6	O1	GTM muxed output	
	IOM_REF0_6		Reference input 0	
	—	O2	Reserved	
	QSPI3_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	EVADC_EMUX00	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC60	O7	T12 PWM channel 60	
	IOM_MON1_2		Monitor input 1	
	IOM_REF1_6		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-51 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	CCU60_CC61INC			T12 capture input 61
	SENT_SENT1C			Receive input channel 1
	GPT120_T3EUDA			Count direction control input of core timer T3
	CCU60_CCPOS1A			Hall capture input 1
	QSPI3_SCLKA			Slave SPI clock inputs
	CCU61_T13HRB			External timer start 13
	P02.7			O0
	GTM_TOUT7	O1	GTM muxed output	
	IOM_REF0_7	O2	Reference input 0	
	—		Reserved	
	QSPI3_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	EVADC_EMUX01	O5	Control of external analog multiplexer interface 0	
	SENT_SPC1	O6	Transmit output	
	CCU60_CC61	O7	T12 PWM channel 61	
	IOM_MON1_1	O7	Monitor input 1	
	IOM_REF1_5		Reference input 1	
9	P02.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CCU60_CC62INC			T12 capture input 62
	SENT_SENT0C			Receive input channel 0
	CCU60_CCPOS2A			Hall capture input 2
	GPT120_T4INA			Trigger/gate input of timer T4
	CCU61_T12HRC			External timer start 12
	CCU61_T13HRC			External timer start 13
	P02.8	O0	General-purpose output	
	GTM_TOUT8	O1	GTM muxed output	
	IOM_REF0_8	O2	Reference input 0	
	QSPI3_SLSO5		Master slave select output	
	ASCLIN8_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	EVADC_EMUX02	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC62	O7	T12 PWM channel 62	
	IOM_MON1_0	O7	Monitor input 1	
IOM_REF1_4	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-52 Port 10 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
99	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWC4IN			HWCFG4 pin input
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	IOM_REF2_9			Reference input 2
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	ASCLIN2_ASLSO	O6		Slave select signal output
—	O7	Reserved		
100	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWC5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-53 Port 11 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
91	P11.2	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
92	P11.3	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
93	P11.6	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-53 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
95	P11.8	I	SLOW / PU1 / VFLEX / ES	General-purpose input
	CAN12_RXDD			CAN receive input node 2
	P11.8	O0		General-purpose output
	GTM_TOUT124	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved
94	P11.9	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-53 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
96	P11.10	I	FAST / PU1 / VFLEX / ES	General-purpose input	
	CAN03_RXDD			CAN receive input node 3	
	ERAY0_RXDB1			Receive Channel B1	
	ASCLIN1_ARXE			Receive input	
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)	
	QSPI1_SLSIA			Slave select input	
	P11.10	O0	General-purpose output		
	GTM_TOUT99	O1	GTM muxed output		
	—	O2	Reserved		
	QSPI0_SLSO3	O3	Master slave select output		
	QSPI1_SLSO3	O4	Master slave select output		
	—	O5	Reserved		
	—	O6	Reserved		
	CCU60_CC62	O7	T12 PWM channel 62		
IOM_MON1_0		Monitor input 1			
IOM_REF1_4		Reference input 1			
97	P11.11	I	FAST / PU1 / VFLEX / ES	General-purpose input	
	P11.11			O0	General-purpose output
	GTM_TOUT100			O1	GTM muxed output
	—			O2	Reserved
	QSPI0_SLSO4			O3	Master slave select output
	QSPI1_SLSO4			O4	Master slave select output
	—			O5	Reserved
	ERAY0_TXENB			O6	Transmit Enable Channel B
	CCU60_CC61			O7	T12 PWM channel 61
	IOM_MON1_1				Monitor input 1
	IOM_REF1_5				Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-53 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
98	P11.12	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

Table 2-54 Port 13 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
88	P13.1	I	FAST / PU1 / VEXT / ES6	General-purpose input
	CAN10_RXDD			CAN receive input node 0
	ASCLIN10_ARXD			Receive input
	P13.1	O0		General-purpose output
	GTM_TOUT92	O1		GTM muxed output
	—	O2		Reserved
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-54 Port 13 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
89	P13.2	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GPT120_CAPINA			Trigger input to capture value of timer T5 into CAPREL register
	P13.2	O0		General-purpose output
	GTM_TOUT93	O1		GTM muxed output
	ASCLIN10_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
90	P13.3	I	FAST / PU1 / VEXT / ES6	General-purpose input
	P13.3			General-purpose output
	GTM_TOUT94	O1		GTM muxed output
	ASCLIN10_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-55 Port 14 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
81	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12			Monitor input 2
	IOM_REF2_12			Reference input 2
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6			Monitor input 2
	IOM_REF2_6			Reference input 2
	ASCLIN0_ASCLK	O6		Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
IOM_REF1_1	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-55 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
82	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1			O0
	GTM_TOUT81	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12	O3	Reference input 2	
	—		Reserved	
	—		Reserved	
	—		Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
CCU60_COUT63	O7	T13 PWM channel 63		
IOM_MON1_6		Monitor input 1		
IOM_REF1_0		Reference input 1		

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-55 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
83	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0	General-purpose output	
	GTM_TOUT83	O1	GTM muxed output	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI2_SLSO3	O3	Master slave select output	
	ASCLIN1_ASLSO	O4	Slave select signal output	
	ASCLIN3_ASLSO	O5	Slave select signal output	
	—	O6	Reserved	
	—	O7	Reserved	
84	P14.5	I	FAST / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0	General-purpose output	
	GTM_TOUT85	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	ERAY0_TXDB	O6	Transmit Channel B	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-56 Port 15 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
76	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPIO_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7	O6		Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
77	P15.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN02_RXDA			CAN receive input node 2
	ASCLIN1_ARXA			Receive input
	QSPI2_SLSIB			Slave select input
	SCU_E_REQ7_2			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.1	O0		General-purpose output
	GTM_TOUT72	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13	O3		Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPI2_SLSO5	O3		Master slave select output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-56 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
78	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	QSPI2_HSICINA			Highspeed capture channel
	P15.2	O0		General-purpose output
	GTM_TOUT73	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12			Reference input 2
	QSPI2_SLSO0	O3		Master slave select output
	—	O4		Reserved
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ASCLK	O6		Shift clock output
	—	O7		Reserved
79	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	QSPI2_HSICINB			Highspeed capture channel
	P15.3	O0		General-purpose output
	GTM_TOUT74	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12			Reference input 2
	QSPI2_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7		Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-56 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
80	P15.5	I	FAST / PU1 / VEXT / ES	General-purpose input
	ASCLIN1_ARXB			Receive input
	QSPI2_MTSRA			Slave SPI data input
	SCU_E_REQ4_3			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P15.5	O0		General-purpose output
	GTM_TOUT76	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13		Monitor input 2	
	IOM_REF2_13		Reference input 2	
	QSPI2_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1		Monitor input 1	
IOM_REF1_5	Reference input 1			

Table 2-57 Port 20 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
64	P20.2	I	S / PU / VEXT	General-purpose input This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			Testmode Enable Input

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-57 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
69	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0		General-purpose output
	GTM_TOUT64	O1		GTM muxed output
	ASCLIN1_ASLSO	O2		Slave select signal output
	QSPIO_SLSO0	O3		Master slave select output
	QSPI1_SLSO0	O4		Master slave select output
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5			Monitor input 2
	IOM_REF2_5			Reference input 2
	—	O6		Reserved
	CCU61_CC60	O7		T12 PWM channel 60
	IOM_MON1_8			Monitor input 1
IOM_REF1_13	Reference input 1			
70	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPIO_SLSIB			Slave select input
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P20.9	O0		General-purpose output
	GTM_TOUT65	O1		GTM muxed output
	—	O2		Reserved
	QSPIO_SLSO1	O3		Master slave select output
	QSPI1_SLSO1	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_CC61	O7		T12 PWM channel 61
	IOM_MON1_9			Monitor input 1
IOM_REF1_12	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-57 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
71	P20.10	I	FAST / PU1 / VEXT / ES	General-purpose input
	P20.10	O0		General-purpose output
	GTM_TOUT66	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPIO_SLSO6	O3		Master slave select output
	QSPIO_SLSO7	O4		Master slave select output
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	CCU61_CC62	O7		T12 PWM channel 62
	IOM_MON1_10			Monitor input 1
IOM_REF1_11	Reference input 1			
72	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_SCLKA			Slave SPI clock inputs
	P20.11	O0		General-purpose output
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPIO_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
IOM_REF1_10	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-57 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
73	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13			Monitor input 0
	—	O2		Reserved
	QSPIO_MRST	O3		Slave SPI data output
	IOM_MON2_0			Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPIO_MTSR	O4		Master SPI data output
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9	Reference input 1			
74	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPIO_SLSO2	O3		Master slave select output
	QSPIO1_SLSO2	O4		Master slave select output
	QSPIO_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
	IOM_REF1_8			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-57 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
75	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	DMU_FDEST			Enter destructive debug mode
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15	O2		Monitor input 0
	—			Reserved
	QSPIO_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

Table 2-58 Port 21 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
56	P21.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_7			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_7			Mux input channel 0 of TIM module 0
	SCU_EMGSTOP_PORT_B			Emergency stop Port Pin B input request
	ASCLIN11_ARXE			Receive input
	P21.2	O0		General-purpose output
	GTM_TOUT53	O1		GTM muxed output
	ASCLIN3_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-58 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
57	P21.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_6			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_6			Mux input channel 1 of TIM module 0
	P21.3	O0		General-purpose output
	GTM_TOUT54	O1		GTM muxed output
	ASCLIN11_ASCLK	O2		Shift clock output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		
58	P21.4	I	FAST / PU1 / VEXT / ES6	General-purpose input
	GTM_TIM1_IN2_6			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_6			Mux input channel 2 of TIM module 0
	P21.4	O0		General-purpose output
	GTM_TOUT55	O1		GTM muxed output
	ASCLIN11_ASLSO	O2		Slave select signal output
	—	O3		Reserved
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-58 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
59	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	General-purpose input PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input
	P21.6	O0	General-purpose output	
	GTM_TOUT57	O1	GTM muxed output	
	ASCLIN3_ASLSO	O2	Slave select signal output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T3OUT	O7	External output for overflow/underflow detection of core timer T3	
	CBS_TGO2	O	Trigger output	
DAP3	I/O	DAP: DAP3 Data I/O		

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-58 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
61	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	P21.7			O0
	GTM_TOUT58	O1	GTM muxed output	
	ASCLIN3_ATX	O2	Transmit output	
	IOM_MON2_15		Monitor input 2	
	IOM_REF2_15		Reference input 2	
	ASCLIN3_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T6OUT	O7	External output for overflow/underflow detection of core timer T6	
	CBS_TGO3	O	Trigger output	
	DAP2	I/O	DAP: DAP2 Data I/O	
TDO	O	JTAG Module Data Output		

Table 2-59 Port 23 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
51	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	ASCLIN6_ARXF			Receive input
	P23.1	O0	General-purpose output	
	GTM_TOUT42	O1	GTM muxed output	
	ASCLIN1_ARTS	O2	Ready to send output	
	—	O3	Reserved	
	GTM_CLK0	O4	CGM generated clock	
	CAN10_TXD	O5	CAN transmit output node 0	
	CCU_EXTCLK0	O6	External Clock 0	
	ASCLIN6_ASCLK	O7	Shift clock output	

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-60 Port 33 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function	
41	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input	
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1	
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0	
	GPT120_T4EUIDB			Count direction control input of timer T4	
	ASCLIN2_ACTSB			Clear to send input	
	CCU61_CCPOS2C			Hall capture input 2	
	SENT_SENT5C			Receive input channel 5	
	CAN13_RXDB			CAN receive input node 3	
	IOM_PIN_5			GPIO pad input to FPC	
	P33.5			O0	General-purpose output
	GTM_TOUT27	O1	GTM muxed output		
	IOM_MON0_5		Monitor input 0		
	IOM_GTM_5	GTM-provided inputs to EXOR combiner			
	QSPI0_SLSO7	O2	Master slave select output		
	QSPI1_SLSO7	O3	Master slave select output		
	—	O4	Reserved		
	EVADC_EMUX11	O5	Control of external analog multiplexer interface 1		
	—	O6	Reserved		
ASCLIN5_ASLSO	O7	Slave select signal output			
42	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input	
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1	
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0	
	GPT120_T2EUIDB			Count direction control input of timer T2	
	SENT_SENT4C			Receive input channel 4	
	CCU61_CCPOS1C			Hall capture input 1	
	ASCLIN8_ARXD			Receive input	
	IOM_PIN_6			GPIO pad input to FPC	
	P33.6			O0	General-purpose output
	GTM_TOUT28			O1	GTM muxed output
	IOM_MON0_6	Monitor input 0			
	IOM_GTM_6	GTM-provided inputs to EXOR combiner			
	ASCLIN2_ASLSO	O2	Slave select signal output		
	QSPI2_SLSO11	O3	Master slave select output		
	—	O4	Reserved		
	EVADC_EMUX10	O5	Control of external analog multiplexer interface 1		
	—	O6	Reserved		
	—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-60 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
43	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7			O0
	GTM_TOUT29	O1	GTM muxed output	
	IOM_MON0_7		Monitor input 0	
	IOM_GTM_7		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	ASCLIN8_ATX	O4	Transmit output	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-60 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
44	P33.8	I	FAST / HighZ / VEVR SB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_PORT_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0	General-purpose output	
	GTM_TOUT30	O1	GTM muxed output	
	IOM_MON0_8	O2	Monitor input 0	
	ASCLIN2_ATX		Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14	Reference input 2		
	—	O3	Reserved	
	—	O4	Reserved	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5	O6	Monitor input 2	
	IOM_REF2_5		Reference input 2	
	—		Reserved	
	CCU61_COUT62	O7	T12 PWM channel 62	
	IOM_MON1_13	O	Monitor input 1	
IOM_REF1_8	Reference input 1			
SMU_FSP0		FSP[1..0] Output Signals - Generated by SMU_core		

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-60 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
45	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	QSPI3_HSIICINA			Highspeed capture channel
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0	General-purpose output	
	GTM_TOUT31	O1	GTM muxed output	
	IOM_MON0_9		Monitor input 0	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	—	O3	Reserved	
	ASCLIN2_ASCLK	O4	Shift clock output	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ATX	O6	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	CCU61_CC62	O7	T12 PWM channel 62	
IOM_MON1_10	Monitor input 1			
IOM_REF1_11	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-60 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
46	P33.10	I	FAST / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI3_HSICINB			Highspeed capture channel
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0	General-purpose output	
	GTM_TOUT32	O1	GTM muxed output	
	IOM_MON0_10		Monitor input 0	
	QSPI1_SLSO6	O2	Master slave select output	
	—	O3	Reserved	
	ASCLIN1_ASLSO	O4	Slave select signal output	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_COUT61	O7	T12 PWM channel 61	
	IOM_MON1_12		Monitor input 1	
IOM_REF1_9		Reference input 1		
SMU_FSP1	O	FSP[1..0] Output Signals - Generated by SMU_core		

Table 2-61 Analog Inputs

Pin	Symbol	Ctrl.	Buffer Type	Function
38	AN0	I	D / HighZ / VDDM	Analog Input 0
	EVADC_G0CH0			Analog input channel 0, group 0
37	AN1	I	D / HighZ / VDDM	Analog Input 1
	EVADC_G0CH1			Analog input channel 1, group 0
36	AN2	I	D / HighZ / VDDM	Analog Input 2
	EVADC_G0CH2			Analog input channel 2, group 0
35	AN3	I	D / HighZ / VDDM	Analog Input 3
	EVADC_G0CH3			Analog input channel 3, group 0
34	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G0CH4			Analog input channel 4, group 0
	EVADC_G8CH8			Analog input channel 8, group 8
33	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G0CH5			Analog input channel 5, group 0
	EVADC_G8CH9			Analog input channel 9, group 8

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-61 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
32	AN6	I	D / HighZ / VDDM	Analog Input 6
	EVADC_G0CH6			Analog input channel 6, group 0
	EVADC_G8CH10			Analog input channel 10, group 8
28	AN7	I	D / HighZ / VDDM	Analog Input 7
	EVADC_G0CH7			Analog input channel 7, group 0
	EVADC_G8CH11			Analog input channel 11, group 8
27	AN8	I	D / HighZ / VDDM	Analog Input 8
	EVADC_G1CH0			Analog input channel 0, group 1
	EVADC_G8CH12			Analog input channel 12, group 8
26	AN9	I	D / HighZ / VDDM	Analog Input 9
	EVADC_G1CH1			Analog input channel 1, group 1
	EVADC_G8CH13			Analog input channel 13, group 8
25	AN11	I	D / HighZ / VDDM	Analog Input 11
	EVADC_G1CH3			Analog input channel 3, group 1
	EVADC_G8CH15			Analog input channel 15, group 8
24	AN12	I	D / HighZ / VDDM	Analog Input 12
	EVADC_G1CH4			Analog input channel 4, group 1
23	AN13	I	D / HighZ / VDDM	Analog Input 13
	EVADC_G1CH5			Analog input channel 5, group 1
22	AN14	I	D / HighZ / VDDM	Analog Input 14
	EVADC_G1CH6			Analog input channel 6, group 1
21	AN15	I	D / HighZ / VDDM	Analog Input 15
	EVADC_G1CH7			Analog input channel 7, group 1
20	AN32/P40.4	I	S / HighZ / VDDM	Analog Input 32
	SENT_SENT4A			Receive input channel 4
	EVADC_G8CH0			Analog input channel 0, group 8
	CCU60_CCPOS2D			Hall capture input 2
19	AN33/P40.5	I	S / HighZ / VDDM	Analog Input 33
	SENT_SENT5A			Receive input channel 5
	EVADC_G8CH1			Analog input channel 1, group 8
	CCU61_CCPOS0D			Hall capture input 0
18	AN34	I	D / HighZ / VDDM	Analog Input 34
	EVADC_G8CH2			Analog input channel 2, group 8
17	AN35	I	D / HighZ / VDDM	Analog Input 35
	EVADC_G8CH3			Analog input channel 3, group 8

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-61 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
16	AN36/P40.6	I	S / HighZ / VDDM	Analog Input 36
	SENT_SENT0A			Receive input channel 0
	EVADC_G8CH4			Analog input channel 4, group 8
	CCU61_CCPOS1B			Hall capture input 1
15	AN37/P40.7	I	S / HighZ / VDDM	Analog Input 37
	SENT_SENT1A			Receive input channel 1
	EVADC_G8CH5			Analog input channel 5, group 8
	CCU61_CCPOS1D			Hall capture input 1
14	AN38/P40.8	I	S / HighZ / VDDM	Analog Input 38
	SENT_SENT2A			Receive input channel 2
	EVADC_G8CH6			Analog input channel 6, group 8
	CCU61_CCPOS2B			Hall capture input 2
13	AN39/P40.9	I	S / HighZ / VDDM	Analog Input 39
	SENT_SENT3A			Receive input channel 3
	EVADC_G8CH7			Analog input channel 7, group 8
	CCU61_CCPOS2D			Hall capture input 2

Table 2-62 System I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
48	VCAP1	I/O	—	External Switch Capacitor
49	VCAP0	I/O	—	External Switch Capacitor
53	XTAL1	I	XTAL / VEXT	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
54	XTAL2	O	XTAL / VEXT	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
60	TMS	I	FAST /	JTAG Module State Machine Control Input
	DAP1	I/O	PD2 / VEXT	DAP: DAP1 Data I/O
62	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	JTAG Module Reset/Enable Input
63	TCK	I	FAST /	JTAG Module Clock Input
	DAP0	I	PD2 / VEXT	DAP: DAP0 Clock Input

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-62 System I/O (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
65	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		ESR1 pin input
66	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
67	$\overline{\text{ESR0}}$	I/O	FAST / OD / VEXT	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR0WKP	I		ESR0 pin input

Table 2-63 Supply

Pin	Symbol	Ctrl.	Buffer Type	Function
30	VDDM	I	—	ADC Analog Power Supply (5V / 3.3V)
86	VDDP3	I	—	Flash Power Supply (3.3V)
29	VAREF1	I	—	Positive Analog Reference Voltage 1
39	VEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
11	VDD	I	—	Digital Core Power Supply (1.25V)
12	VEXT	I	—	External Power Supply (5V / 3.3V)
52	VDD	I	—	Digital Core Power Supply (1.25V)
68	VDD	I	—	Digital Core Power Supply (1.25V)
85	VEXT	I	—	External Power Supply (5V / 3.3V)
47	VEXT	I	—	External Power Supply (5V / 3.3V)
87	VDD	I	—	Digital Core Power Supply (1.25V)
40	VDD	I	—	Digital Core Power Supply (1.25V)
50	VDDO	I	—	Switch capacitor EVRC Core regulator VDD supply output which shall be connected to other VDD pins externally on PCB level

TC33x/TC32x Pin Definition and Functions: TQFP-100 Package Variant Pin

Table 2-63 Supply (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
E-PAD	VSS	I	—	Digital Ground
31	VSSM	I	—	Analog Ground for VDDM
55	VEXT	I	—	Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)

2.5 TQFP-80 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP

Note: In the following QFP package the VFLEX supply is internally connected to VEXT supply and thus does not show up in the corresponding package drawings neither supply tables as a dedicated pin.

Note: In TQFP80 package variant for TC33x/TC32x there are only three QSPI instances available – namely QSPI0, QSPI1, and QSPI3. Although some QSPI2 instance signals are bonded out, some required signals can not be bonded in this package. Hence QSPI2 is not usable here.

Table 2-64 Port 00 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
10	P00.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	CCU61_CTRAPA			Trap input capture
	CCU60_T12HRE			External timer start 12
	P00.0	O0		General-purpose output
	GTM_TOUT9	O1		GTM muxed output
	IOM_REF0_9			Reference input 0
	ASCLIN3_ASCLK	O2		Shift clock output
	ASCLIN3_ATX	O3		Transmit output
	IOM_MON2_15			Monitor input 2
	IOM_REF2_15			Reference input 2
	—	O4		Reserved
	CAN10_TXD	O5		CAN transmit output node 0
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
IOM_REF1_0	Reference input 1			

Table 2-65 Port 02 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
1	P02.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_2			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_2			Mux input channel 0 of TIM module 0
	CCU61_CC60INB			T12 capture input 60
	ASCLIN2_ARXG			Receive input
	CCU60_CC60INA			T12 capture input 60
	SCU_E_REQ3_2			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.0	O0	General-purpose output	
	GTM_TOUT0	O1	GTM muxed output	
	IOM_REF0_0	O2	Reference input 0	
	ASCLIN2_ATX		Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14	O3	Reference input 2	
	QSPI3_SLSO1		Master slave select output	
	—	O4	Reserved	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5	O6	Monitor input 2	
	IOM_REF2_5		Reference input 2	
	ERAY0_TXDA	O6	Transmit Channel A	
	CCU60_CC60	O7	T12 PWM channel 60	
IOM_MON1_2	Monitor input 1			
IOM_REF1_6	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-65 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
2	P02.1	I	SLOW / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN1_2			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_2			Mux input channel 1 of TIM module 0
	ERAY0_RXDA2			Receive Channel A2
	ASCLIN2_ARXB			Receive input
	CAN00_RXDA			CAN receive input node 0
	SCU_E_REQ2_1			ERU Channel 2 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P02.1	O0	General-purpose output	
	GTM_TOUT1	O1	GTM muxed output	
	IOM_REF0_1		Reference input 0	
	—	O2	Reserved	
	QSPI3_SLSO2	O3	Master slave select output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT60	O7	T12 PWM channel 60	
	IOM_MON1_3		Monitor input 1	
	IOM_REF1_3		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-65 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
3	P02.2	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN2_2			Mux input channel 2 of TIM module 1	
	GTM_TIM0_IN2_2			Mux input channel 2 of TIM module 0	
	CCU61_CC61INB			T12 capture input 61	
	CCU60_CC61INA			T12 capture input 61	
	P02.2			O0	General-purpose output
	GTM_TOUT2			O1	GTM muxed output
	IOM_REF0_2				Reference input 0
	ASCLIN1_ATX			O2	Transmit output
	IOM_MON2_13				Monitor input 2
	IOM_REF2_13				Reference input 2
	QSPI3_SLSO3			O3	Master slave select output
	—			O4	Reserved
	CAN02_TXD	O5	CAN transmit output node 2		
	IOM_MON2_7		Monitor input 2		
	IOM_REF2_7		Reference input 2		
	ERAY0_TXDB	O6	Transmit Channel B		
	CCU60_CC61	O7	T12 PWM channel 61		
	IOM_MON1_1		Monitor input 1		
IOM_REF1_5		Reference input 1			
4	P02.3	I	SLOW / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN3_2			Mux input channel 3 of TIM module 1	
	GTM_TIM0_IN3_2			Mux input channel 3 of TIM module 0	
	ERAY0_RXDB2			Receive Channel B2	
	CAN02_RXDB			CAN receive input node 2	
	ASCLIN1_ARXG			Receive input	
	P02.3			O0	General-purpose output
	GTM_TOUT3			O1	GTM muxed output
	IOM_REF0_3				Reference input 0
	ASCLIN2_ASLSO			O2	Slave select signal output
	QSPI3_SLSO4			O3	Master slave select output
	—			O4	Reserved
	—			O5	Reserved
	—			O6	Reserved
	CCU60_COUT61			O7	T12 PWM channel 61
	IOM_MON1_4				Monitor input 1
	IOM_REF1_2				Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-65 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function	
5	P02.4	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN4_1			Mux input channel 4 of TIM module 1	
	GTM_TIM0_IN4_1			Mux input channel 4 of TIM module 0	
	CCU61_CC62INB			T12 capture input 62	
	QSPI3_SLSIA			Slave select input	
	CCU60_CC62INA			T12 capture input 62	
	CAN11_RXDA			CAN receive input node 1	
	P02.4			O0	General-purpose output
	GTM_TOUT4			O1	GTM muxed output
	IOM_REF0_4				Reference input 0
	ASCLIN2_ASCLK	O2	Shift clock output		
	QSPI3_SLSO0	O3	Master slave select output		
	—	O4	Reserved		
	—	O5	Reserved		
	ERAY0_TXENA	O6	Transmit Enable Channel A		
	CCU60_CC62	O7	T12 PWM channel 62		
	IOM_MON1_0		Monitor input 1		
IOM_REF1_4		Reference input 1			
6	P02.5	I	FAST / PU1 / VEXT / ES	General-purpose input	
	GTM_TIM1_IN5_1			Mux input channel 5 of TIM module 1	
	GTM_TIM0_IN5_1			Mux input channel 5 of TIM module 0	
	QSPI3_MRSTA			Master SPI data input	
	SENT_SENT3C			Receive input channel 3	
	P02.5			O0	General-purpose output
	GTM_TOUT5			O1	GTM muxed output
	IOM_REF0_5				Reference input 0
	CAN11_TXD			O2	CAN transmit output node 1
	QSPI3_MRST			O3	Slave SPI data output
	IOM_MON2_3		Monitor input 2		
	IOM_REF2_3		Reference input 2		
	—	O4	Reserved		
	—	O5	Reserved		
	ERAY0_TXENB	O6	Transmit Enable Channel B		
	CCU60_COUT62	O7	T12 PWM channel 62		
	IOM_MON1_5		Monitor input 1		
IOM_REF1_1		Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-65 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
7	P02.6	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_1			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_1			Mux input channel 6 of TIM module 0
	CCU60_CC60INC			T12 capture input 60
	SENT_SENT2C			Receive input channel 2
	GPT120_T3INA			Trigger/gate input of core timer T3
	CCU60_CCPOS0A			Hall capture input 0
	CCU61_T12HRB			External timer start 12
	QSPI3_MTSRA			Slave SPI data input
	P02.6			O0
	GTM_TOUT6	O1	GTM muxed output	
	IOM_REF0_6		Reference input 0	
	—	O2	Reserved	
	QSPI3_MTSR	O3	Master SPI data output	
	—	O4	Reserved	
	EVADC_EMUX00	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC60	O7	T12 PWM channel 60	
	IOM_MON1_2		Monitor input 1	
	IOM_REF1_6		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-65 Port 02 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
8	P02.7	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_1			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_1			Mux input channel 7 of TIM module 0
	CCU60_CC61INC			T12 capture input 61
	SENT_SENT1C			Receive input channel 1
	GPT120_T3EUDA			Count direction control input of core timer T3
	CCU60_CCPOS1A			Hall capture input 1
	QSPI3_SCLKA			Slave SPI clock inputs
	CCU61_T13HRB			External timer start 13
	P02.7			O0
	GTM_TOUT7	O1	GTM muxed output	
	IOM_REF0_7	O2	Reference input 0	
	—		Reserved	
	QSPI3_SCLK	O3	Master SPI clock output	
	—	O4	Reserved	
	EVADC_EMUX01	O5	Control of external analog multiplexer interface 0	
	SENT_SPC1	O6	Transmit output	
	CCU60_CC61	O7	T12 PWM channel 61	
	IOM_MON1_1	O7	Monitor input 1	
	IOM_REF1_5		Reference input 1	
9	P02.8	I	SLOW / PU1 / VEXT / ES	General-purpose input
	CCU60_CC62INC			T12 capture input 62
	SENT_SENT0C			Receive input channel 0
	CCU60_CCPOS2A			Hall capture input 2
	GPT120_T4INA			Trigger/gate input of timer T4
	CCU61_T12HRC			External timer start 12
	CCU61_T13HRC			External timer start 13
	P02.8	O0	General-purpose output	
	GTM_TOUT8	O1	GTM muxed output	
	IOM_REF0_8	O2	Reference input 0	
	QSPI3_SLSO5		Master slave select output	
	ASCLIN8_ASCLK	O3	Shift clock output	
	—	O4	Reserved	
	EVADC_EMUX02	O5	Control of external analog multiplexer interface 0	
	—	O6	Reserved	
	CCU60_CC62	O7	T12 PWM channel 62	
	IOM_MON1_0	O7	Monitor input 1	
IOM_REF1_4	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-66 Port 10 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
79	P10.5	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN2_4			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_4			Mux input channel 2 of TIM module 0
	PMS_HWCFG4IN			HWCFG4 pin input
	P10.5	O0		General-purpose output
	GTM_TOUT107	O1		GTM muxed output
	IOM_REF2_9			Reference input 2
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14			Monitor input 2
	IOM_REF2_14			Reference input 2
	QSPI3_SLSO8	O3		Master slave select output
	QSPI1_SLSO9	O4		Master slave select output
	GPT120_T6OUT	O5		External output for overflow/underflow detection of core timer T6
	ASCLIN2_ASLSO	O6		Slave select signal output
—	O7	Reserved		
80	P10.6	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN3_4			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_4			Mux input channel 3 of TIM module 0
	ASCLIN2_ARXD			Receive input
	QSPI3_MTSRB			Slave SPI data input
	PMS_HWCFG5IN			HWCFG5 pin input
	P10.6	O0		General-purpose output
	GTM_TOUT108	O1		GTM muxed output
	IOM_REF2_10			Reference input 2
	ASCLIN2_ASCLK	O2		Shift clock output
	QSPI3_MTSR	O3		Master SPI data output
	GPT120_T3OUT	O4		External output for overflow/underflow detection of core timer T3
	—	O5		Reserved
	QSPI1_MRST	O6		Slave SPI data output
IOM_MON2_1		Monitor input 2		
IOM_REF2_1		Reference input 2		
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-67 Port 11 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
72	P11.2	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.2	O0		General-purpose output
	GTM_TOUT95	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO5	O3		Master slave select output
	QSPI1_SLSO5	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT63	O7		T13 PWM channel 63
	IOM_MON1_6			Monitor input 1
	IOM_REF1_0			Reference input 1
73	P11.3	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MRSTB			Master SPI data input
	P11.3	O0		General-purpose output
	GTM_TOUT96	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MRST	O3		Slave SPI data output
	IOM_MON2_1			Monitor input 2
	IOM_REF2_1			Reference input 2
	ERAY0_TXDA	O4		Transmit Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5			Monitor input 1
	IOM_REF1_1			Reference input 1
74	P11.6	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_SCLKB			Slave SPI clock inputs
	P11.6	O0		General-purpose output
	GTM_TOUT97	O1		GTM muxed output
	ERAY0_TXENB	O2		Transmit Enable Channel B
	QSPI1_SCLK	O3		Master SPI clock output
	ERAY0_TXENA	O4		Transmit Enable Channel A
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT61	O7		T12 PWM channel 61
	IOM_MON1_4			Monitor input 1
	IOM_REF1_2			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-67 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
75	P11.9	I	FAST / PU1 / VFLEX / ES	General-purpose input
	QSPI1_MTSRB			Slave SPI data input
	ERAY0_RXDA1			Receive Channel A1
	P11.9	O0		General-purpose output
	GTM_TOUT98	O1		GTM muxed output
	—	O2		Reserved
	QSPI1_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU60_COUT60	O7		T12 PWM channel 60
	IOM_MON1_3			Monitor input 1
	IOM_REF1_3			Reference input 1
76	P11.10	I	FAST / PU1 / VFLEX / ES	General-purpose input
	CAN03_RXDD			CAN receive input node 3
	ERAY0_RXDB1			Receive Channel B1
	ASCLIN1_ARXE			Receive input
	SCU_E_REQ6_3			ERU Channel 6 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	QSPI1_SLSIA			Slave select input
	P11.10	O0		General-purpose output
	GTM_TOUT99	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SLSO3	O3		Master slave select output
	QSPI1_SLSO3	O4		Master slave select output
	—	O5		Reserved
	—	O6		Reserved
	CCU60_CC62	O7		T12 PWM channel 62
	IOM_MON1_0			Monitor input 1
IOM_REF1_4	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-67 Port 11 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
77	P11.11	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.11	O0		General-purpose output
	GTM_TOUT100	O1		GTM muxed output
	—	O2		Reserved
	QSPIO_SLSO4	O3		Master slave select output
	QSPI1_SLSO4	O4		Master slave select output
	—	O5		Reserved
	ERAY0_TXENB	O6		Transmit Enable Channel B
	CCU60_CC61	O7		T12 PWM channel 61
	IOM_MON1_1			Monitor input 1
	IOM_REF1_5			Reference input 1
78	P11.12	I	FAST / PU1 / VFLEX / ES	General-purpose input
	P11.12	O0		General-purpose output
	GTM_TOUT101	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	GTM_CLK2	O3		CGM generated clock
	ERAY0_TXDB	O4		Transmit Channel B
	CAN03_TXD	O5		CAN transmit output node 3
	IOM_MON2_8			Monitor input 2
	IOM_REF2_8			Reference input 2
	CCU_EXTCLK1	O6		External Clock 1
	CCU60_CC60	O7		T12 PWM channel 60
	IOM_MON1_2			Monitor input 1
	IOM_REF1_6			Reference input 1

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-68 Port 14 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
65	P14.0	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN3_5			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_5			Mux input channel 3 of TIM module 0
	P14.0	O0		General-purpose output
	GTM_TOUT80	O1		GTM muxed output
	ASCLIN0_ATX	O2		Transmit output
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	ERAY0_TXDA	O3		Transmit Channel A
	ERAY0_TXDB	O4		Transmit Channel B
	CAN01_TXD	O5		CAN transmit output node 1
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ASCLK	O6		Shift clock output
	CCU60_COUT62	O7		T12 PWM channel 62
	IOM_MON1_5		Monitor input 1	
	IOM_REF1_1		Reference input 1	

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-68 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
66	P14.1	I	FAST / PU1 / VEXT / ES2	General-purpose input
	GTM_TIM1_IN4_3			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_3			Mux input channel 4 of TIM module 0
	ERAY0_RXDA3			Receive Channel A3
	ASCLIN0_ARXA			Receive input
	ERAY0_RXDB3			Receive Channel B3
	CAN01_RXDB			CAN receive input node 1
	SCU_E_REQ3_1			ERU Channel 3 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	PMS_PINAWKP			PINA (P14.1) pin input
	P14.1			O0
	GTM_TOUT81	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU60_COUT63	O7	T13 PWM channel 63	
	IOM_MON1_6		Monitor input 1	
IOM_REF1_0	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-68 Port 14 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
67	P14.3	I	SLOW / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_3			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_3			Mux input channel 6 of TIM module 0
	PMS_HWCFG3IN			HWCFG3 pin input
	ASCLIN2_ARXA			Receive input
	SCU_E_REQ1_0			ERU Channel 1 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P14.3	O0	General-purpose output	
	GTM_TOUT83	O1	GTM muxed output	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	QSPI2_SLSO3	O3	Master slave select output	
	ASCLIN1_ASLSO	O4	Slave select signal output	
	ASCLIN3_ASLSO	O5	Slave select signal output	
—	O6	Reserved		
—	O7	Reserved		
68	P14.5	I	FAST / PU2 / VEXT / ES	General-purpose input
	GTM_TIM1_IN0_4			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_4			Mux input channel 0 of TIM module 0
	PMS_HWCFG1IN			HWCFG1 pin input
	P14.5	O0	General-purpose output	
	GTM_TOUT85	O1	GTM muxed output	
	—	O2	Reserved	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	ERAY0_TXDB	O6	Transmit Channel B	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-69 Port 15 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
61	P15.0	I	FAST / PU1 / VEXT / ES	General-purpose input
	P15.0	O0		General-purpose output
	GTM_TOUT71	O1		GTM muxed output
	ASCLIN1_ATX	O2		Transmit output
	IOM_MON2_13			Monitor input 2
	IOM_REF2_13			Reference input 2
	QSPIO_SLSO13	O3		Master slave select output
	—	O4		Reserved
	CAN02_TXD	O5		CAN transmit output node 2
	IOM_MON2_7			Monitor input 2
	IOM_REF2_7			Reference input 2
	ASCLIN1_ASCLK	O6		Shift clock output
	—	O7		Reserved
	62	P15.1		I
CAN02_RXDA		CAN receive input node 2		
ASCLIN1_ARXA		Receive input		
QSPI2_SLSIB		Slave select input		
SCU_E_REQ7_2		ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)		
P15.1		O0	General-purpose output	
GTM_TOUT72		O1	GTM muxed output	
ASCLIN1_ATX		O2	Transmit output	
IOM_MON2_13			Monitor input 2	
IOM_REF2_13			Reference input 2	
QSPI2_SLSO5		O3	Master slave select output	
—		O4	Reserved	
—		O5	Reserved	
—		O6	Reserved	
—	O7	Reserved		

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-69 Port 15 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
63	P15.2	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI2_SLSIA			Slave select input
	QSPI2_MRSTE			Master SPI data input
	QSPI2_HSICINA			Highspeed capture channel
	P15.2	O0	General-purpose output	
	GTM_TOUT73	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12	O3	Reference input 2	
	QSPI2_SLSO0		Master slave select output	
	—	O4	Reserved	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ASCLK	O6	Shift clock output	
	—	O7	Reserved	
64	P15.3	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN01_RXDA			CAN receive input node 1
	ASCLIN0_ARXB			Receive input
	QSPI2_SCLKA			Slave SPI clock inputs
	QSPI2_HSICINB			Highspeed capture channel
	P15.3	O0	General-purpose output	
	GTM_TOUT74	O1	GTM muxed output	
	ASCLIN0_ATX	O2	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12	O3	Reference input 2	
	QSPI2_SCLK		Master SPI clock output	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-70 Port 20 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
51	P20.2	I	S / PU / VEXT	General-purpose input This pin is latched at power on reset release to enter test mode.
	$\overline{\text{TESTMODE}}$			Testmode Enable Input
55	P20.8	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN7_3			Mux input channel 7 of TIM module 1
	GTM_TIM0_IN7_3			Mux input channel 7 of TIM module 0
	P20.8	O0	General-purpose output	
	GTM_TOUT64	O1	GTM muxed output	
	ASCLIN1_ASLSO	O2	Slave select signal output	
	QSPI0_SLSO0	O3	Master slave select output	
	QSPI1_SLSO0	O4	Master slave select output	
	CAN00_TXD	O5	CAN transmit output node 0	
	IOM_MON2_5		Monitor input 2	
	IOM_REF2_5		Reference input 2	
	—	O6	Reserved	
	CCU61_CC60	O7	T12 PWM channel 60	
	IOM_MON1_8		Monitor input 1	
IOM_REF1_13		Reference input 1		
56	P20.9	I	FAST / PU1 / VEXT / ES	General-purpose input
	CAN03_RXDE			CAN receive input node 3
	ASCLIN1_ARXC			Receive input
	QSPI0_SLSIB			Slave select input
	SCU_E_REQ7_0			ERU Channel 7 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	P20.9	O0	General-purpose output	
	GTM_TOUT65	O1	GTM muxed output	
	—	O2	Reserved	
	QSPI0_SLSO1	O3	Master slave select output	
	QSPI1_SLSO1	O4	Master slave select output	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_CC61	O7	T12 PWM channel 61	
	IOM_MON1_9		Monitor input 1	
IOM_REF1_12		Reference input 1		

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-70 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
57	P20.11	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI0_SCLKA			Slave SPI clock inputs
	P20.11			O0
	GTM_TOUT67	O1		GTM muxed output
	—	O2		Reserved
	QSPI0_SCLK	O3		Master SPI clock output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT60	O7		T12 PWM channel 60
	IOM_MON1_11			Monitor input 1
	IOM_REF1_10			Reference input 1
58	P20.12	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPI0_MRSTA			Master SPI data input
	IOM_PIN_13			GPIO pad input to FPC
	P20.12	O0		General-purpose output
	GTM_TOUT68	O1		GTM muxed output
	IOM_MON0_13	O2		Monitor input 0
	—			Reserved
	QSPI0_MRST			O3
	IOM_MON2_0	O4		Monitor input 2
	IOM_REF2_0			Reference input 2
	QSPI0_MTSR			O4
	—	O5		Reserved
	—	O6		Reserved
	CCU61_COUT61	O7		T12 PWM channel 61
	IOM_MON1_12			Monitor input 1
IOM_REF1_9	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-70 Port 20 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
59	P20.13	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_SLSIA			Slave select input
	IOM_PIN_14			GPIO pad input to FPC
	P20.13	O0		General-purpose output
	GTM_TOUT69	O1		GTM muxed output
	IOM_MON0_14			Monitor input 0
	—	O2		Reserved
	QSPIO_SLSO2	O3		Master slave select output
	QSPIO_SLSO2	O4		Master slave select output
	QSPIO_SCLK	O5		Master SPI clock output
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13			Monitor input 1
IOM_REF1_8	Reference input 1			
60	P20.14	I	FAST / PU1 / VEXT / ES	General-purpose input
	QSPIO_MTSRA			Slave SPI data input
	IOM_PIN_15			GPIO pad input to FPC
	DMU_FDEST			Enter destructive debug mode
	P20.14	O0		General-purpose output
	GTM_TOUT70	O1		GTM muxed output
	IOM_MON0_15			Monitor input 0
	—	O2		Reserved
	QSPIO_MTSR	O3		Master SPI data output
	—	O4		Reserved
	—	O5		Reserved
	—	O6		Reserved
	—	O7		Reserved

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-71 Port 21 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
46	P21.6/TDI	I	FAST / PD / PU2 / VEXT / ES3	General-purpose input PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
	GTM_TIM1_IN4_8			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_8			Mux input channel 4 of TIM module 0
	GPT120_T5EUDA			Count direction control input of timer T5
	ASCLIN3_ARXF			Receive input
	CBS_TGI2			Trigger input
	TDI			JTAG Module Data Input
	P21.6	O0	General-purpose output	
	GTM_TOUT57	O1	GTM muxed output	
	ASCLIN3_ASLSO	O2	Slave select signal output	
	—	O3	Reserved	
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T3OUT	O7	External output for overflow/underflow detection of core timer T3	
CBS_TGO2	O	Trigger output		
DAP3	I/O	DAP: DAP3 Data I/O		

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-71 Port 21 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
48	P21.7/TDO	I	FAST / PU2 / VEXT / ES4	General-purpose input
	GTM_TIM1_IN5_7			Mux input channel 5 of TIM module 1
	GTM_TIM0_IN5_7			Mux input channel 5 of TIM module 0
	GPT120_T5INA			Trigger/gate input of timer T5
	CBS_TGI3			Trigger input
	P21.7			O0
	GTM_TOUT58	O1	GTM muxed output	
	ASCLIN3_ATX	O2	Transmit output	
	IOM_MON2_15		Monitor input 2	
	IOM_REF2_15		Reference input 2	
	ASCLIN3_ASCLK		O3	Shift clock output
	—	O4	Reserved	
	—	O5	Reserved	
	—	O6	Reserved	
	GPT120_T6OUT	O7	External output for overflow/underflow detection of core timer T6	
	CBS_TGO3	O	Trigger output	
	DAP2	I/O	DAP: DAP2 Data I/O	
TDO	O	JTAG Module Data Output		

Table 2-72 Port 23 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
41	P23.1	I	FAST / PU1 / VEXT / ES	General-purpose input
	GTM_TIM1_IN6_4			Mux input channel 6 of TIM module 1
	GTM_TIM0_IN6_4			Mux input channel 6 of TIM module 0
	ASCLIN6_ARXF			Receive input
	P23.1	O0	General-purpose output	
	GTM_TOUT42	O1	GTM muxed output	
	ASCLIN1_ARTS	O2	Ready to send output	
	—	O3	Reserved	
	GTM_CLK0	O4	CGM generated clock	
	CAN10_TXD	O5	CAN transmit output node 0	
	CCU_EXTCLK0	O6	External Clock 0	
	ASCLIN6_ASCLK	O7	Shift clock output	

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-73 Port 33 Functions

Pin	Symbol	Ctrl.	Buffer Type	Function
30	P33.4	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN0_10			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_10			Mux input channel 0 of TIM module 0
	CCU61_CTRAPC			Trap input capture
	ASCLIN5_ARXB			Receive input
	IOM_PIN_4			GPIO pad input to FPC
	P33.4	O0	General-purpose output	
	GTM_TOUT26	O1	GTM muxed output	
	IOM_MON0_4		Monitor input 0	
	IOM_GTM_4		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ARTS	O2	Ready to send output	
	QSPI2_SLSO12	O3	Master slave select output	
	—	O4	Reserved	
	EVADC_EMUX12	O5	Control of external analog multiplexer interface 1	
—	O6	Reserved		
CAN13_TXD	O7	CAN transmit output node 3		
31	P33.5	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_8			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_8			Mux input channel 1 of TIM module 0
	GPT120_T4EUDB			Count direction control input of timer T4
	ASCLIN2_ACTSB			Clear to send input
	CCU61_CCPOS2C			Hall capture input 2
	SENT_SENT5C		Receive input channel 5	
	CAN13_RXDB		CAN receive input node 3	
	IOM_PIN_5		GPIO pad input to FPC	
	P33.5		O0	General-purpose output
	GTM_TOUT27	O1	GTM muxed output	
	IOM_MON0_5		Monitor input 0	
	IOM_GTM_5		GTM-provided inputs to EXOR combiner	
	QSPI0_SLSO7	O2	Master slave select output	
QSPI1_SLSO7	O3	Master slave select output		
—	O4	Reserved		
EVADC_EMUX11	O5	Control of external analog multiplexer interface 1		
—	O6	Reserved		
ASCLIN5_ASLSO	O7	Slave select signal output		

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-73 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
32	P33.6	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN2_9			Mux input channel 2 of TIM module 1
	GTM_TIM0_IN2_9			Mux input channel 2 of TIM module 0
	GPT120_T2EADB			Count direction control input of timer T2
	SENT_SENT4C			Receive input channel 4
	CCU61_CCPOS1C			Hall capture input 1
	ASCLIN8_ARXD			Receive input
	IOM_PIN_6			GPIO pad input to FPC
	P33.6	O0	General-purpose output	
	GTM_TOUT28	O1	GTM muxed output	
	IOM_MON0_6		Monitor input 0	
	IOM_GTM_6		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ASLSO	O2	Slave select signal output	
	QSPI2_SLSO11	O3	Master slave select output	
	—	O4	Reserved	
	EVADC_EMUX10	O5	Control of external analog multiplexer interface 1	
	—	O6	Reserved	
	—	O7	Reserved	
33	P33.7	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN3_9			Mux input channel 3 of TIM module 1
	GTM_TIM0_IN3_9			Mux input channel 3 of TIM module 0
	CAN00_RXDE			CAN receive input node 0
	GPT120_T2INB			Trigger/gate input of timer T2
	CCU61_CCPOS0C			Hall capture input 0
	SCU_E_REQ4_0			ERU Channel 4 inputs 0 to 5 (0 is the LSB and 5 is the MSB)
	IOM_PIN_7			GPIO pad input to FPC
	P33.7	O0	General-purpose output	
	GTM_TOUT29	O1	GTM muxed output	
	IOM_MON0_7		Monitor input 0	
	IOM_GTM_7		GTM-provided inputs to EXOR combiner	
	ASCLIN2_ASCLK	O2	Shift clock output	
	—	O3	Reserved	
	ASCLIN8_ATX	O4	Transmit output	
	—	O5	Reserved	
	—	O6	Reserved	
	—	O7	Reserved	

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-73 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
34	P33.8	I	FAST / HighZ / VEVR SB	General-purpose input
	GTM_TIM1_IN4_7			Mux input channel 4 of TIM module 1
	GTM_TIM0_IN4_7			Mux input channel 4 of TIM module 0
	ASCLIN2_ARXE			Receive input
	SCU_EMGSTOP_PORT_A			Emergency stop Port Pin A input request
	IOM_PIN_8			GPIO pad input to FPC
	P33.8	O0		General-purpose output
	GTM_TOUT30	O1		GTM muxed output
	IOM_MON0_8			Monitor input 0
	ASCLIN2_ATX	O2		Transmit output
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	—	O3		Reserved
	—	O4		Reserved
	CAN00_TXD	O5		CAN transmit output node 0
	IOM_MON2_5		Monitor input 2	
	IOM_REF2_5		Reference input 2	
	—	O6		Reserved
	CCU61_COUT62	O7		T12 PWM channel 62
	IOM_MON1_13		Monitor input 1	
IOM_REF1_8	Reference input 1			
SMU_FSP0	O		FSP[1..0] Output Signals - Generated by SMU_core	

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-73 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
35	P33.9	I	SLOW / PU1 / VEVRSB / ES5	General-purpose input
	GTM_TIM1_IN1_9			Mux input channel 1 of TIM module 1
	GTM_TIM0_IN1_9			Mux input channel 1 of TIM module 0
	QSPI3_HUSICINA			Highspeed capture channel
	IOM_PIN_9			GPIO pad input to FPC
	P33.9	O0	General-purpose output	
	GTM_TOUT31	O1	GTM muxed output	
	IOM_MON0_9		Monitor input 0	
	ASCLIN2_ATX	O2	Transmit output	
	IOM_MON2_14		Monitor input 2	
	IOM_REF2_14		Reference input 2	
	—	O3	Reserved	
	ASCLIN2_ASCLK	O4	Shift clock output	
	CAN01_TXD	O5	CAN transmit output node 1	
	IOM_MON2_6		Monitor input 2	
	IOM_REF2_6		Reference input 2	
	ASCLIN0_ATX	O6	Transmit output	
	IOM_MON2_12		Monitor input 2	
	IOM_REF2_12		Reference input 2	
	CCU61_CC62	O7	T12 PWM channel 62	
IOM_MON1_10	Monitor input 1			
IOM_REF1_11	Reference input 1			

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-73 Port 33 Functions (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
36	P33.10	I	FAST / PU1 / VEVR SB / ES5	General-purpose input
	GTM_TIM1_IN0_9			Mux input channel 0 of TIM module 1
	GTM_TIM0_IN0_9			Mux input channel 0 of TIM module 0
	QSPI3_HSICINB			Highspeed capture channel
	CAN01_RXDD			CAN receive input node 1
	ASCLIN0_ARXD			Receive input
	IOM_PIN_10			GPIO pad input to FPC
	P33.10	O0	General-purpose output	
	GTM_TOUT32	O1	GTM muxed output	
	IOM_MON0_10		Monitor input 0	
	QSPI1_SLSO6	O2	Master slave select output	
	—	O3	Reserved	
	ASCLIN1_ASLSO	O4	Slave select signal output	
	—	O5	Reserved	
	—	O6	Reserved	
	CCU61_COUT61	O7	T12 PWM channel 61	
	IOM_MON1_12		Monitor input 1	
	IOM_REF1_9		Reference input 1	
	SMU_FSP1	O	FSP[1..0] Output Signals - Generated by SMU_core	

Table 2-74 Analog Inputs

Pin	Symbol	Ctrl.	Buffer Type	Function
27	AN4	I	D / HighZ / VDDM	Analog Input 4
	EVADC_G0CH4			Analog input channel 4, group 0
	EVADC_G8CH8			Analog input channel 8, group 8
26	AN5	I	D / HighZ / VDDM	Analog Input 5
	EVADC_G0CH5			Analog input channel 5, group 0
	EVADC_G8CH9			Analog input channel 9, group 8
22	AN8	I	D / HighZ / VDDM	Analog Input 8
	EVADC_G1CH0			Analog input channel 0, group 1
	EVADC_G8CH12			Analog input channel 12, group 8
21	AN9	I	D / HighZ / VDDM	Analog Input 9
	EVADC_G1CH1			Analog input channel 1, group 1
	EVADC_G8CH13			Analog input channel 13, group 8
20	AN11	I	D / HighZ / VDDM	Analog Input 11
	EVADC_G1CH3			Analog input channel 3, group 1
	EVADC_G8CH15			Analog input channel 15, group 8

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-74 Analog Inputs (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
19	AN12	I	D / HighZ / VDDM	Analog Input 12
	EVADC_G1CH4			Analog input channel 4, group 1
18	AN13	I	D / HighZ / VDDM	Analog Input 13
	EVADC_G1CH5			Analog input channel 5, group 1
17	AN14	I	D / HighZ / VDDM	Analog Input 14
	EVADC_G1CH6			Analog input channel 6, group 1
16	AN15	I	D / HighZ / VDDM	Analog Input 15
	EVADC_G1CH7			Analog input channel 7, group 1
15	AN32/P40.4	I	S / HighZ / VDDM	Analog Input 32
	SENT_SENT4A			Receive input channel 4
	EVADC_G8CH0			Analog input channel 0, group 8
	CCU60_CCPOS2D			Hall capture input 2
14	AN33/P40.5	I	S / HighZ / VDDM	Analog Input 33
	SENT_SENT5A			Receive input channel 5
	EVADC_G8CH1			Analog input channel 1, group 8
	CCU61_CCPOS0D			Hall capture input 0
13	AN34	I	D / HighZ / VDDM	Analog Input 34
	EVADC_G8CH2			Analog input channel 2, group 8

Table 2-75 System I/O

Pin	Symbol	Ctrl.	Buffer Type	Function
38	VCAP1	I/O	—	External Switch Capacitor
39	VCAP0	I/O	—	External Switch Capacitor
43	XTAL1	I	XTAL / VEXT	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.
44	XTAL2	O	XTAL / VEXT	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
47	TMS	I	FAST /	JTAG Module State Machine Control Input
	DAP1	I/O	PD2 / VEXT	DAP: DAP1 Data I/O
49	$\overline{\text{TRST}}$	I	FAST / PU2 / VEXT	JTAG Module Reset/Enable Input
50	TCK	I	FAST /	JTAG Module Clock Input
	DAP0	I	PD2 / VEXT	DAP: DAP0 Clock Input

TC33x/TC32x Pin Definition and Functions: TQFP-80 Package Variant Pin

Table 2-75 System I/O (cont'd)

Pin	Symbol	Ctrl.	Buffer Type	Function
52	$\overline{\text{ESR1}}$	I/O	FAST / PU1 / VEXT	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
	PMS_ESR1WKP	I		ESR1 pin input
53	$\overline{\text{PORST}}$	I/O	PORST / PD / VEXT	PORST pin Power On Reset Input. Additional strong PD in case of power fail.

Table 2-76 Supply

Pin	Symbol	Ctrl.	Buffer Type	Function
24	VDDM	I	—	ADC Analog Power Supply (5V / 3.3V)
70	VDDP3	I	—	Flash Power Supply (3.3V)
23	VAREF1	I	—	Positive Analog Reference Voltage 1
28	VEVRSB	I	—	Standby Power Supply (5V / 3.3V) for the Standby SRAM
69	VEXT	I	—	External Power Supply (5V / 3.3V)
11	VDD	I	—	Digital Core Power Supply (1.25V)
12	VEXT	I	—	External Power Supply (5V / 3.3V)
71	VDD	I	—	Digital Core Power Supply (1.25V)
42	VDD	I	—	Digital Core Power Supply (1.25V)
54	VDD	I	—	Digital Core Power Supply (1.25V)
29	VDD	I	—	Digital Core Power Supply (1.25V)
37	VEXT	I	—	External Power Supply (5V / 3.3V)
40	VDDO	I	—	Switch capacitor EVRC Core regulator VDD supply output which shall be connected to other VDD pins externally on PCB level
E-PAD	VSS	I	—	Digital Ground
25	VSSM	I	—	Analog Ground for VDDM
45	VEXT	I	—	Digital Power Supply for Oscillator (shall be supplied with same level as used for VEXT), VEXT(OSC)

2.6 Sequence of Pads in Pad Frame for feature package L and LP
Table 2-77 Pad List

Number	Pad Name	Pad Type	X	Y	Comment
1	VSS	Vx	261999	185148	Supply Voltage
2	P15.0	FAST / PU1 / VEXT / ES	362997	185148	General-purpose I/O
3	VEXT	Vx	432297	338112	Supply Voltage
4	P15.1	FAST / PU1 / VEXT / ES	482697	185148	General-purpose I/O
5	P15.2	FAST / PU1 / VEXT / ES	533097	344106	General-purpose I/O
6	P15.3	FAST / PU1 / VEXT / ES	583497	185148	General-purpose I/O
7	P15.4	FAST / PU1 / VEXT / ES	633897	344106	General-purpose I/O
8	P15.5	FAST / PU1 / VEXT / ES	684297	185148	General-purpose I/O
9	P15.6	FAST / PU1 / VEXT / ES	734697	344106	General-purpose I/O
10	P15.7	FAST / PU1 / VEXT / ES	781695	185148	General-purpose I/O
11	P15.8	FAST / PU1 / VEXT / ES	828693	344106	General-purpose I/O
12	VSS	Vx	875691	185148	Supply Voltage
13	VEXT	Vx	940689	338112	Supply Voltage
14	VSS	Vx	987687	185148	Supply Voltage
15	VDD	Vx	1034685	338112	Supply Voltage
16	P14.0	FAST / PU1 / VEXT / ES2	1081683	185148	General-purpose I/O
17	P14.1	FAST / PU1 / VEXT / ES2	1128681	344106	General-purpose I/O
18	P14.2	SLOW / PU2 / VEXT / ES	1175679	185148	General-purpose I/O
19	P14.3	SLOW / PU2 / VEXT / ES	1222677	344106	General-purpose I/O
20	P14.4	SLOW / PU2 / VEXT / ES	1269675	185148	General-purpose I/O
21	P14.5	FAST / PU2 / VEXT / ES	1316673	344106	General-purpose I/O
22	VSS	Vx	1381671	185148	Supply Voltage
23	P14.6	FAST / PU1 / VEXT / ES	1443267	344106	General-purpose I/O
24	RESERVED	Vx	1490265	185148	OTPMust be bonded to VSS

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
25	VEXT	Vx	1537263	344106	Supply Voltage
26	VEXT	Vx	1611261	185148	Supply Voltage
27	VEXT	Vx	1685259	344106	Supply Voltage
28	VSS	Vx	1732257	185148	Supply Voltage
29	No PAD	—	1846485	344106	Supply Voltage
30	VDDP3	Vx	1914255	185148	Supply Voltage
31	VDDP3	Vx	1979253	344106	Supply Voltage
32	VDDP3	Vx	2053251	185148	Supply Voltage
33	VDD	Vx	2136249	344106	Supply Voltage
34	VDD	Vx	2228247	185148	Supply Voltage
35	VDD	Vx	2320245	344106	Supply Voltage
36	VSS	—	2394243	185148	Supply Voltage
37	P14.7	SLOW / PU1 / VEXT / ES	2468241	338112	General-purpose I/O
38	P14.8	SLOW / PU1 / VEXT / ES	2515239	175644	General-purpose I/O
39	P14.9	FAST / PU1 / VEXT / ES	2562237	322614	General-purpose I/O
40	P14.10	FAST / PU1 / VEXT / ES	2609235	175644	General-purpose I/O
41	P13.0	FAST / PU1 / VEXT / ES6	2656233	344106	General-purpose I/O
42	P13.1	FAST / PU1 / VEXT / ES6	2703231	185148	General-purpose I/O
43	P13.2	FAST / PU1 / VEXT / ES6	2750229	344106	General-purpose I/O
44	P13.3	FAST / PU1 / VEXT / ES6	2797227	185148	General-purpose I/O
45	VDDP_3V3_F LVIO	—	2844225	344106	Supply Voltage
46	VSS	Vx	2927439	185148	Supply Voltage
47	VFLEX	Vx	2974437	344106	Supply Voltage
48	P11.2	FAST / PU1 / VFLEX / ES	3021435	185148	General-purpose I/O
49	P11.3	FAST / PU1 / VFLEX / ES	3068433	344106	General-purpose I/O
50	P11.6	FAST / PU1 / VFLEX / ES	3115431	185148	General-purpose I/O
51	P11.9	FAST / PU1 / VFLEX / ES	3162429	344106	General-purpose I/O

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
52	P11.8	SLOW / PU1 / VFLEX / ES	3209427	185148	General-purpose I/O
53	VDD	Vx	3256425	338112	Supply Voltage
54	VSS	Vx	3346623	185148	Supply Voltage
55	P11.10	FAST / PU1 / VFLEX / ES	3417021	344106	General-purpose I/O
56	P11.11	FAST / PU1 / VFLEX / ES	3464019	185148	General-purpose I/O
57	P11.12	FAST / PU1 / VFLEX / ES	3511017	344106	General-purpose I/O
58	VSS	Vx	3585231	185148	Supply Voltage
59	VEXT	Vx	3632229	338112	Supply Voltage
60	VDD	Vx	3750795	338112	Supply Voltage
61	VSS	Vx	3848499	185148	Supply Voltage
62	P10.0	FAST / PU1 / VEXT / ES	3962241	338112	General-purpose I/O
63	P10.1	FAST / PU1 / VEXT / ES	4012641	185148	General-purpose I/O
64	P10.2	FAST / PU1 / VEXT / ES	4063041	344106	General-purpose I/O
65	P10.3	FAST / PU1 / VEXT / ES	4113441	185148	General-purpose I/O
66	P10.4	FAST / PU1 / VEXT / ES	4163841	338112	General-purpose I/O
67	P10.5	SLOW / PU2 / VEXT / ES	4233141	185148	General-purpose I/O
68	P10.6	SLOW / PU2 / VEXT / ES	4333941	185148	General-purpose I/O
69	P10.7	SLOW / PU1 / VEXT / ES	4413996	293499	General-purpose I/O
70	P10.8	SLOW / PU1 / VEXT / ES	4413996	394497	General-purpose I/O
71	VEXT	Vx	4251528	486495	Supply Voltage
72	VSS	Vx	4404492	536895	Supply Voltage
73	P02.0	FAST / PU1 / VEXT / ES	4245534	587295	General-purpose I/O
74	P02.1	SLOW / PU1 / VEXT / ES	4404492	637695	General-purpose I/O
75	P02.2	FAST / PU1 / VEXT / ES	4245534	688095	General-purpose I/O
76	P02.3	SLOW / PU1 / VEXT / ES	4404492	735093	General-purpose I/O

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
77	P02.4	FAST / PU1 / VEXT / ES	4245534	796491	General-purpose I/O
78	P02.5	FAST / PU1 / VEXT / ES	4404492	843489	General-purpose I/O
79	P02.6	FAST / PU1 / VEXT / ES	4245534	890487	General-purpose I/O
80	P02.7	FAST / PU1 / VEXT / ES	4404492	937485	General-purpose I/O
81	P02.8	SLOW / PU1 / VEXT / ES	4245534	984483	General-purpose I/O
82	VSS	Vx	4404492	1085481	Supply Voltage
83	VDD	Vx	4245534	1193499	Supply Voltage
84	VDD	Vx	4404492	1312497	Supply Voltage
85	VDD	Vx	4245534	1431495	Supply Voltage
86	VSS	—	4404492	1550493	Supply Voltage
87	VEXT	Vx	4251528	1660491	Supply Voltage
88	VSS	Vx	4404492	1707489	Supply Voltage
89	VDD	Vx	4251528	1806687	Supply Voltage
90	VSS	Vx	4404492	1916685	Supply Voltage
91	P00.0	FAST / PU1 / VEXT / ES	4245534	2026683	General-purpose I/O
92	VSS	Vx	4404492	2136681	Supply Voltage
93	VDD	Vx	4251528	2246679	Supply Voltage
94	P00.1	SLOW / PU1 / VEXT / ES	4404492	2406870	General-purpose I/O
95	P00.2	SLOW / PU1 / VEXT / ES1	4245534	2453868	General-purpose I/O
96	P00.3	SLOW / PU1 / VEXT / ES1	4404492	2500866	General-purpose I/O
97	P00.4	SLOW / PU1 / VEXT / ES1	4245534	2547864	General-purpose I/O
98	P00.5	SLOW / PU1 / VEXT / ES1	4404492	2594862	General-purpose I/O
99	P00.6	SLOW / PU1 / VEXT / ES1	4245534	2641860	General-purpose I/O
100	P00.7	SLOW / PU1 / VEXT / ES1	4404492	2688858	General-purpose I/O
101	P00.8	SLOW / PU1 / VEXT / ES1	4245534	2735856	General-purpose I/O
102	P00.9	SLOW / PU1 / VEXT / ES1	4404492	2782854	General-purpose I/O

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
103	P00.10	SLOW / PU1 / VEXT / ES1	4245534	2829852	General-purpose I/O
104	P00.11	SLOW / PU1 / VEXT / ES1	4404492	2876850	General-purpose I/O
105	P00.12	SLOW / PU1 / VEXT / ES1	4245534	2923848	General-purpose I/O
106	VSS	Vx	4404492	2970846	Supply Voltage
107	VSS	Vx	4404492	3059838	Supply Voltage
108	VDD	Vx	4245534	3106836	Supply Voltage
109	VDD	Vx	4404492	3162834	Supply Voltage
110	VEXT	Vx	4245534	3209832	Supply Voltage
111	VEXT	Vx	4404492	3256830	Supply Voltage
112	AN39/P40.9	S / HighZ / VDDM	4245534	3331044	Analog Input 39
113	AN38/P40.8	S / HighZ / VDDM	4404492	3378042	Analog Input 38
114	AN37/P40.7	S / HighZ / VDDM	4245534	3425040	Analog Input 37
115	AN36/P40.6	S / HighZ / VDDM	4404492	3472038	Analog Input 36
116	AN35	D / HighZ / VDDM	4245534	3519036	Analog Input 35
117	AN34	D / HighZ / VDDM	4404492	3566034	Analog Input 34
118	AN33/P40.5	S / HighZ / VDDM	4245534	3619035	Analog Input 33
119	AN32/P40.4	S / HighZ / VDDM	4404492	3666033	Analog Input 32
120	AN15	D / HighZ / VDDM	4245534	3719034	Analog Input 15
121	AN14	D / HighZ / VDDM	4404492	3766032	Analog Input 14
122	AN13	D / HighZ / VDDM	4245534	3819033	Analog Input 13
123	AN12	D / HighZ / VDDM	4404492	3866031	Analog Input 12
124	AN11	D / HighZ / VDDM	4404492	3978522	Analog Input 11
125	AN10	D / HighZ / VDDM	4320522	4062492	Analog Input 10
126	AN9	D / HighZ / VDDM	4220523	4062492	Analog Input 9

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
127	AN8	D / HighZ / VDDM	4120524	4062492	Analog Input 8
128	AN7	D / HighZ / VDDM	4020525	4062492	Analog Input 7
129	VAREF0	Vx	3973527	3903534	Supply Voltage
130	VAGND0	Vx	3920526	4062492	Supply Voltage
131	VDDM	Vx	3873528	3903534	Supply Voltage
132	VSSM	Vx	3826530	4062492	Supply Voltage
133	VDDM	Vx	3779532	3903534	Supply Voltage
134	VSSM	Vx	3732534	4062492	Supply Voltage
135	AN6	D / HighZ / VDDM	3685536	3903534	Analog Input 6
136	AN5	D / HighZ / VDDM	3638538	4062492	Analog Input 5
137	AN4	D / HighZ / VDDM	3591540	3903534	Analog Input 4
138	AN3	D / HighZ / VDDM	3544542	4062492	Analog Input 3
139	AN2	D / HighZ / VDDM	3497544	3903534	Analog Input 2
140	AN1	D / HighZ / VDDM	3450546	4062492	Analog Input 1
141	AN0	D / HighZ / VDDM	3403548	3903534	Analog Input 0
142	VSS	Vx	3277593	4062492	Supply Voltage
143	VDD	Vx	3203595	3909528	Supply Voltage
144	VEVRSB	Vx	3147597	4062492	Supply Voltage
145	VEVRSB	Vx	3100599	3903534	Supply Voltage
146	VSS	Vx	3053601	4062492	Supply Voltage
147	VSS	Vx	2952603	4062492	Supply Voltage
148	VDD	Vx	2905605	3903534	Supply Voltage
149	VDD	Vx	2858607	4062492	Supply Voltage
150	VDD	Vx	2764611	3903534	Supply Voltage
151	VSS	Vx	2717613	4062492	Supply Voltage
152	P34.1	SLOW / PU1 / VEVRSB / ES5	2655315	3903534	General-purpose I/O
153	P34.2	SLOW / PU1 / VEVRSB / ES	2608317	4062492	General-purpose I/O
154	P34.3	SLOW / PU1 / VEVRSB / ES	2561319	3903534	General-purpose I/O

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
155	P33.0	SLOW / PU1 / VEVRSB / ES5	2449323	4062492	General-purpose I/O
156	P33.1	SLOW / PU1 / VEVRSB / ES5	2402325	3903534	General-purpose I/O
157	P33.2	SLOW / PU1 / VEVRSB / ES5	2355327	4062492	General-purpose I/O
158	P33.3	SLOW / PU1 / VEVRSB / ES5	2308329	3903534	General-purpose I/O
159	P33.4	SLOW / PU1 / VEVRSB / ES5	2261331	4062492	General-purpose I/O
160	P33.5	SLOW / PU1 / VEVRSB / ES5	2214333	3903534	General-purpose I/O
161	P33.6	SLOW / PU1 / VEVRSB / ES5	2167335	4062492	General-purpose I/O
162	P33.7	SLOW / PU1 / VEVRSB / ES5	2120337	3903534	General-purpose I/O
163	VSS	Vx	2037339	4062492	Supply Voltage
164	VDD	Vx	1990341	3909528	Supply Voltage
165	P33.8	FAST / HighZ / VEVRSB	1943343	4062492	General-purpose I/O
166	P33.9	SLOW / PU1 / VEVRSB / ES5	1896345	3903534	General-purpose I/O
167	P33.10	FAST / PU1 / VEVRSB / ES5	1849347	4062492	General-purpose I/O
168	P33.11	FAST / PU1 / VEVRSB / ES5	1802349	3903534	General-purpose I/O
169	VSS	Vx	1755351	4062492	Supply Voltage
170	P33.12	FAST / PU1 / VEVRSB / ES5	1708353	3903534	General-purpose I/O
171	VEVRSB	Vx	1661355	4071996	Supply Voltage
172	VSS	Vx	1559655	4062492	Supply Voltage
174	VEXT	Vx	1412055	3903534	Supply Voltage

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
175	VEXT	Vx	1358955	4062492	Supply Voltage
176	VEXT	Vx	1300455	3903534	Supply Voltage
177	VCAP1	Vx	1247355	4062492	
178	VCAP1	Vx	1194255	3903534	
181	VCAP0	Vx	993555	3903534	
182	VCAP0	Vx	940455	4062492	
184	VDD	Vx	745119	3903534	Supply Voltage
185	VDD	Vx	692001	4062492	Supply Voltage
186	VDD	Vx	638883	3903534	Supply Voltage
187	VSS	Vx	585765	4062492	Supply Voltage
188	VSS	Vx	484695	4062492	Supply Voltage
190	P32.4	FAST / PU1 / VEXT / ES	255699	4071996	General-purpose I/O
191	P23.5	FAST / PU1 / VEXT / ES	175644	3973941	General-purpose I/O
192	P23.1	FAST / PU1 / VEXT / ES	185148	3872943	General-purpose I/O
193	VSS	Vx	185148	3771945	Supply Voltage
194	P22.0	FAST / PU1 / VEXT / ES6	185148	3670947	General-purpose I/O
195	VSS	Vx	185148	3569949	Supply Voltage
196	P22.1	FAST / PU1 / VEXT / ES6	344106	3509451	General-purpose I/O
197	P22.2	FAST / PU1 / VEXT / ES6	185148	3459051	General-purpose I/O
198	P22.3	FAST / PU1 / VEXT / ES6	344106	3408651	General-purpose I/O
199	P22.4	FAST / PU1 / VEXT / ES	175644	3361653	General-purpose I/O
200	VEXT	Vx	344106	3314655	Supply Voltage
201	VSS	Vx	185148	3213657	Supply Voltage
202	VDD	Vx	344106	3103659	Supply Voltage
203	VDD	Vx	185148	2993661	Supply Voltage
204	VDD	Vx	362646	2867337	Supply Voltage
205	VSS	Vx	185148	2817927	Supply Voltage
206	XTAL1	XTAL / VEXT	185148	2660778	XTAL pad1 XTAL1. Main Oscillator/PLL/Clock Generator Input.

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
207	XTAL2	XTAL / VEXT	185148	2561778	XTAL pad2 XTAL2. Main Oscillator/PLL/Clock Generator OUTPUT
208	VSS	Vx	185148	2404629	Supply Voltage
209	VEXT	Vx	362646	2355219	Supply Voltage
210	VEXT	Vx	344106	2224341	Supply Voltage
211	VSS	Vx	185148	2177343	Supply Voltage
212	P21.0	FAST / PU1 / VEXT / ES	338112	2130345	General-purpose I/O
213	P21.1	FAST / PU1 / VEXT / ES	175644	2083347	General-purpose I/O
214	P21.2	FAST / PU1 / VEXT / ES	344106	2036349	General-purpose I/O
215	P21.3	FAST / PU1 / VEXT / ES	185148	1989351	General-purpose I/O
216	P21.4	FAST / PU1 / VEXT / ES6	344106	1942353	General-purpose I/O
217	P21.5	FAST / PU1 / VEXT / ES6	185148	1895355	General-purpose I/O
218	VDD	Vx	338112	1848357	Supply Voltage
219	VSS	Vx	185148	1787859	Supply Voltage
220	P21.6/TDI	FAST / PD / PU2 / VEXT / ES3	344106	1727361	General-purpose I/O PD during Reset and in DAP/DAPE or JTAG mode. After Reset release and when not in DAP/DAPE or JTAG mode: PU. In Standby mode: HighZ.
221	TMS	FAST / PD2 / VEXT	185148	1680363	JTAG Module State Machine Control Input
222	P21.7/TDO	FAST / PU2 / VEXT / ES4	344106	1633365	General-purpose I/O
223	$\overline{\text{TRST}}$	FAST / PU2 / VEXT	185148	1586367	JTAG Module Reset/Enable Input
224	TCK	FAST / PD2 / VEXT	344106	1539369	JTAG Module Clock Input
225	VEXT	Vx	185148	1492371	Supply Voltage
226	P20.0	FAST / PU1 / VEXT / ES	344106	1445373	General-purpose I/O
227	VSS	Vx	185148	1398375	Supply Voltage
228	P20.1	SLOW / PU1 / VEXT / ES	338112	1342377	General-purpose I/O

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame
Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
229	P20.2	S / PU / VEXT	185148	1295379	General-purpose I/O This pin is latched at power on reset release to enter test mode.
230	P20.3	SLOW / PU1 / VEXT / ES	344106	1248381	General-purpose I/O
231	$\overline{\text{ESR1}}$	FAST / PU1 / VEXT	185148	1201383	ESR1 Port Pin input - can be used to trigger a reset or an NMI ESR1: External System Request Reset 1. Default NMI function. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
232	$\overline{\text{PORST}}$	PORST / PD / VEXT	344106	1154385	PORST pin Power On Reset Input. Additional strong PD in case of power fail.
233	$\overline{\text{ESR0}}$	FAST / OD / VEXT	185148	1107387	ESR0 Port Pin input - can be used to trigger a reset or an NMI ESR0: External System Request Reset 0. Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset. This is valid additionally after deactivation of PORST_N until the internal reset phase has finished. See also SCU chapter for details. Default after power-on can be different. See also SCU chapter 'Reset Control Unit' and SCU_IOCRR register description. PMS_EVRWUP: EVR Wakeup Pin
234	VDD	Vx	344106	1060389	Supply Voltage
235	VDD	Vx	185148	995391	Supply Voltage
236	VDD	Vx	344106	921393	Supply Voltage

TC33x/TC32x Pin Definition and Functions: Sequence of Pads in Pad Frame

Table 2-77 Pad List (cont'd)

Number	Pad Name	Pad Type	X	Y	Comment
237	VSS	Vx	185148	874395	Supply Voltage
238	P20.6	SLOW / PU1 / VEXT / ES	344106	755541	General-purpose I/O
239	P20.7	FAST / PU1 / VEXT / ES	185148	705141	General-purpose I/O
240	P20.8	FAST / PU1 / VEXT / ES	344106	654741	General-purpose I/O
241	P20.9	FAST / PU1 / VEXT / ES	185148	604341	General-purpose I/O
242	P20.10	FAST / PU1 / VEXT / ES	344106	553941	General-purpose I/O
243	P20.11	FAST / PU1 / VEXT / ES	185148	503541	General-purpose I/O
244	P20.12	FAST / PU1 / VEXT / ES	344106	453141	General-purpose I/O
245	P20.13	FAST / PU1 / VEXT / ES	185148	383841	General-purpose I/O
246	P20.14	FAST / PU1 / VEXT / ES	185148	283041	General-purpose I/O

Whenever in table of section 3 'Electrical Specification' the term 'neighbor pads' is used, the detailed definition is provided by [Figure 2-77](#). This statement is also valid for next/nearest neighbor pads.

In order to find out who is affecting operation on a target pad (interfering) a number of active close-neighbor pads (ACNP) has to be defined.

Finding close-neighbor pads:

The Pad Ring has four edges: bottom, left, top, right. Each edge is limited, i.e. it has two ends.

Each pad has two direct (first) neighbors unless it is located at the end of the edge. In that case it only has one neighbor. Similarly, each pad has two indirect (second) neighbors unless it or its first neighbor is located at the end of the edge. These first and second neighbors we will collectively call Close-Neighbor pads. Therefore each pad has 2 to 4 close-neighbor pads.

Finding close-neighbors can be done with the following sequence:

- 1.) Choose a target pad and lookup its "X" and "Y" coordinates in tables [Figure 2-77](#).
- 2.) Find first and second neighbors by calculating "X" and "Y" distance from the selected pad. [Figure 2-77](#) is sorted by "Y" coordinate, which might help locate the 4 close-neighbor candidates (if the pad is near the edge, it might end up with less than 4 close-neighbors).

Defining active pads:

Pad is active if it is currently in use and if it doesn't have "Vxx" in the name.

Figuring out number of active close-neighbor pads follow next rules:

- If the first neighbor is active, then we count it and also check if second neighbor (on the same side of selected pad) is active.
- If the first neighbor is not active, then we do not check the second on the same side.

2.7 Legend

The data in this chapter 2 match with the file TC33xpd_IO_Spirit_v1.0.0.1.17.xml.

Column "Ctrl.":

I = Input (for GPIO port lines with IOCR bit field Selection PCx = 0XXX_B)

O = Output (for GPIO port lines the 'O' represents in most cases the port HWOUT function)

O0 = Output with IOCR bit field selection PCx = 1X000_B

O1 = Output with IOCR bit field selection PCx = 1X001_B (ALT1)

O2 = Output with IOCR bit field selection PCx = 1X010_B (ALT2)

O3 = Output with IOCR bit field selection PCx = 1X011_B (ALT3)

O4 = Output with IOCR bit field selection PCx = 1X100_B (ALT4)

O5 = Output with IOCR bit field selection PCx = 1X101_B (ALT5)

O6 = Output with IOCR bit field selection PCx = 1X110_B (ALT6)

O7 = Output with IOCR bit field selection PCx = 1X111_B (ALT7)

Column "Buffer Type":

FAST = Pad class FAST (5V/3.3V)

SLOW = Pad class SLOW (5V/3.3V)

LVDS_TX = Pad class LVDS Transmit

LVDS_RX = Pad class LVDS Receive

S = Pad class S (Analog Input overlaid with General Purpose Input)

D = Pad class D (Analog Input)

Porst = Porst input Pad

XTAL1 = XTAL1 input Pad

XTAL2 = XTAL2 input Pad

PU = with pull-up device connected during reset ($\overline{\text{PORST}} = 0$)

PU1 = with pull-up device connected during reset ($\overline{\text{PORST}} = 0$)¹⁾

PU2 = with pull-up device connected during startup and reset, HighZ in Standby mode

PD = with pull-down device connected during reset ($\overline{\text{PORST}} = 0$)

PD1 = with pull-down device connected during reset ($\overline{\text{PORST}} = 0$)¹⁾

PD2 = with pull-down device connected during startup and reset, HighZ in Standby mode

OD = open drain during reset ($\overline{\text{PORST}} = 0$)

ES = Supports Emergency Stop

ES1 = ES. ES can be overruled by VADC, control via P00_PCSR

ES2 = ES. ES can be overruled by DXCPL - DAP over CAN physical layer, No overruling for DXCM - Debug over CAN message

ES3 = ES. ES can be overruled by JTAG mode if this pin is used as TDI

ES4 = ES. ES can be overruled by JTAG or Three Pin DAP mode

ES5 = ES. ES can be overruled by the Standby Controller - SCR - if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR

1) The default state of GPIOs (Px.y) during and after PORST active is controlled via HWCFG6 (P14.4). Pls. see also chapter PMS, HWCFG[6].

TC33x/TC32x Pin Definition and Functions:Legend

ES6 = ES. On LVDS TX pads the ES affects the pads only in CMOS mode, not in LVDS mode. Thus, only when LPCRx.TX_EN selects the CMOS Mode, the output is switched off in the ES event.

3 Electrical Specification

3.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC33x/TC32x and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column "Symbol":

- **CC**
Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC33x/TC32x and must be regarded for a system design.
- **SR**
Such parameters indicate **S**ystem **R**equirements which must be provided by the microcontroller system in which the TC33x/TC32x designed in.

Electrical Specification Absolute Maximum Ratings

3.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the Operational Conditions of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Storage Temperature	T_{ST} SR	-65	-	150	°C	upto 65h @ $T_J = 150^\circ\text{C}$
Voltage at V_{DD} power supply pins with respect to V_{SS} ^{1) 2)}	V_{DD} SR	-	-	1.65	V	upto 2.8h
		-	-	1.45	V	upto 72h
Voltage at V_{DDP3} power supply pins with respect to V_{SS}	V_{DDP3} SR	-	-	4.43	V	
Voltage at V_{DDM} , V_{EXT} , V_{FLEX} and $V_{EVR SB}$ power supply pins with respect to V_{SS}	V_{DDM} SR	-	-	6.75	V	upto 2.8h
		-	-	5.6	V	upto 72h
Voltage on all other input pins with respect to V_{SS} ³⁾	V_{IN} SR	-0.7	-	6.75	V	
Voltage on all analog and class S input pins with respect to V_{SS} ³⁾	V_{IN} SR	-0.7	-	6.75	V	
Input current on any pin during overload condition ^{4) 5)}	I_{IN} SR	-10	-	10	mA	
Absolute maximum sum of all input circuit currents during overload condition. ⁴⁾	ΣI_{IN} SR	-100	-	100	mA	

- 1) Valid for cumulated for up to 2.8h and pulse forms followed a power supply switch on phase, where the rise and fall times are related to the system capacities and coils.
- 2) Due to EVRC output voltage oscillation during switch off phase V_{DD} can drop down to -0.72V. For V_{DD} an input level down to -0.72V during switch off phase will not cause any damage or reliability problem.
- 3) Voltages below V_{INmin} have no impact to the device reliability as long as the times and currents defined in section Pin Reliability in Overload for the affected pad(s) are not violated.
- 4) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device.
- 5) The specified min. and max. values represent the current limits, which have to be maintained, in case of a short circuit condition on the output of any Fast, RFast, Slow and Class S pad, not being used during operation. This covers also output currents due to switching in operation for $C_L=200\text{pF}$.

3.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

The following table defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- allowed time interval (defined in Note column) for overload condition is not exceeded. If no time limit is defined the allowed time includes both 'Operation Lifetime hours' and 'Inactive Lifetime hours'. The number of hours in [Table 3-50](#) and [Table 3-51](#) are examples only and the applicable numbers are defined by the customer profiles accepted by Infineon.
- **Operating Conditions** are met for
 - pad supply levels
 - temperature

If a pin current is out of the **Operating Conditions** but within the overload parameters, then the parameters functionality of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Table 3-2 Overload Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current on any digital pin during overload condition	I_{IN}	-5	-	5	mA	except LVDS pins
		-15 ¹⁾	-	15 ¹⁾	mA	except LVDS pins; limited to max. 20 pulses with 1ms pulse length
Input current on LVDS pin during overload condition	I_{INLVDS}	-3	-	3	mA	
Input current on analog input pin during overload condition	I_{INANA}	-3	-	3	mA	
		-5	-	5	mA	limited to 60h over lifetime
Absolute sum of all analog input currents for analog inputs during overload condition	I_{INSA}	-20	-	20	mA	
Absolute maximum sum of all input circuit currents during overload condition (digital and analog combined)	ΣI_{INS}	-100	-	100	mA	
Signal voltage over/undershoot at GPIOs	V_{OUS}	$V_{SS} - 2$	-	$V_{EXT/FLEX} + 2$	V	limited to 60h over lifetime; Valid for non LVDS and analog pads
Sum of all inactive device pin currents	I_{IDS}	-100	-	100	mA	
Static pin output current	$I_{OUT\ CC}$	-	-	2.5	mA	100% duty cycle; output driver = medium
		-	-	5	mA	100% duty cycle; output driver = strong

Electrical Specification Pin Reliability in Overload

Table 3-2 Overload Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for digital inputs, negative	$K_{OV\text{DN}}$ CC	-	-	$3 \cdot 10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor fast pads; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	$1 \cdot 10^{-4}$		Overload injected on GPIO non LVDS pad and affecting neighbor slow pads; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
Overload coupling factor for digital inputs, positive	$K_{OV\text{DP}}$ CC	-	-	$1.5 \cdot 10^{-3}$		Overload injected on GPIO non LVDS pad and affecting neighbor GPIO non LVDS pads
Overload coupling factor for analog inputs, negative ²⁾	$K_{OV\text{AN}}$ CC	-	-	$1 \cdot 10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
		-	-	$1 \cdot 10^{-5}$		else; $-5\text{mA} < I_{\text{IN}} < 0\text{mA}$
Overload coupling factor for analog inputs, positive ²⁾	$K_{OV\text{AP}}$ CC	-	-	$2 \cdot 10^{-4}$		Analog inputs overlaid with slow pads or pull down diagnostics; $0\text{mA} < I_{\text{IN}} < 5\text{mA}$
		-	-	$2 \cdot 10^{-5}$		else; $0\text{mA} < I_{\text{IN}} < 5\text{mA}$

1) Reduced VADC result accuracy and / or GPIO input levels (V_{IL} and V_{IH}) can differ from specified parameters.

2) Overload coupling on analog inputs is caused by parasitic effects between pads, input multiplexers and surrounding structures. The given parameters have been verified for all permutations of channels. Also watch multiple connections of a pin to several channels.

3.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC33x/TC32x. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC33x/TC32x must be static regulated voltages.

All parameters specified in the following tables refer to these operating conditions (see table below), unless otherwise noticed in the Note / Test Condition column.

Table 3-3 Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SRI frequency	f_{SRI} SR	-	-	300	MHz	
CPU Frequency (All CPUs)	f_{CPUx} SR	-	-	300	MHz	
PLL0 output frequency	f_{PLL0} SR	20	-	300	MHz	
SPB frequency	f_{SPB} SR	-	-	100	MHz	
FSI2 frequency	f_{FSI2} SR	-	-	300	MHz	
FSI frequency	f_{FSI} SR	20	-	100	MHz	
GTM frequency	f_{GTM} SR	-	-	200	MHz	
STM frequency	f_{STM} SR	-	-	100	MHz	
ERAY frequency	f_{ERAY} SR	-	80	-	MHz	
BBB frequency	f_{BBB} SR	-	-	150	MHz	
VADC frequency	f_{ADC} SR	-	-	160	MHz	
ASCLIN Operating Frequency	$f_{ASCLINx}$ SR	-	-	200	MHz	
CAN frequency	f_{CAN} SR	-	-	80	MHz	
PLL1 output frequency from PER PLL	f_{PLL1} SR	20	-	320	MHz	
PLL2 output frequency from PER PLL	f_{PLL2} SR	20	-	200	MHz	
QSPI Frequency	f_{QSPI} SR	-	-	200	MHz	
MCANH frequency	f_{MCANH} CC	-	-	100	MHz	
Ambient Temperature	T_A SR	-40	-	125	°C	valid for all SAK products
		-40	-	150	°C	valid for all SAL products with package
		-40	-	170	°C	valid for all SAL products without package
Junction Temperature	T_J SR	-40	-	150	°C	valid for all SAK products
		-40	-	170	°C	valid for all SAL products
Core Supply Voltage	V_{DD} SR	1.125 ¹⁾	1.25	1.375 ²⁾	V	
ADC analog supply voltage	V_{DDM} SR	2.97	5.0	5.5 ³⁾	V	

Electrical Specification Operating Conditions
Table 3-3 Operating Conditions (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Digital external supply voltage for pads and EVR	V_{EXT} SR	4.5	5.0	5.5 ³⁾	V	Nominal 5V Pad / Port Pin supply range. 5V pad parameters are valid.
		2.97	3.3	3.63	V	Nominal 3.3V Pad / Port Pin supply range with VDDP3 supplied externally and EVR33 inactive. 3.3V pad parameters are valid.
		3.6	-	4.5	V	Flash configured in cranking mode; Flash read operation with reduced performance. EVR33 active in low voltage mode. 3.3V pad parameters are valid.
		2.97	-	3.6	V	Incase EVR33 is active, Flash configured in sleep mode and execution switched to RAM. 3.3V pad parameters are valid.
Digital supply voltage for Flex port	V_{FLEX} SR	2.97	-	4.0	V	3.3V pad parameters are valid
		4.5	5.0	5.5 ³⁾	V	5V pad parameters are valid
Digital supply voltage for Flash	V_{DDP3} SR	2.97	3.3	3.63 ⁴⁾	V	
		2.6	-	3.63	V	Flash configured in cranking mode; Flash read operation with reduced performance.
Digital ground voltage	V_{SS} SR	0	-	-	V	
Analog ground voltage for V_{DDM}	V_{SSM} CC	-0.1	0	0.1	V	
Digital external supply voltage for EVR and during Standby mode	V_{EVRSB} SR	2.97 ⁵⁾	-	5.5	V	V_{EVRSB} is bonded together with V_{EXT} supply pin in smaller LQFP packages.
Voltage to ensure defined pad states	V_{DDPPA} CC	1.3 ⁶⁾	-	-	V	

1) For V_{DD} $1.08V \leq V_{DD} < 1.125V$ operation is still possible but with relaxed parameters.

2) Voltage overshoot to 1.69V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.

Electrical Specification Operating Conditions

- 3) Voltage overshoot to 6.5V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
- 4) Voltage overshoot to 4.29V is permissible, provided the duration is less than 2h cumulated. Reduced ADC accuracy and leakage is increased.
- 5) V_{EVRSB} supply voltage can drop down upto 2.6V during Standby mode. It is required to have a capacitor of 100nF on V_{EVRSB} supply pin.
- 6) HWCFG[6] pin is latched and pull-up or tristate is activated at Port pins when VEXT has reached this level.

Limitation of Supply Voltage over Time

The maximum operation voltage for $V_{\text{EXT/FLEX/DDM}}$ supply rails is limited over the complete lifetime.

The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-4 Example Voltage Profile

$V_{\text{EXT/FLEX/DDM}}$	Duration [h]
$5.4 \text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 5.5 \text{ V}$	$\leq 5\%$ of lifetime
$5.15 \text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 5.4 \text{ V}$	$\leq 15\%$ of lifetime
$4.85 \text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 5.15 \text{ V}$	$\leq 60\%$ of lifetime
$4.6 \text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 4.85 \text{ V}$	$\leq 15\%$ of lifetime
$4.5 \text{ V} < V_{\text{EXT/FLEX/DDM}} \leq 4.6 \text{ V}$	$\leq 5\%$ of lifetime

The maximum operation voltage for V_{DD} supply rails is limited over the complete lifetime.

The following voltage profile is an example. Application specific voltage profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-5 Example Voltage Profile

V_{DD}	Duration [h]
$1.325 \text{ V} < V_{\text{DD}} \leq 1.375 \text{ V}$	$\leq 5\%$ of lifetime
$1.275 \text{ V} < V_{\text{DD}} \leq 1.325 \text{ V}$	$\leq 15\%$ of lifetime
$1.225 \text{ V} < V_{\text{DD}} \leq 1.275 \text{ V}$	$\leq 60\%$ of lifetime
$1.175 \text{ V} < V_{\text{DD}} \leq 1.225 \text{ V}$	$\leq 15\%$ of lifetime
$1.125 \text{ V} < V_{\text{DD}} \leq 1.175 \text{ V}$	$\leq 5\%$ of lifetime

3.5 5 V / 3.3 V switchable Pads

Pad classes slow GPIO and fast GPIO support both Automotive Level (AL) or TTL level (TTL) operation. Parameters are defined for AL operation and degrade in TTL operation.

Table 3-6 $\overline{\text{PORST}}$ Pad

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
$\overline{\text{PORST}}$ pad Output current	I_{PORST} CC	13	-	-	mA	$V_{\text{EXT}} = 2.97\text{V}$; $V_{\text{PORST}} = 0.9\text{V}$
Spike filter always blocked pulse duration	t_{SF1} CC	-	-	80	ns	
Spike filter pass-through blocked pulse duration	t_{SF2} CC	260	-	-	ns	without additional $\overline{\text{PORST}}$ Digital Filter active ($\text{PORSTDF} = 0$).
Input hysteresis ¹⁾	HYS CC	$0.055 * V_{\text{EXT}}$	-	-	V	non of the neighbor pads are used as output; TTL (degraded, used for CIF)
Pull-down current ²⁾	I_{PDL} CC	-	-	130	μA	V_{IH} ; TTL (degraded, used for CIF)
		15	-	-	μA	V_{IL} ; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-450	-	450	nA	$T_{\text{J}} \leq 150^{\circ}\text{C}$; $(0.1 * V_{\text{EXT}}) < V_{\text{IN}} < (0.9 * V_{\text{EXT}})$
		-500	-	500	nA	$T_{\text{J}} \leq 150^{\circ}\text{C}$; else
		-900	-	900	nA	$T_{\text{J}} \leq 170^{\circ}\text{C}$; $(0.1 * V_{\text{EXT}}) < V_{\text{IN}} < (0.9 * V_{\text{EXT}})$
		-950	-	950	nA	$T_{\text{J}} \leq 170^{\circ}\text{C}$; else
Input high voltage level	V_{IH} SR	1.4	-	-	V	TTL (degraded, used for CIF); $V_{\text{EXT}} = 2.97\text{V}$
		2.0	-	-	V	TTL; $V_{\text{EXT}} = 4.5\text{V}$
Input low voltage level	V_{IL} SR	-	-	0.5	V	TTL (degraded, used for CIF); $V_{\text{EXT}} = 2.97\text{V}$
		-	-	0.8	V	TTL; $V_{\text{EXT}} = 4.5\text{V}$
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

2) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Electrical Specification 5 V / 3.3 V switchable Pads
Table 3-7 Fast 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2\text{mA}$
		31	55	80	Ohm	strong driver; $I_{OH/OL} = 8\text{mA}$
Rise / Fall time ^{1) 2)}	t_{RF} CC	1.6	-	3.2	ns	$C_L = 25\text{pF}$; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/EVRSB}$ to 0.8 * $V_{EXT/FLEX/EVRSB}$
		$4+0.55 \cdot C_L$	$4+0.75 \cdot C_L$	$12+1.0 \cdot C_L$	ns	driver = medium; $C_L \leq 200\text{pF}$
		$1.0+0.18 \cdot C_L$	$2.5+0.27 \cdot C_L$	$5.0+0.35 \cdot C_L$	ns	driver = strong edge = medium; $C_L \leq 200\text{pF}$
		$0.5+0.08 \cdot C_L$	$0.5+0.11 \cdot C_L$	$1.0+0.17 \cdot C_L$	ns	driver = strong edge = sharp ; $C_L \leq 200\text{pF}$
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis ³⁾	HYS CC	0.09 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * $V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ⁴⁾	I_{PUH} CC	30	-	-	μA	V_{IH} ; AL or TTL
		-	-	130	μA	V_{IL} ; AL or TTL
Pull-down current ⁵⁾	I_{PDL} CC	-	-	130	μA	V_{IH} ; AL or TTL
		30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL

Electrical Specification 5 V / 3.3 V switchable Pads
Table 3-7 Fast 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-1500	-	1500	nA	$T_J \leq 150^\circ\text{C}$; else
		-2000	-	2000	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-2500	-	2500	nA	$T_J \leq 170^\circ\text{C}$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB} =$ constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

- 1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
- 2) Rise / fall times are defined 10% - 90% of pad supply voltage.
- 3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
- 4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
- 5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-8 Fast 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2\text{mA}$
		31	55	80	Ohm	strong driver; $I_{OH/OL} = 8\text{mA}$

Electrical Specification 5 V / 3.3 V switchable Pads
Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise / Fall time ^{1) 2)}	t_{RF} CC	1.6	-	4.5	ns	$C_L = 25\text{pF}$; driver = strong sharp edge; from 0.2 * $V_{EXT/FLEX/EVRSB}$ to 0.8 * $V_{EXT/FLEX/EVRSB}$
		-	-	5	ns	$C_L = 25\text{pF}$; driver = strong sharp edge; from 0.8V to 2.0V (RMII)
		$2+0.57*C_L$	$5.5+0.75*C_L$	$10+1.25*C_L$	ns	driver = medium; $C_L \leq 200\text{pF}$
		$1.5+0.18*C_L$	$1.5+0.28*C_L$	$8+0.4*C_L$	ns	driver = strong edge = medium; $C_L \leq 200\text{pF}$
		$0.75+0.08*C_L$	$0.75+0.11*C_L$	$2.5+0.21*C_L$	ns	driver = strong edge = sharp ; $C_L \leq 200\text{pF}$
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis ³⁾	HYS CC	$0.055 * V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.09 * V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		$0.055 * V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ⁴⁾	I_{PUH} CC	17	-	-	μA	V_{IH} ; AL and TTL (degraded, used for CIF)
		11	-	-	μA	V_{IH} ; TTL
		-	-	80	μA	V_{IL} ; AL and TTL and TTL (degraded, used for CIF)

Electrical Specification 5 V / 3.3 V switchable Pads
Table 3-8 Fast 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pull-down current ⁵⁾	I_{PDL} CC	-	-	105	μ A	V_{IH} ; AL and TTL (degraded, used for CIF)
		-	-	115	μ A	V_{IH} ; TTL
		19	-	-	μ A	V_{IL} ; AL and TTL
		15	-	-	μ A	V_{IL} ; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-1100	-	1100	nA	$T_J \leq 150^\circ\text{C}$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-1500	-	1500	nA	$T_J \leq 150^\circ\text{C}$; else
		-2000	-	2000	nA	$T_J \leq 170^\circ\text{C}$; (0.1 * $V_{EXT/FLEX/EVRSB}$) < V_{IN} < (0.9 * $V_{EXT/FLEX/EVRSB}$)
		-2500	-	2500	nA	$T_J \leq 170^\circ\text{C}$; else
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/EVRSB}$	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)
Input low voltage level	V_{IL} SR	-	-	0.42 * $V_{EXT/FLEX/EVRSB}$	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB} =$ constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.

2) Rise / fall times are defined 10% - 90% of pad supply voltage.

3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.

4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.

5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Electrical Specification 5 V / 3.3 V switchable Pads
Table 3-9 Slow 5V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2\text{mA}$
Rise / Fall time ^{1) 2)}	t_{RF} CC	$4+0.55 \cdot C_L$	$4+0.75 \cdot C_L$	$12+1 \cdot C_L$	ns	driver = medium edge = medium ; $C_L \leq 200\text{pF}$
		$1.5+0.25 \cdot C_L$	$2.5+0.40 \cdot C_L$	$7+0.55 \cdot C_L$	ns	driver = medium edge = sharp ; $C_L \leq 200\text{pF}$
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis ³⁾	HYS CC	$0.09 \cdot V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; AL
		$0.075 \cdot V_{EXT/FLEX/EVRSB}$	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ⁴⁾	I_{PUH} CC	30	-	-	μA	V_{IH} ; AL or TTL; except VGATE1P; except VGATE1N and $T_J > 150^\circ\text{C}$
		-	-	130	μA	V_{IL} ; AL or TTL; except VGATE1P; except VGATE1N and $T_J > 150^\circ\text{C}$
Pull-down current ⁵⁾	I_{PDL} CC	-	-	130	μA	V_{IH} ; AL or TTL
		30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL
Input leakage current	I_{OZ} CC	-300	-	300	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/EVRSB})$
		-400	-	400	nA	$T_J \leq 150^\circ\text{C}$; else
		-600	-	600	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 \cdot V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 \cdot V_{EXT/FLEX/EVRSB})$
		-750	-	750	nA	$T_J \leq 170^\circ\text{C}$; else

Electrical Specification 5 V / 3.3 V switchable Pads
Table 3-9 Slow 5V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input high voltage level	V_{IH} SR	0.7 * $V_{EXT/FLEX/E}$ V_{RSB}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	V_{IL} SR	-	-	0.44 * $V_{EXT/FLEX/E}$ V_{RSB}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	V_{ILD} SR	-50	-	50	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB} =$ constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

- 1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
- 2) Rise / fall times are defined 10% - 90% of pad supply voltage.
- 3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
- 4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
- 5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-10 Slow 3.3V GPIO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of pad output	R_{DSON} CC	125	225	320	Ohm	medium driver; $I_{OH/OL} = 2mA$
Rise / Fall time ^{1) 2)}	t_{RF} CC	$2+0.57*C_L$	$5.5+0.75*C_L$	$10+1.25*C_L$	ns	driver = medium edge = medium ; $C_L \leq 200pF$
		$2+0.30*C_L$	$3.5+0.50*C_L$	$5+0.70*C_L$	ns	driver = medium edge = sharp ; $C_L \leq 200pF$
Asymmetry of sending	t_{TX_ASYM} CC	-1	-	1	ns	valid for all data rates excluding clock tolerance
Input frequency	f_{IN} CC	-	-	160	MHz	

Electrical Specification 5 V / 3.3 V switchable Pads

Table 3-10 Slow 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis ³⁾	<i>HYS</i> CC	0.055 * $V_{EXT/FLEX/E}$ VRSB	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * $V_{EXT/FLEX/E}$ VRSB	-	-	V	non of the neighbor pads are used as output; TTL
		0.055 * $V_{EXT/FLEX/E}$ VRSB	-	-	V	non of the neighbor pads are used as output;TTL (degraded, used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ⁴⁾	I_{PUH} CC	17	-	-	μ A	V_{IH} ; AL and TTL (degraded, used for CIF); except VGATE1P; except VGATE1N and $T_J > 150^\circ\text{C}$
		11	-	-	μ A	V_{IH} ; TTL; except VGATE1P; except VGATE1N and $T_J > 150^\circ\text{C}$
		-	-	80	μ A	V_{IL} ; AL and TTL and TTL (degraded, used for CIF); except VGATE1P; except VGATE1N and $T_J > 150^\circ\text{C}$
Pull-down current ⁵⁾	I_{PDL} CC	-	-	105	μ A	V_{IH} ; AL and TTL (degraded, used for CIF)
		-	-	115	μ A	V_{IH} ; TTL
		19	-	-	μ A	V_{IL} ; AL and TTL
		15	-	-	μ A	V_{IL} ; TTL (degraded, used for CIF)

Electrical Specification 5 V / 3.3 V switchable Pads

Table 3-10 Slow 3.3V GPIO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-300	-	300	nA	$T_J \leq 150^\circ\text{C}$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-400	-	400	nA	$T_J \leq 150^\circ\text{C}$; else
		-600	-	600	nA	$T_J \leq 170^\circ\text{C}$; $(0.1 * V_{EXT/FLEX/EVRSB}) < V_{IN} < (0.9 * V_{EXT/FLEX/EVRSB})$
		-750	-	750	nA	$T_J \leq 170^\circ\text{C}$; else
Input high voltage level	V_{IH} SR	0.7 *	-	-	V	AL
		$V_{EXT/FLEX/EVRSB}$	-	-	V	TTL
		2.0	-	-	V	TTL (degraded, used for CIF)
Input low voltage level	V_{IL} SR	-	-	0.42 *	V	AL
		-	-	$V_{EXT/FLEX/EVRSB}$	V	TTL
		-	-	0.8	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; $V_{EXT/FLEX/EVRSB} = \text{constant}$; AL
		-	-	0.5	V	TTL (degraded, used for CIF)
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

- 1) In the formulas the value of C_L needs to be entered in pF to obtain results in ns.
- 2) Rise / fall times are defined 10% - 90% of pad supply voltage.
- 3) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
- 4) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
- 5) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-11 Class S 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	

Electrical Specification 5 V / 3.3 V switchable Pads

Table 3-11 Class S 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input hysteresis ¹⁾	HYS_{CC}	0.09 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; AL
		0.075 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL
		75	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ²⁾	$I_{PUH_{CC}}$	30	-	-	μA	V_{IH} ; AL or TTL
		-	-	130	μA	V_{IL} ; AL or TTL
Pull-down current ³⁾	$I_{PDL_{CC}}$	-	-	130	μA	V_{IH} ; AL or TTL
		30	-	-	μA	V_{IL} ; AL
		28	-	-	μA	V_{IL} ; TTL
Input leakage current	$I_{OZ_{CC}}$	-150	-	150	nA	$T_J \leq 150^\circ C$; else
		-300	-	300	nA	$T_J \leq 170^\circ C$; else
Input high voltage level	$V_{IH_{SR}}$	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
Input low voltage level	$V_{IL_{SR}}$	-	-	0.44 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
Input low threshold variation	$V_{ILD_{SR}}$	-50	-	50	mV	max. variation of 1ms; V_{DDM} = constant; AL
Pin capacitance	$C_{IO_{CC}}$	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	$t_{SET_{CC}}$	-	-	100	ns	

- 1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
- 2) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
- 3) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Electrical Specification 5 V / 3.3 V switchable Pads
Table 3-12 Class S 3.3V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input frequency	f_{IN} CC	-	-	160	MHz	
Input hysteresis ¹⁾	HYS CC	0.055 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; AL
		0.09 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL
		0.065 * V_{DDM}	-	-	V	non of the neighbor pads are used as output; TTL (degraded used for CIF)
		125	-	-	mV	two of the neighbor pads are used as output with driver=strong and edge=sharp; AL
Pull-up current ²⁾	I_{PUH} CC	17	-	-	μ A	V_{IH} ; AL and TTL (degraded, used for CIF)
		11	-	-	μ A	V_{IH} ; TTL
		-	-	80	μ A	V_{IL}
Pull-down current ³⁾	I_{PDL} CC	-	-	105	μ A	V_{IH} ; AL and TTL (degraded, used for CIF)
		-	-	115	μ A	V_{IH} ; TTL
		19	-	-	μ A	V_{IL} ; AL and TTL
		15	-	-	μ A	V_{IL} ; TTL (degraded, used for CIF)
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150^\circ\text{C}$; else
		-300	-	300	nA	$T_J \leq 150^\circ\text{C}$; PDD option available, or AltRef option available
		-300	-	300	nA	$T_J \leq 170^\circ\text{C}$; else
		-600	-	600	nA	$T_J \leq 170^\circ\text{C}$; PDD option available
Input high voltage level	V_{IH} SR	0.7 * V_{DDM}	-	-	V	AL
		2.0	-	-	V	TTL
		1.4	-	-	V	TTL (degraded, used for CIF)

Electrical Specification 5 V / 3.3 V switchable Pads
Table 3-12 Class S 3.3V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input low voltage level	V_{IL} SR	-	-	0.42 * V_{DDM}	V	AL
		-	-	0.8	V	TTL
		-	-	0.5	V	TTL (degraded, used for CIF)
Input low threshold variation	V_{ILD} SR	-33	-	33	mV	max. variation of 1ms; V_{DDM} = constant; AL
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added
Pad set-up time to get an software update of the configuration active	t_{SET} CC	-	-	100	ns	

- 1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can't be guaranteed that it suppresses switching due to external system noise.
- 2) Values for Pull-up resistor is defined via parameter R_{MDU} in table VADC 5V.
- 3) Values for Pull-down resistor is defined via parameter R_{MDD} in table VADC 5V.

Table 3-13 Class D

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current	I_{OZ} CC	-150	-	150	nA	$T_J \leq 150^\circ\text{C}$; else
		-300 ¹⁾	-	300 ¹⁾	nA	$T_J \leq 150^\circ\text{C}$; PDD option available, or AltRef option available
		-300	-	300	nA	$T_J \leq 170^\circ\text{C}$; else
		-600 ²⁾	-	600 ²⁾	nA	$T_J \leq 170^\circ\text{C}$; PDD option available, or AltRef option available
Pin capacitance	C_{IO} CC	-	2	3	pF	in addition 2.5pF from package to be added

- 1) For AN11, 100 nA need to be added.
- 2) For AN11, 200 nA need to be added .

Electrical Specification 5 V / 3.3 V switchable Pads

Table 3-14 ADC Reference Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage current for V_{AREF}	I_{OZ2} CC	-1	-	1	μA	$T_J \leq 150^\circ\text{C}$; $V_{AREF} < V_{DDM}$; used for EVADC
		-2	-	2	μA	$T_J \leq 170^\circ\text{C}$; $V_{AREF} < V_{DDM}$; used for EVADC
		-3.5	-	3.5	μA	$T_J \leq 150^\circ\text{C}$; $V_{AREF} \leq V_{DDM} + 50\text{mV}$; used for EVADC
		-7	-	7	μA	$T_J \leq 170^\circ\text{C}$; $V_{AREF} \leq V_{DDM} + 50\text{mV}$; used for EVADC

Table 3-15 Driver Mode Selection for Slow Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	X	0	Speed grade 1	medium sharp edge (sm)
X	X	1	Speed grade 2	medium medium edge (m)

Table 3-16 Driver Mode Selection for Fast Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	Reserved, do not use this combination

Table 3-17 Driver Mode Selection for RFast Pads

PDx.2	PDx.1	PDx.0	Port Functionality	Driver Setting
X	0	0	Speed grade 1	Strong sharp edge (ss)
X	0	1	Speed grade 2	Strong medium edge (sm)
X	1	0	Speed grade 3	medium (m)
X	1	1	Speed grade 4	Do not use this combination

3.6 VADC Parameters

The accuracy of the converter results depends on the reference voltage range. The parameters in the table below are valid for a reference voltage range of $(V_{AREF} - V_{AGND}) \geq 4.5 \text{ V}$. If the reference voltage range is below 4.5 V by a factor of k (e.g. 3.3 V), the accuracy parameters increase by a factor of $1.1/k$ (e.g. $1.1 \times 4.5 / 3.3 = 1.5$).

Noise on supply voltage V_{DDM} influences the conversion. The accuracy (error) parameters are defined for a supply voltage ripple of below 20 mVpp up to 10 MHz (below 5 mVpp above 10 MHz).

Digital functions overlapping analog inputs influence accuracy.

The total unadjusted error (TUE) is defined without noise. The overall deviation depends on TUE and EN_{RMS} (depending on the noise distribution). Example: For a noise distribution of 4 sigma and $EN_{RMS} = 1.0$ the additional peak-peak noise error is $\pm(4 \times 1.0) = 8 \text{ LSB}_{12}$.

The noise reduction feature improves the result by adding additional conversion steps. The conversion times, therefore, increase accordingly ($4 \times t_{ADCI} + 3 \times t_{ADC}$ for each of 1, 3, or 7 steps).

Table 3-18 VADC 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVADC IVR output voltage	$V_{DDK \text{ CC}}$	1.13	-	1.33	V	Measured at low temperature.
Deviation of IVR output voltage V_{DDK}	$dV_{DDK \text{ CC}}$	-2	-	2	%	Based on device-specific value
Analog reference voltage ¹⁾	$V_{AREF \text{ SR}}$	4.5	5.0	$V_{DDM} + 0.05$	V	$4.5 \text{ V} \leq V_{DDM} \leq 5.5 \text{ V}$
		2.97	3.3	$V_{DDM} + 0.05$	V	$2.97 \text{ V} \leq V_{DDM} < 4.5 \text{ V}$
Analog reference ground	$V_{AGND \text{ SR}}$	V_{SSM}	V_{SSM}	V_{SSM}	V	V_{SSM} and V_{AGND} are connected together
Analog input voltage range	$V_{AIN \text{ SR}}$	V_{AGND}	-	V_{AREF}	V	V_{AIN} is limited by the respective pad supply voltage; see pin configuration (buffer type)
Converter reference clock	$f_{ADCI \text{ SR}}$	16	40	53.33	MHz	$4.5 \text{ V} \leq V_{DDM} \leq 5.5 \text{ V}$
		16	20	26.67	MHz	$2.97 \text{ V} \leq V_{DDM} < 4.5 \text{ V}$
Total Unadjusted Error ^{2) 3)}	$TUE \text{ CC}$	-4	-	4	LSB	12-bit resolution for primary/secondary groups, 10-bit resolution for fast compare channels
INL Error ²⁾	$EA_{INL \text{ CC}}$	-3	-	3	LSB	
DNL error ²⁾⁴⁾	$EA_{DNL \text{ CC}}$	-1	-	3	LSB	
Gain Error ²⁾	$EA_{GAIN \text{ CC}}$	-3.5	-	3.5	LSB	
Offset Error ²⁾³⁾	$EA_{OFF \text{ CC}}$	-4	-	4	LSB	
RMS Noise ^{2)5) 6)}	$EN_{RMS \text{ CC}}$	-	0.5	0.8	LSB	Noise reduction level 3
		-	0.5	1.0	LSB	Standard conversion

Electrical Specification VADC Parameters

Table 3-18 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reference input charge consumption per conversion (from V_{AREF}) ^{7) 8) 9)}	Q_{CONV} CC	-	-	20	pC	$V_{AIN} = 0$ V (worst case), precharging disabled
		-	-	10	pC	$V_{AIN} = 0$ V (worst case), precharging enabled, $V_{DDM} - 5\% < V_{AREF} < V_{DDM} + 50$ mV
Switched capacitance of an analog input	C_{AINS} CC	-	2.5	3.4	pF	Input buffer disabled
Analog input charge consumption ¹⁰⁾	Q_{AINS} CC	-	-	3.5	pC	Primary groups and fast compare channels; $V_{AIN} = V_{AREF}$; $V_{DDM} = 5.0$ V; input buffer enabled; $T_J \leq 150^\circ\text{C}$
		-	-	3.8	pC	Primary groups and fast compare channels; $V_{AIN} = V_{AREF}$; $V_{DDM} = 5.0$ V; input buffer enabled; $T_J > 150^\circ\text{C}$
		-	-	4.4	pC	Secondary groups; $V_{AIN} = V_{AREF}$; $V_{DDM} = 5.0$ V; input buffer enabled; $T_J \leq 150^\circ\text{C}$
		-	-	4.8	pC	Secondary groups; $V_{AIN} = V_{AREF}$; $V_{DDM} = 5.0$ V; input buffer enabled; $T_J > 150^\circ\text{C}$

Electrical Specification VADC Parameters
Table 3-18 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sampling time	t_S SR	100	-	-	ns	Primary group or fast compare channel, 4.5 V $\leq V_{DDM} \leq 5.5$ V; input buffer disabled
		300	-	-	ns	Primary group or fast compare channel, 4.5 V $\leq V_{DDM} \leq 5.5$ V; input buffer enabled
		500	-	-	ns	Secondary group, 4.5 V $\leq V_{DDM} \leq 5.5$ V; input buffer disabled
		700	-	-	ns	Secondary group, 4.5 V $\leq V_{DDM} \leq 5.5$ V; input buffer enabled
		200	-	-	ns	Primary Group or fast compare channel, 2.97 V $\leq V_{DDM} < 4.5$ V; input buffer disabled
		400	-	-	ns	Primary group or fast compare channel, 2.97 V $\leq V_{DDM} < 4.5$ V; input buffer enabled
		1000	-	-	ns	Secondary group, 2.97 V $\leq V_{DDM} < 4.5$ V; input buffer disabled
		1200	-	-	ns	Secondary group, 2.97 V $\leq V_{DDM} < 4.5$ V; input buffer enabled
Sampling time for calibration	t_{SCAL} SR	50	-	-	ns	4.5 V $\leq V_{DDM} \leq 5.5$ V
		100	-	-	ns	2.97 V $\leq V_{DDM} < 4.5$ V
Input buffer switch-on time	t_{BUF} CC	-	0.4	1	μ s	
Wakeup time	t_{WU} CC	-	0.1	0.2	μ s	Fast standby mode
		-	1.6	3	μ s	Slow standby mode
Broken wire detection delay against V_{AREF}	t_{BWR} CC	-	100	-	cycles	Result above 80% of full scale range, analog input buffer disabled
Broken wire detection delay against V_{AGND}	t_{BWG} CC	-	100	-	cycles	Result below 10% of full scale range, analog input buffer disabled
Converter diagnostics unit resistance ¹¹⁾	R_{CSD} CC	45	-	75	kOhm	
Converter diagnostics voltage accuracy	dV_{CSD} CC	-10	-	10	%	Percentage refers to V_{DDM}

Electrical Specification VADC Parameters

Table 3-18 VADC 5V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the multiplexer diagnostics pull-up device	$R_{MDU\ CC}$	30	-	42	kOhm	$0\ V \leq V_{IN} \leq 0.9 \cdot V_{DDM}$, Automotive Levels
		56	-	78	kOhm	$0\ V \leq V_{IN} \leq 0.9 \cdot V_{DDM}$, TTL Levels
Resistance of the multiplexer diagnostics pull-down device	$R_{MDD\ CC}$	43	-	58	kOhm	$0.1 \cdot V_{DDM} \leq V_{IN} \leq V_{DDM}$, Automotive level
		18	-	25	kOhm	$0.1 \cdot V_{DDM} \leq V_{IN} \leq V_{DDM}$, TTL level
Resistance of the pull-down test device	$R_{PDD\ CC}$	-	-	0.3	kOhm	Measured at pad input voltage $V_{IN} = V_{DDM} / 2$.

- 1) These limits apply to the standard reference input as well as to the alternate reference input.
- 2) Parameter depends on reference voltage range and supply ripple, see introduction. Resulting worst case combined error is arithmetic combination of TUE and EN_{RMS} . Tests are done with postcalibration disabled, after completing the startup calibration.
- 3) Analog inputs mapped to pads of the type SLOW influence accuracy. The values for this parameter increase by 3 LSB_{12} .
- 4) Monotonic characteristic, no missing codes when calibrated.
- 5) Parameter EN_{RMS} refers to a 1 sigma distribution.
- 6) Analog inputs mapped to pads of the type SLOW the RMS noise (EN_{RMS}) can be up to 2 LSB_{12} (soft switching for DC/DC enabled).
- 7) For reduced reference voltages $V_{AREF} < 3.375V$, the consumed charge Q_{CONV} is reduced by the factor of $k2 = V_{AREF} [V] / 3.375$. For reduced reference voltages $4.5V < V_{AREF} \leq 3.375V$, Q_{CONV} is not reduced.
- 8) Maximum charge increases by 15 pC when BWD (Broken Wire Detection) is active.
- 9) Fast compare channels only consume 1/3 of the charge for a primary/secondary group.
- 10) For analog inputs with overlaid digital GPIOs or with PDD function this value increases by 1 pC.
- 11) Use a sample time of at least 1.1 μs to enable proper settling of the test voltage.

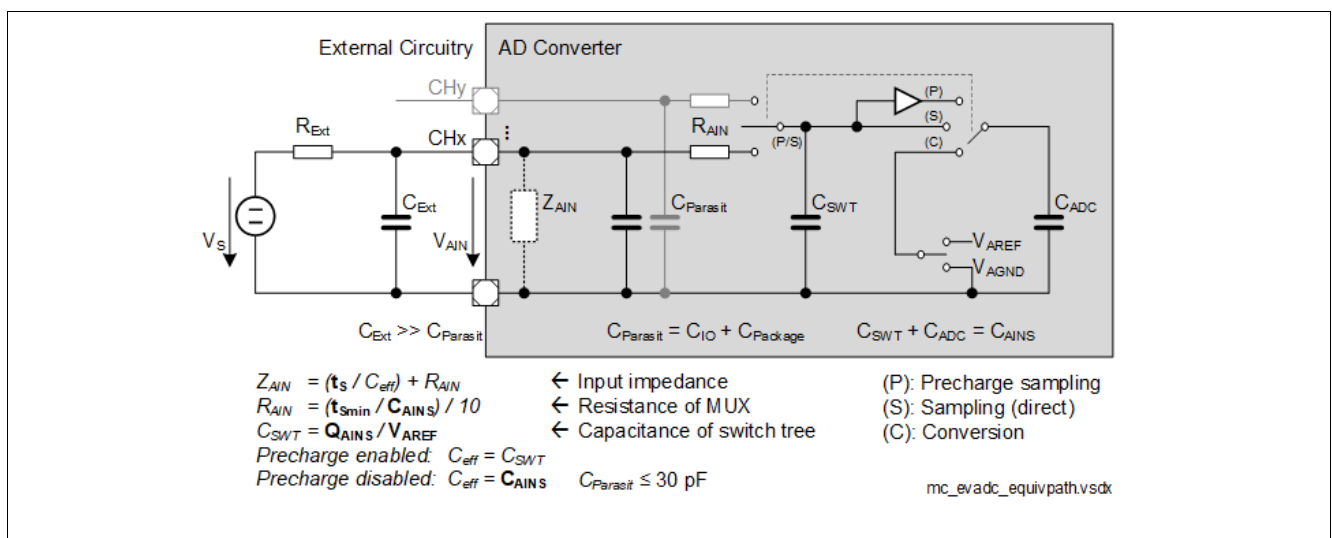


Figure 3-1 Equivalent Circuitry for Analog Inputs

3.7 MHz Oscillator

OSC_XTAL is used as accurate and exact clock source. OSC_XTAL supports 16 MHz to 40 MHz crystals external outside of the device. Support of ceramic resonators is also provided.

Table 3-19 OSC_XTAL

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-70	-	70	μA	$V_{IN} > 0\text{V}$; $V_{IN} < V_{EXT}$
Oscillator frequency	f_{OSC} SR	4	-	40	MHz	Direct Input Mode selected, if shaper is not bypassed
		16	-	40	MHz	External Crystal Mode selected
Oscillator start-up time	t_{OSCS} CC	-	-	3 ¹⁾	ms	$20\text{MHz} \leq f_{OSC}$ and 8pF load capacitance
Input voltage at XTAL1 ²⁾	V_{IX} SR	-0.7	-	$V_{EXT} + 0.5$	V	If shaper is not bypassed
Input amplitude (peak to peak) at XTAL1	V_{PPX} SR	$0.3 * V_{EXT}$	-	$V_{EXT} + 1.0$	V	If shaper is not bypassed; $f_{OSC} > 25\text{MHz}$
		$0.35 * V_{EXT}$	-	$V_{EXT} + 1.0$	V	If shaper is not bypassed; $f_{OSC} \leq 25\text{MHz}$
Internal load capacitor	C_{L0} CC	1.30	1.40	1.55	pF	enabled via bit OSCCON.CAP0EN
Internal load capacitor	C_{L1} CC	3.05	3.35	3.70	pF	enabled via bit OSCCON.CAP1EN
Internal load capacitor	C_{L2} CC	7.85	8.70	9.55	pF	enabled via bit OSCCON.CAP2EN
Internal load capacitor	C_{L3} CC	12.05	13.35	14.65	pF	enabled via bit OSCCON.CAP3EN
Internal load stray capacitor between XTAL1 and XTAL2	C_{XINTS} CC	1.15	1.20	1.25	pF	
Internal load stray capacitor between XTAL1 and ground	C_{XTAL1} CC	-	2.5	4	pF	
Duty cycle at XTAL1 ³⁾	DC_{X1} SR	35	-	65	%	$V_{XTAL1} = 0.5 * V_{PPX}$
Absolute RMS jitter at XTAL1 ³⁾	J_{ABSX1} SR	-	-	28	ps	10 KHz to $f_{OSC}/2$
Slew rate at XTAL1 ³⁾	SR_{XTAL1} SR	0.3	-	-	V/ns	Maximum 30% difference between rising and falling slew rate

1) t_{OSCS} is defined from the moment when the Oscillator Mode is set to External Crystal Mode until the oscillations reach an amplitude at XTAL1 of $0.3 * V_{EXT}$. This value depends on the frequency of the used external crystal. For faster crystal frequencies this value decrease.

2) For Supply ($V_{EXT} < 5.3\text{V}$ V_{IX}) min could be down to -0.9V. For XTAL1 an input level down to -0.9V will not cause a damage or a reliability problem operating with an external crystal.

3) Square wave input signal for XTAL1.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

3.8 Back-up Clock

The back-up clock provides an alternative clock source.

Table 3-20 Back-up Clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Back-up clock accuracy before trimming	f_{BACKUT} CC	70	100	130	MHz	$V_{\text{EXT}} \geq 2.97\text{V}$
Back-up clock accuracy after trimming ¹⁾	f_{BACKT} CC	98	100	102	MHz	$V_{\text{EXT}} \geq 2.97\text{V}$
Standby clock	f_{SB} CC	25	70	110	kHz	$V_{\text{EXT}} \geq 2.97\text{V}$

1) A short term trimming providing the accuracy required by LIN communication is possible by periodic trimming every 2 ms for temperature and voltage drifts up to temperatures of 125 celcius

3.9 Temperature Sensor

Table 3-21 DTS PMS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion ¹⁾	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Calibration reference accuracy	T_{CALACC} CC	-1	-	1	°C	calibration points @ $T_J=-40^{\circ}\text{C}$ and $T_J=127^{\circ}\text{C}$
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) After warm reset t_M is not restarted and is measured from last conversion.

Table 3-22 DTS Core

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time for each conversion ¹⁾	t_M CC	-	-	2.7	ms	Measured from cold power-on reset release
Temperature difference between on chip temperature sensors	ΔT CC	-3	-	3	°C	
Calibration reference accuracy	T_{CALACC} CC	-2	-	2	°C	calibration points @ $T_J=-40^{\circ}\text{C}$ and $T_J=127^{\circ}\text{C}$
Accuracy over temperature range	T_{NL} CC	-2	-	2	°C	T_{CALACC} has to be added in addition
DTS temperature range	T_{SR} SR	-40	-	170	°C	

1) After warm reset t_M is not restarted and is measured from last conversion.

3.10 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following table and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:

The real (realistic) power pattern defines the following conditions:

- $T_J = 150\text{ °C}$
- $f_{SRI} = f_{CPUx} = 200\text{ MHz}$
- $f_{SPB} = f_{STM} = 100\text{ MHz}$
- $V_{DD} = 1.275\text{ V}$
- $V_{DDP3/FLEX} = 3.366\text{ V}$
- $V_{EXT / EVRSB} = V_{DDM} = 5.1\text{ V}$
- one cores is active without lockstep core (IPC=0.6)
- the following peripherals are inactive: HSM, FCE, and MTU

The max power pattern defines the following conditions:

- $T_J = 150\text{ °C}$
- $f_{SRI} = f_{CPUx} = 300\text{ MHz}$
- $f_{GTM} = 200\text{ MHz}$
- $f_{SPB} = f_{STM} = f_{BAUD1} = f_{BAUD2} = f_{ASCLINx} = 100\text{ MHz}$
- $V_{DD} = 1.375\text{ V}$
- $V_{DDP3 / FLEX} = 3.63\text{ V}$
- $V_{EXT / EVRSB} = V_{DDM} = 5.5\text{ V}$
- all cores are active including one lockstep core (IPC=1.2)
- the following module is inactive: MTU

Table 3-23 Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
\sum Sum of I_{DD} core and peripheral supply currents (incl. $I_{DDPORST} + \sum I_{DDCx0} + \sum I_{DDCxx} + I_{DDGTM} + I_{DDSB}$)	$I_{DDRAIL\ CC}$	-	-	300 ¹⁾	mA	max power pattern; valid for Feature Package L, and LP products; $f_{SRI}=f_{CPU}=300\text{ MHz}$.
		-	-	220	mA	real power pattern; valid for Feature Package L, and LP products; $f_{SRI}=f_{CPU}=200\text{ MHz}$.

Electrical Specification Power Supply Current
Table 3-23 Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core current during active power-on reset (PORST pin held low). Leakage current of core domain. ²⁾	$I_{DDPORST}$ CC	-	-	47	mA	$V_{DD} = 1.275V$; $T_J = 125^\circ C$; valid for Feature Package L, and LP products
		-	-	81	mA	$V_{DD} = 1.275V$; $T_J = 150^\circ C$; valid for Feature Package L, and LP products
		-	-	105	mA	$V_{DD} = 1.275V$; $T_J = 160^\circ C$; valid for Feature Package L, and LP products
		-	-	125	mA	$V_{DD} = 1.275V$; $T_J = 165^\circ C$; valid for Feature Package L, and LP products
Σ Sum of I_{DDP3} 3.3 V supply currents	$I_{DDP3RAIL}$ CC	-	-	35	mA	max power pattern incl. Flash read current and Dflash programming current.
		-	-	26 ³⁾	mA	real power pattern incl. Flash read current and Dflash programming current.
Σ Sum of external I_{EXT} supply currents (incl. $I_{EXTFLEX} + I_{EVR SB} + I_{EXTLVDS}$)	$I_{EXTRAIL}$ CC	-	-	44	mA	max power pattern
		-	-	39	mA	real power pattern
I_{EXT} and I_{FLEX} supply current	$I_{EXTFLEX}$ CC	-	-	11 ²⁾⁴⁾	mA	real power pattern with port activity absent; PORST output inactive.
$I_{EVR SB}$ supply current ²⁾	$I_{EVR SB}$ CC	-	-	8.5	mA	real power pattern; PMS/EVR module current considered without SCR and Standby RAM during RUN mode.
Σ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC} + I_{DDMEDSADC}$)	I_{DDM} CC	-	-	6	mA	real power pattern

Electrical Specification Power Supply Current
Table 3-23 Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Σ Sum of all currents (incl. $I_{EXTRAIL}+I_{DDMRIL}+I_{DDx3RAIL}+I_{DD}$)	I_{DDTOT} CC	-	-	291	mA	real power pattern; valid for Feature Package L, and LP products; fSRI=fCPU=200 MHz.
		-	-	391	mA	max power pattern; valid for Feature Package L, and LP products; fSRI=fCPU=300 MHz.
Σ Sum of all currents with DC-DC EVRC regulator active ⁵⁾	$I_{DDTOTDC3}$ CC	-	-	200	mA	real power pattern; valid for Feature Package L, and LP products; fSRI=fCPU=200 MHz; EVR SCDCDC active; $V_{EXT} = 3.3V$
Σ Sum of all currents with DC-DC EVRC regulator active ⁵⁾	$I_{DDTOTDC5}$ CC	-	-	170	mA	real power pattern; valid for Feature Package L, and LP products; fSRI=fCPU=200 MHz; EVR SCDCDC active; $V_{EXT} = 5V$
Σ Sum of all currents (SLEEP mode) ²⁾	I_{SLEEP} CC	-	-	25	mA	All CPUs in idle, All peripherals in sleep, $f_{SRI/SPB} = 1 MHz$ via LPDIV divider; $T_J = 25^\circ C$
Σ Sum of all currents (STANDBY mode) drawn at V_{EVRSB} supply pin ⁶⁾	$I_{STANDBY}$ CC	-	-	130 ⁷⁾	μA	32 kB Standby RAM block active. SCR inactive. Power to remaining domains switched off. $T_J = 25^\circ C$; $V_{EVRSB} = 5V$
Maximum power dissipation ⁸⁾	PD SR	-	-	860	mW	max power pattern; valid for Feature Package L, and LP products; fSRI=fCPU=300 MHz.
		-	-	600	mW	real power pattern; valid for Feature Package L, and LP products; fSRI=fCPU=200 MHz.

Electrical Specification Power Supply Current

- 1) IDDRAIL for max power pattern conditions at $T_j=165^{\circ}\text{C}$ is limited to 390 mA.
- 2) Limits are defined for real power pattern ($V_{DD}=1.275\text{V}$). For max power pattern limit has to be multiplied by the factor 1.22.
- 3) Realistic Pflash read pattern with 50% Pflash bandwidth utilization and a code mix of 50% 0s and 50% 1s. A common decoupling capacitor of at least 100nF for (V_{DDP3}) is used. Continuous Dflash programming in burst mode with 3.3 V supply and realistic Pflash read access in parallel. Erase currents of the corresponding flash modules are less than the respective programming currents at V_{DDP3} pin. Programming and erasing flash may generate transient current spikes of up to 45 mA / 20 ns which are handled by the decoupling and buffer capacitors. This parameter is relevant for external power supply dimensioning and not for thermal considerations.
- 4) The current consumption includes only minimal port activity.
- 5) The total current drawn from external regulator is estimated with 72% EVRC SMPS regulator efficiency. IDDTOTDCx is calculated from IDDTOT using the scaled core current $[(I_{DD} \times V_{DD}) / (V_{in} \times \text{Efficiency})]$ and constitutes all other rail currents and IDDM.
- 6) The same current limits apply also for the other power pattern.
- 7) Σ Sum of all currents during RUN mode at VEVR33 supply pin is less than (IEVR33 + 4 mA Standby RAM current + ISCR33 if SCR active). Σ It is recommended to have at least 100 nF decoupling capacitor at this pin. 32kB of Standby SRAM contributes less than 10uA to IStandby current.
- 8) The values are only valid if all supplies are applied from external and do not contain the power losses of EVR33 and EVRC.

Table 3-24 Module Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DDP3} supply current for programming of a Pflash or Dflash bank ¹⁾	$I_{DDP3PROG}$ CC	-	-	25	mA	Pflash 3.3V programming current adder when using external 3.3V supply.
		-	-	9 ²⁾	mA	Pflash 3.3V programming current adder when using external 5V supply.
Σ Sum of external I_{DDM} supply currents (incl. $I_{DDMEVADC} + I_{DDMEDSADC}$)	I_{DDM} CC	-	-	6	mA	real power pattern; current for EVADC modules; 2 EVADC modules active.
		-	-	12 ³⁾	mA	max power pattern; current for EVADC modules only; 4 EVADC modules active.
I_{DDP3} supply current for erasing of a Pflash or Dflash bank	$I_{DDP3ERASE}$ CC	-	-	25	mA	Pflash 3.3V erasing current adder when using external 3.3V supply.

Electrical Specification Power Supply Current
Table 3-24 Module Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCR 8-bit Standby Controller current incl. PMS in STANDBY Mode drawn at $V_{EVR\text{SB}}$ supply pin	$I_{\text{SCR\text{SB}}}$ CC	-	-	7	mA	SCR power pattern incl. PMS current consumption with fback clock active; $f_{\text{SYS_SCR}} = 20\text{MHz}$; $T_{\text{J}} = 150^{\circ}\text{C}$
		-	0.150	-	mA	SCR power pattern incl. PMS current consumption with fback inactive; $f_{\text{SYS_SCR}} = 70\text{kHz}$; $T_{\text{J}} = 25^{\circ}\text{C}$
SCR 8-bit Standby Controller CPU in IDLE mode ⁴⁾	$I_{\text{SCR\text{IDLE}}}$ CC	-	-	3.5	mA	real power pattern. CPU set into idle mode.

- 1) The same current limits apply also for the other power pattern.
- 2) During Pflash programming at 5V, additional 2 mA is drawn at VEXT supply rail.
- 3) A single VADC unit consumes approx. 1.3 mA.
- 4) Limits are defined for real power pattern ($V_{\text{DD}} = 1.275\text{V}$). For max power pattern limit has to be multiplied by the factor 1.22.

Table 3-25 Module Core Current Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core current of CPUx main core with CPUx lockstep core inactive	$I_{\text{DDC}\text{x0}}$ CC	-	-	70	mA	max power pattern; $f_{\text{CPU}} = 300\text{MHz}$; $\text{IPC} = 1.2$
		-	-	45	mA	real power pattern; $f_{\text{CPU}} = 300\text{MHz}$; $\text{IPC} = 0.6$
I_{DD} core current of CPUx main core with CPUx lockstep core active	$I_{\text{DDC}\text{xx}}$ CC	-	-	$I_{\text{DDC}\text{x0}} + 50$	mA	max power pattern; $f_{\text{CPU}} = 300\text{MHz}$; $\text{IPC} = 1.2$
		-	-	$I_{\text{DDC}\text{x0}} + 40$	mA	real power pattern; $f_{\text{CPU}} = 300\text{MHz}$; $\text{IPC} = 0.6$
I_{DD} core current added by GTM	$I_{\text{DDG}\text{T\text{M}}}$ CC	-	-	48	mA	max power pattern
		-	-	30	mA	real power pattern; 2xTIMx, 2xTOMx & 1xATOMx active at 100MHz.
I_{DD} core current added by HSM	$I_{\text{DDH}\text{SM}}$ CC	-	-	20 ¹⁾	mA	max power pattern; HSM running at 100MHz.

Electrical Specification Power Supply Infrastructure and Supply Start-up

Table 3-25 Module Core Current Consumption (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
I_{DD} core dynamic current added by LBIST	$I_{DDLBI\text{ST}} \text{ CC}$	-	-	200 ²⁾	mA	LBIST Configuration A; $1.2\text{V} \leq V_{DD}$
I_{DD} core dynamic current added by MBIST	$I_{DDMBI\text{ST}} \text{ CC}$	-	-	200	mA	Non Destructive Test (4N) on all RAMs sequentially; fMBIST = 300MHz; tMBIST < 6ms.

1) The current consumption includes basic HSM activity incl. AES module.

2) LBIST is executed either during start-up phase or can be triggered by application software. Secondary voltage monitors are inactive during the LBIST execution time (t_{LBIST}).

During the start-up phase externally supplied V_{DD} voltage has to be equal or greater than 1.2V (V_{DD} nominal - 4%) for static accuracy.

If V_{DD} is supplied internally by EVRC, EVRC takes care not to violate the V_{DD} 1.2V static under voltage limit.

3.10.1 Calculating the 1.25 V Current Consumption

The current consumption of the 1.25 V rail compose out of two parts:

- Static current consumption
- Dynamic current consumption

The static current consumption is related to the device temperature T_J and the dynamic current consumption depends of the configured clocking frequencies and the software application executed. These two parts needs to be added in order to get the rail current consumption.

(3.1)

$$I_0 = 0,92 \left[\frac{\text{mA}}{\text{C}} \right] e^{0,0265 T_J[\text{C}]}$$

(3.2)

$$I_0 = 0,128 \left[\frac{\text{mA}}{\text{C}} \right] e^{0,0417 T_J[\text{C}]}$$

Equation (3.1) defines the typical static current consumption and **Equation (3.2)** defines the maximum static current consumption. Both functions are valid for $V_{DD} = 1.275 \text{ V}$.

3.11 Power Supply Infrastructure and Supply Start-up

3.11.1 Supply Ramp-up and Ramp-down Behavior

Start-up slew rates for supply rails shall comply to SR (see [Table 3-29](#) Supply Ramp).

3.11.1.1 Single Supply mode (a)

Electrical Specification Power Supply Infrastructure and Supply Start-up

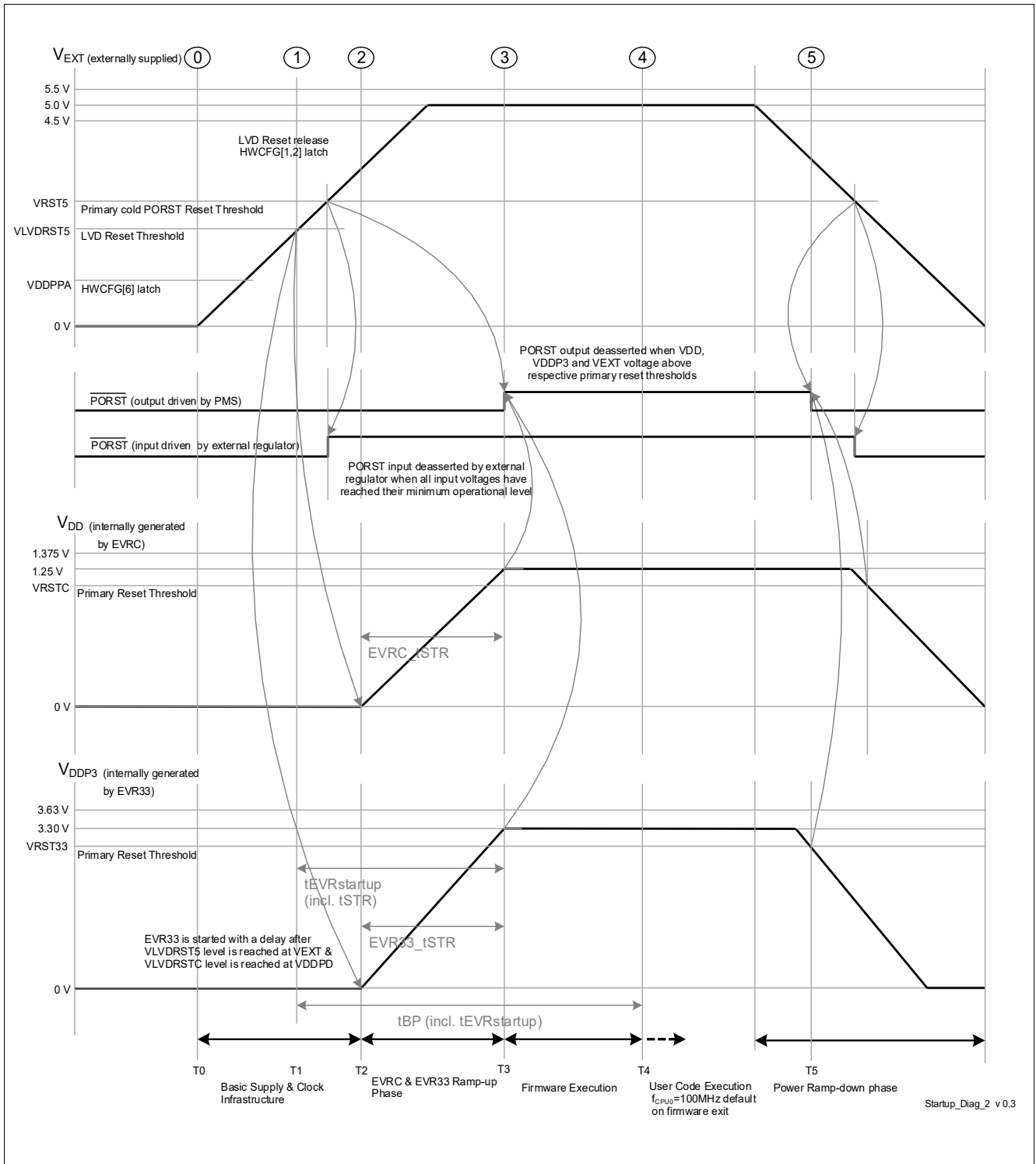


Figure 3-2 Single Supply mode (a) - V_{EXT} (5 V) single supply

$V_{EXT} = 5\text{ V}$ single supply mode. V_{DD} and V_{DDP3} are generated internally by the EVRC and EVR33 internal regulators.

- The rate at which current is drawn from the external regulator (dI_{EXT}/dt) is limited during the basic infrastructure and EVRx regulator start-up phase (T0 up to T2) to a maximum of 100 mA with 100 μs settling time. Start-up slew rates for supply rails shall comply to parameter SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

Electrical Specification Power Supply Infrastructure and Supply Start-up

- Furthermore it is also ensured that the current drawn from the regulator (dI_{DD}/dt) is limited during the Firmware start-up phase (T3 up to T4) to a maximum of 100 mA with 100 us settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that μC asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the μC when at least one among the three supply domains (V_{DD} , V_{DDP3} or V_{EXT}) violate their primary under-voltage reset thresholds. The PORST (output) is de-asserted by the μC when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dI_{DD}) is expected.
- The power sequence as shown in [Figure 3-2](#) is enumerated below
 - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[1:2,4,5,6] and TESTMODE pins. These events are initiated after LVD reset release at T1 after V_{EXT} and VEVR SB supply rails have reached VLVD RST5 level and internal pre-regulator VDDPD voltage has reached VLVD RSTC level.
 - T2 refers to the point in time where consequently a soft start of EVRC and EVR33 regulators are initiated. PORST (input) does not have any affect on EVR33 or EVRC output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the t_{STR} time to avoid overshoots.
 - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVRC and EVR33 regulators have ramped up. (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as $t_{EVRstart-up}$.
 - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as t_{BP} .
 - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (V_{DD} , V_{DDP3} or V_{EXT}) drop below their respective primary under-voltage reset thresholds.

3.11.1.2 Single Supply mode (e)

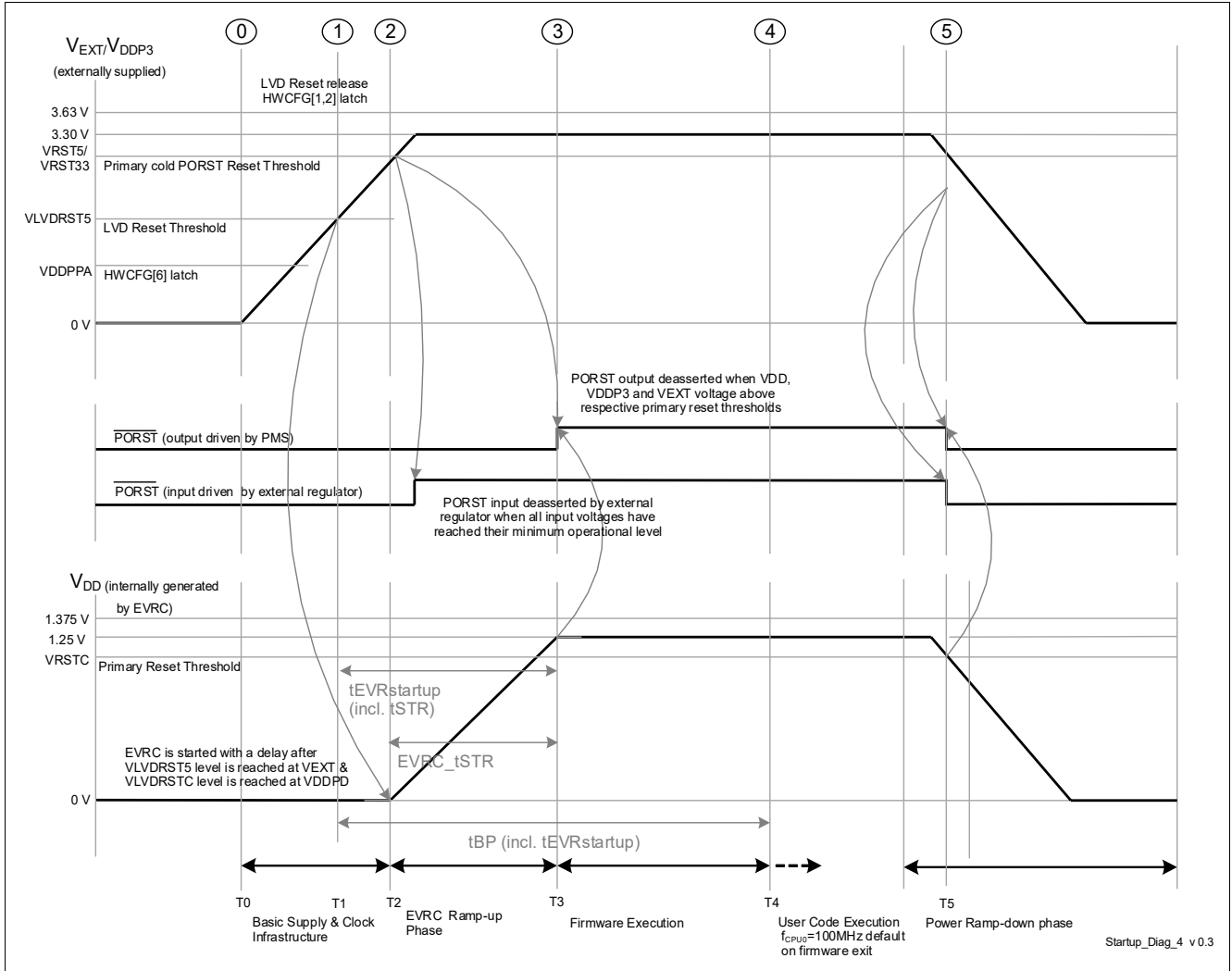


Figure 3-3 Single Supply mode (e) - (V_{EXT} & V_{DDP3}) 3.3 V single supply

$V_{EXT} = V_{DDP3} = 3.3$ V single supply mode. V_{DD} is generated internally by the EVRC regulator.

- The rate at which current is drawn from the external regulator (dI_{EXT}/dt) is limited in the Start-up phase to a maximum of 100 mA with 100 μ s settling time. Start-up slew rates for supply rails shall comply to SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until the external supply is above the respective primary reset threshold.
- PORST (output) active means that μ C asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the μ C when at least one among the three supply domains (V_{DD} , V_{DDP3} or V_{EXT}) violate their primary under-voltage reset thresholds. The PORST (output) is de-asserted by the μ C when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dI_{DD}) is expected.

 Electrical Specification Power Supply Infrastructure and Supply Start-up

- The power sequence as shown in [Figure 3-3](#) is enumerated below
 - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[1:2,4,5,6] and TESTMODE pins. These events are initiated after LVD reset release at T1 after V_{EXT} and VEVR SB supply rails have reached VLVD RST5 level and internal pre-regulator VDDPD voltage has reached VLVD RSTC level.
 - T2 refers to the point in time where consequently a soft start of EVRC regulator is initiated. PORST (input) does not have any affect on EVRC output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR time to avoid overshoots.
 - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVRC regulator has ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup.
 - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP.
 - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (V_{DD} , V_{DDP3} or V_{EXT}) drop below their respective primary under-voltage reset thresholds.

3.11.1.3 External Supply mode (d)

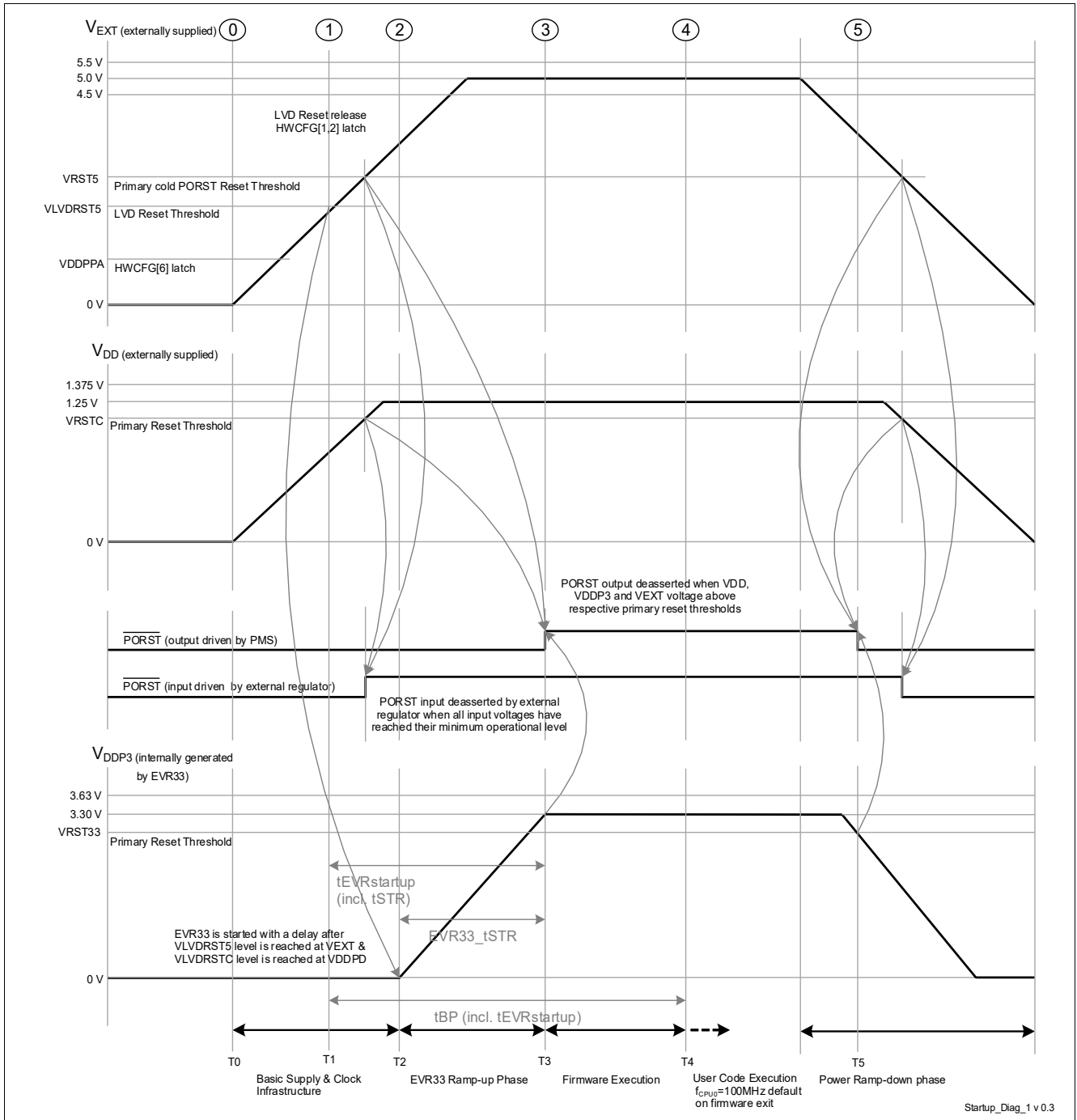


Figure 3-4 External Supply mode (d) - V_{EXT} and V_{DD} externally supplied

V_{EXT} = 5 V and V_{DD} supplies are externally supplied. 3.3V is generated internally by the EVR33 regulator.

- External supplies V_{EXT} and V_{DD} may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Start-up slew rates for supply rails shall comply to SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification. It is expected that during start-up, V_{EXT} ramps up before V_{DD} rail. In case V_{DD} voltage rail is ramped up before V_{EXT}; V_{DD} supply overshoots during start-up shall be limited within the operational voltage range.

Electrical Specification Power Supply Infrastructure and Supply Start-up

- The rate at which current is drawn from the external regulator (dI_{EXT}/dt or dI_{DD}/dt) is limited in the Start-up phase to a maximum of 100 mA with 100 μ s settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that μ C asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the μ C when at least one among the three supply domains (V_{DD} , V_{DDP3} or V_{EXT}) violate their primary under-voltage reset thresholds. The PORST (output) is de-asserted by the μ C when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dI_{DD}) is expected.
- The power sequence as shown in [Figure 3-4](#) is enumerated below
 - T1 up to T2 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[1:2,4,5,6] and TESTMODE pins. These events are initiated after LVD reset release at T1 after V_{EXT} and VEVRSB supply rails have reached VLVD RST5 level and internal pre-regulator VDDPD voltage has reached VLVD RSTC level.
 - T2 refers to the point in time where consequently a soft start of EVR33 regulator is initiated. PORST (input) does not have any affect on EVR33 output and regulators continue to generate the respective voltages though PORST is asserted and the device is in reset state. The generated voltage follows a soft ramp-up over the tSTR time to avoid overshoots.
 - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. EVR33 regulators has ramped up. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated. The time between T1 and T3 is documented as tEVRstartup.
 - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP.
 - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided or generated supplies (V_{DD} , V_{DDP3} or V_{EXT}) drop below their respective primary under-voltage reset thresholds.

3.11.1.4 External Supply mode (h)

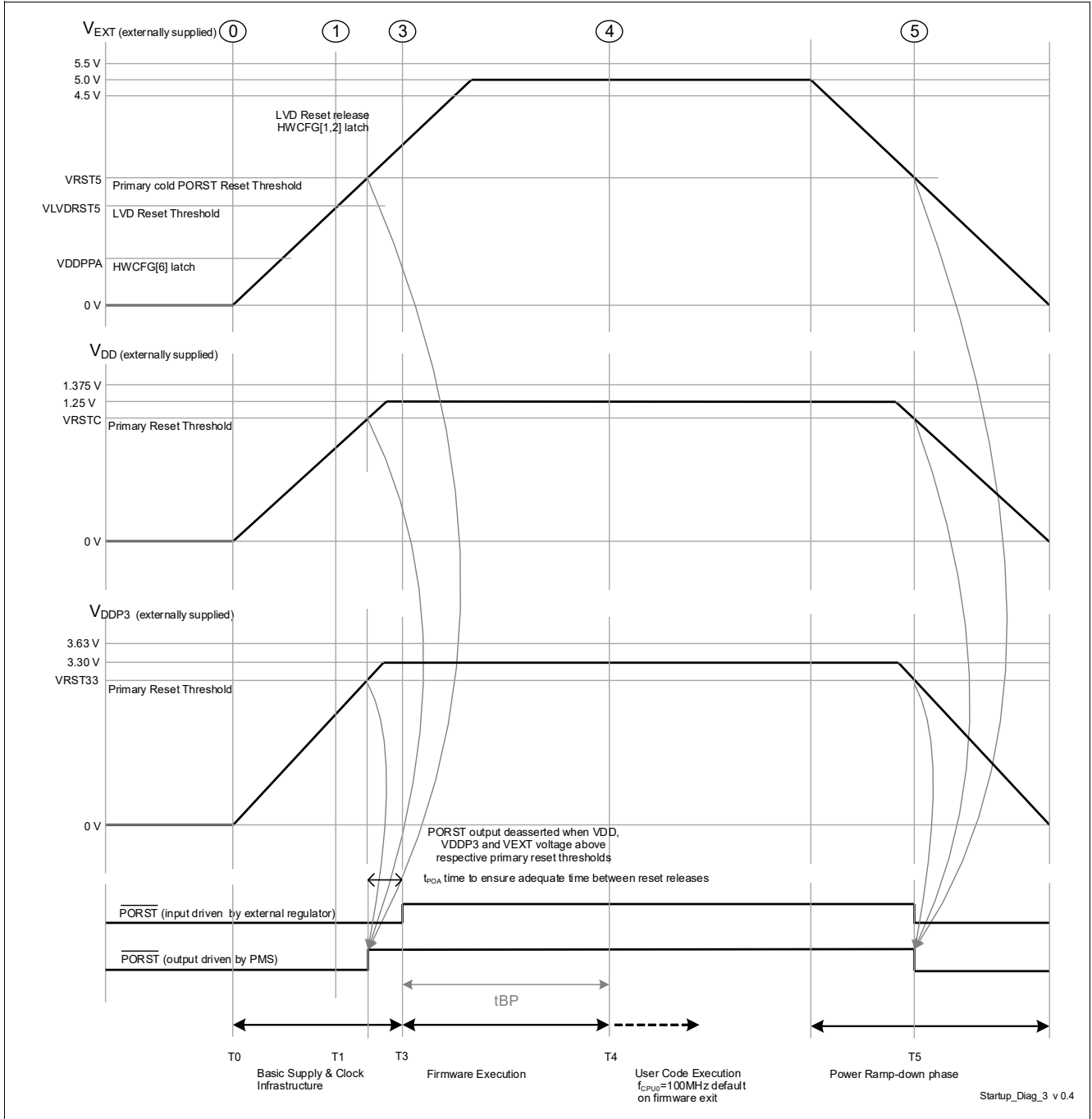


Figure 3-5 External Supply mode (h) - V_{EXT} , V_{DDP3} & V_{DD} externally supplied

All supplies, namely V_{EXT} , V_{DDP3} & V_{DD} are externally supplied.

- External supplies V_{EXT} , V_{DDP3} & V_{DD} may ramp-up or ramp-down independent of each other with regards to start, rise and fall time(s). Start-up slew rates for supply rails shall comply to SR. The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification. It is expected that during start-up, V_{EXT} ramps up before V_{DDP3} and V_{DD} rails. In case smaller voltage rails are ramped up before V_{EXT} , V_{DD} and V_{DDP3} supply overshoots during start-up shall be limited within the operational voltage ranges of the respective rails.

Electrical Specification Power Supply Infrastructure and Supply Start-up

- The rate at which current is drawn from the external regulator (dI_{EXT}/dt , dI_{DD}/dt or dI_{DDP3}/dt) is limited in the Start-up phase to a maximum of 100 mA with 100 μ s settling time.
- PORST is active/asserted when either PORST (input) or PORST (output) is active/asserted.
- PORST (input) active means that the reset is held active by external agents by pulling the PORST pin low. It is recommended to keep the PORST (input) asserted until all the external supplies are above their primary reset thresholds.
- PORST (output) active means that μ C asserts the reset internally and drives the PORST pin low thus propagating the reset to external devices. The PORST (output) is asserted by the μ C when at least one among the three supply domains (V_{DD} , V_{DDP3} or V_{EXT}) violate their primary under-voltage reset thresholds. The PORST (output) is de-asserted by the μ C when all supplies are above their primary reset thresholds and the basic supply and clock infrastructure is available. During reset release at T3, the load jump of up to 150 mA (dI_{DD}) is expected.
- The power sequence as shown in [Figure 3-5](#) is enumerated below
 - T1 up to T3 refers to the period in time when basic supply and clock infrastructure components are available as the external supply ramps up. The bandgap and internal clock sources are started. The supply mode is evaluated based on the HWCFG[1:2,4,5,6] and TESTMODE pins. These events are initiated after LVD reset release at T1 after V_{EXT} and VEVRSB supply rails have reached VLVD RST5 level and internal pre-regulator VDDPD voltage has reached VLVD RSTC level.
 - T3 refers to the point in time when all supplies are above their primary reset thresholds denoted by VRST5, VRST33 and VRSTC supply voltage levels. PORST (output) is de-asserted and HWCFG[3:5] pins are latched on PORST rising edge by SCU. Firmware execution is initiated.
 - T4 refers to the point in time when Firmware execution is completed and User code execution starts with CPU0 at a default frequency of 100 MHz. The time between T0 and T4 is documented as tBP.
 - T5 refers to the point in time during the ramp-down phase when at least one of the externally provided supplies (V_{DD} , V_{DDP3} or V_{EXT}) drop below their respective primary under-voltage reset thresholds.

3.12 Reset Timing

Table 3-26 Reset

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time	t_B CC	-	-	400	μ s	operating with max. frequencies, with valid BMI header
System Reset Boot Time	t_{BS} CC	-	-	1.1	ms	RAM initialization and HSM boot time are not included, with valid BMI header
Cold Power on Reset Boot Time ¹⁾	t_{BP} CC	-	-	3.1	ms	$dVEXT/dT=1V/ms$. $VEXT > VLVD RST5$. Boot time after Cold PORST including EVR ramp-up and Firmware execution time; RAM initialization and HSM boot time are not included.
		-	-	1.6	ms	Firmware execution time after PORST release without EVR ramp-up; RAM initialization and HSM boot time is not included
Minimum cold PORST reset hold time in case of power fail event issued by EVR primary monitors	t_{EVRPOR} CC	$10^{2)}$	-	-	μ s	
PMS Infrastructure, EVRC and EVR33 overall start-up time till cold PORST reset release	$t_{EVRstartup}$ CC	-	-	1	ms	$dV/dT=1V/ms$. EVRC and EVR33 active
Minimum PORST active hold time externally after power supplies are stable at operating levels after start-up	t_{POA} SR	$1^{3)}$	-	-	ms	
Configurable PORST digital filter delay in addition to analog pad filter delay	$t_{PORSTDF}$ CC	600	-	1200	ns	
Warm Reset Sequencing Delay	$t_{WARMRSTSEQ}$ CC	-	-	180	μ s	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} CC	$16 / f_{SPB}$	-	-	ns	

Electrical Specification Reset Timing

Table 3-26 Reset (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	-	-	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	$8000/f_{BAC}$ KT	-	$18000/f_{BA}$ CKT	s	
Ports inactive after PORST reset active	t_{PIP} CC	-	-	160	ns	
Hold time from PORST rising edge	t_{POH} SR	150	-	-	ns	
Setup time to PORST rising edge	t_{POS} SR	0	-	-	ns	
Warm PORST reset boot time	t_{BWP} CC	-	-	1.5	ms	without RAM initialization
LBIST execution time extending the boot time	t_{LBIST} CC	-	-	6	ms	LBIST Configuration A; $1.2V \leq V_{DD}$
SCR reset boot time	t_{SCR} CC	-	-	5	μ s	User Mode 0
		-	-	16	μ s	User Mode 1
		-	13.3	-	μ s	WDT double bit ECC, soft reset
Minimum external supplies hold time after warm reset assertion	$t_{SUPHOLD}$ CC	-	-	250	μ s	external supplies are V_{EVRSB} , V_{EXT} , V_{FLEX} , V_{DDM} , V_{DDP3} and V_{DD}

- RAM initialization add 500 μ s in addition.
- Cold PORST reset is driven by uC and maintained in an extended voltage range between VDDPPA limit and absolute maximum rating VEXT/VEVRSB voltage limits.
- The reset release on supply ramp-up or supply restoration is delayed by a voltage hysteresis of 1.5% (default value) above the undervoltage reset limit implemented on VEXT, VDDP3 and VDD rails. This mechanism helps to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released.

Electrical Specification Reset Timing

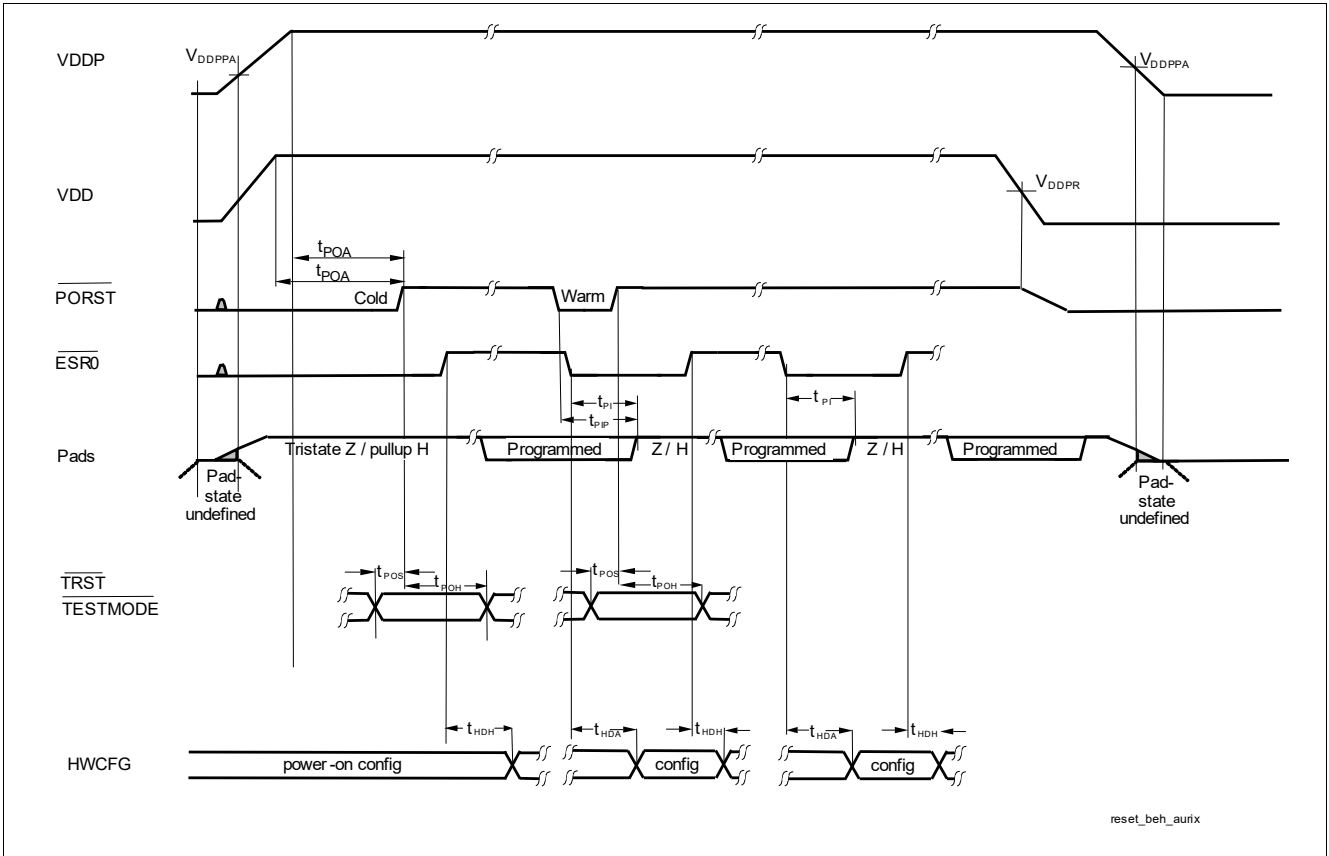


Figure 3-6 Power, Pad and Reset Timing

3.13 EVR

Table 3-27 EVR33 LDO

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage range	V_{IN} SR	3.60 ¹⁾	-	5.50	V	Normal RUN mode
		2.97 ²⁾	-	5.50	V	Low voltage cranking mode
Output voltage operational range including load/line regulation and aging ³⁾	V_{OUT} CC	2.97	3.3	3.63	V	Normal RUN mode
		2.60	3.3	3.63	V	Low voltage cranking mode; $I_{DDP3}=50mA$
Output V_{DDx3} static voltage accuracy after trimming and aging without dynamic load/line regulation.	V_{OUTT} CC	3.225	3.3	3.375	V	Normal RUN mode
		2.78	3.3	3.375	V	Low voltage cranking mode; $I_{DDP3}=50mA$
Output buffer capacitance on V_{OUT}	C_{OUT} SR	1.45	2.2	3	μF	
Output buffer capacitor ESR	C_{OUTESR} SR	-	-	100 ⁴⁾	mOhm	$f > 0.5MHz$; $f < 10MHz$
Maximum output current of the regulator	I_{MAX} CC	60 ⁵⁾	-	-	mA	Normal RUN mode
Startup time	t_{STR} CC	-	500	1000	μs	Normal RUN mode
External V_{IN} supply ramp ⁶⁾	dV_{in}/dt SR	-	1	-	V/ms	
Ripple on Output Voltage	ΔV_{OUTTC} CC	-	-	33	mV	$V_{EXT} \geq 2.97V$; $V_{EXT} \leq 5.5V$; $I_{OUTTC} \geq 10mA$; $I_{OUTTC} \leq 60mA$; $\Delta V_{OUTTC} = (\text{peak to peak ripple} / 2)$
Load step response ⁷⁾	dV_{out}/dI_{out} CC	-165	-	-	mV	Normal RUN mode; $dI=10$ to $60mA$; $dt=20ns$; $T_{settle}=20us$
		-	-	165	mV	Normal RUN mode; $dI=60$ to $10mA$; $dt=20ns$; $T_{settle}=20us$
		-180	-	-	mV	Low voltage cranking mode; $dI=10$ to $50mA$; $dt=20ns$; $T_{settle}=20us$
		-	-	180	mV	Low voltage cranking mode; $dI=50$ to $10mA$; $dt=20ns$; $T_{settle}=20us$

Table 3-27 EVR33 LDO (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line step response	dV_{out}/dV_{in} CC	-	-	40	mV	$dV_{in}/dT=1V/ms$; $dV=3.6$ to $5V$; $I_{MAX}=60mA$
		-40	-	-	mV	$dV_{in}/dT=1V/ms$; $dV=5$ to $3.6V$; $I_{MAX}=60mA$
		-	-	280	mV	$dV_{in}/dT=50V/ms$; $dV=3.6$ to $5V$; $I_{MAX}=60mA$
		-165	-	-	mV	$dV_{in}/dT=50V/ms$; $dV=5$ to $3.6V$; $I_{MAX}=60mA$

- 1) A maximum pass device dropout voltage of 300mV is included in the minimum input voltage to ensure optimal pass device performance during normal operation.
- 2) VEXT Input voltage drop up to 2.97V leading to VDDP3 output voltage drop upto 2.6V can be tolerated if Flash is switched before to low performance mode.
- 3) No external inductive load permissible if EVR33 is used.
- 4) It is also recommended that the resistance of the supply trace from the pin to the EVR output capacitor is less than 100 mOhm. An additional decoupling capacitor of 100nF shall be located close to the pin before Cout.
- 5) In case EVR33 is not used, Injection current into 3.3V VDDP3 supply rail with active sink on 5V VEXT rail should be limited to 500 mA if during power sequencing 3.3V is supplied before 5V by external regulator.
- 6) EVR is robust against residual voltage ramp-up starting between 0 - 2.97 V. A VEXT voltage ramp range between 0.5V/min upto 120V/ms is covered in robustness validation. The generated voltage itself follows a soft ramp-up over the tSTR time to avoid overshoots.
- 7) Settling time is defined until output voltage is within +/-1% of the mean(VOUTT) of the individual device.

Table 3-28 Supply Monitors

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Primary Undervoltage Reset threshold for V_{DDP3} before trimming ¹⁾	V_{RST33} CC	-	-	3.00	V	by reset release before EVR trimming on supply ramp-up
Primary undervoltage reset threshold for V_{DD} before trimming	V_{RSTC} CC	-	-	1.138	V	by reset release before trimming on supply ramp-up including 2 LSB voltage Hysteresis
V_{EXT} primary undervoltage monitor accuracy after trimming ²⁾	$V_{EXTPRIUV}$ CC	2.86	2.92	2.97	V	V_{EXT} = Undervoltage cold PORST Primary Monitor Threshold
V_{DDP3} primary undervoltage monitor accuracy after trimming ²⁾	$V_{DDP3PRIUV}$ CC	2.86 ³⁾	2.90	2.97	V	VDDP3 = Undervoltage cold PORST Primary Monitor Threshold
V_{DD} primary undervoltage monitor accuracy after trimming ²⁾	$V_{DDPRIUV}$ CC	1.08 ³⁾	1.105	1.125	V	VDD = Undervoltage cold PORST Primary Monitor Threshold

Table 3-28 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EVR primary monitor measurement latency for a new supply value	t_{PRIUV} CC	-	-	300	ns	The supply ramp / line jump slope is limited to 50V/ms for V_{EXT} , V_{DDP3} and V_{DD} rails.
V_{EXT} , V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming ^{4) 5)}	V_{EXTMON} CC	5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EBh(UV)/ECh(OV). For BGA packages: EVRMONFILT.SWDFI L=1
		5.3	5.4	5.5	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5.4V=EBh(UV)/ECh(OV). For QFP packages: EVRMONFILT.SWDFI L=2
		3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,UV). For BGA packages: EVRMONFILT.SWDFI L=1.
		3.2	3.3	3.4	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=3.3V=90h(OV,UV). For QFP packages: EVRMONFILT.SWDFI L=2
		4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV)/C9h(OV). For BGA packages: EVRMONFILT.SWDFI L=1

Table 3-28 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{EXT} , V_{DDM} & V_{EVRSB} secondary supply monitor accuracy after trimming (cont'd)	V_{EXTMON} CC	4.5	4.6	4.7	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=4.6V=C8h(UV)/C9h(OV). For QFP packages: EVRMONFILT.SWDFI L=2
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV)/DAh(OV). For BGA packages: EVRMONFILT.SWDFI L=1
		4.9	5.0	5.1	V	SWDxxVAL, VDDMxxVAL & SBxxVAL monitoring threshold=5V=D9h(UV)/DAh(OV). For QFP packages: EVRMONFILT.SWDFI L=2
V_{DDP3} secondary supply monitor accuracy after trimming ⁵⁾	$V_{DDP3MON}$ CC	2.97	3.035	3.1	V	EVR33xxVAL monitoring threshold=3.035V=CBh(UV)/CCh(OV). EVRMONFILT.EVR33 FIL = 3.
		3.235	3.30	3.365	V	EVR33xxVAL monitoring threshold=3.3V=DDh(OV,UV). EVRMONFILT.EVR33 FIL = 3.
		3.5	3.565	3.63	V	EVR33xxVAL monitoring threshold=3.565V=EEh(UV)/EFh(OV). EVRMONFILT.EVR33 FIL = 3.

Table 3-28 Supply Monitors (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DD} & V_{DDPD} secondary supply monitor accuracy after trimming ⁵⁾	V_{DDMON} CC	1.125	1.15	1.175	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.15V=C7h(UV)/C8h(OV). EVRMONFILT.EVRCFIL = 1.
		1.225	1.25	1.275	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.25V=D9h(OV,UV). EVRMONFILT.EVRCFIL = 1.
		1.325	1.35	1.375	V	EVRCxxVAL & PRExxVAL monitoring threshold=1.35V=EAh(UV)/EBh(OV). EVRMONFILT.EVRCFIL = 1.
V_{EXT} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRST5}$ CC	2.3	-	2.72	V	Power-down
		2.4	-	2.75	V	Power-up
V_{EVR5B} LVD Primary undervoltage reset Monitor threshold	$V_{LVDRST5B}$ CC	2.18	-	2.47	V	Power-down
		2.21	-	2.5	V	Power-up
V_{EXT} and V_{EVR5B} PBIST primary overvoltage Monitor threshold	V_{PBIST5} CC	5.63	-	-	V	
Primary undervoltage reset threshold for V_{EXT} before trimming	V_{RST5} CC	-	-	3.0	V	by last cold PORST release on supply ramp-up including voltage hysteresis.
EVR secondary monitor measurement latency for all 6 supply rails	t_{MON} CC	-	-	3.2	μ s	HPOSC and SHPBG bandgap trimmed. Filter inactive.

- 1) The reset release on supply ramp-up is delayed by a time duration 20-40 μ s after reaching undervoltage reset threshold and by a voltage hysteresis of 1.5% above the undervoltage reset limit. These mechanisms serve as hysteresis to avoid multiple consecutive cold PORST events during slow supply ramp-ups owing to voltage drop/current jumps when reset is released. The reset limit of 2,97V at pin is for the case with 3.3V generated internally from EVR33. In case the 3.3V supply is provided externally, the bondwire drop will cause a reset at a higher voltage of 3.0V at the VDDP3 pin.
- 2) The monitor tolerances constitute the inherent variation of the band gap and ADC over process, voltage and temperature operational ranges. The VxxPRIUV parameters are device individually tested in production with +-1% tolerance about the VxxPRIUV limits. All voltages are measured on pins.
- 3) VRSTxx parameters are relevant only for the first cold PORST release. Later the reset levels are trimmed by the Firmware and reflected as VxxPRIUV parameters before device is used with full performance. The cold PORST is released with a voltage hysteresis on all the primary monitors to avoid consecutive PORST toggling behavior.
- 4) In case the application is using 3.3V single supply (Single Supply mode (e), i.e. VEXT and VDDP3 are shorted together), it is recommended to use secondary supply monitoring on channel VDDP3, because of the better accuracy of parameter VDDP3MON.

- 5) To monitor voltage level not provided in conditions the values for OV and UV thresholds can be generated by a linear interpolation or extrapolation based on the given points.

Table 3-29 Supply Ramp

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External V_{EXT} & $V_{EVR SB}$ supply ramp-up and ramp-down slope 1) 2) 3)	dV_{EXT}/dt SR	8.3E-6	1	100	V/ms	
External V_{DDP3} supply ramp-up and ramp-down slope ¹⁾³⁾	dV_{DDP3}/dt SR	8.3E-6	1	100	V/ms	
External V_{DD} supply ramp-up and ramp-down slope ¹⁾³⁾	dV_{DD}/dt SR	8.3E-6	1	100	V/ms	
External V_{DDM} supply ramp-up and ramp-down slope ¹⁾³⁾	dV_{DDM}/dt SR	8.3E-6	1	100	V/ms	

- 1) The device is robust against residual voltage ramp-up starting between 0 - 2.97 V for V_{EXT} , $V_{EVR SB}$, V_{DDP3} and V_{DDM} and 0-1 V for V_{DD} . A voltage ramp range between 0.5V/min upto 120V/ms is covered in robustness validation.
- 2) Also valid in case EVR33 or EVRC is used. The generated voltage itself follows a soft ramp-up over the tSTR time to avoid overshoots.
- 3) The slope is defined as the maximal tangential slope between 0% to 100% voltage level. Actual waveform may not represent the specification.

Up to 1,000,000 power cycles, matching the limits defined in table 'Supply Ramp', are allowed for TC33x/TC32x without any restriction to reliability.

Table 3-30 EVR13 SMPS

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input V_{EXT} voltage range	V_{IN} SR	2.97	-	5.5	V	
SMPS regulator output voltage range including load/line regulation and aging	V_{DDDC} CC	1.125	-	1.375	V	$V_{EXT} > 2.97V$; $I_{DDDC} = 10\text{ mA} - I_{MAX}$; $f_{DCDC} = 1.85\text{MHz}$; untrimmed
SMPS regulator static voltage output accuracy after trimming without dynamic load/line regulation.	$V_{DDDC T}$ CC	1.225	1.25 ¹⁾	1.275	V	$V_{EXT} > 2.97V$; $I_{DDDC} = 10\text{ mA} - I_{MAX}$; $f_{DCDC} = 1.85\text{MHz}$
Programmable switching frequency	f_{DCDC} SR	1.6	1.85	2.0	MHz	Nominal Start-up frequency is 1.85 MHz.

Table 3-30 EVR13 SMPS (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Startup time	t_{STRDC} CC	-	-	1.1	ms	SCDCDC Start-up Mode. It is defined between VEXTPRIUV reset threshold upto nominal VDD setpoint voltage; $I_{DDSTART} < 170$ mA; $V_{DDSTART}$ overshoot < 75 mV; $dI_{EXTSTART} / dt < 100$ mA / 50us
Switching frequency modulation spread	Δf_{DCSPR} CC	-	10.74%	-	Hz	3 clock spreading @ nominal 1.85 MHz (54 clock Oversampling Factor)
Maximum ripple at I_{MAX}	ΔV_{DDDC} CC	-	-	12	mV	$\Delta V_{DDDC} = (\text{Peak to Peak ripple} / 2)$; $V_{EXT} = 3.3V \pm 10\%$; $I_{DDDC} = 10$ mA - I_{MAXSC} ; $f_{DCDC} = 1.85MHz$
		-	-	16	mV	$\Delta V_{DDDC} = (\text{Peak to Peak ripple} / 2)$; $V_{EXT} = 5V \pm 10\%$; $I_{DDDC} = 10$ mA - I_{MAXBYP} ; $f_{DCDC} = 1.85MHz$
No load current consumption of SMPS regulator	I_{DCNL} CC	-	-	1.8	mA	$f_{DCDC} = 1.85MHz$; $I_{DDDC} = 10$ mA - ISLEEP; $V_{EXT} > 2.97$ V; $T_J = 165^\circ C$
SMPS regulator load transient response	dV_{DDDC} / dI_{OUT} CC	-38	-	38	mV	$dI < \pm 100mA$; $f_{DCDC} = 1.85MHz$; $t_r = 0.1\mu s$; $t_f = 0.1\mu s$; $t_{settle} = 100\mu s$; $V_{DDDC} = 1.25V$; including ripple
		-50	-	75	mV	$dI < -200mA$; $f_{DCDC} = 1.85MHz$; $t_r = 0.1\mu s$; $t_f = 0.1\mu s$; $t_{settle} = 100\mu s$; $V_{DDDC} = 1.25V$; including ripple

Table 3-30 EVR13 SMPS (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum output current	I_{MAX} CC	400	-	-	mA	IMAXBYP; $V_{EXT} > 2.97V$; $V_{DD} = 1.125V$; $f_{DCDC} = 1.85MHz$; Bypass mode
		220 ²⁾	-	-	mA	IMAXSC; $V_{EXT} > 2.97V$; $V_{DD} = 1.125V$; $f_{DCDC} = 1.85MHz$; SC 1/2 mode with Bypass mode disabled.
		-	250	-	mA	IMAXSC; $V_{EXT} = 3.3V$; $V_{DD} = 1.25V$; $f_{DCDC} = 1.85MHz$; SC 1/2 mode with Bypass mode disabled.
SMPS regulator line transient response	dV_{DDDC} / dV_{IN} CC	-26	-	26	mV	$dV_{EXT}/dt=1V/ms$, IDDC=10-400mA, $t_{settle}<100\mu s$, including Ripple; $dV_{EXT} < 2.97 - 5.5V$
		-75	-	75	mV	$dV_{EXT}/dt=50V/ms$, IDDC=10-400mA, $t_{settle}<100\mu s$, including Ripple; $dV_{EXT} < 2.97 - 5.5V$
SMPS regulator efficiency	n_{DC} CC	-	72	-	%	$V_{EXT}=3.3V$; $I_{DDDC}=250mA$; $f_{DCDC}=1.85MHz$
		-	51	-	%	$V_{EXT}=3.3V$; $I_{DDDC}=400mA$; $f_{DCDC}=1.85MHz$
		-	42	-	%	$V_{EXT}=5V$; $I_{DDDC}=400mA$; $f_{DCDC}=1.85MHz$

1) In case of SCDCDC EVRC mode, It shall be ensured that the VDD output pin shall be connected on PCB level to all other VDD Input pins.

2) It is recommended when using the SCDCDC EVRC that the current is limited to the maximum value to have highest efficiency. EVR SRCSCDC Interrupt shall be raised in case current exceeds and Bypass mode is activated.

Table 3-31 EVR13 SMPS External components

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor value ¹⁾	C_{OUT} SR	8.84	13.6	18.36	μF	$I_{DDDC} = 10mA$ upto IMAX

Table 3-31 EVR13 SMPS External components (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
External output capacitor ESR	C_{OUT_ESR} SR	-	-	25	mOhm	$f \geq 0.5\text{MHz}$; $f \leq 7\text{MHz}$
		-	-	100	Ohm	$f=100\text{Hz}$
External input capacitor value ¹⁾	C_{IN} SR	3.06	4.7	6.35	μF	$I_{DDDC} = 10\text{mA}$ upto IMAX
External input capacitor ESR	C_{IN_ESR} SR	-	-	25	mOhm	$f \geq 0.5\text{MHz}$; $f \leq 10\text{MHz}$
		-	-	100	Ohm	$f=100\text{Hz}$
External flying capacitor value ¹⁾	C_{FLY} SR	0.65	¹²⁾	1.35	μF	$I_{DDDC} = 10\text{mA}$ upto IMAX
Flying capacitor ESR	C_{FLY_ESR} SR	-	-	25	mOhm	$f \geq 0.5\text{MHz}$; $f \leq 10\text{MHz}$
		-	-	100	Ohm	$f=100\text{Hz}$

1) Capacitor min-max range represent typical +35% tolerance including DC bias effect. The trace resistance from the capacitor to the supply or ground rail should be limited to 25 mOhm.

2) It is recommended to place the flying capacitor close to the pins without vias to have minimal routing resistance from pin to the capacitor terminal of less than 25mOhm.

3.14 System Phase Locked Loop (SYS_PLL)

Table 3-32 PLL System

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DCO Input frequency range	f_{REF} CC	10	-	40	MHz	
Modulation Amplitude	MA CC	0	-	2	%	
Peak Period jitter	DP CC	-200	-	200	ps	without modulation (PLL output frequency)
Peak Accumulated Jitter	D_{PP} CC	-5	-	5	ns	without modulation
Total long term jitter	J_{TOT} CC	-	-	11.5	ns	including modulation; MA 1.25%; f_{REF} 20MHz
System frequency deviation	f_{SYSD} CC	-	-	0.01	%	with active modulation
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
PLL lock-in time	t_L CC	4	-	100	μ s	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20$ pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of $V_{PP} = 100$ mV for noise frequencies below 300 KHz and $V_{PP} = 40$ mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

3.15 Peripheral Phase Locked Loop (PER_PLL)

Table 3-33 PLL Peripheral

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Peak Accumulated jitter at SYSCLK pin	D_{PP} CC	-1000	-	1000	ps	Peak only
Peak accumulated jitter	D_{PPI} CC	-700	-	700	ps	Peak only
RMS Accumulated jitter	D_{RMS} CC	-100	-	100	ps	measured over 1 μ s; $f_{REF} = 20$ MHz and $f_{DCO} = 640$ MHz or $f_{REF} = 25$ MHz and $f_{DCO} = 800$ MHz
Peak Period jitter	DP CC	-200	-	200	ps	$f_{DCO} = 640$ MHz or $f_{DCO} = 800$ MHz
Absolute RMS jitter (PLL out)	J_{ABS10} CC	-125	-	125	ps	$f_{REF} = 10$ MHz; $f_{DCO} = 640$ MHz
Absolute RMS jitter (PLL out)	J_{ABS20} CC	-85	-	85	ps	$f_{REF} = 20$ MHz; $f_{DCO} = 640$ MHz
Absolute RMS jitter (PLL out)	J_{ABS25} CC	-85	-	85	ps	$f_{REF} = 25$ MHz; $f_{DCO} = 800$ MHz
DCO frequency range	f_{DCO} CC	400	-	800	MHz	
DCO input frequency range	f_{REF} CC	10	-	40	MHz	
PLL lock-in time	t_L CC	4	-	100	μ s	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed $C_L = 20$ pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the power supply voltage, is limited to a peak-to-peak voltage of $V_{PP} = 100$ mV for noise frequencies below 300 KHz and $V_{PP} = 40$ mV for noise frequencies above 300 KHz. These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

3.16 AC Specifications

All AC parameters are specified for the complete operating range defined in [Chapter 3.4](#) unless otherwise noted in column Note / Test Condition.

Unless otherwise noted in the figures the timings are defined with the following guidelines:

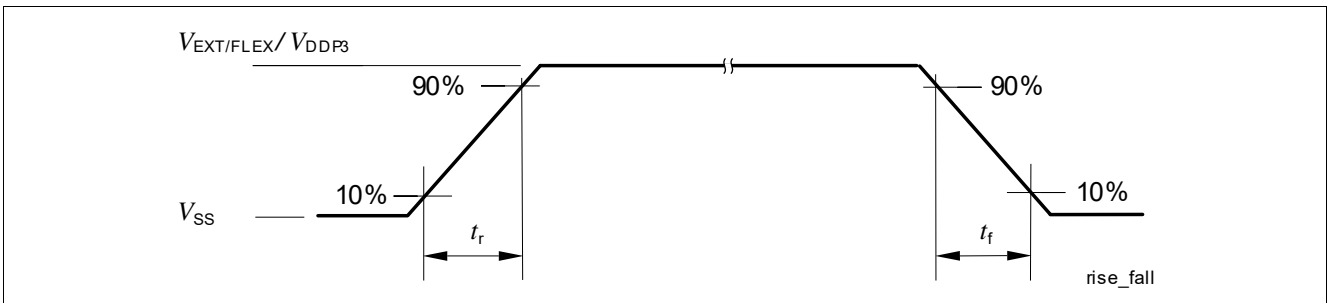


Figure 3-7 Definition of rise / fall times

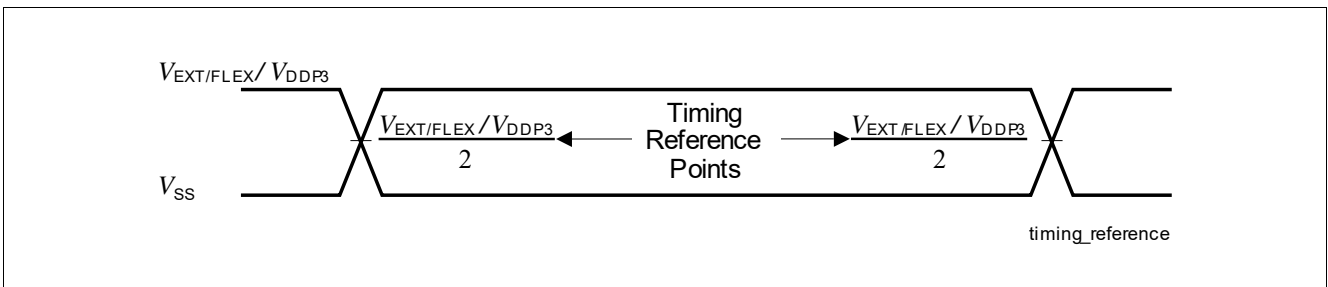


Figure 3-8 Time Reference Point Definition

3.17 JTAG Parameters

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Table 3-34 JTAG

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	-	-	ns	
TCK high time	t_2 SR	10	-	-	ns	
TCK low time	t_3 SR	10	-	-	ns	
TCK clock rise time	t_4 SR	-	-	4	ns	
TCK clock fall time	t_5 SR	-	-	4	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6.0	-	-	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6.0	-	-	ns	
TDO valid after TCK falling edge (propagation delay)	t_8 CC	3.0	-	-	ns	$C_L \leq 20\text{pF}$
		-	-	25	ns	$C_L \leq 50\text{pF}$
TDO hold after TCK falling edge	t_{18} CC	2	-	-	ns	
TDO high impedance to valid from TCK falling edge	t_9 CC	-	-	25	ns	$C_L \leq 50\text{pF}$
TDO valid output to high impedance from TCK falling edge	t_{10} CC	-	-	25	ns	$C_L \leq 50\text{pF}$

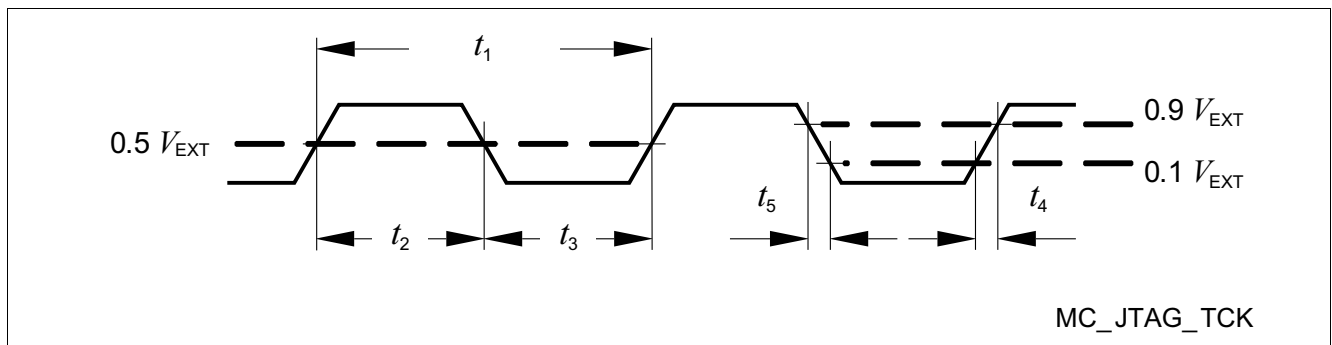


Figure 3-9 Test Clock Timing (TCK)

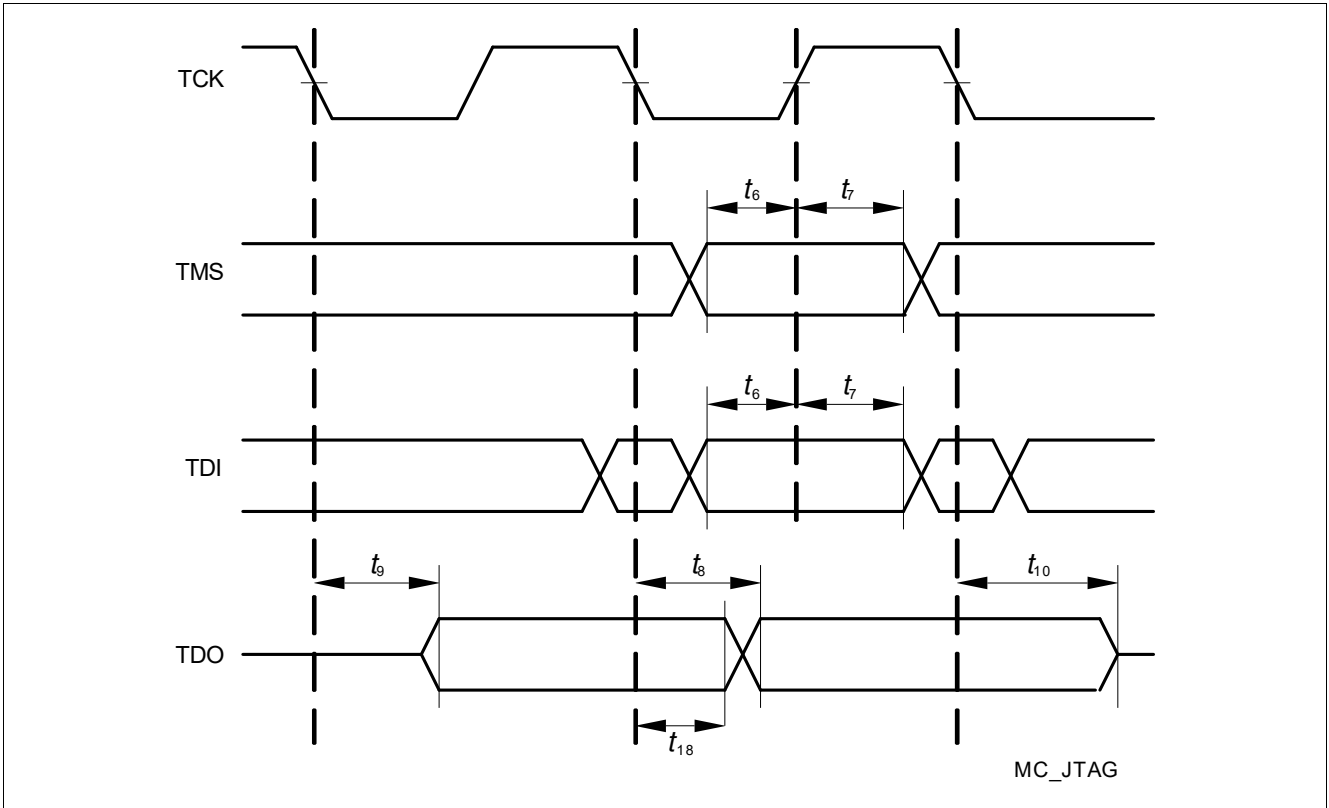


Figure 3-10 JTAG Timing

3.18 DAP Parameters

The following parameters are applicable for communication through the DAP debug interface.

Table 3-35 DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP0 clock fall time	t_{15} SR	-	-	1	ns	f=160MHz
		-	-	4	ns	f=40MHz
		-	-	2	ns	f=80MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	4	-	-	ns	
		5	-	-	ns	f=40MHz
DAP1 hold after DAP0 rising edge	t_{17} SR	2	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	4	-	-	ns	$C_L=20\text{pF}$; f=160MHz
		8	-	-	ns	$C_L=20\text{pF}$; f=80MHz
		10	-	-	ns	$C_L=50\text{pF}$; f=40MHz
DAP0 high time	t_{12} SR	2	-	-	ns	
DAP0 low time	t_{13} SR	2	-	-	ns	
DAP0 clock period	t_{11} SR	6.25	-	-	ns	

Table 3-36 SCR DAP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock rise time	t_{14} SR	-	-	8	ns	f=20MHz
DAP0 clock fall time	t_{15} SR	-	-	8	ns	f=20MHz
DAP1 setup to DAP0 rising edge	t_{16} SR	10	-	-	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	10	-	-	ns	
DAP1 valid per DAP0 clock period	t_{19} CC	30	-	-	ns	$C_L=20\text{pF}$; f=20MHz
DAP0 high time	t_{12} SR	15	-	-	ns	
DAP0 low time	t_{13} SR	15	-	-	ns	
DAP0 clock period	t_{11} SR	50	-	-	ns	

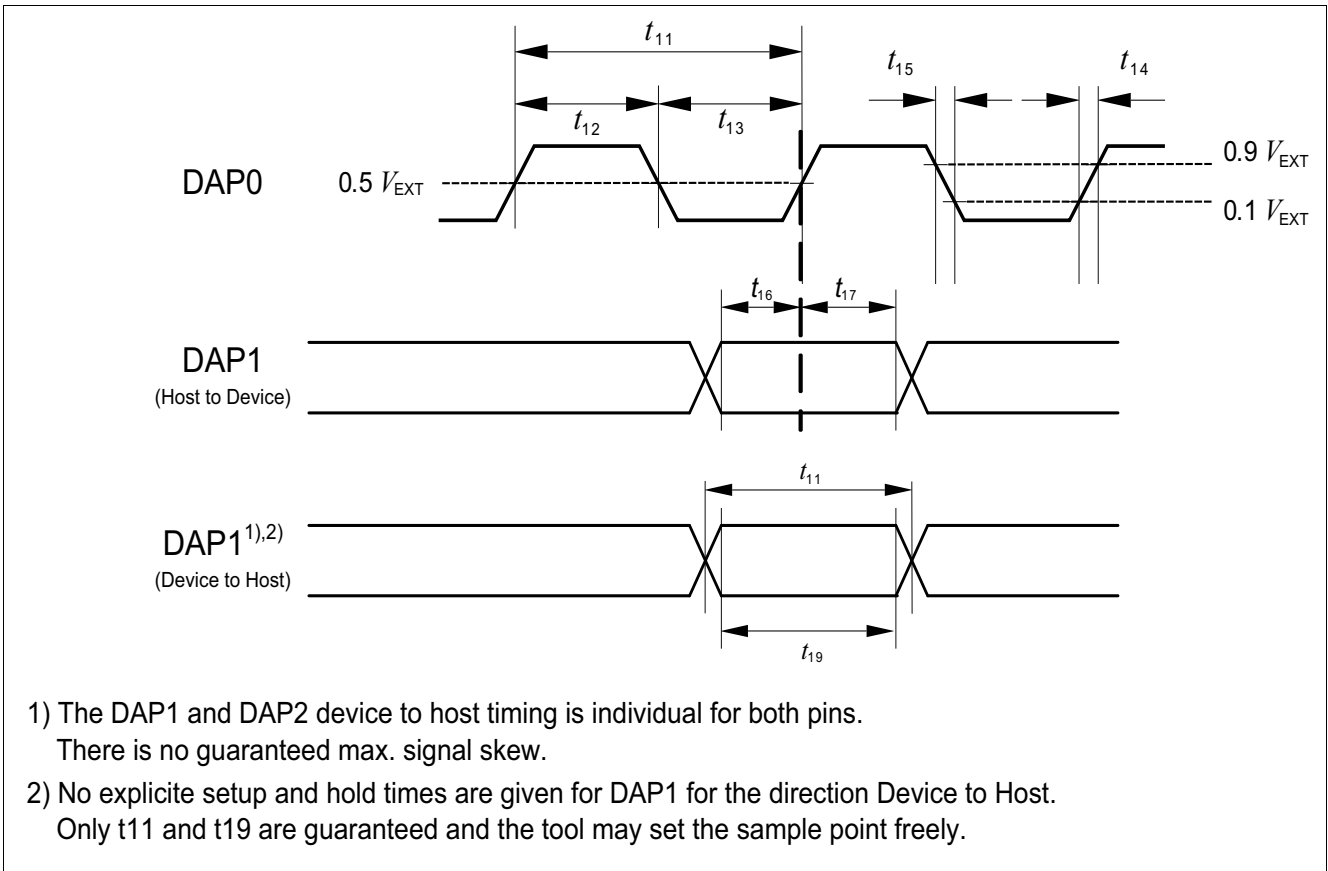


Figure 3-11 DAP Timing

Note: The DAP1 and DAP2 device to host timing is individual for both pins. There is no guaranteed max. signal skew.

3.19 ASCLIN SPI Master Timing

This section defines the timings for the ASCLIN in the TC33x/TC32x.

Note: Pad asymmetry is already included in the following timings.

Table 3-37 Master Mode strong sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	20	-	-	ns	$C_L=25\text{pF}$
Deviation from ideal duty cycle	t_{500} CC	-2	-	2	ns	$C_L=25\text{pF}$
MTSR delay from ASCLKO shifting edge	t_{51} CC	-3.5	-	3.5	ns	$C_L=25\text{pF}$
ASLSON delay from the first ASCLKO edge	t_{510} CC	-3	-	3.5	ns	$C_L=25\text{pF}$
MRST setup to ASCLKO latching edge	t_{52} SR	25	-	-	ns	$C_L=25\text{pF}$
MRST hold from ASCLKO latching edge	t_{53} SR	-2	-	-	ns	$C_L=25\text{pF}$

Table 3-38 Master Mode strong medium (sm) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	50	-	-	ns	$C_L=50\text{pF}$
Deviation from ideal duty cycle	t_{500} CC	-5	-	5	ns	$C_L=50\text{pF}$
MTSR delay from ASCLKO shifting edge	t_{51} CC	-7	-	7	ns	$C_L=50\text{pF}$
ASLSON delay from the first ASCLKO edge	t_{510} CC	-7	-	7	ns	$C_L=50\text{pF}$
MRST setup to ASCLKO latching edge	t_{52} SR	35	-	-	ns	$C_L=50\text{pF}$
MRST hold from ASCLKO latching edge	t_{53} SR	-5	-	-	ns	$C_L=50\text{pF}$

Table 3-39 Master Mode medium (m) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
ASCLKO clock period	t_{50} CC	160	-	-	ns	$C_L=50\text{pF}$
Deviation from ideal duty cycle	t_{500} CC	-10	-	10	ns	$C_L=50\text{pF}$
MTSR delay from ASCLKO shifting edge	t_{51} CC	-20	-	20	ns	$C_L=50\text{pF}$
ASLSON delay from the first ASCLKO edge	t_{510} CC	-20	-	20	ns	$C_L=50\text{pF}$

Electrical Specification ASCLIN SPI Master Timing

Table 3-39 Master Mode medium (m) output pads (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MRST setup to ASCLKO latching edge	t_{52} SR	80	-	-	ns	$C_L=50pF$
MRST hold from ASCLKO latching edge	t_{53} SR	-15	-	-	ns	$C_L=50pF$

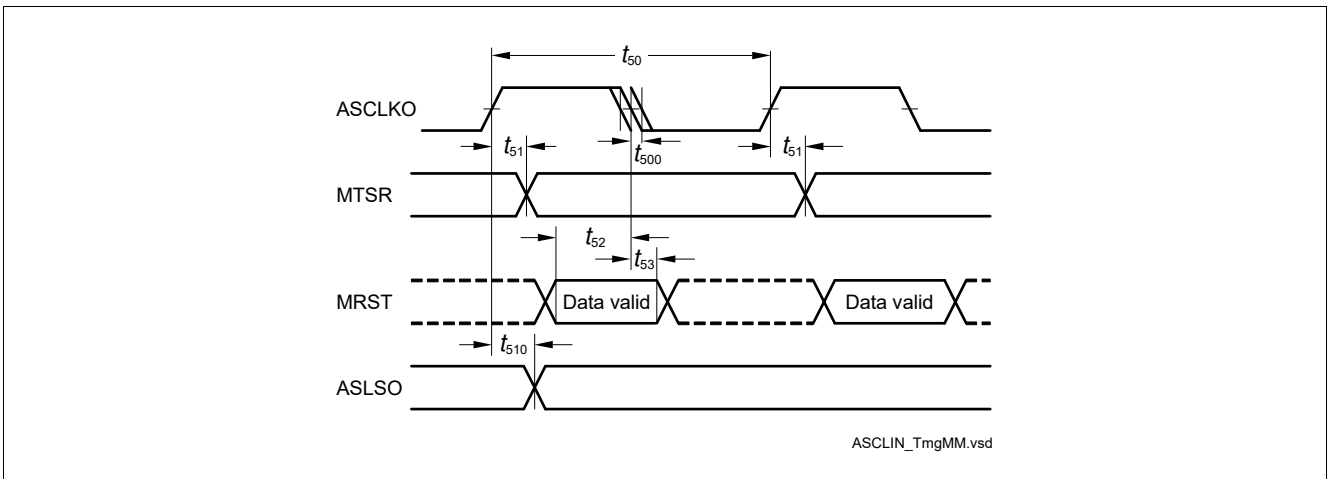


Figure 3-12 ASCLIN SPI Master Timing

Electrical Specification QSPI Timings, Master and Slave Mode

3.20 QSPI Timings, Master and Slave Mode

This section defines the timings for the QSPI in the TC33x/TC32x.

It is assumed that SCLKO, MTSR, and SLSO pads have the same pad settings:

Note: Pad asymmetry is already included in the following timings.

Table 3-40 Master Mode Timing, LVDS output pads for data and clock

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	20 ¹⁾	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-1 ¹⁾	-	1 ¹⁾	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-3 ¹⁾	-	4 ¹⁾	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4 ¹⁾	-	5.5 ¹⁾	ns	$C_L=25\text{pF}$, driver strength ss
		-10 ¹⁾	-	10 ¹⁾	ns	$C_L=25\text{pF}$, driver strength sm
		-30 ¹⁾	-	30 ¹⁾	ns	$C_L=25\text{pF}$, driver strength m
MRST setup to SCLK latching edge	t_{52} SR	18 ¹⁾	-	-	ns	CL=25pF; valid for LVDS Input pads of QSPI2 only
MRST hold from SCLK latching edge	t_{53} SR	-1 ¹⁾	-	-	ns	CL=25pF; valid for LVDS Input pads only

1) The load ($C_L=25\text{pF}$) defined in the condition list is a load definition for the single end signal SLSO and does not intend to add an additional load inside the differential signal lines. For single end signals the load definition defines the max length of the signal on the PCB layout. For the LVDS pads the IEEE Std 1596.3-1996 load definitions apply.

Table 3-41 Master Mode Strong Sharp (ss) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=25pF
Deviation from the ideal duty cycle	t_{500} CC	-2	-	2	ns	CL=25pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-4	-	5	ns	CL=25pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-4	-	5	ns	CL=25pF
MRST setup to SCLK latching edge	t_{52} SR	25 ^{1) 2)}	-	-	ns	CL=25pF
MRST hold from SCLK latching edge	t_{53} SR	-2 ¹⁾²⁾	-	-	ns	CL=25pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Electrical Specification QSPI Timings, Master and Slave Mode

Table 3-42 Master Mode Strong Medium (sm) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	50	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-5	-	5	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-7	-	7	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-7	-	7	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	35 ^{1) 2)}	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-5 ¹⁾²⁾	-	-	ns	CL=50pF

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-43 Master Mode Medium (m) output pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKO clock period	t_{50} CC	160	-	-	ns	CL=50pF
Deviation from the ideal duty cycle	t_{500} CC	-10	-	10	ns	CL=50pF
MTSR delay from SCLKO shifting edge	t_{51} CC	-20	-	20	ns	CL=50pF
SLSOn deviation from the ideal programmed position	t_{510} CC	-20	-	20	ns	CL=50pF
MRST setup to SCLK latching edge	t_{52} SR	80 ^{1) 2)}	-	-	ns	CL=50pF
MRST hold from SCLK latching edge	t_{53} SR	-15 ¹⁾²⁾	-	-	ns	CL=50pF
		-13 ¹⁾²⁾	-	-	ns	CL=50pF; SCR SSC

1) For compensation of the average on-chip delay the QSPI module provides the bit fields ECONz.A, B and C.

2) The setup and hold times are valid for both settings of the input pads thresholds: TTL and AL.

Table 3-44 Slave mode timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period	t_{54} SR	$4 \times T_{MAX}$	-	-	ns	
SCLK duty cycle	t_{55}/t_{54} SR	40	-	60	%	
MTSR setup to SCLK latching edge	t_{56} SR	6	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL

Electrical Specification QSPI Timings, Master and Slave Mode

Table 3-44 Slave mode timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MTSR hold from SCLK latching edge	t_{57} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI setup to first SCLK shift edge	t_{58} SR	4	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
SLSI hold from last SCLK latching edge	t_{59} SR	3	-	-	ns	Input Level AL
		6	-	-	ns	Input Level TTL
MRST delay from SCLK shift edge	t_{60} CC	5	-	35	ns	driver = strong edge = medium ; $C_L=50pF$
		2	-	24	ns	driver = strong edge = sharp ; $C_L=50pF$
		15	-	80	ns	medium driver ; $C_L=50pF$
		14	-	-	ns	medium driver ; $C_L=50pF$; SCR SSC

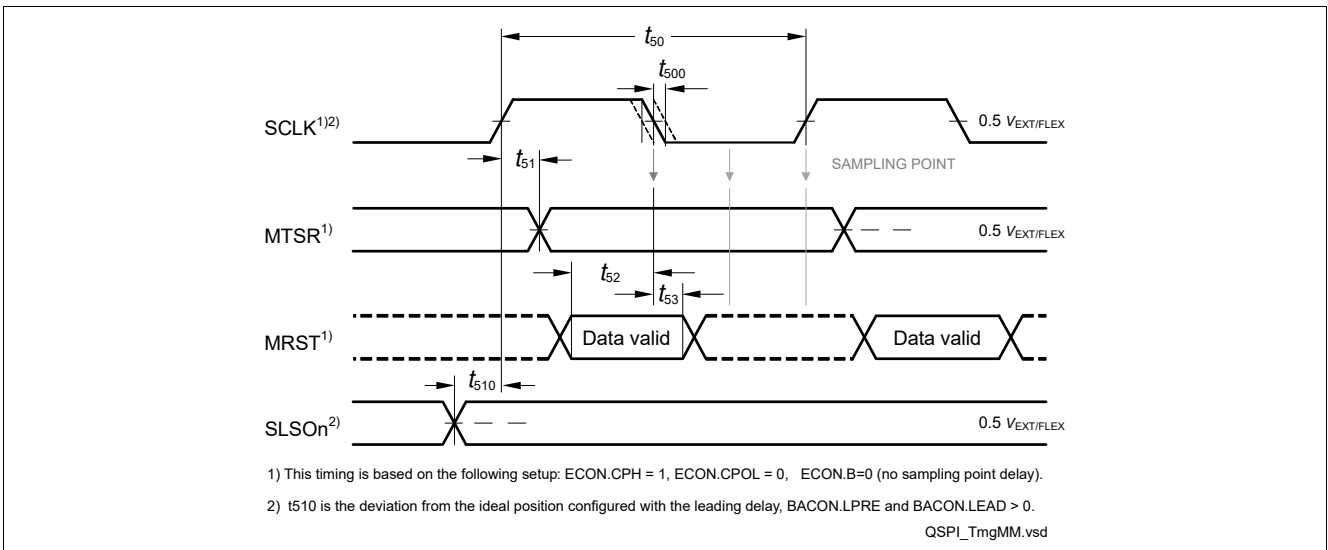


Figure 3-13 Master Mode Timing

Electrical Specification QSPI Timings, Master and Slave Mode

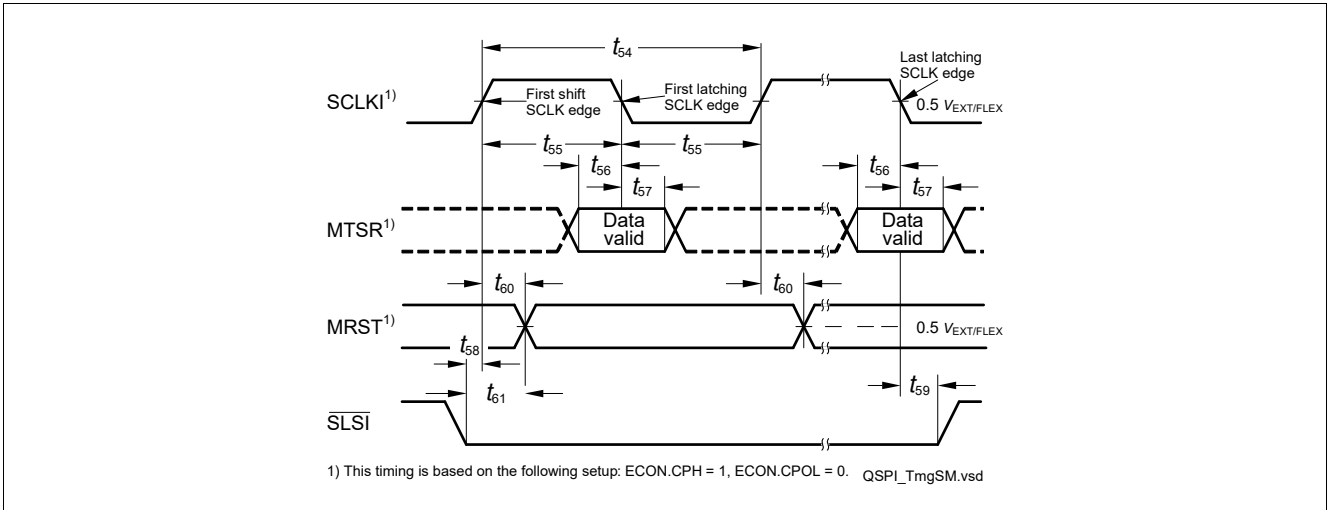


Figure 3-14 Slave Mode Timing

3.21 E-Ray Parameters

The timings of this section are valid for the strong driver and sharp edge settings of the output drivers with $C_L = 25$ pF.

Table 3-45 Transmit Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time of TxEN	$t_{dCCTxENRise25CC}$	-	-	9	ns	$C_L=25pF$
Fall time of TxEN	$t_{dCCTxENFall25CC}$	-	-	9	ns	$C_L=25pF$
Sum of rise and fall time	$t_{dCCTxRise25+dCCTxFall25CC}$	-	-	9	ns	20% - 80% ; $C_L=25pF$
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxEN	$t_{dCCTxEN01CC}$	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxEN	$t_{dCCTxEN10CC}$	-	-	25	ns	
Asymmetry of sending	$t_{tx_asym}CC$	-2.45	-	2.45	ns	$C_L=25pF$
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, rising edge of TxD	$t_{dCCTxD01CC}$	-	-	25	ns	
Sum of delay between TP1_FF and TP1_CC and delays derived from TP1_FFi, falling edge of TxD	$t_{dCCTxD10CC}$	-	-	25	ns	
TxD signal sum of rise and fall time at TP1_BD	$t_{txd_sum}CC$	-	-	9	ns	

Table 3-46 Receive Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept25SR}$	-30.5	-	43.0	ns	$C_L=25pF$
Acceptance of asymmetry at receiving part	$t_{dCCTxAsymAccept15SR}$	-31.5	-	44.0	ns	$C_L=15pF$
Threshold for detecting logical high	$T_{uCCLogic1SR}$	35	-	70	%	
Threshold for detecting logical low	$T_{uCCLogic0SR}$	30	-	65	%	

Table 3-46 Receive Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, rising edge of RxD	$t_{dCCRxD01}$ CC	-	-	10	ns	
Sum of delay between TP4_CC and TP4_FF and delays derived from TP4_FFi, falling edge of RxD	$t_{dCCRxD10}$ CC	-	-	10	ns	

3.22 FSP Parameter

Table 3-47 Safety

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Skew between FSP0 and FSP1	t_{FSPSKEW} CC	-8	-	9	ns	$C_L=50\text{pF}$, driver strength m
		-5	-	6	ns	$C_L=50\text{pF}$, driver strength sm
		-4	-	5	ns	$C_L=50\text{pF}$, driver strength ss

Electrical Specification Flash Target Parameters

3.23 Flash Target Parameters

Table 3-48 Flash

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program Flash Erase Time per logical sector ¹⁾	t_{ERP} CC	-	-	0.5	s	cycle count < 1000
Program Flash Erase Time per Multi-Sector Command ¹⁾	t_{MERP} CC	-	-	0.5	s	For consecutive logical sectors in a physical sector with total range ≤ 512 kByte; cycle count < 1000
Program Flash program time per page in 5 V mode ¹⁾	t_{PRP5} CC	-	-	80	μs	32 Byte
Program Flash program time per page in 3.3 V mode ¹⁾	t_{PRP3} CC	-	-	115	μs	32 Byte
Program Flash program time per burst in 5 V mode ¹⁾	t_{PRPB5} CC	-	-	220	μs	256 Byte
Program Flash program time per burst in 3.3 V mode ¹⁾	t_{PRPB3} CC	-	-	530	μs	256 Byte
Program Flash program time for 1 MByte with burst programming in 3.3 V mode excluding communication ¹⁾	t_{PRPB3_1MB} CC	-	-	2.2	s	Derived value for documentation purpose
Program Flash program time for 1 MByte with burst programming in 5 V mode excluding communication ¹⁾	t_{PRPB5_1MB} CC	-	-	1	s	Derived value for documentation purpose
Program Flash program time for complete PFlash with burst programming in 5 V mode excluding communication ¹⁾	t_{PRPB5_PF} CC	-	-	2	s	Derived value for documentation purpose
Write Page Once adder ¹⁾	t_{ADD} CC	-	-	20	μs	Adder to Program Time when using Write Page Once
Program Flash suspend to read latency ¹⁾	t_{SPNDP} CC	-	-	120	μs	For Write Burst, Verify Erased and for multi-(logical) sector erase commands
Data Flash Erase Disturb Limit (single ended sensing mode)	N_{DFD} CC	-	-	50	cycles	
Data Flash Erase Disturb Limit (complement sensing mode)	N_{DFDC} CC	-	-	500	cycles	
UCB Erase Disturb Limit	N_{UCBD} CC	-	-	500	cycles	

Electrical Specification Flash Target Parameters
Table 3-48 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Program time data flash per page ¹⁾²⁾	t_{PRD} CC	-	-	75	μ s	8 Byte
Complete Device Flash Erase Time PFlash and DFlash ^{1)3) 4) 5)}	t_{ER_Dev} CC	-	1.8	3	s	Valid for less than 1000 cycles, w/o UCB. Derived value for documentation purpose.
Data Flash program time per burst ¹⁾²⁾	t_{PRDB} CC	-	-	140	μ s	32 Byte
Data Flash suspend to read latency ¹⁾	t_{SPNDD} CC	-	-	120	μ s	
Wait time after margin change	$t_{FL_MarginDel}$ CC	-	-	2	μ s	
Program Flash Endurance per Logical Sector	N_{E_P} CC	-	-	1000	cycles	Replace logical sector command shall be used if a sector fails during erase or program
Number of erase operations per physical sector in program flash	N_{ERP} CC	-	-	16000	cycles	
Program Flash Retention Time, Sector	t_{RET} CC	20	-	-	years	Max. 1000 erase/program cycles
UCB Retention Time	t_{RTU} CC	20	-	-	years	Max. 100 erase/program cycles per UCB, max 500 erase/program cycles for all UCBs together
Data Flash access delay	t_{DF} CC	-	-	100	ns	see RFLASH of DMU register HF_DWAIT
Data Flash ECC Delay	t_{DFECC} CC	-	-	20	ns	see RECC of DMU register HF_DWAIT
Program Flash access delay	t_{PF} CC	-	-	30	ns	see RFLASH of DMU register HF_PWAIT
Program Flash ECC delay	t_{PFECC} CC	-	-	10	ns	see RECC and CECC of DMU register HF_PWAIT
Number of erase operations on DF0 over lifetime (complement sensing mode) ⁶⁾	N_{ERD0C} CC	-	-	4000000	cycles	
Number of erase operations on DF0 over lifetime (single ended sensing mode) ⁷⁾	N_{ERD0S} CC	-	-	750000	cycles	

Electrical Specification Flash Target Parameters
Table 3-48 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase operations on DF1 over lifetime (complement sensing mode) ⁶⁾	N_{ERD1C} CC	-	-	2000000	cycles	
Number of erase operations on DF1 over lifetime (single ended sensing mode) ⁷⁾	N_{ERD1S} CC	-	-	500000	cycles	
Data Flash Endurance per EEPROMx sector (complement sensing mode) ⁸⁾	N_{E_EEP10C} CC	-	-	500000	cycles	Max. data retention time 10 years
DataFlash Endurance per EEPROMx sector (single ended sensing mode) ⁸⁾	N_{E_EEP10S} CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Data Flash Endurance per HSMx sector (complement sensing mode) ⁸⁾	N_{E_HSMC} CC	-	-	250000	cycles	Max. data retention time 10 years
Data Flash Endurance per HSMx sector (single ended sensing mode) ⁸⁾	$N_{E_HSM S}$ CC	-	-	125000	cycles	Retention time and Tj according below example temperature profile
		-	-	125000	cycles	max data retention time 20y, Tj=110°C
		-	-	125000	cycles	max data retention time 8.2y, Tj=125°C
Junction temperature limit for PFlash program/erase operations	$T_{JPFlash}$ SR	-	-	150	°C	
Data Flash Erase Time per Sector ¹⁾³⁾⁵⁾	t_{ERD1} CC	-	-	0.5	s	Max. 1000 erase/program cycles
Data Flash Erase Time per Sector ¹⁾³⁾⁵⁾	t_{ERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10 and NE_HSM parameters
DataFlash Adder on Erase Time per 32kByte erase size when using complement sensing mode ¹⁾	$t_{ER_ADDC32C}$ CC	-	-	50	ms	Adder per 32 kByte on erase time; applicable only when using complement mode

Electrical Specification Flash Target Parameters
Table 3-48 Flash (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Multi-Sector Command ¹⁾³⁾⁵⁾	t_{MERD1} CC	-	-	0.5	s	Max 1000 erase/program cycles; For consecutive logical sectors ≤ 256 KBytes
Data Flash Erase Time per Multi-Sector Command ¹⁾³⁾⁵⁾	t_{MERDM} CC	-	-	1.5	s	Max allowed cycles, see NE_EEP10x and NE_HSMx Parameters; For consecutive logical sectors ≤ 256 kByte
Program Flash Access Delay at reduced VDDP3 voltage supply during cranking	$t_{PF_low_VDDP3}$ CC	-	-	60	ns	see register DMU_HF_PWAIT.CFLASH
Data Flash Erase Verify time per page (Complement Sensing) ²⁾	$t_{VER_PAGE_DC}$ CC	-	-	10	μ s	Time per 8 Byte page for Verify Erased Page command
Data Flash Erase Verify time per page (Single Ended Sensing) ¹⁾	$t_{VER_PAGE_DS}$ CC	-	-	10	μ s	Time per 8 Byte page for Verify Erased Page command
Program Flash Erase Verify time per page ¹⁾	$t_{VER_PAGE_P}$ CC	-	-	10	μ s	Time per 32 Byte page for Verify Erased Page command
Data Flash Erase Verify time per sector (Complement Sensing) ¹⁾	$t_{VER_SEC_DC}$ CC	-	-	200	μ s	Time per 2 KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per sector (Single Ended Sensing) ¹⁾	$t_{VER_SEC_DS}$ CC	-	-	360	μ s	Time per 4 KB sector for Verify Erased Logical Sector Range command
Program Flash Erase Verify time per sector ¹⁾	$t_{VER_SEC_P}$ CC	-	-	360	μ s	Time per 16KB sector for Verify Erased Logical Sector Range command
Data Flash Erase Verify time per wordline (Complement Sensing) ¹⁾	$t_{VER_WL_DC}$ CC	-	-	30	μ s	
Data Flash Erase Verify time per wordline (Single Ended Sensing) ¹⁾	$t_{VER_WL_DS}$ CC	-	-	50	μ s	
Program Flash Erase Verify time per wordline ¹⁾	$t_{VER_WL_P}$ CC	-	-	30	μ s	

1) Only valid for $f_{FSI} = 100$ MHz.

2) Time is not dependent on program mode (5V or 3.3V).

Electrical Specification Flash Target Parameters

- 3) Under out-of-spec conditions (e.g. over-cycling) or in case of activation of WL oriented defects, the duration of erase processes may be increased by up to 50%.
- 4) Using 512 kByte / 256 kByte erase commands (PFlash / DFlash).
- 5) If the DataFlash is operated in Complement Sensing Mode the erase time is increased by $\text{erase_size} / 32\text{kByte} \times t_{\text{ER_ADDC32C}}$
- 6) Allows segmentation of addressable memory into 8 logical sectors; round robin cycling must still be done to consider erase disturb limit N_{DFD} .
- 7) Allows segmentation of addressable memory into 6 logical sectors; round robin cycling must still be done to consider erase disturb limit N_{DFD} .
- 8) Only valid when a robust EEPROM emulation algorithm is used. For more details see the Users Manual.

3.24 Quality Declarations

Table 3-49 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Moisture Sensitivity Level	MSL CC	-	-	3		Conforming to Jedec J-STD--020C for 240C
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM} SR	-	-	500	V	for all other balls/pins; conforming to JESD22-C101-C
		-	-	750	V	for corner balls/pins; conforming to JESD22-C101-C
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	-	2000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins according to Human Body Model (HBM)	V_{HBM1} SR	-	-	2000	V	
Operation Lifetime	t_{OP} CC	-	-	24500	hour	see below temperature profile as an example

Example Temperature Profile

The following temperature profile is an example. Application specific temperature profiles need to be aligned and approved by Infineon Technologies for the fulfillment of quality and reliability targets.

Table 3-50 Example Temperature Profile

$T_j =$	Duration [h]	Comment
$\leq 170^\circ\text{C}$	≤ 30	
$\leq 160^\circ\text{C}$	≤ 120	
$\leq 150^\circ\text{C}$	≤ 220	
$\leq 140^\circ\text{C}$	≤ 350	
$\leq 130^\circ\text{C}$	≤ 780	
$\leq 120^\circ\text{C}$	≤ 1600	
$\leq 110^\circ\text{C}$	≤ 3000	
$\leq 100^\circ\text{C}$	≤ 7000	
$\leq 90^\circ\text{C}$	≤ 8000	
$\leq 80^\circ\text{C}$	≤ 2400	
$\leq 70^\circ\text{C}$	≤ 1000	
	≤ 24500	total time

Table 3-51 Example Inactive Lifetime Temperature Profile

T_J =	Duration [h]	Comment
$\leq 55^\circ\text{C}$	≤ 150700	

3.25 Package Outline

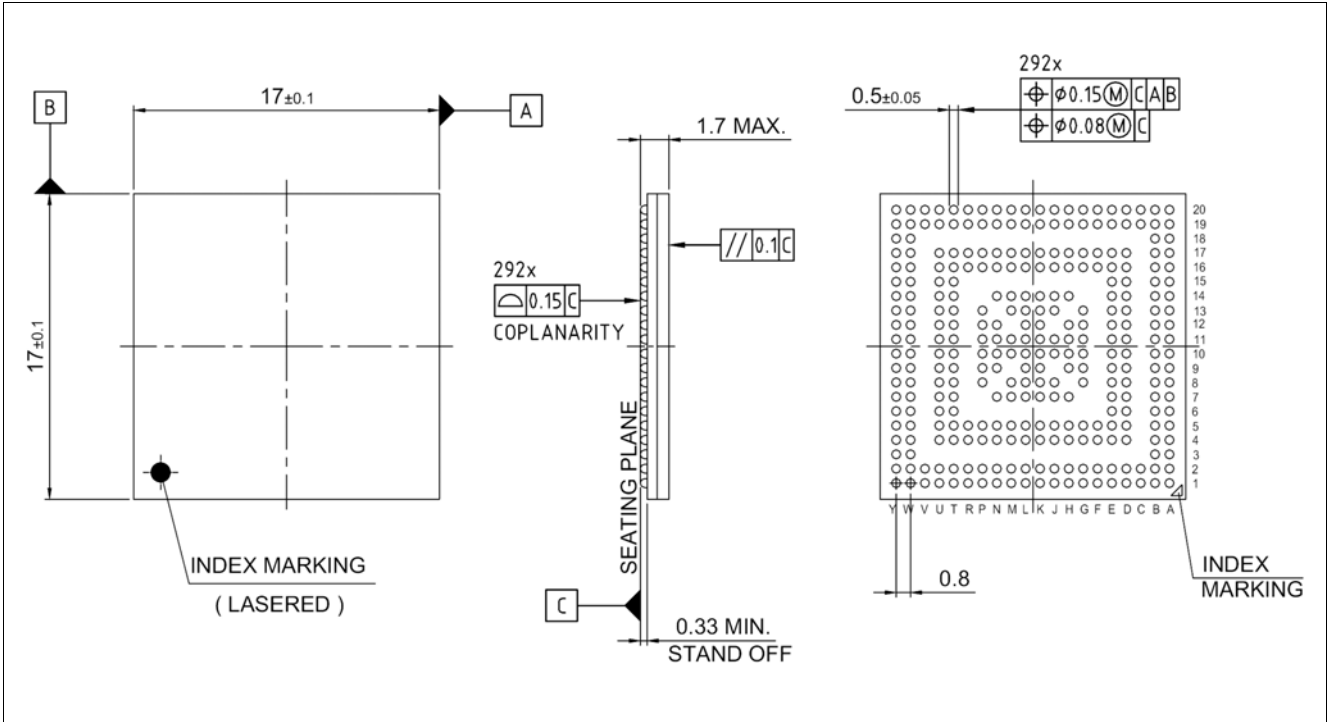


Figure 3-15 Package Outlines LFBGA-292

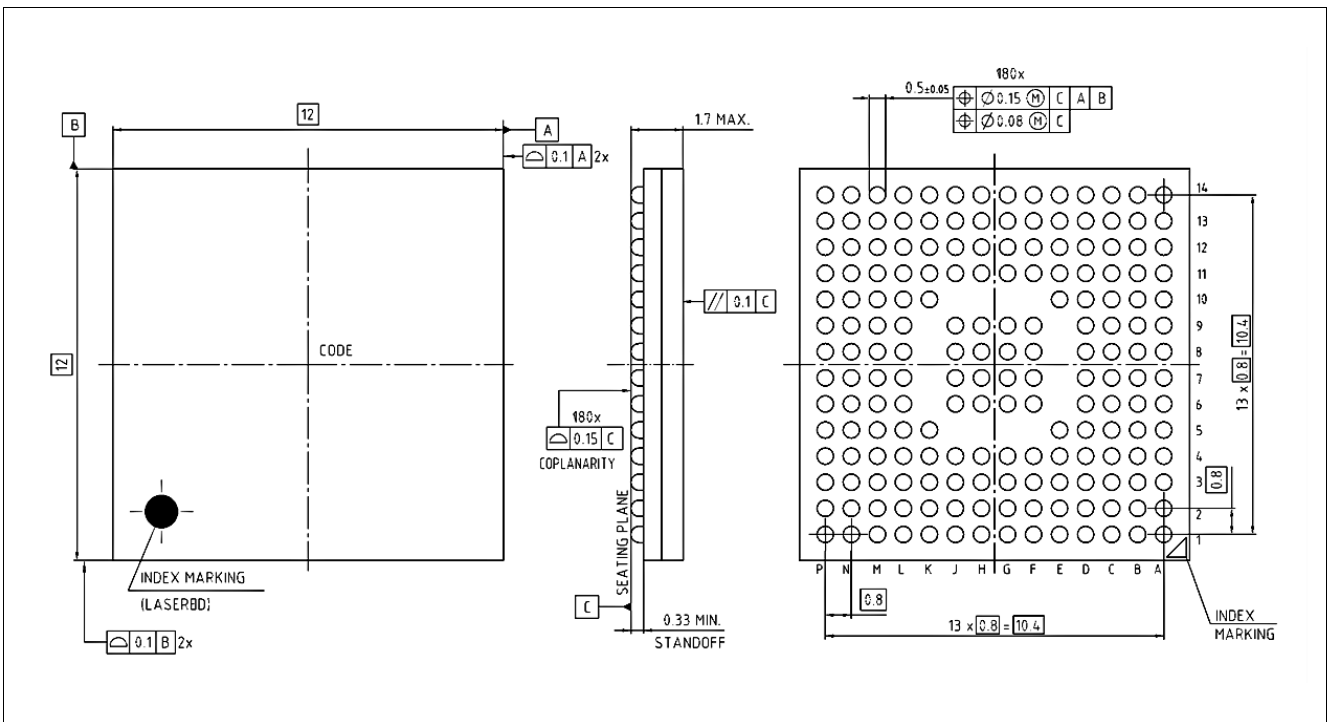


Figure 3-16 Package Outlines LFBGA-180

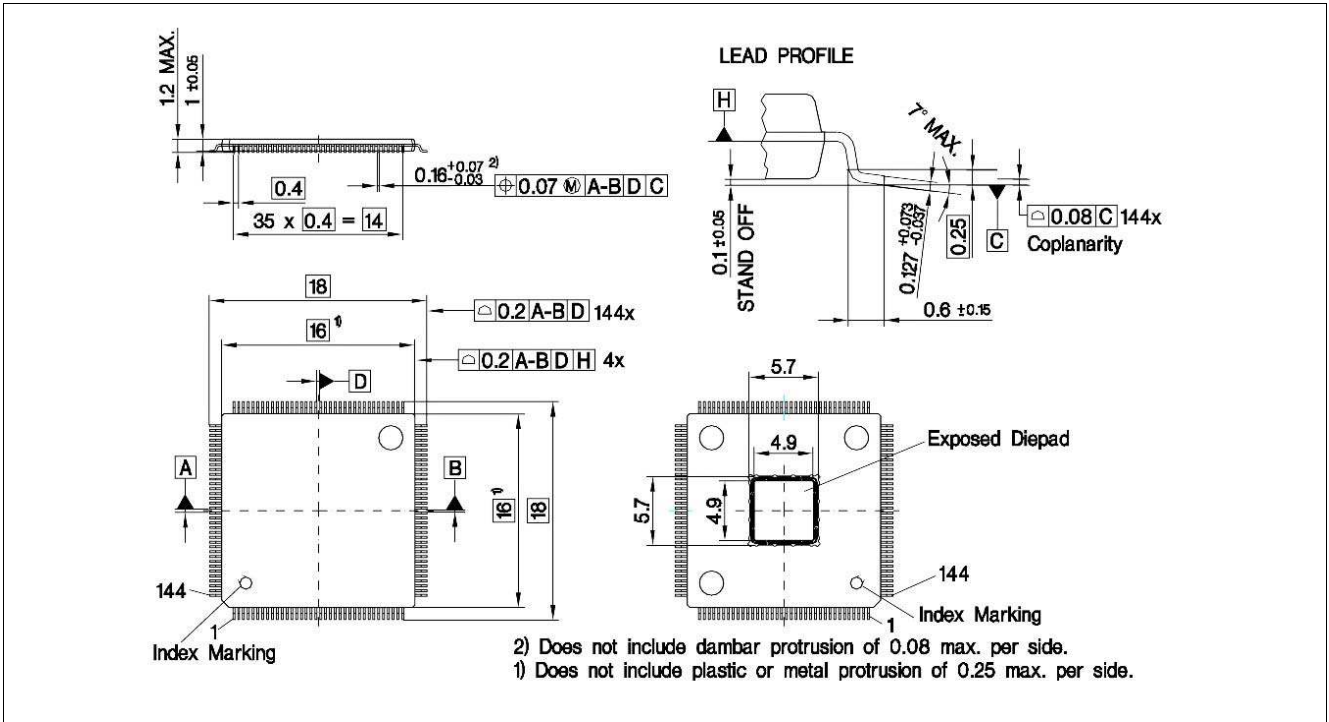


Figure 3-17 Package Outlines TQFP-144

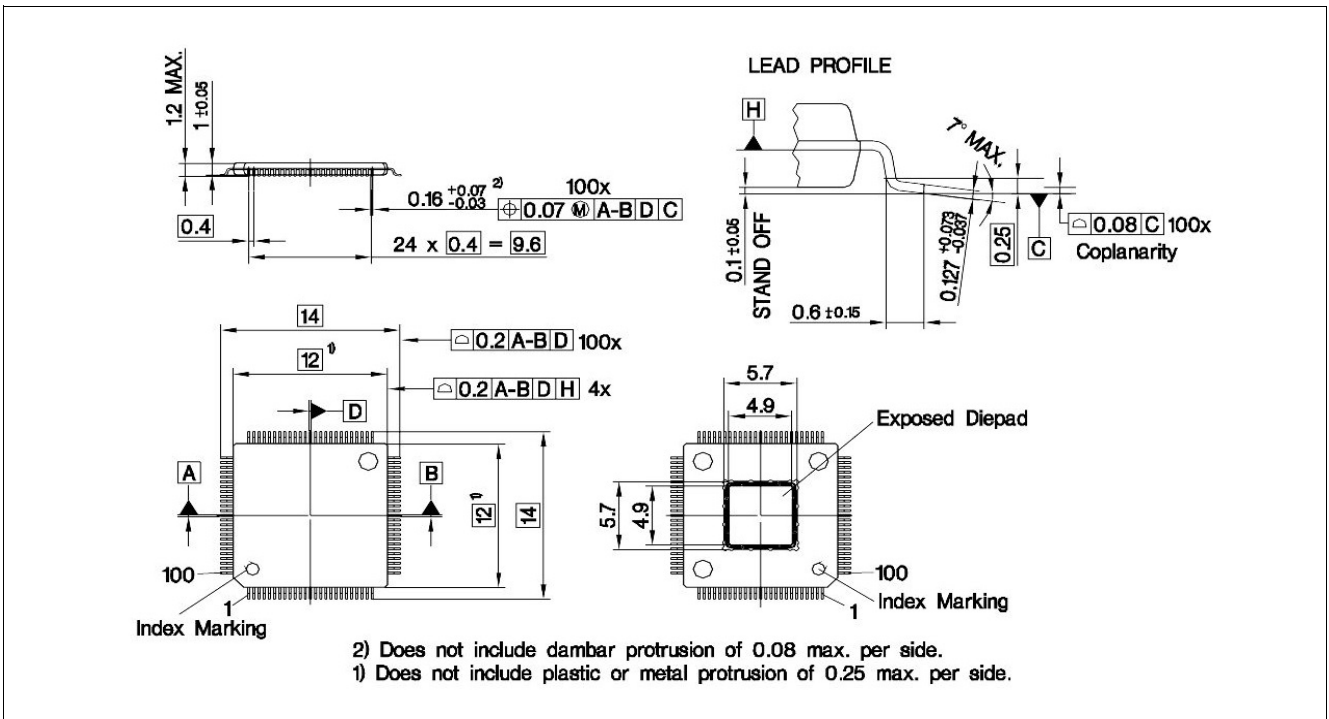


Figure 3-18 Package Outlines TQFP-100

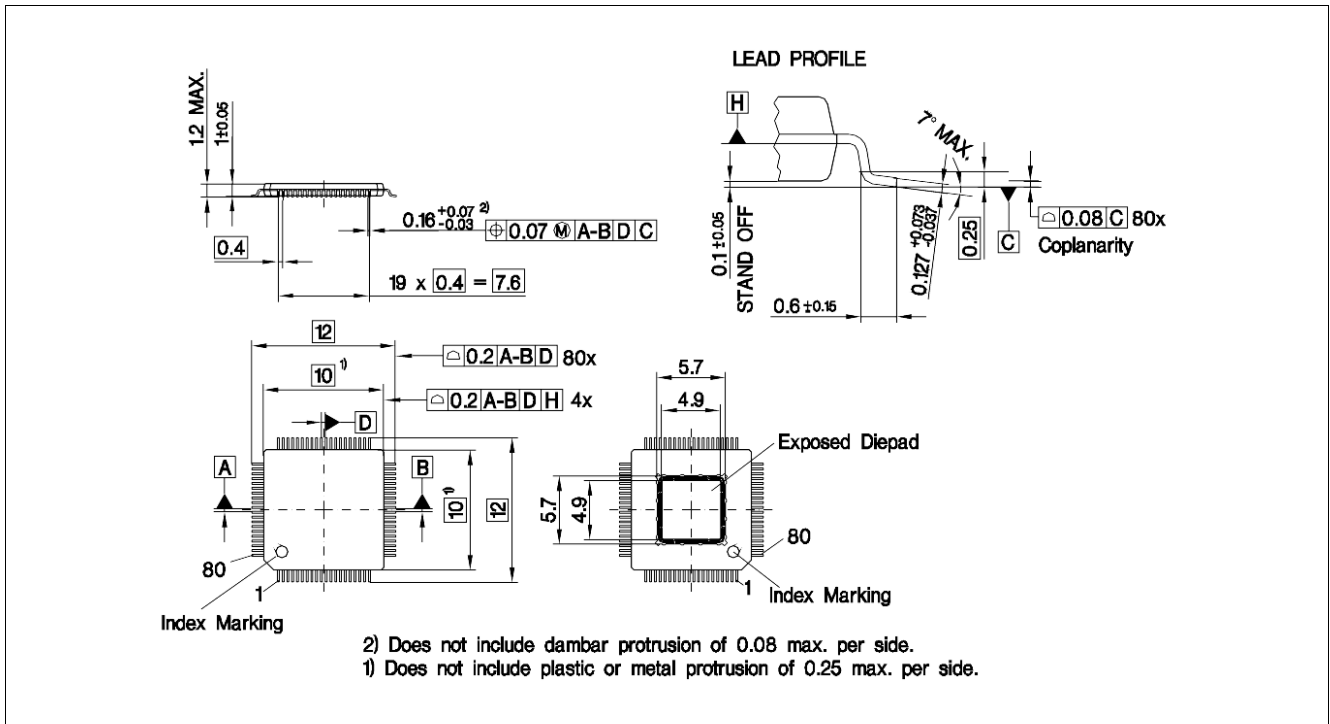


Figure 3-19 Package Outlines TQFP-80

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: <http://www.infineon.com/products>.

3.25.1 Package Parameters

Table 3-52 Package Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to ambient) ¹⁾	RTH_JA CC	-	-	23	K/W	LFBGA-292
		-	-	16	K/W	LFBGA180; Top Cooling
		-	-	14	K/W	LFBGA292; Top Cooling
		-	-	20	K/W	TQFP-100
		-	-	18	K/W	TQFP-144
		-	-	22	K/W	TQFP-80
Thermal resistance (junction to case bottom) ¹⁾	RTH_JCB CC	-	-	4.5	K/W	LFBGA-292
		-	-	2	K/W	TQFP-100
		-	-	2	K/W	TQFP-144
		-	-	2	K/W	TQFP-80

Table 3-52 Package Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance (junction to case top) ¹⁾	RTH_JCT CC	-	-	5	K/W	LFBGA-292
		-	-	10	K/W	TQFP-100
		-	-	10	K/W	TQFP-144
		-	-	10	K/W	TQFP-80

1) The top and bottom thermal resistances between the case and the ambient (RTH_CTA, RTH_CBA) are to be combined with the thermal resistances between the junction and the case given above (RTH_JCT, RTH_JCB), in order to calculate the total thermal resistance between the junction and the ambient (RTH_JA). The thermal resistances between the case and the ambient (RTH_CTA, RTH_CBA) depend on the external system (PCB, case) characteristics and are under user responsibility. The junction temperature can be calculated using the following equation: $T_J = T_A + RTH_JA * P_D$, where the RTH_JA is the total thermal resistance between the junction and the ambient.

Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

4 History

Version 0.4 is the first version of this document.

4.1 Changes from Version 0.4 to Version 0.6

Changes in chapter “Summary of Features”

- Changes in table “Platform Feature Overview” for feature values of SRAM, Data Flash, DMA, EVADC, and GTM

Changes in chapter “TC33x Pin Definition and Functions”

- Changes in sub-chapter “LFBGA-292 Package Variant Pin Configuration of TC33x for feature package LP”
 - Changes in “Port 22 Functions” table; added QSPI functions at P22.0
 - Changes in “Port 22 Functions” table; added QSPI and IOM functions at P22.1
 - Changes in “Port 22 Functions” table; added QSPI functions at P22.2
 - Changes in “Port 22 Functions” table; added QSPI functions at P22.3
 - Changes in table “Analog Inputs”, added functions at ball T9, Y9, T8, U8, W8, U7, Y8, W7
 - Changes in table “System I/O”, deleted functions at ball W17, Y17
 - Changes in table “Supply”, changed functions at ball N14, P13
- Changes in sub-chapter “LFBGA-292 Package Variant Pin Configuration of TC33x for feature package DA, DH, DT, DZ”
 - Changes in “Port 14 Functions” table; added CAN functions at P14.7
 - Changes in “Port 14 Functions” table; added CAN functions at P14.9
 - Changes in “Port 20 Functions” table; added CAN functions at P20.7
 - Changes in table “System I/O”, changed buffer type at ball L7, K7, P10, P11
- Changes in sub-chapter “LFBGA-180 Package Variant Pin Configuration of TC33x for feature package L and LP”
 - Changes in “Port 22 Functions” table; added QSPI functions at P22.0
 - Changes in “Port 22 Functions” table; added QSPI and IOM functions at P22.1
 - Changes in “Port 22 Functions” table; added QSPI functions at P22.2
 - Changes in “Port 22 Functions” table; added QSPI functions at P22.3
 - Changes in table “Analog Inputs”, added EVADC functions at ball N6, L5, M5, P5, N5, N3, M4, N4
 - Changes in table “System I/O”, deleted functions at ball N12, P12
 - Changes in table “Supply”, changed function at ball J8
- Changes in sub-chapter “LFBGA-180 Package Variant Pin Configuration of TC33x for feature package DA”
 - Changes in “Port 20 Functions” table; added CAN function at P20.7
 - Changes in table “Analog Inputs”, changed function at pin K3
 - Changes in table “Analog Inputs”, added function at pin J4
 - Changes in table “Supply”, deleted reserved functionality at pin J4
 - Changes in table “Supply”, added reserved functionality at pin L3
- Changes in sub-chapter “TQFP-144 Package Variant Pin Configuration of TC33x for feature package L and LP”
 - Changes in “Port 22 Functions” table; added QSPI functions at P22.0
 - Changes in “Port 22 Functions” table; added QSPI and IOM functions at P22.1

History Changes from Version 0.4 to Version 0.6

- Changes in “Port 22 Functions” table; added QSPI functions at P22.2
- Changes in “Port 22 Functions” table; added QSPI functions at P22.3
- Changes in “Port 34 Functions” table; changed pin number for P34.1
- Changes in “Port 34 Functions” table; changed pin number for P34.2
- Changes in “Port 34 Functions” table; deleted all functionality of P34.3
- Changes in table “Analog Inputs”, added functions at pins 47, 46, 45, 40, 39, 38, 37, 36
- Changes in table “System I/O”, deleted functionality at pin 70 and 71
- Changes in table “Supply”, added function at pin 53
- Changes in sub-chapter “TQFP-100 Package Variant Pin Configuration of TC33x for feature package L and LP”
 - Changes in table “Analog Inputs”, changed functions at pins 38, 37, 36, 35, 34, 33
 - Changes in table “Analog Inputs”, added function at pin 34, 33, 32, 29, 28, 27, 26, 25
 - Changes in table “System I/O”, deleted functionality at pin 48 and 49
 - Changes in table “Supply”, added function at pin 39
 - Changes in table “Supply”, changed function at pin 40, 31
 - Changes in table “Supply”, deleted function at pin 32
- Changes in sub-chapter “TQFP-80 Package Variant Pin Configuration of TC33x for feature package L and LP”
 - Changes in table “Analog Inputs”, deleted functions at pin 28
 - Changes in table “Analog Inputs”, added function at pins 27, 26, 23, 22, 21, 20
 - Changes in table “System I/O”, deleted functionality at pin 38 and 39
 - Changes in table “Supply”, changed function at pin 25, 29
 - Changes in table “Supply”, added function at pin 28
 - Changes in table “Supply”, deleted function at pin 26
- Changes in sub-chapter “Sequence of Pads in Pad Frame for feature package L and LP”
 - General changes in table “Pad List” concerning “X” and “Y” coordinates, numbers, pad names, pad types, and comments
- Changes in sub-chapter “Sequence of Pads in Pad Frame for feature package DA, DH, DT, and DZ”
 - General changes in table “Pad List” concerning “X” and “Y” coordinates, numbers, pad names, pad types, and comments
 - Added explanation following table “Pad List”
- Changes in sub-chapter “Legend”
 - Changed IO-Spirit versions

Changes in chapter “Electrical Specification”

- Changes in sub-chapter “Pin Reliability in Overload”
 - Changed table numbers in chapter description referring to Temperature Profile
 - Changed wording in test condition for parameter K_{OVAP}
- Changes in sub-chapter “5V/3.3V switchable Pads”
 - Changes in table Slow 5V GPIO for parameter I_{OZ} condition
 - Changes in table Slow 3.3V GPIO for parameter I_{OZ} condition
- Changes in table “LVDS - IEEE standard LVDS general purpose link (GPL)”
 - Changed value of parameter V_1
 - Changed test condition of parameter V_{idth}

History Changes from Version 0.6 to Version 0.7

- Added values and test condition of parameter V_{idth}
- Changed test condition of parameter R_{in}
- Added footnotes
- Changes in table “Current Consumption”
 - Changes in footnote 6)
- Changes in table “Reset”
 - Changed value of parameter t_{PIP}
 - Changed value of parameter t_{BWP}
- Changes in table “Supply Ramp”
 - Added conditions for values of table “Supply Ramp”
- Changes in table “EVR33 LDO”
 - Added values for parameter ΔV_{OUTTC}
- Changes in table “EVR13 SMPS”
 - Changed test condition of parameter V_{DDDC}
 - Changed value of parameter t_{STRDC}
- Changes in table “EVR13 SMPS External components”
 - Changed value of parameter C_{OUT}
- Changes in table “PLL System”
 - Changed value of parameter f_{REF}
- Changes in sub-chapter “ETH RGMII Parameters”
 - Added figure for “ETH RGMII TX Signal Timing (Delay on Destination (DoD))”
 - Added figure for “ETH RGMII RX Signal Timing (Delay on Source (DoS))”
- Changes in sub-chapter “SDMMC Interface Timing”
 - Added figure “SDMMC Timing”
- Changes in table “Flash”
 - Changed value of parameter t_{PRPB5_PF}
 - Changed value of parameter t_{ER_Dev}
- Changes in sub-chapter “Package Outline”
 - Changed figure numbering
- Changes in sub-chapter “Package Parameters”
 - Added values and notes of parameter RTH_JA in table “Package Parameters”

4.2 Changes from Version 0.6 to Version 0.7

General changes in Data Sheet TC33x: Data Sheet splitted and renamed to TC33x/TC32x for feature packages L, LP and TC33xAA for feature packages DA, DH, DT

- Added information for Data Sheet TC32x
- Changed Data Sheet version from 0.6 to version 0.7

Changes in chapter “Summary of Features”

- Changed number of CPUs
- Changed number of Scratch-Pad RAM (PSPR)

History Changes from Version 0.6 to Version 0.7

- Changed number of Scratch-Pad RAM (DSPR)
- Changed number of Data RAM (DLMU)
- Changed number of Channel DMA Controller with safe data transfer
- Changed number of ADC kernels
- Changed number of STM modules
- Same changes according in table “Platform Feature Overview”
- Deleted Debug features for “MCDS light“ and “AGBT” in table “Platform Feature Overview”
- Deleted “SDMMC“ and „Ethernet“ features in table “Platform Feature Overview”
- Deleted „Extension Memory“ in table “Platform Feature Overview”
- Deleted SPU, RIF, HSPDM modules in table “Platform Feature Overview”
- Changed description of CCU6 in table “Platform Feature Overview”
- Changed value for $T_{ambient}$ in table “Platform Feature Overview”

Changes in chapter “TC33x/TC32x Pin Definition and Functions”

- Changed package variant figure numbering in overview list
- Changes in LFBGA-292 Package Variant; Supply Table; VSS ball assignment N12, P12 to function “Digital Ground”
- Deleted sub-chapter LFBGA-292 for feature packages DA, DH, DT, and DZ
- Deleted sub-chapter LFBGA-180 for feature package DA
- Changes in TQFP-144 Package Variant; Supply Table; Pin 145 for VSS changed to Pin E-PAD for function “Digital Ground”
- Changes in TQFP-100 Package Variant; Port 14 Functions Table; Pin 101 added for P14.4
- Changes in TQFP-100 Package Variant; Analog Inputs Table; Pin 29 changed to Pin 28
- Changes in TQFP-100 Package Variant; Analog Inputs Table; Pin 28 changed to Pin 27
- Changes in TQFP-100 Package Variant; Analog Inputs Table; Pin 27 changed to Pin 26
- Changes in TQFP-100 Package Variant; Analog Input Table; former Pin 26 (AN10) assignments deleted
- Changes in TQFP-100 Package Variant; Supply Table; Pin 31 changed to Pin 30
- Changes in TQFP-100 Package Variant; Supply Table; Pin 30 changed to Pin 29
- Changes in TQFP-100 Package Variant; Supply Table; Pin 101 (VSS) changed to Pin E-PAD
- Changes in TQFP-100 Package Variant; Supply Table; Pin 31 added for VSSM
- Changes in TQFP-80 Package Variant; Port 14 Functions Table; Pin 81 added for P14.4
- Changes in TQFP-80 Package Variant; Analog Inputs Table; Pin 23 changed to Pin 22
- Changes in TQFP-80 Package Variant; Analog Inputs Table; Pin 22 changed to Pin 21
- Changes in TQFP-80 Package Variant; Analog Inputs Table; former Pin 21 (AN10) assignments deleted
- Changes in TQFP-80 Package Variant; Supply Table; Pin 25 changed to Pin 24
- Changes in TQFP-80 Package Variant; Supply Table; Pin 24 changed to Pin 23
- Changes in TQFP-80 Package Variant; Supply Table; Pin 81 (VSS) changed to Pin E-PAD
- Changes in TQFP-80 Package Variant; Supply Table; Pin 25 added for VSSM
- Changes in sub-chapter „Sequence of Pads in Pad Frame for feature package L and LP“; number 30 and 31, comment changed to Supply Voltage
- Changes in sub-chapter „Sequence of Pads in Pad Frame for feature package L and LP“; number 39, Pad Type changed to “FAST”

History Changes from Version 0.6 to Version 0.7

- Deleted sub-chapter „Sequence of Pads in Pad Frame for feature packages DA, DH, DT, and DZ“
- Deleted duplicate sentence in description of sub-chapter „Sequence of Pads in Pad Frame for feature package L and LP“
- Changes in sub-chapter “Legend”
- Changed referring IO_Spirit_file version for Datasheet TC33x/TC32x
- Deleted IO_Spirit_file version for Datasheet TC33xED version

Changes in chapter “Electrical Specification”

- Corrected wrong datasheet version number
- **Changes in table “Absolute Maximum Ratings”**
 - Changed wording for parameter ΣI_{IN}
 - Added footnote to parameter I_{IN} (Added footnote 5)
- **Changes in table “Overload Parameters”**
 - Changed spelling for parameter I_{INSA}
 - Deleted values for parameter K_{OVDN}
 - Deleted values for parameter K_{OVDP}
- **Changed datasheet version number in sub-chapter “Operating Conditions”**
 - Deleted parameter ADAS clock frequency in table “Operating Conditions”
- **Changes in table “Fast 5V GPIO”**
 - Deleted values for parameter I_{OZ}
- **Changes in table “Fast 3.3V GPIO”**
 - Deleted values for parameter I_{OZ}
 - Deleted values for parameter V_{ILH}
- **Changes in table “Slow 5V GPIO”**
 - Deleted values for parameter I_{OZ}
- **Changes in table “Slow 3.3V GPIO”**
 - Deleted values for parameter I_{OZ}
 - Deleted values for parameter V_{ILH}
- **Deleted table for “RFast 5V GPIO”**
- **Deleted table for “RFast 3.3V pad”**
- **Deleted driver settings in table “Driver Mode Selection for RFast Pads”**
- **Deleted sub-chapter “High performance LVDS Pads”**
- **Changes in table “VADC 5V”**
 - Deleted sentence regarding “Fast compare operations” in chapter “VADC Parameters”
 - Added value and test condition for parameter V_{AREF}
 - Corrected wrong spelling for parameter $\alpha_{VCS D}$
 - Added test condition for parameter R_{PDD} Changed figure for “Equivalent Circuitry for Analog Inputs”
 - Changed wording in footnote 7)
- **Changes in table “OSC_XTAL”**
 - Changed wording in footnote 1)
 - Changed spelling in footnote 2)
- **Changed and deleted wording in sub-chapter “Power Supply Current”**

- **Changes in table “Current Consumption“**
 - Changed values for parameter I_{DDRAIL} in table “Current Consumption“
 - Deleted values for parameter I_{DDRAIL} in table “Current Consumption“
 - Changed values for parameter $I_{DDPORST}$ in table “Current Consumption“
 - Deleted values for parameter $I_{DDPORST}$ in table “Current Consumption“
 - Changed value for parameter I_{EVRSB} in table “Current Consumption“
 - Changed values and test conditions for parameter I_{DDTOT} in table “Current Consumption“
 - Deleted values for parameter I_{DDTOT} in table “Current Consumption“
 - Changed value and test condition for parameter $I_{DDTOTDC3}$ in table “Current Consumption“
 - Changed value for parameter $I_{DDTOTDC5}$ in table “Current Consumption“
 - Deleted value for parameter $I_{DDTOTDC5}$ in table “Current Consumption“
 - Deleted values for parameter $I_{STANDBY}$ in table “Current Consumption“
 - Changed values for parameter P_D in table “Current Consumption“
 - Deleted values for parameter P_D in table “Current Consumption“
 - Changed test conditions wording for parameter $I_{EXTRAIL}$ in table “Current Consumptions“
 - Changed test conditions wording for parameter I_{DDM} in table “Current Consumptions“
 - Added footnote 1) to table “Current Consumption“
 - Changed footnote order for table “Current Consumption“
 - Changed footnote references for parameters in table “Current Consumption“
- **Changes in table “Module Current Consumption“**
 - Deleted values for parameter $I_{EXTLVDS}$ in table “Module Current Consumption“
 - Changed value for parameter I_{SCRSB} in table “Module Current Consumption“
 - Deleted footnote 3) for table “Module Current Consumption“
 - Changed footnote reference for parameters in table “Module Current Consumption“
- **Changes in table “Module Core Current Consumption“**
 - Changed value and test condition for parameter I_{DDGTM} in table “Module Core Current Consumption“
 - Added values for parameter I_{DDGTM} in table “Module Core Current Consumption“
 - Deleted value for parameter I_{DDGTM} in table “Module Core Current Consumption“
 - Deleted parameter I_{DDSPU1} in table “Module Core Current Consumption“
 - Deleted parameter I_{DDSPU2} in table “Module Core Current Consumption“
 - Deleted parameter $I_{DDSPULJ1}$ in table “Module Core Current Consumption“
 - Deleted parameter $I_{DDSPULJ2}$ in table “Module Core Current Consumption“
 - Deleted footnotes 2), 3) and 4)
 - Changed footnote number 5) to footnote number 2)
- **Changes in table “Reset“**
 - Changed and added values for parameter t_{PI} in table “Reset“
- **Changes in table “Supply Monitors“**
 - Added values to parameter V_{EXTMON} in table “Supply Monitors“
 - Changed test conditions of parameter V_{EXTMON} in table “Supply Monitors“
 - Changed explanation regarding power cycles for table “Supply Ramp“
- **Changes in table “EVR13 SMPS“**
 - Changed values for parameter I_{MAX} in table “EVR13 SMPS“

- Changed value for parameter n_{DC} in table “EVR13 SMPS”
- **Changes in sub-chapter “ASCLIN SPI Master Timing”**
 - Corrected wrong datasheet number in description
- **Changes in sub-chapter “QSPI Timings, Master and Slave Mode”**
 - Corrected wrong datasheet number in description
- **Deleted sub-chapter “Ethernet Interface (ETH) Characteristics”**
- **Deleted sub-chapter “Radar Interface Timing”**
- **Deleted sub-chapter “SDMMC Interface Timing”**
- **Deleted sub-chapter “Parameters Specific to the Emulation Part Only”**
- **Changes in table “Package Parameters”**
 - Added value for parameter RTH_JA in table “Package Parameters”
 - Added value for parameter RTH_JCB in table “Package Parameters”
 - Added value for parameter RTH_JCT in table “Package Parameters”

4.3 Changes from Version 0.7 to Version 1.0

General Change: Status of Datasheet TC33x/TC32x changed from “Target Datasheet/ Target Specification” and “Preliminary” status version 0.7 to “Datasheet” status version 1.0.

Changes in chapter “Summary of Features”

- Changed wording for „CPU”
- Changed wording for “GPT”

Changes in chapter “TC33x/TC32x Pin Definition and Functions”

- Added note for V_{FLEX} / V_{EXT} connection in sub-chapter “TQFP-144 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP”
- Added note for V_{FLEX} / V_{EXT} connection in sub-chapter “TQFP-100 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP”
- Added note for V_{FLEX} / V_{EXT} connection in sub-chapter “TQFP-80 Package Variant Pin Configuration of TC33x/TC32x for feature package L and LP”

Changes in chapter “Electrical Specification”

- Changes in sub-chapter “Absolute Maximum Ratings”
 - Changed value in footnote 5) in table “Absolute Maximum Ratings”
- Changes in sub-chapter “5V/ 3.3V switchable Pads”
 - Added tables for parameter Class S 5V and 3.3 V
- Changes in sub-chapter “Power Supply Current”
 - Added equations and description to paragraph “Calculating the 1.3 V Current Consumption”
 - Changed wording of condition “ $V_{EXT / EVRSB}$ ” for power patterns
 - Deleted symbol of parameter “ $I_{EXTRAIL}$ ” in table “Current Consumption”
 - Changed value of parameter “ $I_{DDTOTDC3}$ ” in table “Current Consumption”
 - Changed value of parameter “ $I_{DDTOTDC5}$ ” in table “Current Consumption”
- Changes in sub-chapter “EVR”

History Changes from Version 1.0 to Version 1.1

- Changed value of parameter “ C_{OUT} ” in table “EVR33 LDO”
- Changed value of parameter “ n_{DC} ” in table “EVR13 SMPS”

4.4 Changes from Version 1.0 to Version 1.1

- **Changes in chapter “Summary of Features”**
 - Changed wording for “DFLASH”
 - Added description for “AEC-Q100”
 - Added description for “ISO 26262 Safety Element”
 - Added description for Data Flash in table “Platform Feature Overview”
 - Added details for parameter GTM/ DTM modules in table “Platform Feature Overview”
 -
- **Changes in chapter “TC33x/TC32x Pin Definition and Functions”**
 - Changed note for sub-chapter “TQFP-144 Package Variant Pin Configuration”
 - Changed note for sub-chapter “TQFP-100 Package Variant Pin Configuration”
 - Changed note for sub-chapter “TQFP-80 Package Variant Pin Configuration”
 - Added note for sub-chapter “TQFP-80 Package Variant Pin Configuration”
 -
- **Changes in chapter “Electrical Specification”**
 - Changed note for parameter t_{TX_ASYM} in table “Fast 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
 - Changed note for parameter t_{TX_ASYM} in table “Fast 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
 - Changed note for parameter t_{TX_ASYM} in table “Slow 5V GPIO” of sub-chapter “5V/3.3V switchable Pads”
 - Changed note for parameter t_{TX_ASYM} in table “Slow 3.3V GPIO” of sub-chapter “5V/3.3V switchable Pads”
 - Changed footnote 3) and 6) of table “VADC 5V” in sub-chapter “VADC Parameters”
 - Added details to parameter $I_{EXTRAIL}$ in table “Current Consumption” for sub-chapter “Power Supply Current”
 - Changed footnote 3) for table “Current Consumption” in sub-chapter “Power Supply Current”
 - Added footnote 8) to table “Current Consumption” in sub-chapter “Power Supply Current”
 - Changed title and figures for sub-chapter “Calculating the 1.25 V Current Consumption”
 - Changed equation figures for sub-chapter “Calculating the 1.25 V Current Consumption”
 - Added sentence to sub-chapter “Supply Ramp-up and Ramp-down Behavior”
 - Changed notes for parameter V_{EXTMON} in table “Supply Monitors” for sub-chapter “EVR”
 - Changed notes for parameter $V_{DDP3MON}$ in table “Supply Monitors” for sub-chapter “EVR”
 - Changed notes for parameter V_{DDMON} in table “Supply Monitors” for sub-chapter “EVR”
 - Changed note for parameter t_{MON} in table “Supply Monitors” for sub-chapter “EVR”
 - Deleted value and note for parameter t_{52} in table “Master Mode Timing, LVDS output pads for data and clock” in sub-chapter “QSPI Timings, Master and Slave Mode”

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