July 2008

FDW9926A

Dual N-Channel 2.5V Specified PowerTrench® MOSFET

General Description

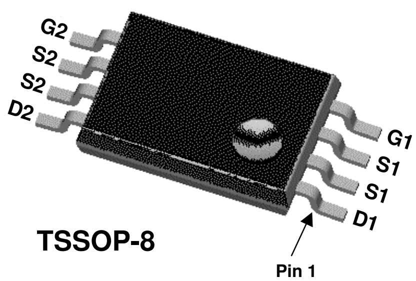
This N-Channel 2.5V specified MOSFET is a rugged gate version of Fairchild's Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 10V).

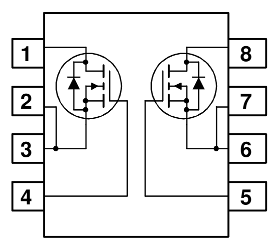
Applications

- Battery protection
- Load switch
- Power management

Features

- 4.5 A, 20 V. $R_{DS(ON)}$ = 32 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 45 mΩ @ V_{GS} = 2.5 V
- Optimized for use in battery circuit applications
- Extended V_{GSS} range (±10V) for battery applications
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low profile TSSOP-8 package





Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Drain Current – Continuous	(Note 1a)	4.5	A
	– Pulsed		30	
P_D	Total Power Dissipation	(Note 1a)	1.0	W
		(Note 1b)	0.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	125	°C/W
		(Note 1b)	208	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
9926A	FDW9926A	13''	12mm	2500 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±12 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	0.6	1.0	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		–3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 4.5 A V_{GS} = 2.5 V, I_D = 3.8 A V_{GS} = 4.5 V, I_D = 4.5A, T_J=125°C		24 34 33	32 45 48	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 4.5 A		19		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		630		pF
C_{oss}	Output Capacitance			150		pF
C_{rss}	Reverse Transfer Capacitance			85		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		1.4		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		8	16	ns
t_r	Turn–On Rise Time			8	16	ns
$t_{d(off)}$	Turn–Off Delay Time			15	26	ns
t_f	Turn–Off Fall Time			4	8	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 4.5 A, V_{GS} = 4.5 V		6.1	9	nC
Q_{gs}	Gate–Source Charge			1.1		nC
Q_{gd}	Gate–Drain Charge			1.8		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				0.83	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.83 A (Note 2)		0.69	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 4.5 A, d_{iF}/d_t = 100 A/µs		14		nS
Q_{rr}	Diode Reverse Recovery Charge			4		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $R_{\theta JA}$ is 125°C/W (steady state) when mounted on a 1 inch² copper pad on FR-4.

b) $R_{\theta JA}$ is 208 °C/W (steady state) when mounted on a minimum copper pad on FR-4.

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

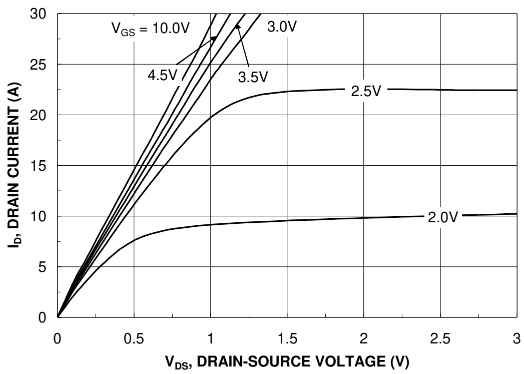


Figure 1. On-Region Characteristics.

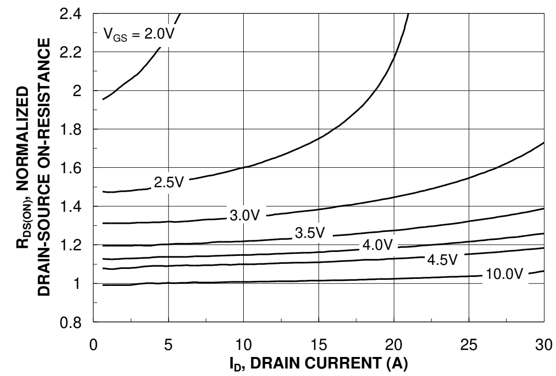


Figure 2. On-Resistance Variation with Drain Current and Gate voltage.

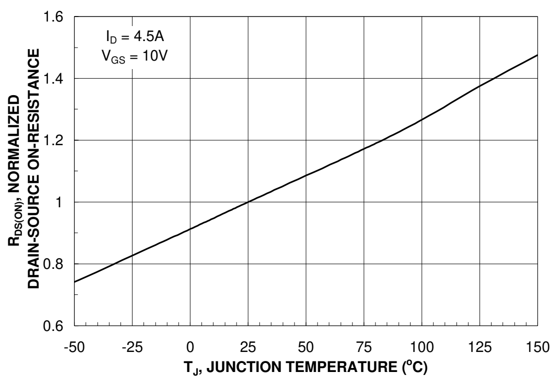


Figure 3. On-Resistance Variation with temperature.

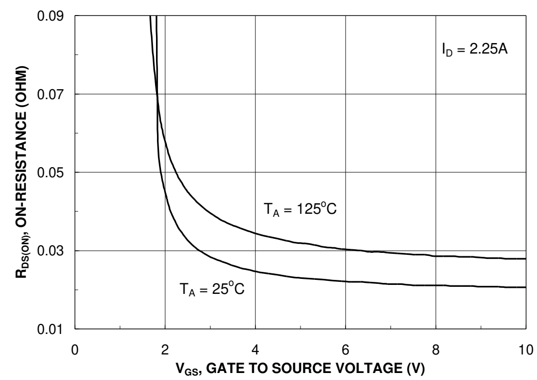


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

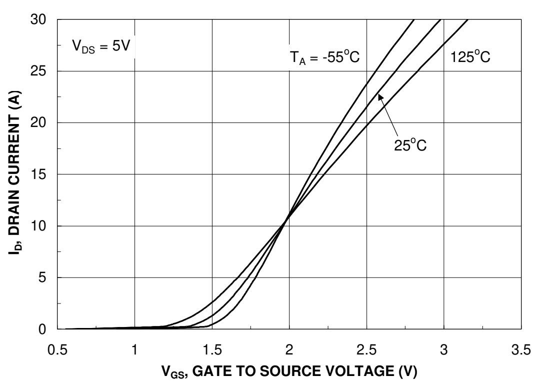


Figure 5. Transfer Characteristics.

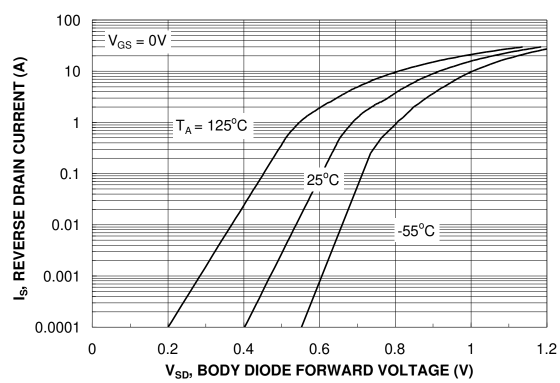


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

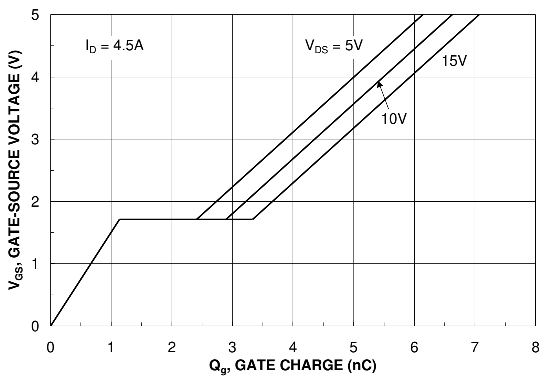


Figure 7. Gate Charge Characteristics.

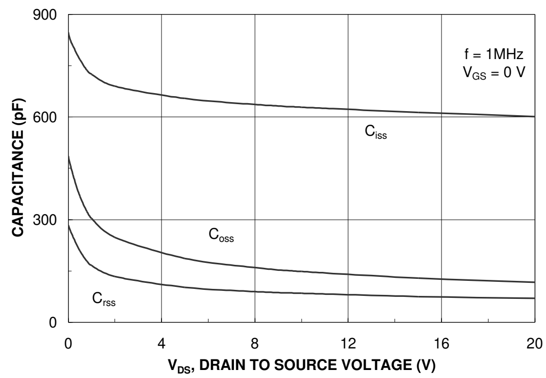


Figure 8. Capacitance Characteristics.

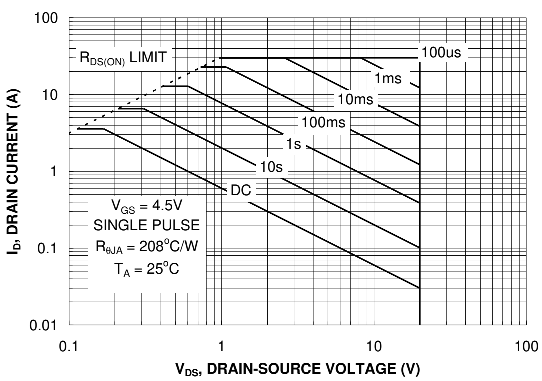


Figure 9. Maximum Safe Operating Area.

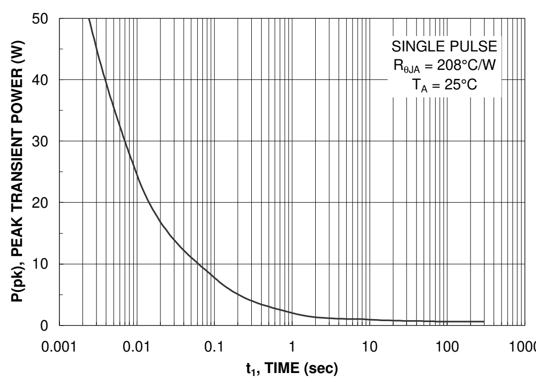


Figure 10. Single Pulse Maximum Power Dissipation.

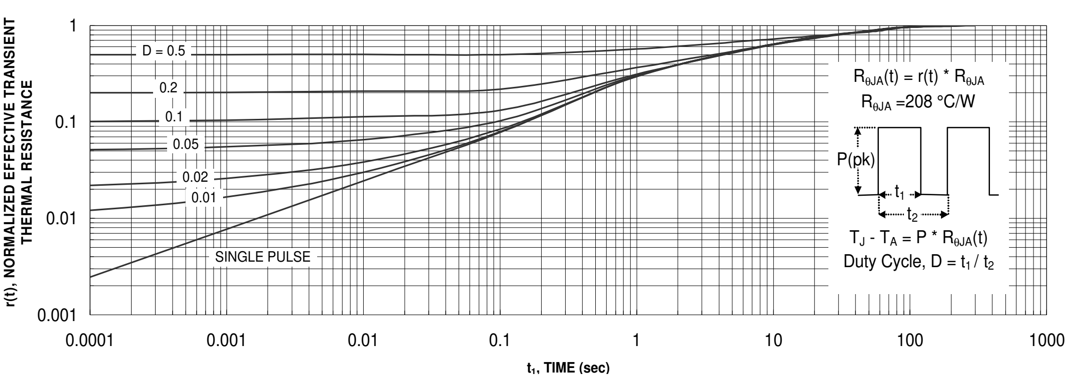


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

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Rev. I35