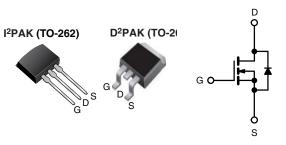


HALOGEN

Power MOSFET



N-Channel MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	800				
R _{DS(on)} (Ω)	V _{GS} = 10 V 3.0				
Q _g max. (nC)	78				
Q _{gs} (nC)	9.6				
Q _{gd} (nC)	45				
Configuration	Single				

FEATURES

- Dynamic dV/dt rating
- · Repetitive avalanche rated
- · Fast switching
- · Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

ORDERING INFORMATION			
Package	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHFBE30S-GE3	SiHFBE30STRL-GE3 ^a	SiHFBE30L-GE3
Lead (Pb)-free	IRFBE30SPbF	IRFBE30STRLPbF ^a	IRFBE30LPbF

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)						
PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	800		
Gate-Source Voltage			V_{GS}	± 20	V	
Continuous Drain Current	V _{GS} at 10 V	T _C = 25 °C	1	4.1		
Continuous Drain Current	V _{GS} at 10 V	T _C = 100 °C	I _D	2.6	Α	
Pulsed Drain Current ^a			I _{DM}	16		
Linear Derating Factor				1.0	W/°C	
Single Pulse Avalanche Energy ^b			E _{AS}	260	mJ	
Avalanche Current ^a			I _{AR}	4.1	А	
Repetitive Avalanche Energy ^a			E _{AR}	13	mJ	
Maximum Power Dissipation	T _C =	25 °C	P_{D}	125	W	
Peak Diode Recovery dV/dt ^c			dV/dt	2.0	V/ns	
Operating Junction and Storage Temperature Range			T _J , T _{stg}	-55 to +150	°C	
Soldering Recommendations (Peak temperature) ^d	for	10 s		300	7	
Mauring Tayous	6.00 0*1	M2 a a wayy		10	lbf ⋅ in	
Mounting Torque	6-32 or M3 screw			1.1	N⋅m	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. V_{DD} = 50 V, starting T_J = 25 °C, L = 29 mH, R_g = 25 Ω , I_{AS} = 4.1 A (see fig. 12)
- c. $I_{SD} \le 4.1 \text{ A}$, $dI/dt \le 100 \text{ A/}\mu\text{s}$, $V_{DD} \le 600 \text{ V}$, $T_J \le 150 \text{ °C}$
- d. 1.6 mm from case

Document Number: 91119



IRFBE30S, SiHFBE30S, IRFBE30L, SiHFBE30L

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THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R _{thJA}	-	-	62		
Case-to-Sink, Flat, Greased Surface	R _{thCS}	-	0.50	-	°C/W	
Maximum Junction-to-Case (Drain)	R _{thJC}	-	-	1.0		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
PARAMETER	SYMBOL	TES	TEST CONDITIONS		TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} :	= 0 V, I _D = 250 μA	800	-	-	V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	Reference	ce to 25 °C, I _D = 1 mA	-	0.90	-	V/°C	
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.0	-	4.0	V	
Gate-Source Leakage	I _{GSS}		V _{GS} = ± 20 V	-	-	± 100	nA	
Zara Cata Valtaga Drain Current		V _{DS} =	= 800 V, V _{GS} = 0 V	-	-	100		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 640 \	/, V _{GS} = 0 V, T _J = 125 °C	-	-	500	μA	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.5 A ^b	-	-	3.0	Ω	
Forward Transconductance	9 _{fs}	V _{DS} =	= 100 V, I _D = 2.5 A	2.5	-	-	S	
Dynamic								
Input Capacitance	C _{iss}		$V_{GS} = 0 V$,	-	1300	-		
Output Capacitance	C _{oss}		$V_{DS} = 25 V$,	-	310	-	pF	
Reverse Transfer Capacitance	C _{rss}	f = 1	.0 MHz, see fig. 5	-	190	-		
Total Gate Charge	Qg			-	-	78		
Gate-Source Charge	Q _{gs}	V _{GS} = 10 V	$V_{GS} = 10 \text{ V}$ $I_D = 4.1 \text{ A}, V_{DS} = 400 \text{ V},$ see fig. 6 and 13 b		-	9.6	nC	
Gate-Drain Charge	Q _{gd}		See fig. 6 dila 16	-	-	45	1	
Turn-On Delay Time	t _{d(on)}			-	12	-		
Rise Time	t _r	$V_{DD} = 400 \text{ V}, I_D = 4.1 \text{ A}, \\ R_g = 12 \ \Omega, R_D = 95 \ \Omega, \text{ see fig. } 10^{\text{ b}}$		-	33	-	ns	
Turn-Off Delay Time	t _{d(off)}			-	82	-		
Fall Time	t _f	1	1		30	-		
Gate Input Resistance	R_g	f = 1 MHz, open drain		0.6	-	1.6	Ω	
Internal Drain Inductance	L _D	Between lead 6 mm (0.25")	from	-	4.5	-	-11	
Internal Source Inductance	L _S	die contact	package and center of die contact		7.5	-	nH	
Drain-Source Body Diode Characteristic	es							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	4.1		
Pulsed Diode Forward Current ^a	I _{SM}			-	-	16	A	
Body Diode Voltage	V _{SD}	T _J = 25 °C	I_{S} , I_{S} = 4.1 A, V_{GS} = 0 V b	-	-	1.8	V	
Body Diode Reverse Recovery Time	t _{rr}	T 05 °C 1	4.1.A. dl/d+ 100.A./h	-	480	720	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	$I_{\rm J}=25^{\circ}\rm C, I_{\rm F}$	= 4.1 A, dl/dt = 100 A/µs b	-	1.8	2.7	nC	
Forward Turn-On Time	t _{on}	Intrinsic tu	ırn-on time is negligible (turn	on is dor	ninated b	y L _S and	L _D)	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width \leq 300 µs; duty cycle \leq 2 %

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

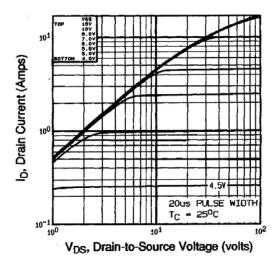


Fig. 1 - Typical Output Characteristics, T_C = 25 °C

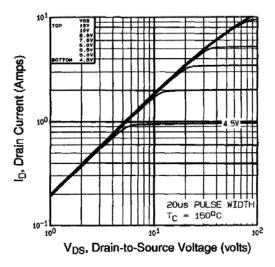


Fig. 2 - Typical Output Characteristics, $T_C = 150$ °C

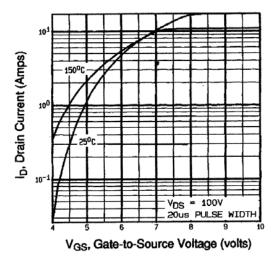


Fig. 3 - Typical Transfer Characteristics

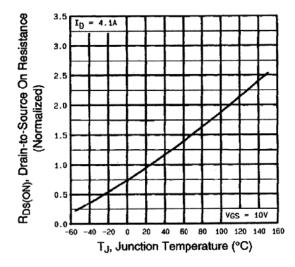


Fig. 4 - Normalized On-Resistance vs. Temperature



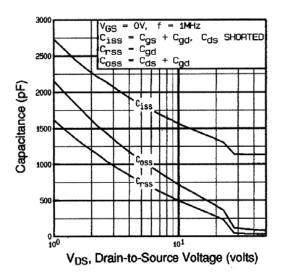


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

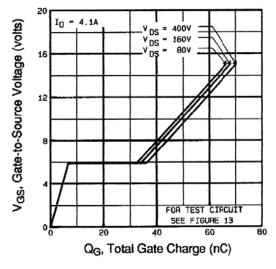


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

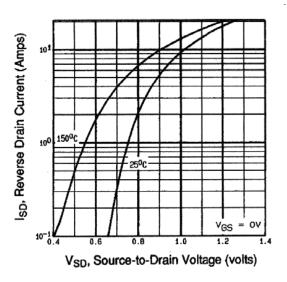


Fig. 7 - Typical Source-Drain Diode Forward Voltage

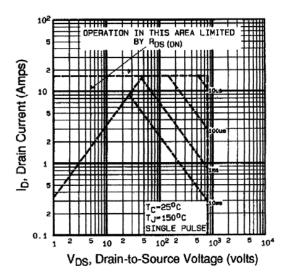


Fig. 8 - Maximum Safe Operating Area

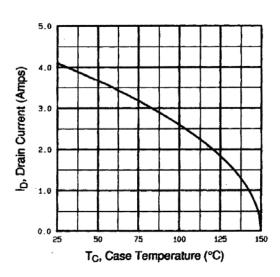


Fig. 9 - Maximum Drain Current vs. Case Temperature

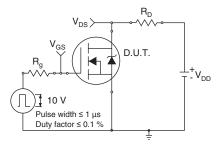


Fig. 10a - Switching Time Test Circuit

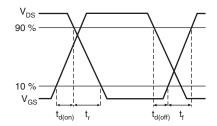


Fig. 10b - Switching Time Waveforms

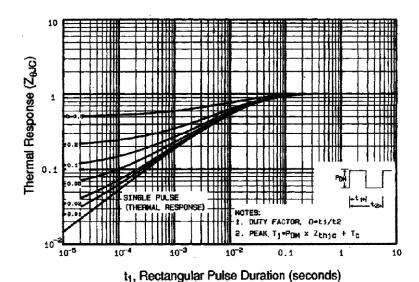


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

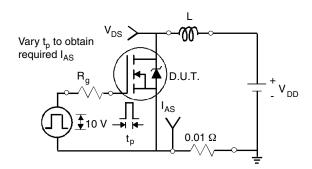


Fig. 12a - Unclamped Inductive Test Circuit

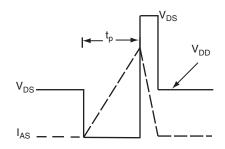


Fig. 12b - Unclamped Inductive Waveforms

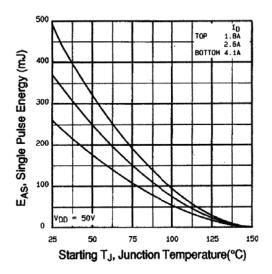


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

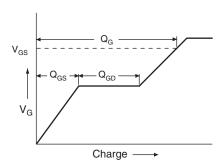


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

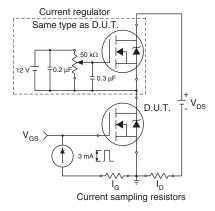
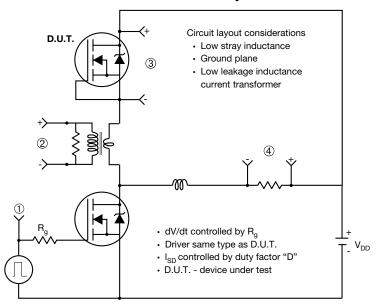


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



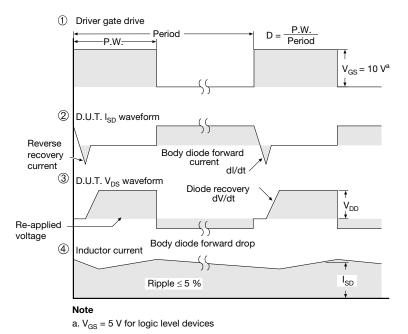


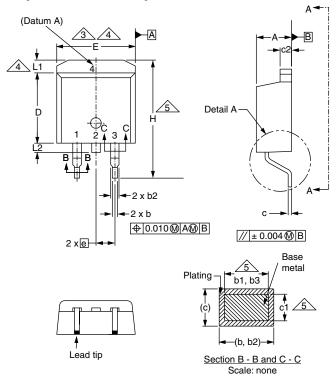
Fig. 14 - For N-Channel

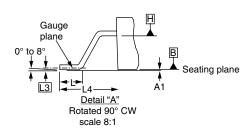
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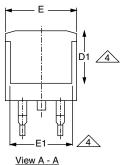




TO-263AB (HIGH VOLTAGE)







	D1 4
E1	4

	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
С	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

DIM. MIN. MAX. MIN. MAX. D1 6.86 - 0.270 - E 9.65 10.67 0.380 0.420 E1 6.22 - 0.245 - e 2.54 BSC 0.100 BSC H 14.61 15.88 0.575 0.625 L 1.78 2.79 0.070 0.110 L1 - 1.65 - 0.066 L2 - 1.78 - 0.070 L3 0.25 BSC 0.010 BSC		MILLIN	MILLIMETERS		HES
E 9.65 10.67 0.380 0.420 E1 6.22 - 0.245 - e 2.54 BSC 0.100 BSC H 14.61 15.88 0.575 0.625 L 1.78 2.79 0.070 0.110 L1 - 1.65 - 0.066 L2 - 1.78 - 0.070	DIM.	MIN.	MAX.	MIN.	MAX.
E1 6.22 - 0.245 - e 2.54 BSC 0.100 BSC H 14.61 15.88 0.575 0.625 L 1.78 2.79 0.070 0.110 L1 - 1.65 - 0.066 L2 - 1.78 - 0.070	D1	6.86	-	0.270	-
e 2.54 BSC 0.100 BSC H 14.61 15.88 0.575 0.625 L 1.78 2.79 0.070 0.110 L1 - 1.65 - 0.066 L2 - 1.78 - 0.070	E	9.65	10.67	0.380	0.420
H 14.61 15.88 0.575 0.625 L 1.78 2.79 0.070 0.110 L1 - 1.65 - 0.066 L2 - 1.78 - 0.070	E1	6.22	-	0.245	i
L 1.78 2.79 0.070 0.110 L1 - 1.65 - 0.066 L2 - 1.78 - 0.070	е	2.54 BSC		0.100	BSC
L1 - 1.65 - 0.066 L2 - 1.78 - 0.070	Н	14.61	15.88	0.575	0.625
L2 - 1.78 - 0.070	L	1.78	2.79	0.070	0.110
	L1	-	1.65	-	0.066
L3 0.25 BSC 0.010 BSC	L2	-	1.78	-	0.070
	L3	0.25	BSC	0.010	BSC
L4 4.78 5.28 0.188 0.208	L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08

DWG: 5970

Notes

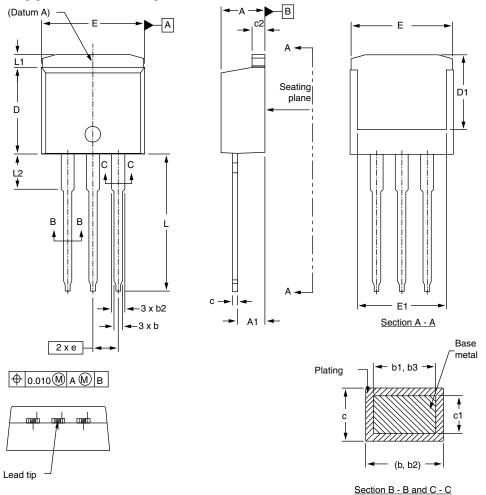
- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimensions are shown in millimeters (inches).
- 3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
- 4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
- 5. Dimension b1 and c1 apply to base metal only.
- 6. Datum A and B to be determined at datum plane H.
- 7. Outline conforms to JEDEC outline to TO-263AB.

Document Number: 91364 www.vishay.com Revision: 15-Sep-08





I²PAK (TO-262) (HIGH VOLTAGE)



	MILLIN	MILLIMETERS		HES
DIM.	MIN.	MAX.	MIN.	MAX.
Α	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
С	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

	MILLIN	METERS	INC	HES	
DIM.	MIN.	MAX.	MIN.	MAX.	
D	8.38	9.65	0.330	0.380	
D1	6.86	-	0.270	-	
Е	9.65	10.67	0.380	0.420	
E1	6.22	-	0.245	-	
е	2.54	BSC	0.100 BSC		
L	13.46	14.10	0.530	0.555	
L1	-	1.65	-	0.065	
L2	3.56	3.71	0.140	0.146	

Scale: None

ECN: S-82442-Rev. A, 27-Oct-08 DWG: 5977

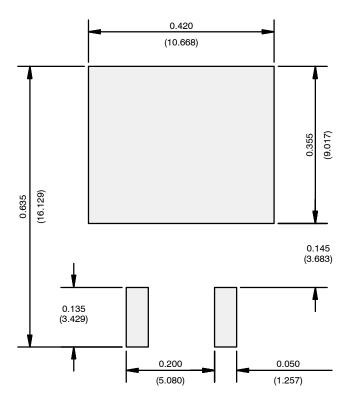
DVVG. 55

- 1. Dimensioning and tolerancing per ASME Y14.5M-1994.
- 2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
- 3. Thermal pad contour optional within dimension E, L1, D1, and E1.
- 4. Dimension b1 and c1 apply to base metal only.





RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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