

## **ADS8402/ADS8406/ADS8412 EVM User's Guide**

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This user's guide describes the characteristics, operation, and use of the ADS8402/ADS8406/ADS8412 16-bit, high-speed, parallel interface, analog-to-digital converter evaluation board. A complete circuit description, schematic diagram, and bill of materials are included.

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## 1 EVM Overview

### 1.1 Features

- Full-featured evaluation board for the ADS8402 (1.25 MHz), ADS8406 (1.25 MHz), and ADS8412 (2 MHz) high-speed 16-bit, single channel, parallel interface SAR-type analog-to-digital converters.
- Onboard Signal Conditioning
- Onboard Reference
- Input and Output Digital Buffers
- Onboard Decoding for Stacking Multiple EVMs

## 2 Analog Interface

The ADS8402/ADS8406/ADS8412EVM analog-to-digital converter has pseudo-bipolar differential input. A pseudo-bipolar differential input is a differential signal (inverting and noninverting input is 180 degrees out of phase) that is level shifted such that the signals levels are always equal to or above zero volts. The peak-to-peak amplitude on each input pin can be as large as the reference voltage. See the respective product data sheet for more information.

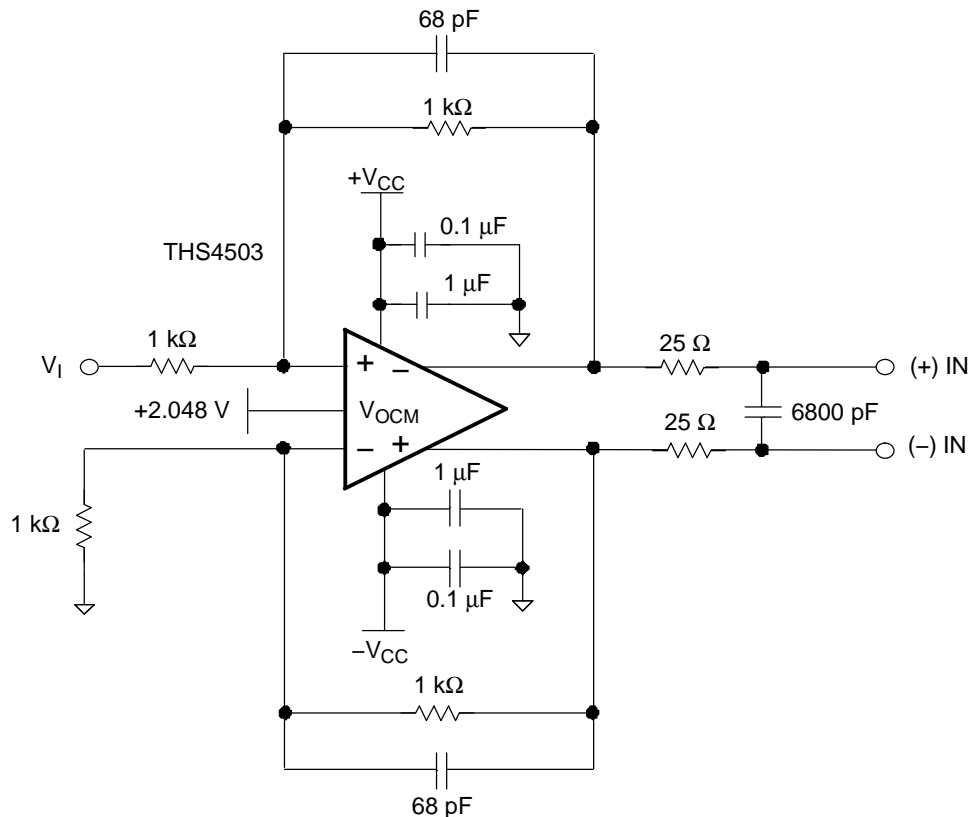
The ADS8402/ADS8406/ADS8412EVM comes installed with the unity gain buffer (U2) wired for single-ended into differential-out configuration. The common-mode voltage is derived from REF3040 reference IC and adjustable using a potentiometer (R9). The common mode voltage pin of the THS4503 is set to 2.0 V on the evaluation module. A single-ended input signal can be applied at pin-connector P1 or via SMA connectors J2 (noninverting input). The buffer circuit can be reconfigured for a differential input by installing resistor R6 and R8 and removing R1. The inverting leg of the differential signal should be applied to either connector P1 pin 1 or SMA connector J4 (inverting input). See [Table 1](#) for pinout of analog connector, P1. See [Section 8](#) for the EVM schematic.

**Table 1. Analog Input Connector**

Description	Signal Name	Connector.pin#		Signal Name	Description
Inverting Input	(-)	P1.1	P1.2	(+)	Noninverting Input
Reserved	N/A	P1.3	P1.4	N/A	Reserved
Reserved	N/A	P1.5	P1.6	N/A	Reserved
Reserved	N/A	P1.7	P1.8	N/A	Reserved
Pin tied to Ground	AGND	P1.9	P1.10	N/A	Reserved
Pin tied to Ground	AGND	P1.11	P1.12	N/A	Reserved
Reserved	N/A	P1.13	P1.14	N/A	Reserved
Pin tied to Ground	AGND	P1.15	P1.16	N/A	Reserved
Pin tied to Ground	AGND	P1.17	P1.18	N/A	Reserved
Reserved	N/A	P1.19	P1.20	REF+	External Reference Input

## 2.1 Signal Conditioning

It is recommended that the analog input to any SAR-type converter be buffered. The amplifier circuit in [Figure 1](#) is the buffer circuit used on the ADS8402/ADS8406/ADS8412EVM. This circuit consists of the THS4503, a high-speed fully differential amplifier configured as a single-ended into differential-out, unity gain buffer. The circuit shown in [Figure 1](#) was optimized to achieve the ac (i.e., SNR, THD, SFDR, etc) specifications listed in the ADS8402, ADS8406, and ADS8412 data sheets. The 68-pF and 6800-pF capacitors in the signal path are polypropylene type, manufactured by WIMA Corporation. Polypropylene capacitors cause the least distortion of the input signal; therefore, they provide good dynamic performance from the converter. A low-cost alternative for the polypropylene type are C0G capacitors by TDK Corporation.



**Figure 1. Input Buffer Circuit**

## 2.2 Reference

The EVM allows users to select from three reference sources. The ADS8402/ADS8406/ADS8412EVM provides an onboard 4.096-V reference, U3. The EVM also has the provision for users to supply a reference voltage via connector P1 pin 20. The user reference voltage and onboard reference voltages can be filtered by installing amplifier U1. The ADS8402, ADS8406, and ADS8412 analog-to-digital converters have a integrated onboard reference buffer; therefore, it is not necessary to buffer the voltage externally. The reference buffer circuit on the EVM is not populated with an amplifier for this reason. The EVM comes installed with on-chip internal reference tied directly to the reference pin of the converter. See [Section 8](#) for a full schematic.

**Table 2. Solder Short Jumper Setting<sup>(1)</sup>**

Reference Designator	Description	Jumper Settings	
		1-2	2-3
SJP2	On-chip internal reference applied to A/D reference pin	Installed <sup>(2)</sup>	
	Apply reference voltage from external source		Installed
SJP3	Apply voltage to amplifier, U2, common-mode voltage pin	Installed <sup>(2)</sup>	N/A
SJP4	Buffer onboard reference, REF3040	Installed	Not installed
	Buffer user reference voltage applied at P1 pin 20	Not installed	installed
SJP5	Select REF3040 for reference voltage	Installed	Not installed
	Select buffered reference voltage	Not Installed	Installed

(1) Designator SJP1 is not used on the EVM.

(2) Factory installed

## 3 Digital Interface

The ADS8402/ADS8406/ADS8412 EVM is designed for easy interfacing to multiple platforms. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient dual-row header/socket combination at P2 and P3. Consult Samtec at [www.samtec.com](http://www.samtec.com) or 1-800-SAMTEC-9 for a variety of mating connector options.

**Table 3. Pinout for Parallel Control Connector P2<sup>(1)</sup>**

Connector.Pin	Signal	Description
P2.1	DC_CS	Daughtercard board-select pin
P2.3		
P2.5		
P2.7	A0	Address line from processor
P2.9	A1	Address line from processor
P2.11	A2	Address line from processor
P2.13		
P2.15		
P2.17		
P2.19	INTc	Set jumper to select BUSY or inverted signal to be applied to this pin.

(1) All even numbered pins of P2 are tied to DGND.

Read ( $\overline{RD}$ ), conversion start ( $\overline{CONVST}$ ) and reset ( $\overline{RESET}$ ) signals to the converter can be assigned to two different addresses in memory via jumper settings. This allows for the stacking of up to two ADS8402EVM, ADS8406EVM, and/or ADS8412EVMs into processor memory. See [Table 4](#) for jumper settings. Note that the evaluation module does not allow the chip select ( $\overline{CS}$ ) line of the converter to be assigned to different memory locations. It is therefore suggested that the  $\overline{CS}$  line be grounded or wired to an appropriate signal of the processor.

**Table 4. Jumper Settings for Decoder Outputs**

Reference Designator	Description	Jumper Settings	
		1-2	2-3
W2	Set A[2..0]= 0x1 to generate $\overline{RD}$ pulse	Installed <sup>(1)</sup>	
	Set A[2..0]=0x2 to generate $\overline{RD}$ pulse		Installed
W5	Set A[2..0]=0x3 to generate $\overline{convst}$ pulse	Installed <sup>(1)</sup>	
	Set A[2..0]=0x4 to generate $\overline{convst}$ pulse		Installed
W4	Set A[2..0]=0x5 to generate $\overline{RESET}$ pulse	Installed <sup>(1)</sup>	
	Set A[2..0]=0x6 to generate $\overline{RESET}$ pulse		Installed

The data bus is available at connector P3; see [Table 5](#) for pinout information.

(1) Factory Installed

**Table 5. Data Bus Connector P3<sup>(1)</sup>**

Connector.Pin	Signal	Description
P3.1	D0	Buffered Data Bit 0 (LSB)
P3.3	D1	Buffered Data Bit 1
P3.5	D2	Buffered Data Bit 2
P3.7	D3	Buffered Data Bit 3
P3.9	D4	Buffered Data Bit 4
P3.11	D5	Buffered Data Bit 5
P3.13	D6	Buffered Data Bit 6
P3.15	D7	Buffered Data Bit 7
P3.17	D8	Buffered Data Bit 8
P3.19	D9	Buffered Data Bit 9
P3.21	D10	Buffered Data Bit 10
P3.23	D11	Buffered Data Bit 11
P3.25	D12	Buffered Data Bit 12
P3.27	D13	Buffered Data Bit 13
P3.29	D14	Buffered Data Bit 14
P3.31	D15	Buffered Data Bit 15

This evaluation module provides direct access to all the analog-to-digital converter control signals via connector J3; see [Table 6](#).

(1) All even-numbered pins of P3 are tied to DGND.

**Table 6. Pinout for Converter Control Connector J3<sup>(1)</sup>**

Connector.Pin	Signal	Description
J3.1	$\overline{CS}$	Chip Select pin. Active Low
J3.3	$\overline{RD}$	Read Pin. Active Low
J3.5	$\overline{CONVST}$	Convert start pin. Active Low
J3.7	BYTE	BYTE mode pin. Used for 8-bit buses
J3.9	$\overline{RESET}$	Reset pin. Active Low
J3.11	BUSY <sup>(2)</sup>	Converter Status Output. High when a conversion is in progress

(1) All even-numbered pins of J3 are tied to DGND.

(2) Error on silkscreen of Rev A evaluation module. J3 pin 11 reads BUS16/18. The signal connected is BUSY, as shown in [Section 8](#).

## 4 Power Supplies

The EVM accepts four power supplies.

- A dual  $\pm V_s$  dc supply for the dual supply operational amplifiers. Maximum voltage recommended is  $\pm 7$  VDC
- A single 5-V dc supply for analog section of the board (A/D + Reference).
- A single 5-V or 3.3-V dc supply for digital section of the board (A/D + address decoder + buffers).

There are two ways to provide these voltages.

1. Wire in voltages at test points on the EVM. See [Table 7](#)

**Table 7. Power Supply Test Points**

Test Point	Signal	Description
TP14	+BVDD	Apply 3.3 VDC or 5 VDC. See ADC data sheet for full range.
TP11	+AVCC	Apply 5 VDC
TP12	+VA	Apply 7 VDC. Positive supply for amplifier
TP13	-VA	Apply -7 VDC. Negative supply for amplifier

2. Use the power connector J1, and derive the voltages elsewhere. The pinout for this connector is shown in [Table 8](#). If using this connector, then set W1 jumper to connect 3.3 VD or 5 VD from the connector to +BVDD. Short between pins 1-2 to select 5 VD, or short between pins 2-3 to select 3.3 VD as the source for the digital buffer voltage supply (+BVDD).

**Table 8. Power Connector, J1, Pinout**

Signal	Power Connector - J1		Signal
+VA (7 V)	1	2	-VA (-7V)
5 VA	3	4	N/C
DGND	5	6	AGND
N/C	7	8	N/C
3.3 VD	9	10	5 VD

## 5 Using the EVM

The ADS8402/ADS8406/ADS8412 EVM serves three functions

1. As a reference design
2. As a prototype board and
3. As software test platform

### 5.1 As a Reference Board

As a reference design, the ADS8402/ ADS8406/ADS8412EVM contains the essential circuitry to showcase the analog-to-digital converter. This essential circuitry includes the input amplifier, reference circuit, and buffers. The EVM analog input circuit is optimized for 100-kHz sine wave; therefore, users may need to adjust the resistor and capacitor values of the A/D input circuit. In ac-type applications where signal distortion is concern, polypropylene capacitors should be used in the signal path.

### 5.2 As a Prototype Board

As a prototype board, the buffer circuit consists of resistor pads for configuring the input as either single-ended or differential input. The input circuit can be modified to accommodate user prototype needs, whether it be evaluating another differential amplifier or limiting noise for best performance. The analog, power, and digital connectors can be made to plug into a standard 0.1-inch breadboard or cables made up to interface direct to a FPGA or processor.

### 5.3 As a Software Test Platform

As a software test platform, connectors P1, P2, and P3 plug into the parallel interface connectors of the 5-6K interface card. The 5-6K interface card sits on the TMS320C5000™ and TMS320C6000™ DSP Platform starter kit (DSK). The ADS8402/ADS8406/ADS8412EVM is then mapped into the processor's memory space. This card also provides an area for signal conditioning. This area can be used to install application circuit(s) for digitization by the ADS8402/ADS8406/ADS8412 analog-to-digital converter. See the 5-6K interface card user's guide ( [SLAU104](#) ) for more information.

The ADS8402/ADS8406/ADS8412EVM provides a simple platform for interfacing to the converter. The EVM provides standard 0.1-inch headers and sockets to wire into prototype boards. The user need only provide 3 address lines (A2, A1, A0) and address valid line (DC\_  $\overline{CS}$ ) to connector P2. To choose which address combinations generates  $\overline{RD}$ ,  $\overline{CONVST}$ , and  $\overline{RESET}$ , set jumpers as shown in [Table 5](#). Recall that the chip select ( $\overline{CS}$ ) signal is not memory mapped or tied to P2; therefore, it must be controlled via a general-purpose pin or shorted to ground at J3 pin 1. If address decoding is not required, the EVM provides direct access to converter data bus via P3 and control via J3.

## 6 ADS8402/ADS8406/ADS8412EVM BOM

Table 9 contains a complete bill of materials for the ADS8402/ ADS8406/ADS8412 EVM. The schematic diagram is also provided for reference. Contact the Product Information Center or e-mail [dataconvapps@list.ti.com](mailto:dataconvapps@list.ti.com) for questions regarding this EVM.

**Table 9. Bill of Materials**

Used	Part Type	Designator	Footprint	MFG	MFG's Part Number	Description
2	0	R15 R21	805	Panasonic - ECG or Alternate	ERJ-6GEY0R00V	Resistor 0.0 $\Omega$ 1/8W 5% 0805 SMD
2	24.9	R12 R13	805	Panasonic - ECG or Alternate	ERJ-6ENF24R9V	Resistor 24.9 $\Omega$ 1/10W 1% 0805 SMD
3	100	R5 R14 R25	805	Panasonic - ECG or Alternate	ERJ-6ENF1000V	Resistor 100 $\Omega$ 1/10W 1% 0805 SMD
1	910	R4	805	Panasonic - ECG or Alternate	ERJ-6GEYJ911V	Resistor 910 $\Omega$ 1/8W 5% 0805 SMD
3	1k	R1 R7 R10	805	Panasonic - ECG or Alternate	ERJ-6ENF1001V	Resistor 1.00 k $\Omega$ 1/10W 1% 0805 SMD
5	10k	R16 R17 R18 R19 R20	603	Panasonic - ECG or Alternate	ERJ-3EKF1002V	Resistor 10.0 k $\Omega$ 1/16W 1% 0603 SMD
1	10k	R24	805	Panasonic - ECG or Alternate	ERJ-6ENF1002V	Resistor 10.0 k $\Omega$ 1/10W 1% 0805 SMD
6	NI	R6 R8 R11 R2 R3 R22	805	Not Installed	Not Installed	
1	49.9	R23	805	Panasonic - ECG or Alternate	ERJ-6ENF49R9V	Resistor 49.9 $\Omega$ 1/10W 1% 0805 SMD
4	1 nF	C3 C5 C11 C23	1206	TDK Corporation or Alternate	C3216C0G1H102JT	Capacitor 1000 pF 50V ceramic NPO 1206
2	68 pF	C34 C35	TH	WIMA	FKP2 68/100/1	68 pF Polypropylene capacitor
1	6800 pF	C17	TH	WIMA	FKP2 6800/100/1	6800 pF Polypropylene capacitor
10	0.01 $\mu$ F	C13 C21 C41 C44 C46 C48 C53 C56 C65 C50	603	TDK Corporation or Alternate	C1608X7R1H103JT	Capacitor 10000 pF 50V ceramic X7R 0603
4	0.01 $\mu$ F	C10 C18 C20 C66	805	TDK Corporation or Alternate	C2012X7R1H103KT	Capacitor 10000 pF 50V ceramic X7R 0805
2	0.01 $\mu$ F	C4 C26	1206	TDK Corporation or Alternate	C3216X7R1H103JT	Capacitor 10000 pF 50V ceramic X7R 1206
15	0.1 $\mu$ F	C8 C25 C40 C42 C43 C47 C51 C52 C54 C55 C57 C58 C62 C63 C64	603	TDK Corporation or Alternate	C1608X7R1E104KT	Capacitor 0.1 $\mu$ F 25V ceramic X7R 0603
7	0.1 $\mu$ F	C7 C9 C15 C22 C32 C36 C45	805	TDK Corporation or Alternate	C2012X7R1H104JT	Capacitor 0.10 $\mu$ F 50V ceramic X7R 0805
6	1 $\mu$ F	C16 C31 C33 C37 C59 C60	805	TDK Corporation or Alternate	C2012X7R1C105KT	Capacitor 1 $\mu$ F 16V ceramic X7R 0805
2	1 $\mu$ F	C2 C28	1206	TDK Corporation or Alternate	C3216X7R1E105KT	Capacitor 1.0 $\mu$ F 25V ceramic X7R 1206
4	10 $\mu$ F	C1 C6 C12 C19	1206	TDK Corporation or Alternate	C3216X5R1C106MT	Capacitor 10 $\mu$ F 16V ceramic X5R 1206
1	10 $\mu$ F	C49	3528	Kemet or Alternate	T491B106K016AS	Capacitor tantalum 10 $\mu$ F 16V 10% SMT
4	10 $\mu$ F	C14 C24 C27 C29	6032	Panasonic - ECG or Alternate	ECS-T1EC106R	Capacitor 10 $\mu$ F 25V tantalum TE SMD
1	22 $\mu$ F	C30	805	TDK Corporation or Alternate	C2012X5R0J226MT	Capacitor CER 22 $\mu$ F 6.3V X5R 20%
3	NI	C38 C39 C61	805			
2	1K	RP1 RP3	CTS_742	CTS Corporation	742C163102JTR	Resistor array 1 k $\Omega$ 16TERM 8RES SMD



**Table 9. Bill of Materials (continued)**

Used	Part Type	Designator	Footprint	MFG	MFG's Part Number	Description
1	100	RP2	CTS_742	CTS Corporation	742C163101JTR	Resistor array 100 Ω 16TRM 8RES SMD
1	10k	R9	BOURNS_32X4W	Bourns	3214W-1-103E	Trimpot 10 kΩ 4 mm Top ADJ SMD
4	BLM21AJ601SN1L	L1 L2 L3 L4	1206	TDK Corporation	MPZ2012S601AT	Chip ferrite beads - 600 Ω at 100 MHz
2	REF3040	U1 U3	3-SOT-23	Texas Instruments	REF3040AIDBZT	REF3040 50 ppm/°C, 50 μA in SOT23-3 CMOS voltage reference
1	THS4503	U2	8-SOP(D)	Texas Instruments	THS4503ID	High-speed fully-differential amplifiers
1	ADS8402	U4	SOCKET_48QFP	Texas Instruments	ADS8402IPFBT <sup>(1)</sup>	ADS8402 16-bit 1.25 MSPS
1	OPA627AU	U8	8-SOP(D)	NOT INSTALLED	NOT INSTALLED	Amplifier
1	NI	U9	8-SOP(D)			Footprint for 8 pin SOIC reference that operates from 5 V
1	SN74AHC1G04DBV	U10	5-SOT(DBV)	Texas Instruments	SN74AHC1G04DBVR	Single inverter gate
1	SN74AHC138PWR	U11	16-TSSOP(PW)	Texas Instruments	SN74AHC138PWR	3-line to 8-line decoder / demultiplexer
3	SN74AHC245PWR	U5 U6 U7	20-TSSOP(PW)	Texas Instruments	SN74AHC245PWR	Octal bus transceiver, 3-state
1	5X2X.1	J1	5X2X.1_SMT_SOCKET	Samtec	TSM-105-01-T-D-V-P	0.025" SMT plug - top side of PWB
1	6X2X.1	J3	6X2X.1_SMT_PLUG_&_SOCKET	Samtec	SSW-106-22-S-D-VS	0.025" SMT socket - bottom side of PWB
				Samtec	TSM-106-01-T-D-V-P	0.025" SMT plug - top side of PWB
2	SMA_PCB_MT	J2 J4	SMA_JACK	AMPHENOL	901-144-4	MaCom #5002-5003-10 / Amphenol #901-144
2	10X2X.1	P1 P2	10X2X.1_SMT_PLUG_&_SOCKET	Samtec	SSW-110-22-S-D-VS	0.025" SMT socket - bottom side of PWB
				Samtec	TSM-110-01-T-D-V-P	0.025" SMT plug - top side of PWB
1	16X2X.1_SMT_PLUG_&_SOCKET	P3	16X2X.1_SMT_PLUG_&_SOCKET	Samtec	SSW-116-22-S-D-VS	0.025" SMT socket - bottom side of PWB
				Samtec	TSM-116-01-T-D-V-P	0.025" SMT plug - top side of PWB
1	SJP2	SJP3	SJP2	NOT INSTALLED	NOT INSTALLED	Pad 2 position Jumper
3	SJP3	SJP2 SJP4 SJP5	SJP3	NOT INSTALLED	NOT INSTALLED	Pad 3 Position Jumper
1	SW-PB	S1	EVQ-PJ	Panasonic	EVQ-PJU04K	Switch
5	3POS_JUMPER	W1 W2 W3 W4 W5	3pos_jump	Samtec	TSW-103-07-L-S	3 Position Jumper _0.1" spacing
14	TP_0.025	TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14	test_point2	Keystone Electronics	5000K-ND	Test Point - Single 0.025" Pin

(1) On ADS8412EVM, the ADS8412IPFBT is installed instead of ADS8402IPFBT. On ADS8406EVM, the ADS8406IPFBT is installed instead of ADS8402IPFBT.

## 7 ADS8402/ADS8406/ADS8412EVM Layouts

This section contains the EVM layouts.

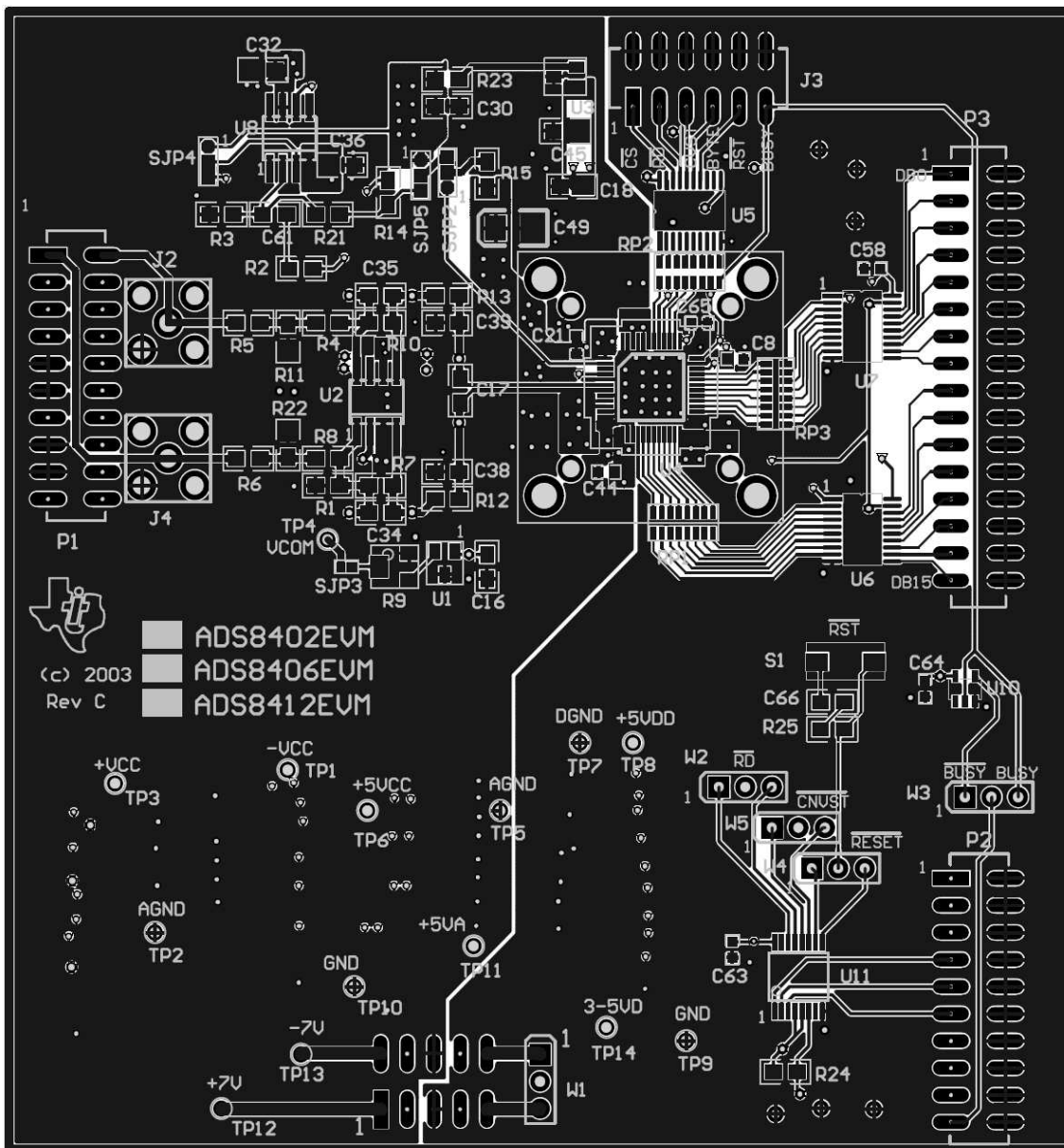


Figure 2. Top - Layer 1

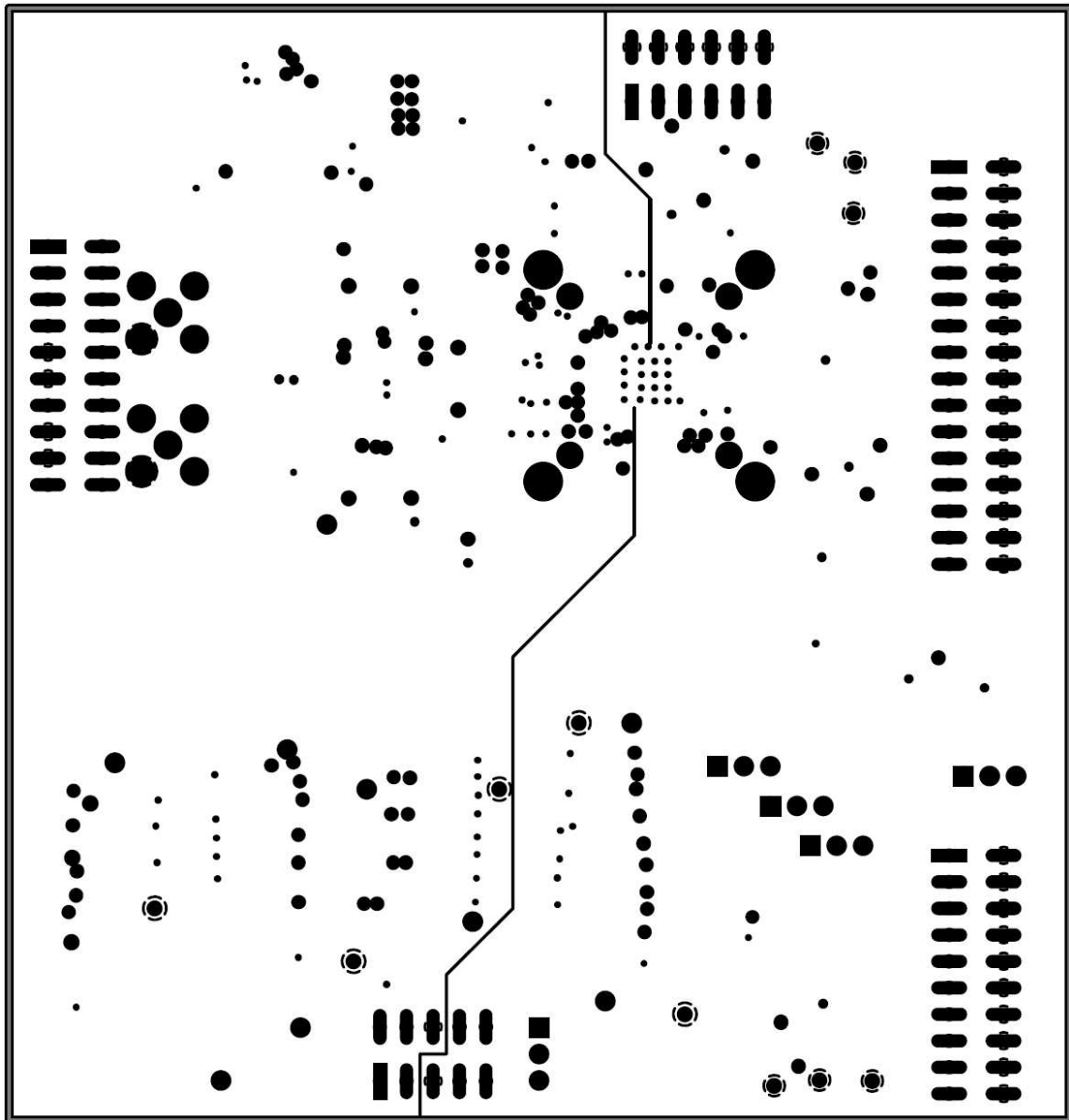


Figure 3. Ground Plane - Layer 2

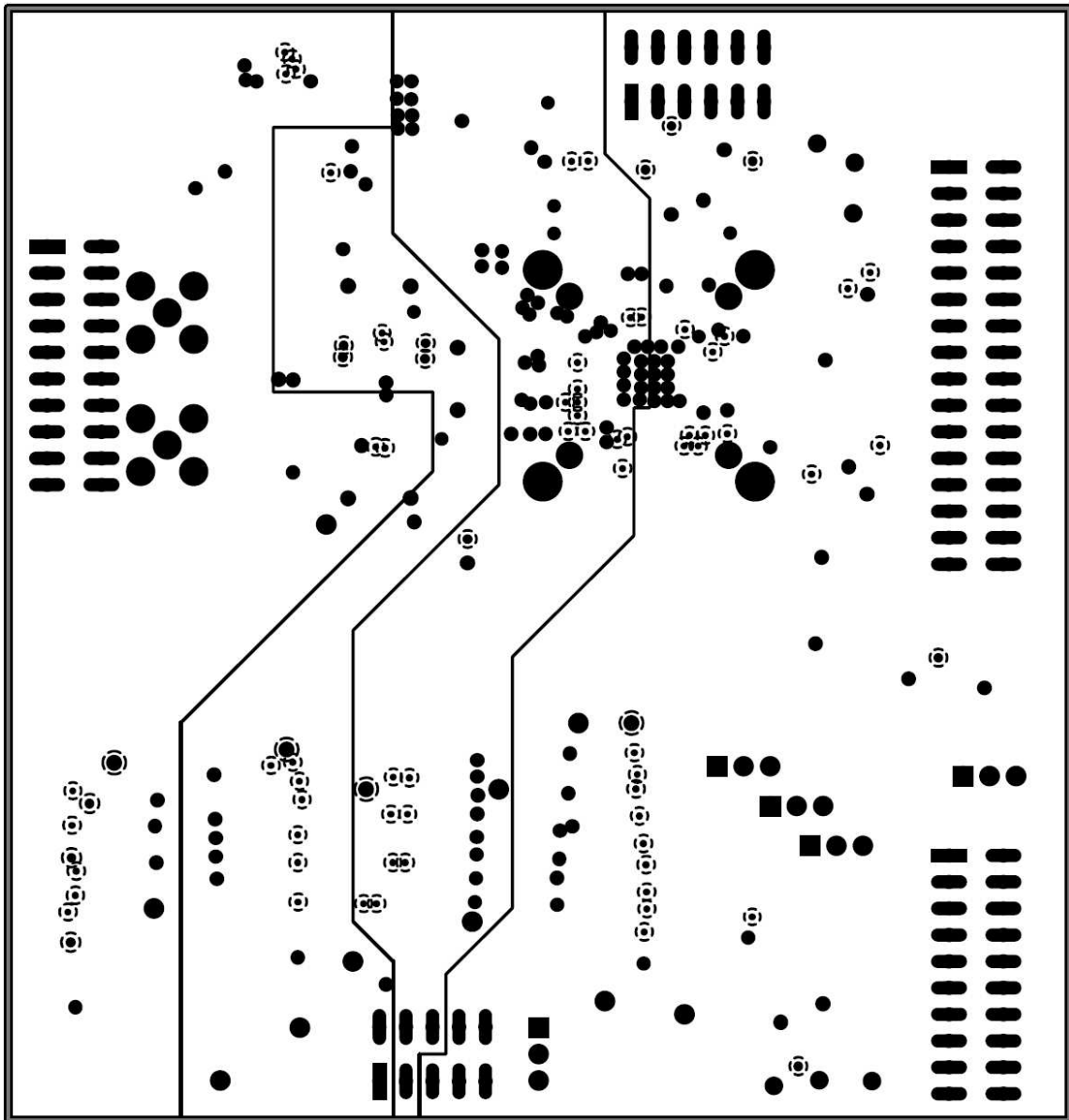


Figure 4. Power Plane - Layer 3

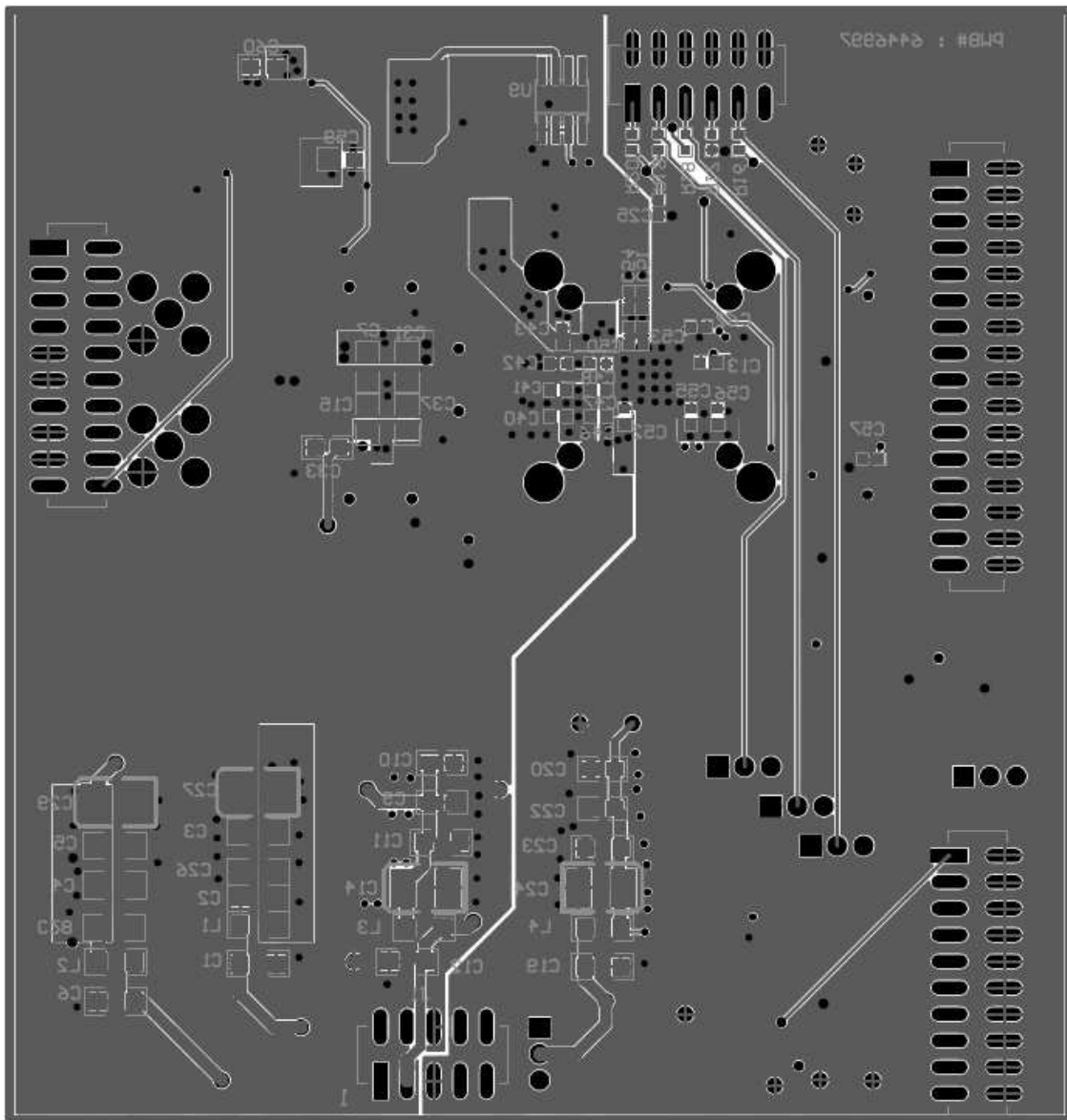
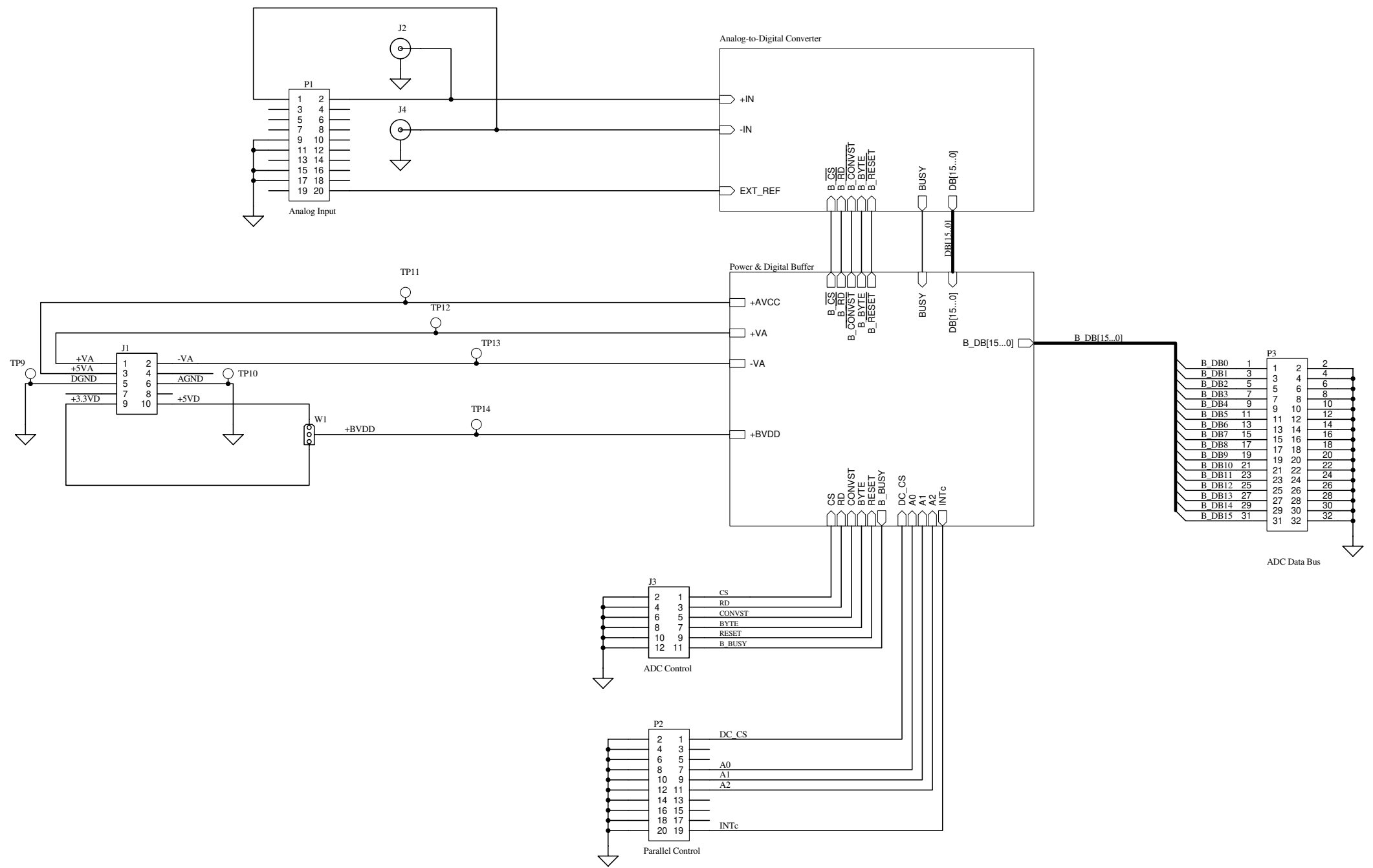


Figure 5. Bottom - Layer 4

## 8 ADS8402/ADS8406/ADS8412EVM Schematic

The schematic is located on the following pages.

Revision History		
REV	ECN Number	Approved



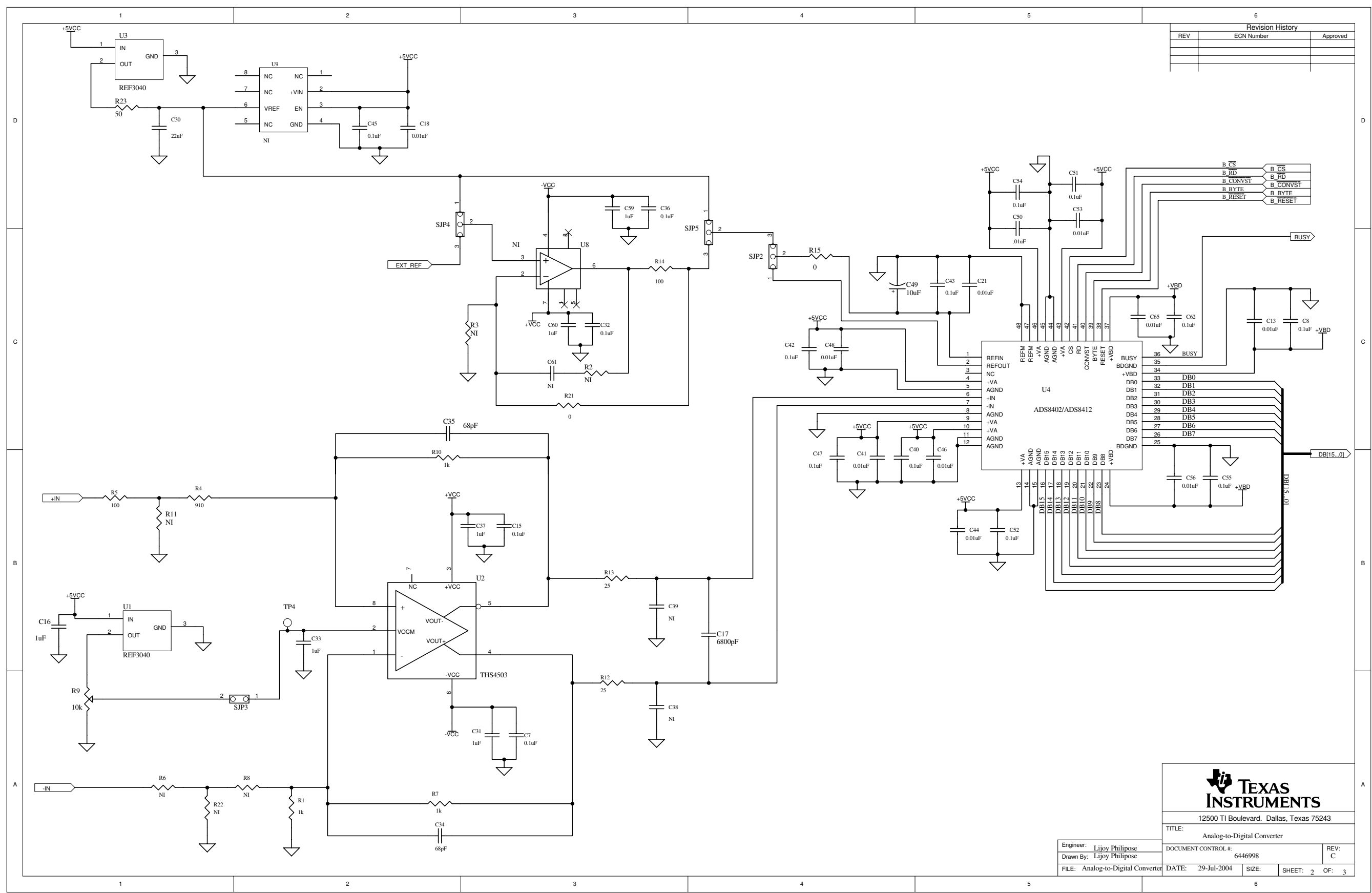
**TEXAS INSTRUMENTS**

12500 TI Boulevard, Dallas, Texas 75243

TITLE: ADS8402/ADS8406/ADS8412EVM Block Diagram

Engineer: Lijoy Philipose	DOCUMENT CONTROL #: 6446998	REV: C
Drawn By: Lijoy Philipose	DATE: 29-Jul-2004	SIZE: SHEET: 1 OF: 3
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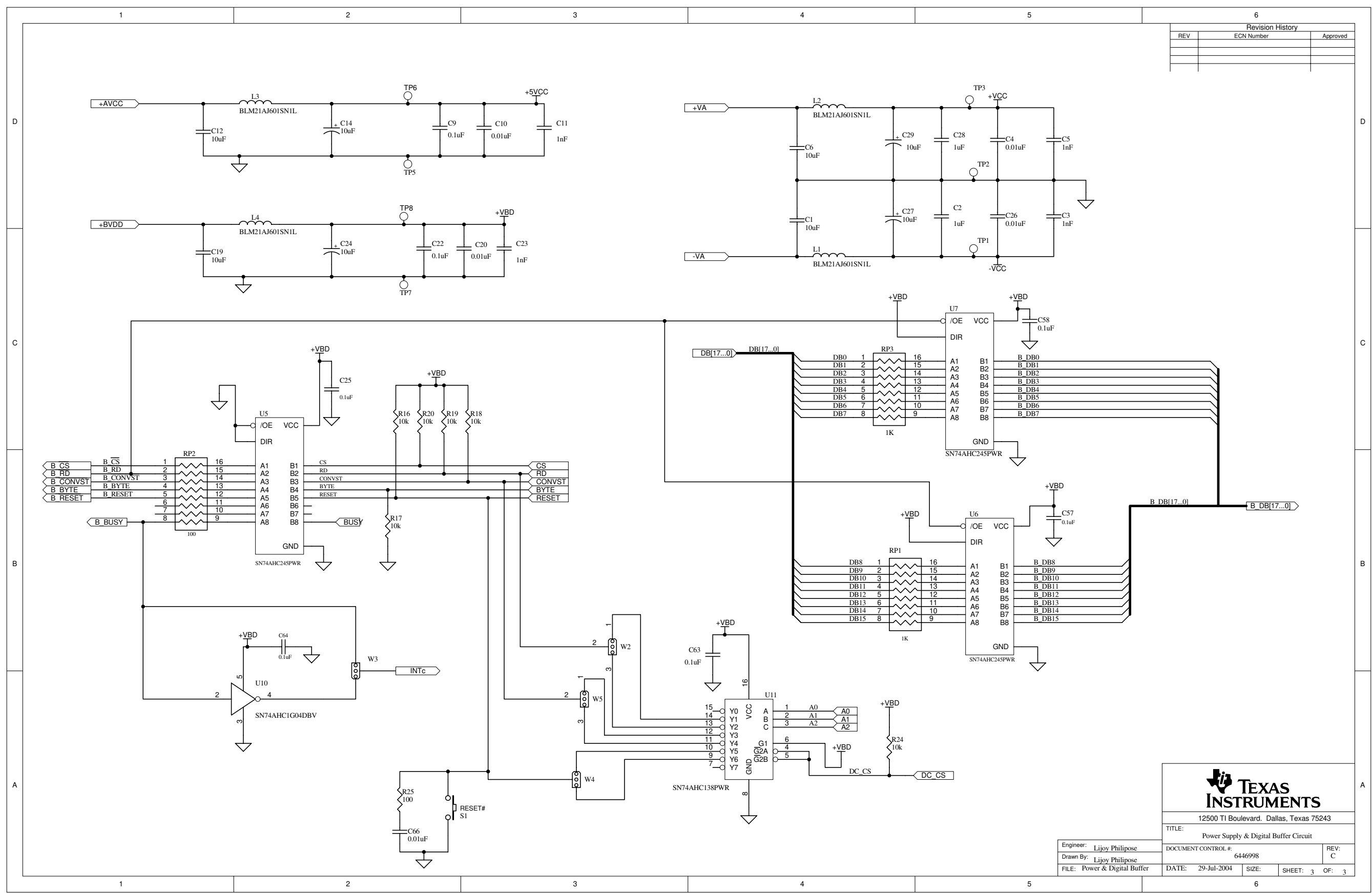
Revision History		
REV	ECN Number	Approved



12500 TI Boulevard, Dallas, Texas 75243

TITLE:	Analog-to-Digital Converter	
DOCUMENT CONTROL #:	6446998	REV: C
Engineer:	Lijoy Philipose	DATE: 29-Jul-2004
Drawn By:	Lijoy Philipose	SIZE: SHEET: 2 OF: 3
FILE: Analog-to-Digital Converter		

Revision History		
REV	ECN Number	Approved



TITLE: Power Supply & Digital Buffer Circuit			
Engineer: Lijoy Philipose	DOCUMENT CONTROL #: 6446998	REV: C	
Drawn By: Lijoy Philipose	DATE: 29-Jul-2004	SIZE:	
FILE: Power & Digital Buffer		SHEET: 3	OF: 3



**Related Documentation from Texas Instruments**

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this document by its title and literature number. Updated documents can also be obtained through the TI Web site at [www.ti.com](http://www.ti.com)

**Data Sheets:**

ADS8402

ADS8406

ADS8412

REF3040

SN74AHC138

SN74AHC245

SN74AHC1G04

THS4503

**Literature Number:**[SLAS154](#)[SLAS426](#)[SLAS384](#)[SBVS032](#)[SCLS258](#)[SCLS230](#)[SCLS318](#)[SLOS352](#)

## FCC Warnings

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

## EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

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## EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of  $\pm 6$  V and the output voltage range of 0 V and 5.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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