Title	***Reference Design Report for a 5 W Adapter Using LinkSwitch™-CV LNK625DG***
Specification	Input: 85 VAC – 265 VAC; Output: 5 V / 1 A
Application	Adapter
Author	Applications Engineering Department
Document Number	RDR-669
Date	July 15, 2020
Revision	1.5

Summary and Features

- Low parts count solution
- Auto-restart output short-circuit, open-loop and over-temperature protection
- Primary side regulated
- Meets EN55022 EMI

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.power.com.

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1 Introduction

This document is an engineering design report describing a 5 W / 5 V adapter power supply using LNK625DG. Input is 85 VAC to 265 VAC.

The document contains the power supply specification, schematic, transformer documentation, performance data and EMI scan.

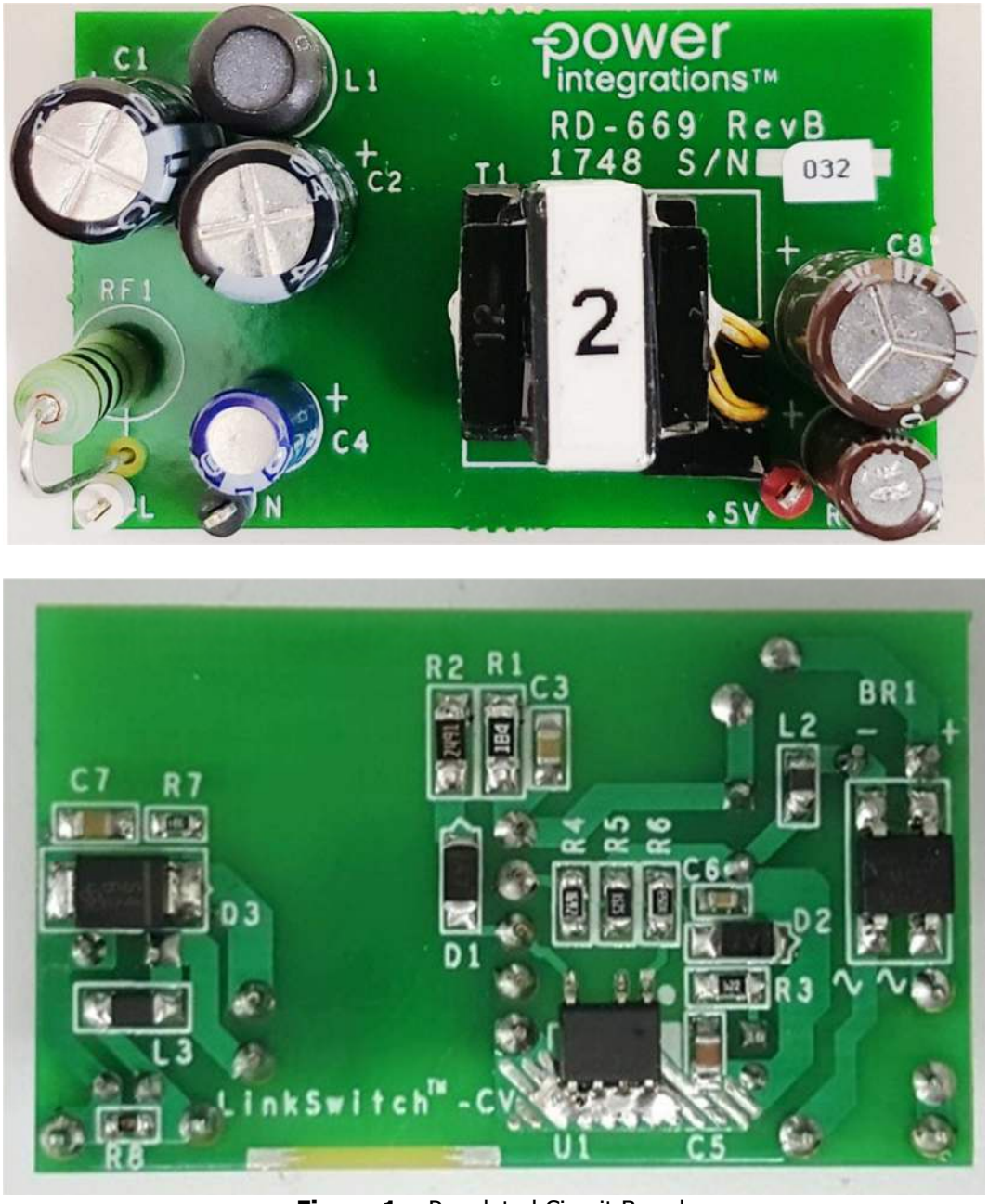

Figure 1 – Populated Circuit Board.

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	$\mathbf{V_{IN}}$	85	115/230	265	VAC	2 Wire.
Frequency	$\mathbf{f_{LINE}}$		50/60		Hz	
Output						
Output Voltage	$\mathbf{V_{OUT}}$	4.75	5.0	5.25	V	
Output Current	$\mathbf{I_{OUT}}$		1.0		A	
Output Voltage Ripple				150	mV	
Continuous Output Power	$\mathbf{P_{OUT}}$		5		W	
Average Efficiency	η	74			%	At Nominal Lines.
EMI	EN55022					
Ambient Temperature	Tamb	0		40	ºC	

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3 Schematic

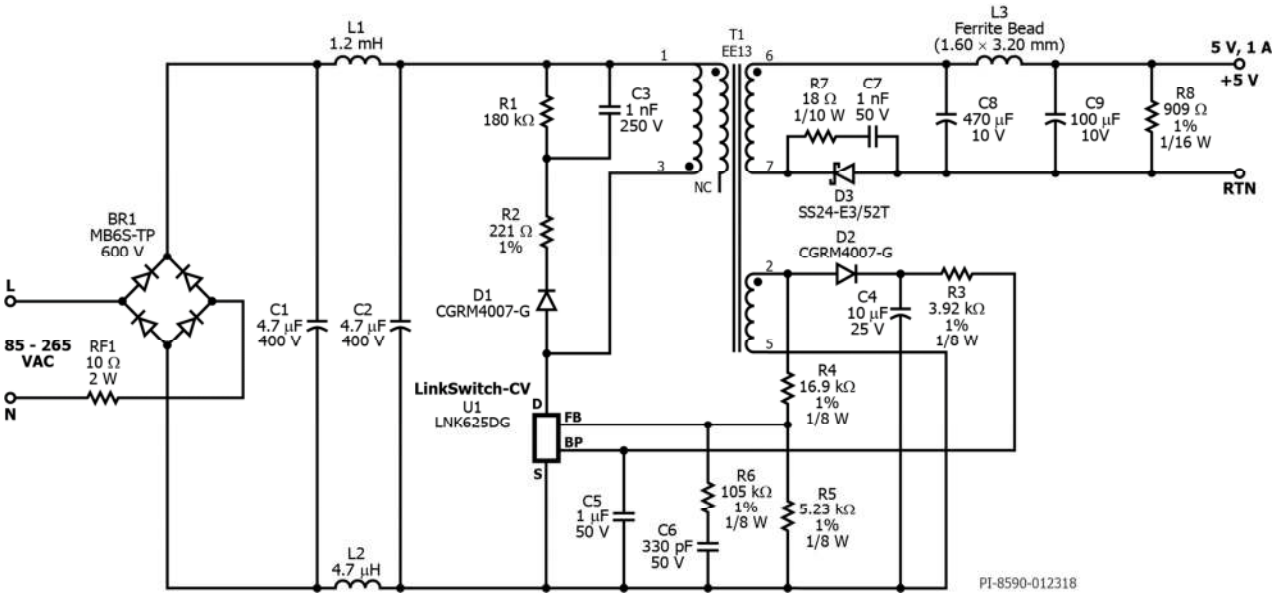

Figure 2 – Schematic.

4 Circuit Description

The schematic in Figure 2 shows an adapter design using the LNK625DG IC that provides constant voltage (CV) performance. The circuit is designed to operate from 85 VAC to 265 VAC input, with an output voltage of 5 V providing a maximum load current of 1 A. It consumes very little standby power and uses no Y capacitor but still meet stringent EMI requirements.

4.1 Input and EMI Filtering

Bridge rectifier BR1 is a full wave rectifier. The rectified DC is then filtered by capacitors C1 and C2. Inductor L1, L2 forms a pi filter with capacitors C1 and C2 which helps to reduce differential EMI noise. This filtering, together with the integrated switching frequency jitter provided in U1 and transformer E-Shield techniques, provide a generous EMI margin without the need for a Y capacitor across the primary and secondary windings of transformer T1.

4.2 LinkSwitch-CV Device

The LinkSwitch-CV family of devices has been developed to cost effectively replace all existing solutions in low power adapter applications. It is optimized for constant voltage (CV) adapter applications while using minimal external parts including the complete elimination of the optocoupler and shunt regulator.

The LNK625DG IC monolithically integrates the 700 V power MOSFET switch and controller, which consists of an oscillator, feedback (sense and logic) circuit, 6 V regulator, BYPASS (BP) pin programming functions, over-temperature protection, frequency jittering, current limit circuit and leading-edge blanking.

The LNK625DG IC also provides a sophisticated range of protection features including auto-restart for control loop component open/short-circuit faults and output short-circuit conditions. The use of a low auto-restart on time reduces the power delivered by more than 95% for output short-circuits and control loop faults. Accurate hysteretic thermal shutdown ensures safe average PCB temperatures under all conditions. Extended creepage distance between high and low voltage pins prevent arcing and helps meet safety requirements. The LinkSwitch-CV IC also can be used without a bias winding as it is completely self-biased.

4.3 Primary Circuit

During U1’s on time current flows through the primary winding of transformer T1 and stores energy in its magnetic field. During U1’s off time, the energy stored in the transformer is transferred to the secondary side, delivering current to both the output capacitors and the load.

The clamp circuit formed by resistors R1 and R2 along with blocking diode D1 and capacitor C3 ensures that the drain node voltage is well below the 700 V rating of the

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internal MOSFET of U1. The clamp circuit is also carefully designed to reduce and dampen any oscillation present in the voltage spike caused by the transformer's leakage inductance.

4.4 Output Rectification

The secondary output is rectified by diode D3 which is placed in the return leg to help reduce EMI and simplify the transformer construction. An RC snubber circuit composed of resistor R7 and capacitor C7 is placed across the output diode to also reduce high frequency EMI. A stable output voltage is maintained by capacitor C8. Inductor L3 and capacitor C9 form an LC post filter which helps to attenuate switching noise and reduces output ripple. Resistor R8 is a preload resistor whose value has been empirically chosen to provide the best possible regulation at light loads without significantly affecting no-load input power or efficiency.

4.5 Feedback Winding

The LinkSwitch-CV IC eliminates the need for an optocoupler for tight output voltage regulation, as good as ±5%, through the use of a feedback winding. The FEEDBACK (FB) pin voltage, which is derived from the voltage divider formed by resistors R4 and R5, is sampled approximately 2.5 μs after U1's internal power MOSFET turns off. Based upon this information the device regulates the output voltage.

The feedback winding was also designed with more turns than necessary so that it may act as a bias winding. The winding provides bias current to U1 through the BP pin and reduces the input power consumption during light loads and no-load conditions. Capacitor C4 provides a stable bias voltage while resistor R3 is chosen to supply the necessary BP pin current. Capacitor C5 is the BP pin capacitor and should be placed as close as possible to the BP pin and SOURCE (S) pins of the device.

5 PCB Layout

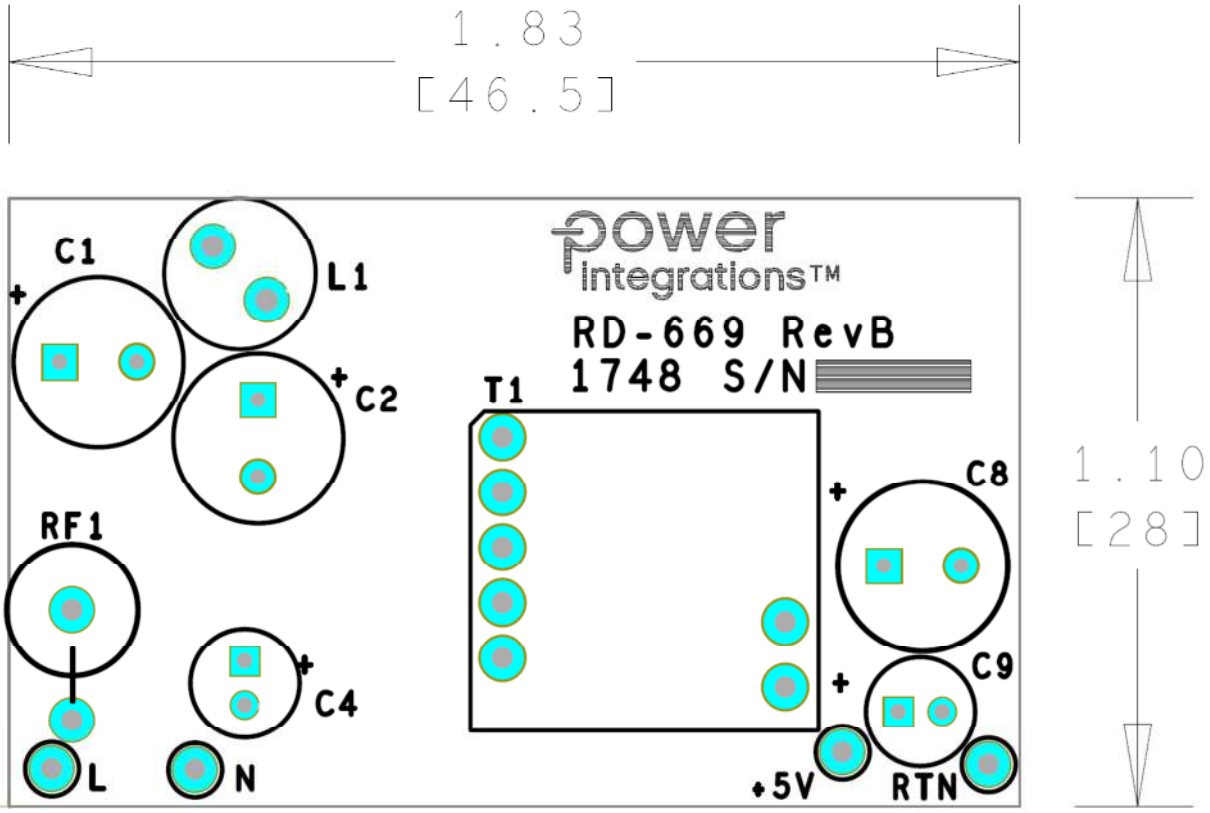

Figure 3 – PCB Layout, Top.

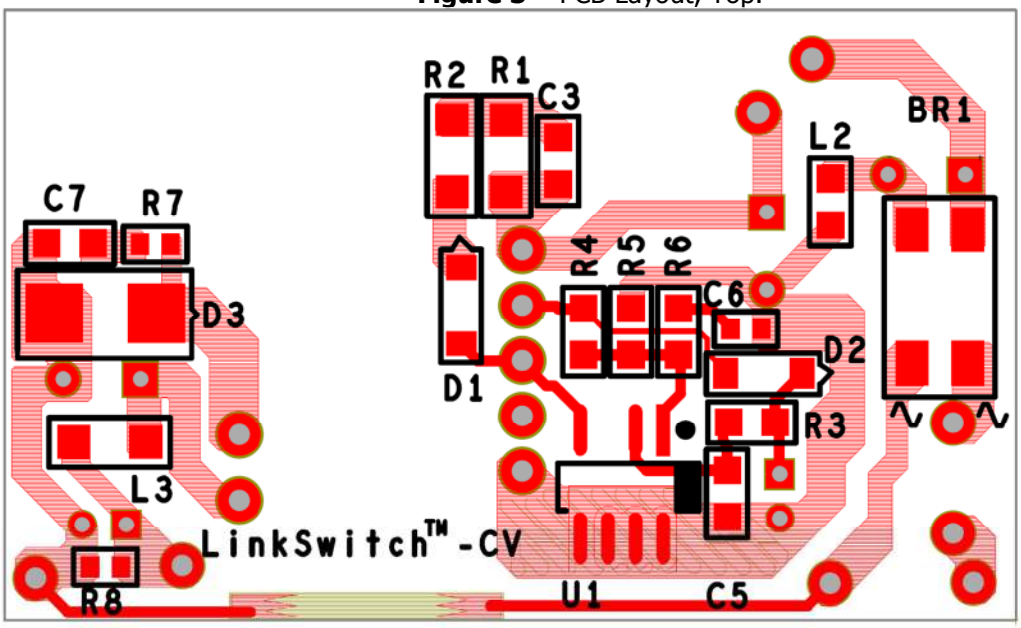

Figure 4 – PCB Layout. Bottom.

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6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 0.5 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	MB6S-TP	Micro Commercial
2	1	C1	4.7 µF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G4R7MK0811MLL3	Taicon
3	1	C2	4.7 µF, 400 V, Electrolytic, (8 x 11.5)	TAQ2G4R7MK0811MLL3	Taicon
4	1	C3	1 nF, 250 V, Ceramic, X7R, 0805	GRM21AR72E102KW01D	Murata
5	1	C4	10 µF, 25 V, Electrolytic, Gen. Purpose, (5 x 12)	ECA-1EM100	Panasonic
6	1	C5	1 µF,50 V, Ceramic, X7R, 0805	C2012X7R1H105M085AC	TDK
7	1	C6	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
8	1	C7	1 nF, 50 V, Ceramic, X7R, 0805	08055C102KAT2A	AVX
9	1	C8	470 µF, 10 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE100ELL471MHB5D	Nippon Chemi-Con
10	1	C9	100 µF, 10 V, Electrolytic, Very Low ESR, 300 mΩ, (5 x 11)	EKZE100ELL101ME11D	Nippon Chemi-Con
11	1	D1	Diode, Standard, 1000V, 1A, Surface Mount, MINISMA, Mini SMA/SOD-123	CGRM4007-G	Comchip
12	1	D2	Diode, Standard, 1000V, 1A, Surface Mount, MINISMA, Mini SMA/SOD-123	CGRM4007-G	Comchip
13	1	D3	40 V, 2 A, Schottky, SMD, DO-214AA	SS24-E3/52T	Vishay
14	1	L1	FIXED IND, 1.2 mH, ±10%,Imax=150 mA, 3.3 Ω max, TH, UNSHIELDED	AIUR-16-122K	Abracon
15	1	L2	4.7 µH, 600 mA SMD INDUCTOR, MULTILAYER	MLZ2012N4R7LT000	TDK
16	1	L3	Ferrite Bead, Z=70 Ω @ 100 MHz, Rdc=0.100 Ω, 1.5 A, -55°C ~ 125°C, 1206 (3216 Metric)	CIB31P700NE	Samsung
17	1	R1	RES, 180 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ184V	Panasonic
18	1	R2	RES, 221 Ω, 1%, 1/4 W, Thick Film, 1206	P221FCT-ND	Panasonic
19	1	R3	RES, 3.92 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF3921V	Panasonic
20	11	R4	RES, 16.9 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ622V	Panasonic
21	1	R5	RES, 5.23 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF5231V	Panasonic
22	1	R6	RES, 105 kΩ, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1053V	Panasonic
23	1	R7	RES, 18 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ180V	Panasonic
24	1	R8	RES, 909 Ω, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF9090V	Panasonic
25	1	RF1	RES, 10 Ω, 5%, 2 W, Wirewound, Fusible	FW20A10R0JA	Bourns
26	1	T1	Bobbin, EE13 (2+5) P V 1 SEC PM9820 Transformer	WS-51319 PNK-62506	Win Shine Premier Magnetics
27	1	U1	LinkSwitch-CV, SO-8C	LNK625DG	Power Integrations
28	1	+5V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000K-ND	Keystone
29	1	RTN	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001K-ND	Keystone
30	1	L	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002K-ND	Keystone
31	1	N	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001K-ND	Keystone

7 Transformer Specification

7.1 Electrical Diagram

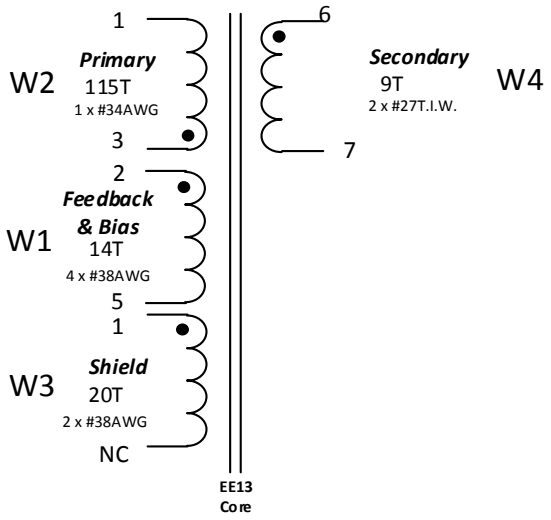

Figure 5 – Transformer Electrical Diagram.

7.2 Mechanical Diagram

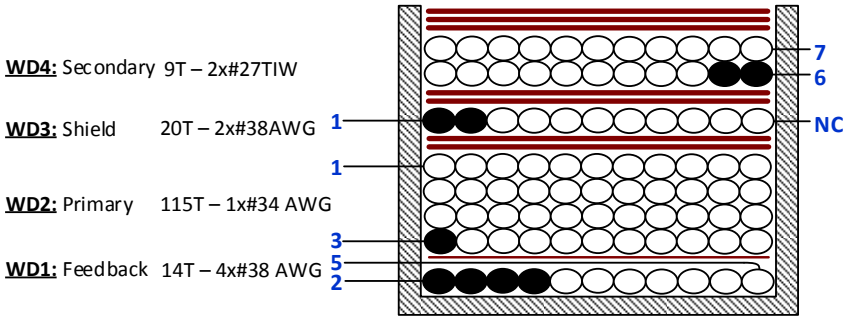

Figure 6 – Transformer Mechanical Diagram.

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7.3 Material List

Item	Description
[1]	Core: EE13, PC95, Gapped for ALG of 100 nH/T².
[2]	Bobbin: Generic, 4 pri. + 2 sec. (High Isolation Bobbin).
[3]	Barrier Tape: Polyester Film [1 mil (25 µm) base thickness], 8.50 mm Wide.
[4]	Varnish.
[5]	Magnet Wire: #34 AWG, Solderable Double Coated.
[6]	Magnet Wire: #38 AWG, Solderable Double Coated.
[7]	Triple Insulated Wire: #27 AWG.
[8]	Magnet Wire: #32 AWG, Solderable Double Coated.

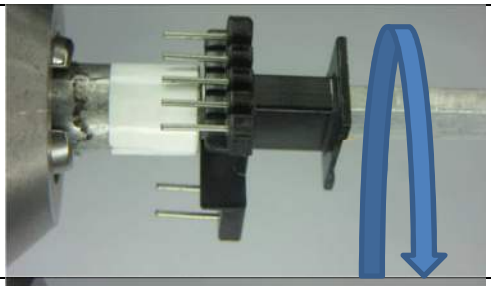
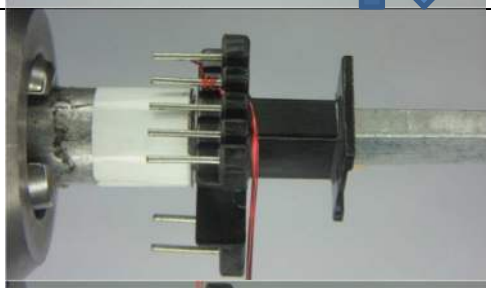
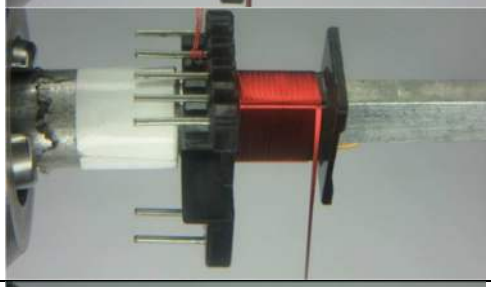
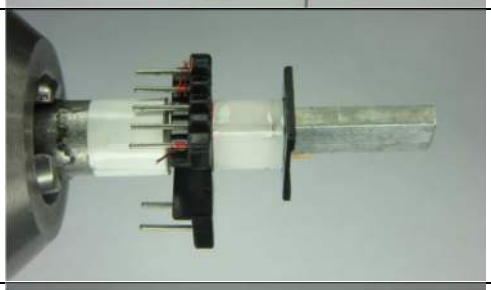
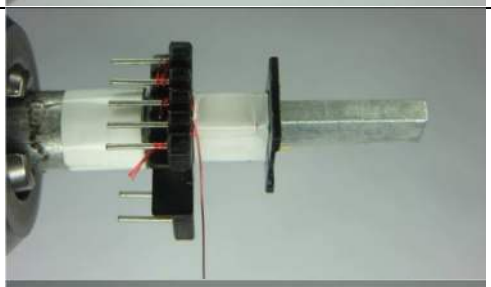
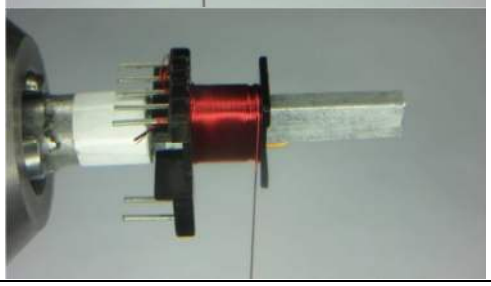
7.4 Electrical Test Specifications

Parameter	Condition	Spec
Electrical Strength, VAC	60 Hz 1 second, from pins 1, 2, 3 ,4, 5 to pins 7, 8, 9, 10.	3000
Nominal Primary Inductance, µH	Measured at 1 V_{PK-PK}, typical switching frequency, between pin 1 to pin 3, with all other windings open.	1369
Tolerance, ±%	Tolerance of Primary Inductance	10.0
Maximum Primary Leakage, µH	Measured between pin 1 to pin 3, with all other windings shorted.	54.77

Although the design of the software considered safety guidelines, it is the user's responsibility to ensure that the user's power supply design meets all applicable safety requirements of user's product.

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at www.powerint.com.

7.5 Transformer Winding Illustrations

Winding Preparation		For the purpose of these instructions, bobbin is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1: Feedback	 	Start on pin(s) 2 and wind 14 turns (x4 AWG #38) in 1 layer from left to right. Terminate at pin 5.
Insulation		Add 1 layer of tape, Item [3], for insulation.
WD2: Primary	 	Start on pin(s) 3 and wind 115 turns (x1 AWG #34) in 4 layers from left to right. Wind in same rotational direction as Feedback winding. At the last layer spread the winding evenly across entire bobbin. Terminate at pin 1 after finish.

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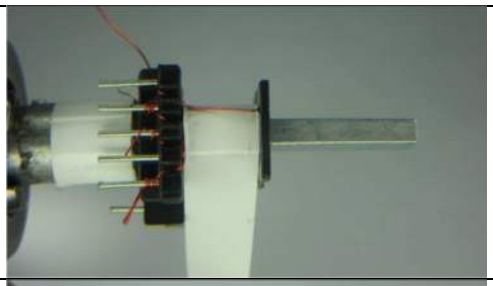
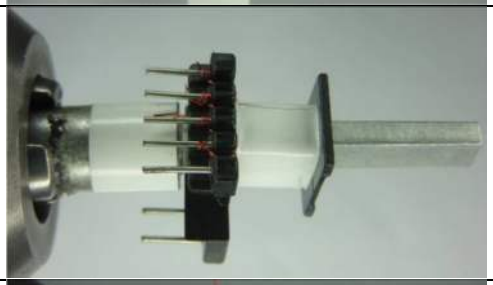
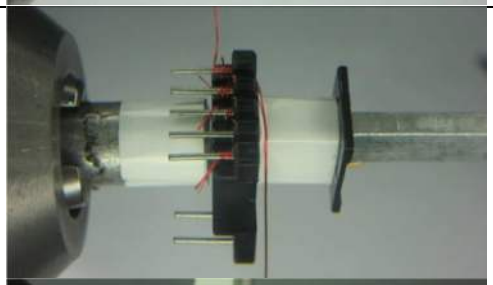
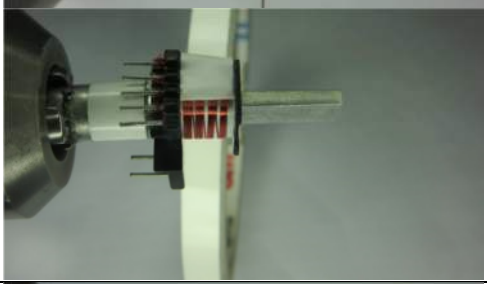
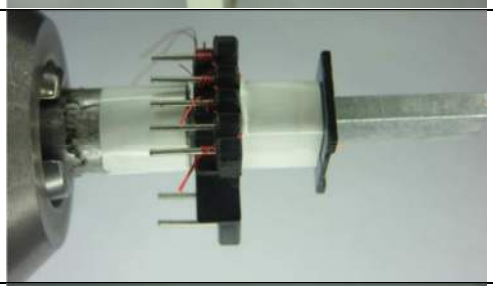
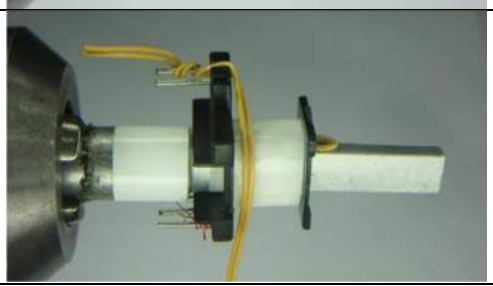
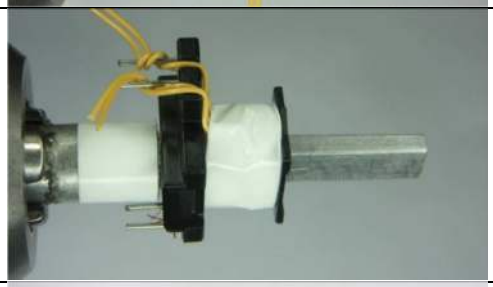
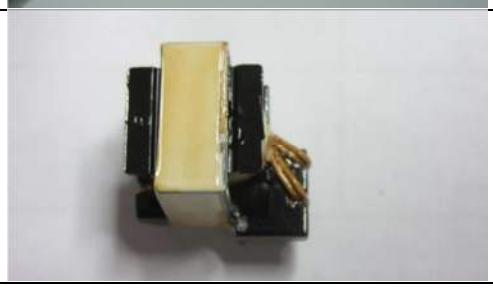
		
Insulation		Add 2 layers of tape, Item [3], for insulation.
WD3: Shield	 	Start on pin(s) 1 and wind 20 turns (x2 AWG #38). Wind in same rotational direction as primary winding. Form a 4 group of 5 turns with spaces in between each group. Leave this end of shield winding not connected.
Insulation		Add 2 layers of tape, Item [3], for insulation.
WD4: Secondary		Start on pin(s) 6 and wind 9 turns (x2 TIW #27) in 2 layers. Wind in clockwise direction. Finish this winding on pin(s) 7.

		
Insulation		Add 3 layers of tape, Item [3], for insulation.
Finish		Dip varnish uniformly in Item [4]. Do not vacuum impregnate.

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8 Performance Data

Note: Data were taken at room temperature. Measurements were taken at the end of PCB.

8.1 Full Load Efficiency vs. Input Line Voltage (at PCB)

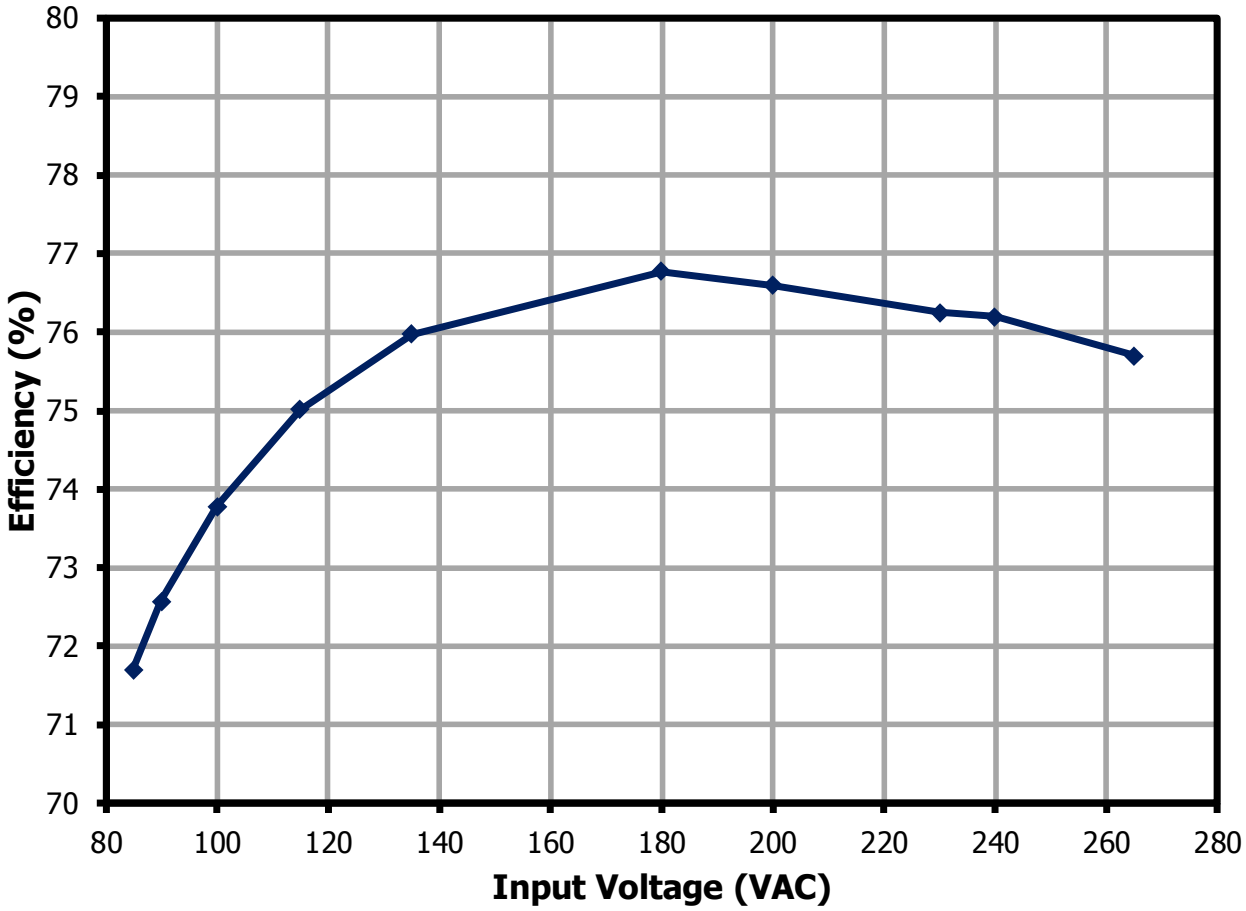

Figure 7 – Efficiency vs. Line Voltage, Room Temperature Measured at the End of the PCB.

8.2 Efficiency vs. Load (at PCB)

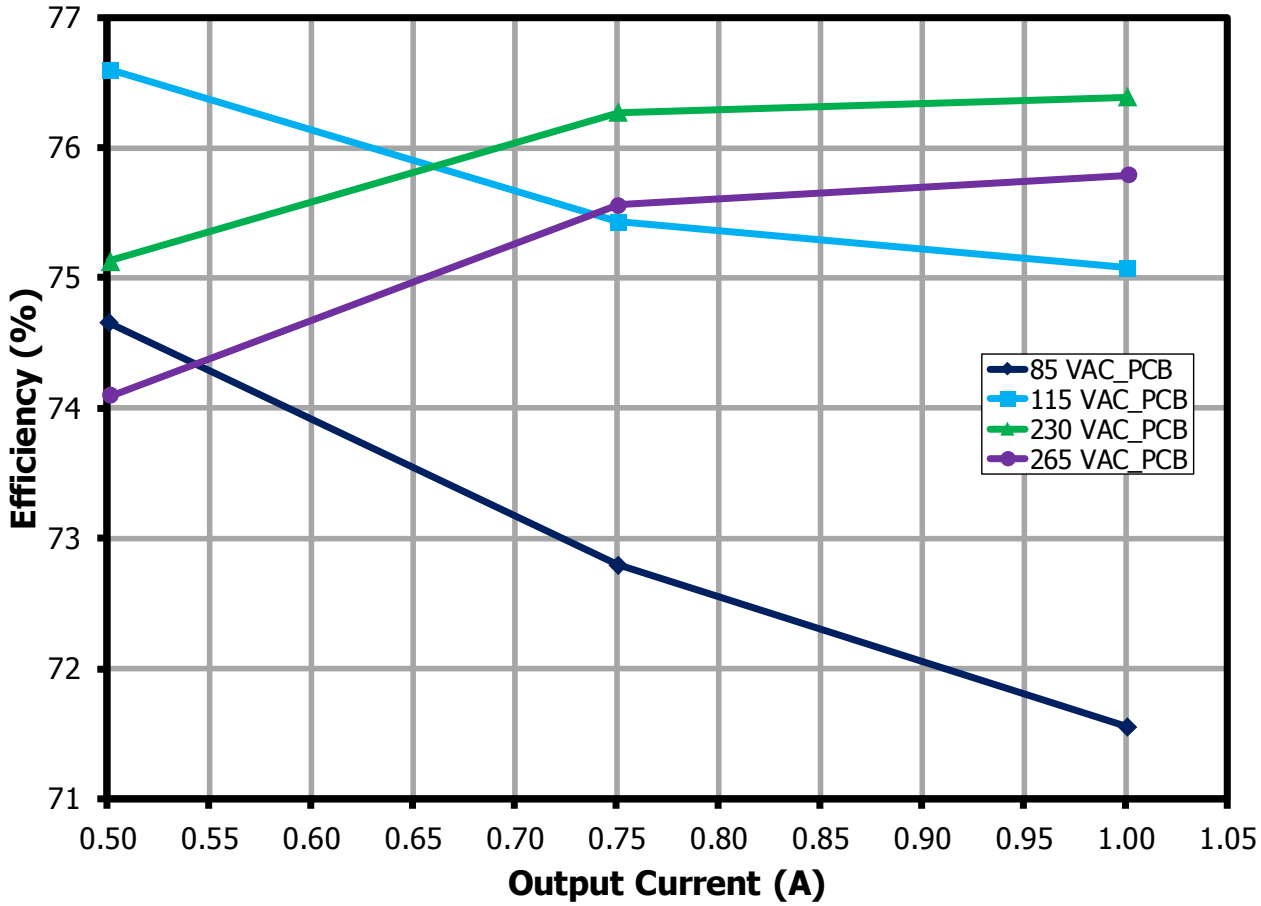

Figure 8 – Efficiency vs. Load, Room Temperature Measured at PCB.

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8.3 Average Efficiency

Requirement	Minimum Average Efficiency (%)		Maximum Power in No-load Mode (W)
DOE VI	≥ 0.0834 x ln(P_{OUT}) – 0.0014 x P_{OUT} + 0.609	73.62%	≤0.100

8.3.1 115 VAC / 60 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	114.95	0.10	6.64	4.98	1.00	4.99	75.08
75%	114.96	0.08	4.99	5.01	0.75	3.76	75.43
50%	114.97	0.06	3.29	5.03	0.50	2.52	76.60
25%	114.98	0.03	1.69	5.05	0.25	1.26	74.85
						Average	**75.49**

8.3.2 230 VAC / 50 Hz

Load (A)	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} at PCB (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency at PCB (%)
100%	229.99	0.06	6.47	4.94	1.00	4.94	76.39
75%	229.99	0.05	4.91	4.99	0.75	3.74	76.27
50%	230.00	0.04	3.33	4.98	0.50	2.50	75.13
25%	230.00	0.02	1.71	4.99	0.25	1.25	73.08
						Average	**75.22**

8.4 No-Load Input Power

	85 VAC	115 VAC	230 VAC	265 VAC
P_{IN}	52 mW	56.4 mW	69.92 mW	67.69 mW

No-load input power soak time: 15 mins.

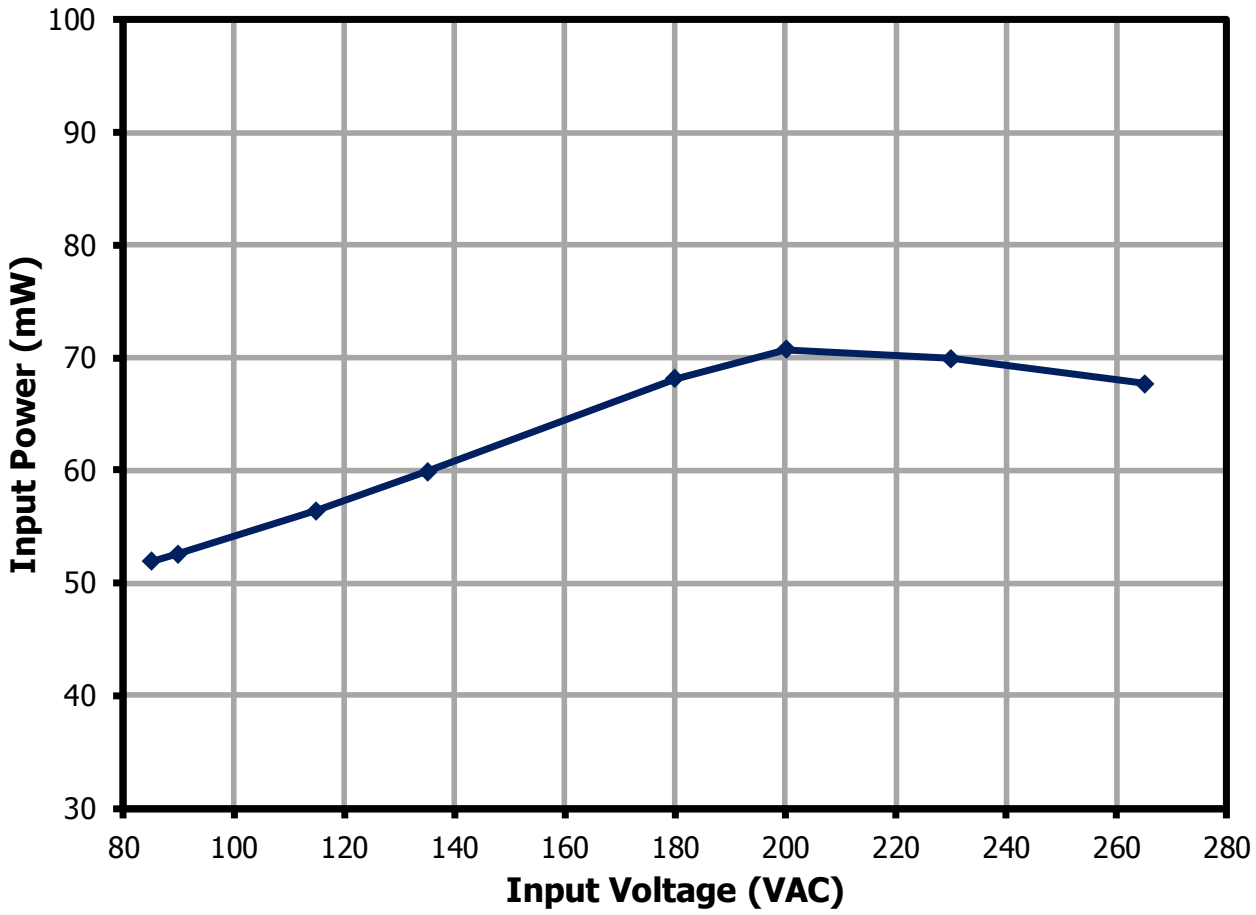

Figure 9 – No-Load Input Power.

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8.5 Line and Load Regulation

8.5.1 Line Regulation at Full Load (at PCB)

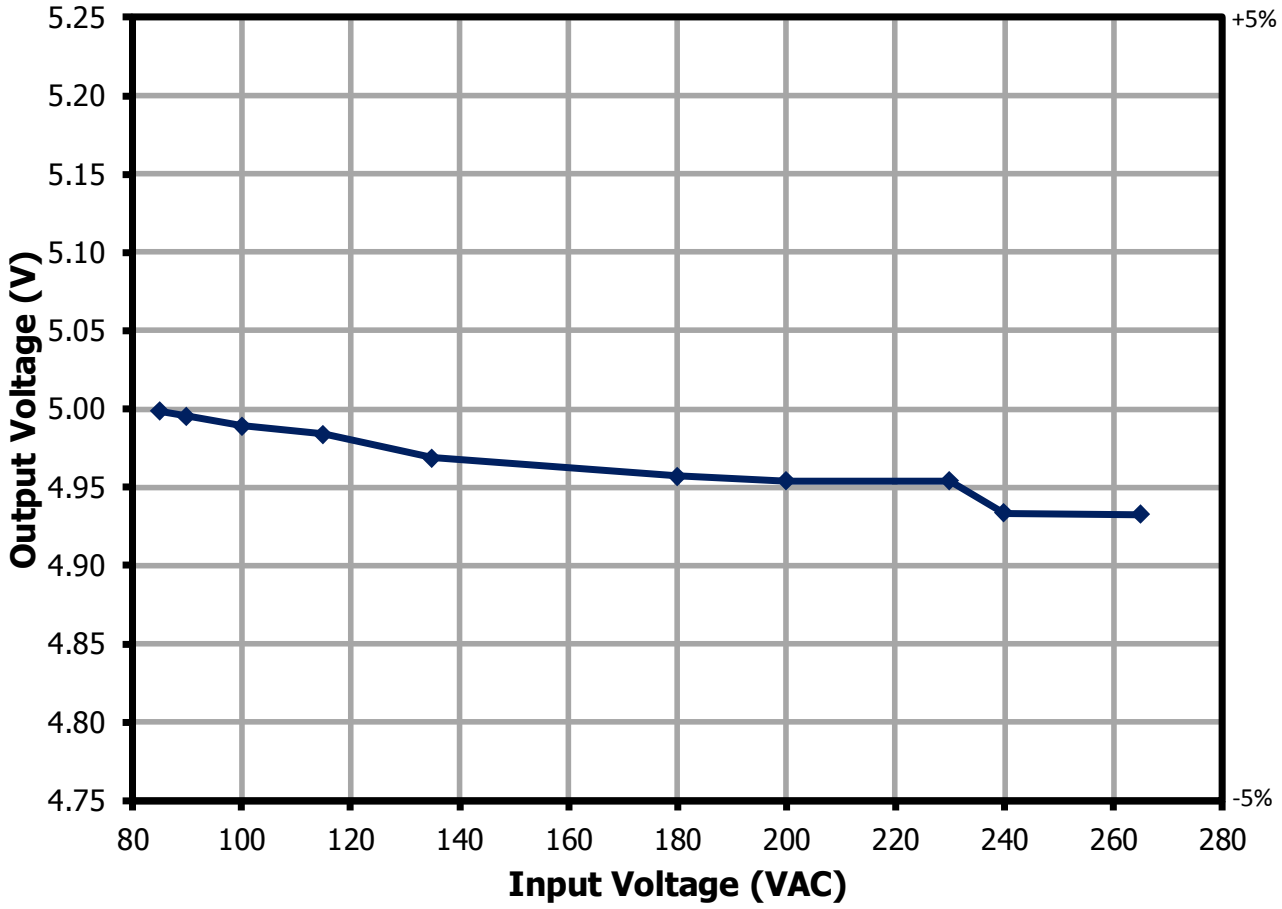

Figure 10 – Line Regulation at Full Load.

8.5.2 Load Regulation (at PCB)

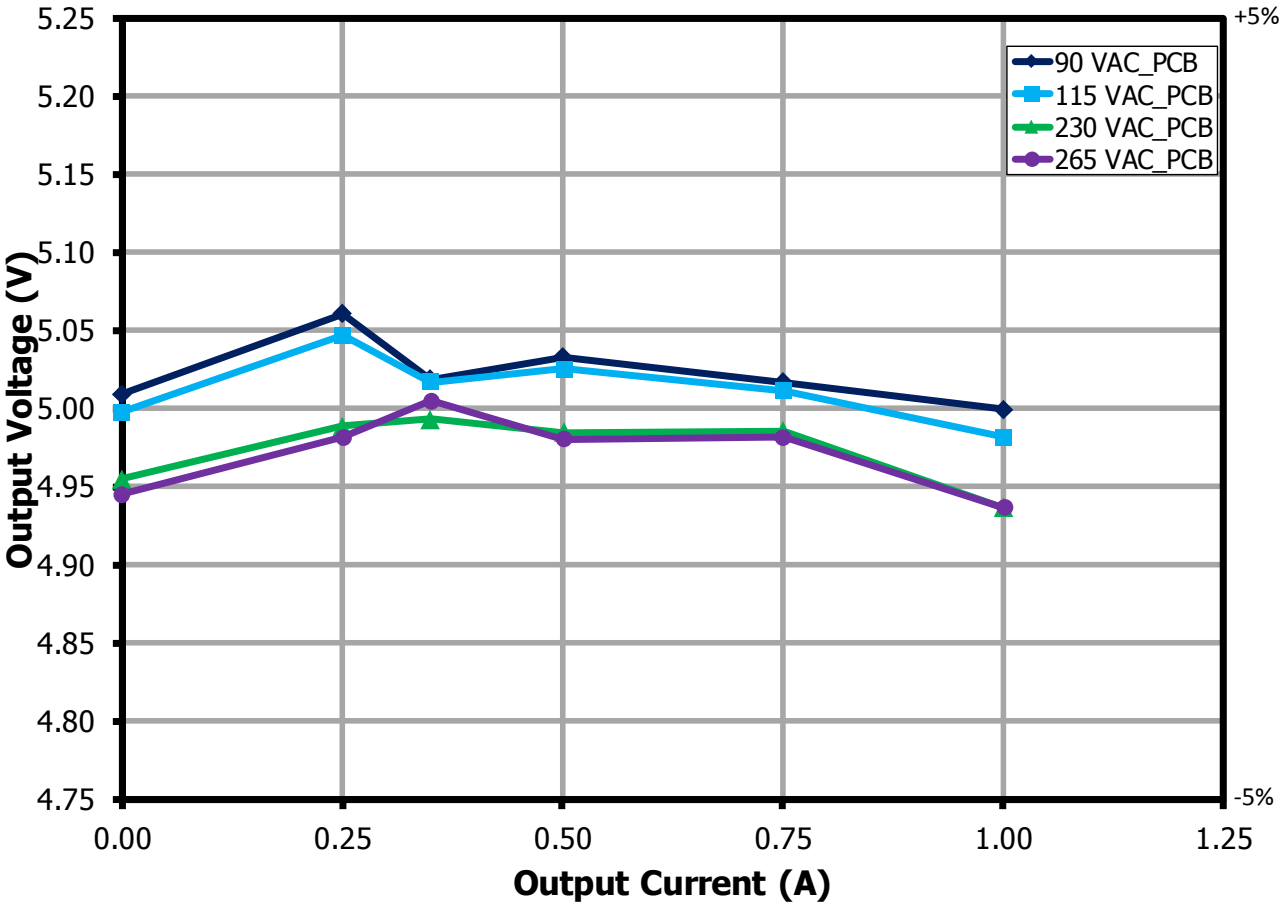

Figure 11 – Load Regulation.

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9 Waveforms

9.1 Drain Voltage and Current, Normal Operation Full Load

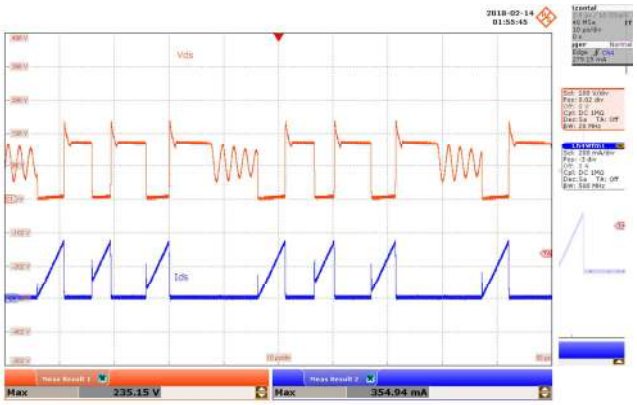

Figure 12 – 85 VAC Input, Full Load.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$: 235.15 V.
$I_{DS(MAX)}$: 354.94 mA.

Figure 13 – 115 VAC Input, Full Load.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$: 274.68 V.
$I_{DS(MAX)}$: 354.94 mA.

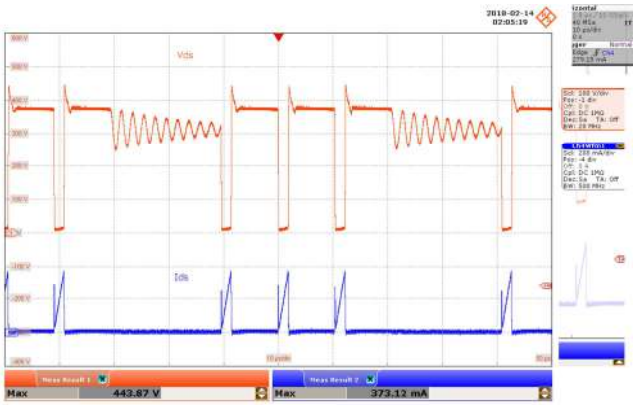

Figure 14 – 230 VAC Input, Full Load.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$: 443.87 V.
$I_{DS(MAX)}$: 373.12 mA.

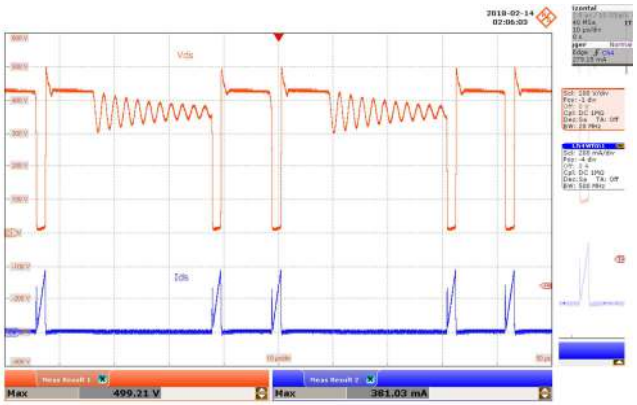

Figure 15 – 265 VAC Input, Full Load.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 200 mA / div., 10 µs / div.
$V_{DS(MAX)}$: 499.21 V.
$I_{DS(MAX)}$: 381.03 mA.

9.2 Drain Voltage and Current Start-up Profile

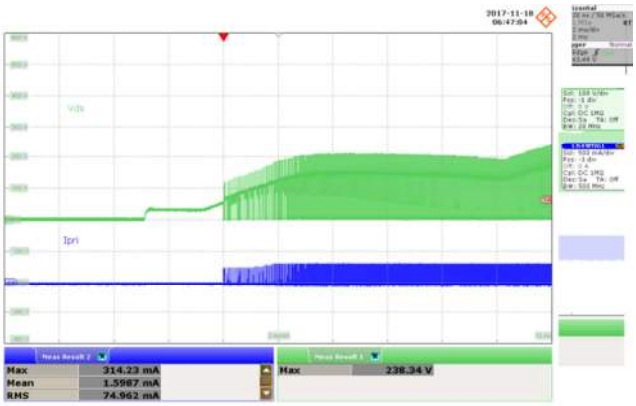

Figure 16 – 85 VAC Input, Full Load.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 500 mA / div., 2 ms / div.
$V_{DS(MAX)}$: 238.34 V.
$I_{DS(MAX)}$: 314.23 mA.

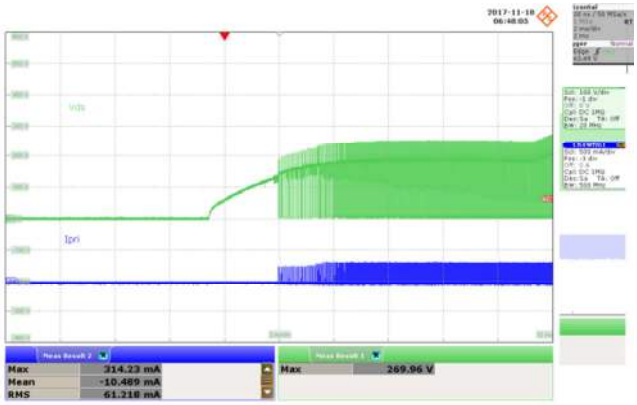

Figure 17 – 115 VAC Input, Full Load.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 2 ms / div.
$V_{DS(MAX)}$: 269.96 V.
$I_{DS(MAX)}$: 314.23 mA.

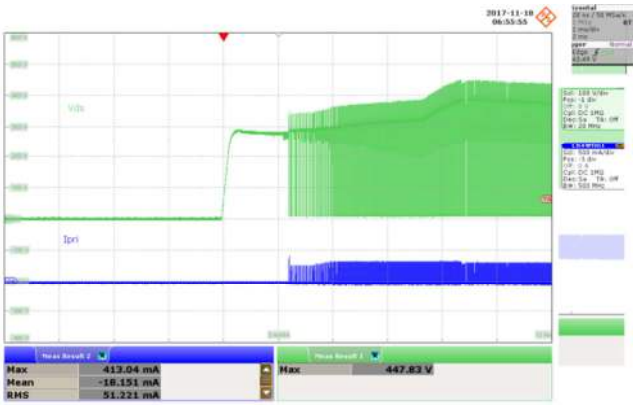

Figure 18 – 230 VAC Input, Full Load.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 2 ms / div.
$V_{DS(MAX)}$: 447.83 V.
$I_{DS(MAX)}$: 413.04 mA.

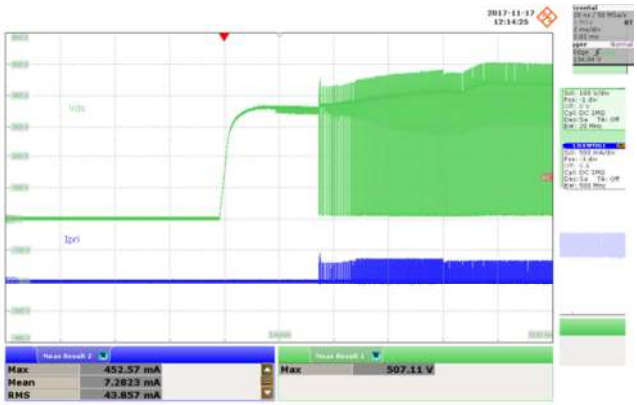

Figure 19 – 265VAC Input, Full Load.
Upper: V_{DS}, 100 V / div.
Lower: I_{DS}, 400 mA / div., 2 ms / div.
$V_{DS(MAX)}$: 507.11 V.
$I_{DS(MAX)}$: 452.57 mA.

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9.3 Output Diode Reverse Voltage

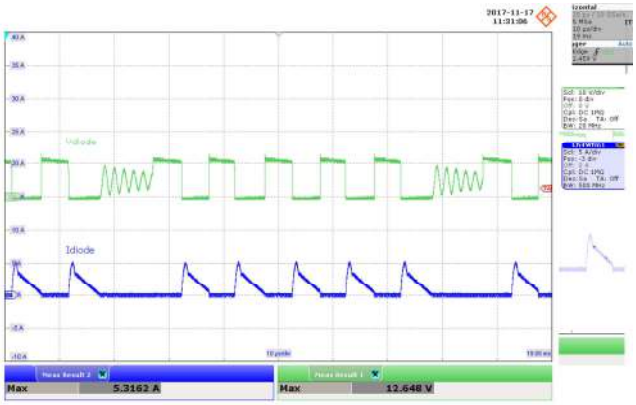

Figure 20 – 85 VAC Input, Full Load.
Upper: V_{DIODE}, 10 V / div.
Lower: I_{DIODE}, 5 A / div., 10 µs / div.
$V_{DIODE(MAX)}$: 12.648 V.
$I_{DIODE(MAX)}$: 5.3162 A.

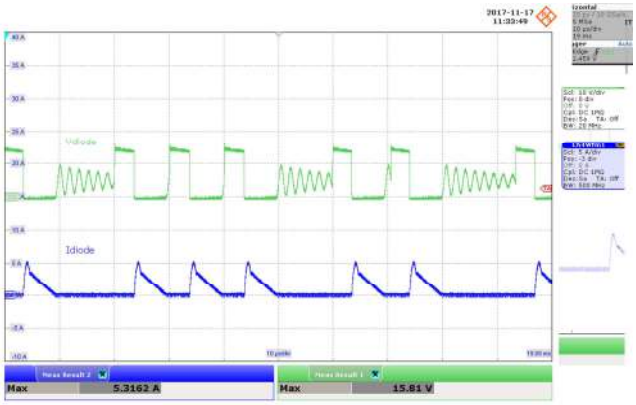

Figure 21 – 115 VAC Input, Full Load.
Upper: V_{DIODE}, 10 V / div.
Lower: I_{DIODE}, 5 A / div., 10 µs / div.
$V_{DIODE(MAX)}$: 15.81 V.
$I_{DIODE(MAX)}$: 5.3162 A.

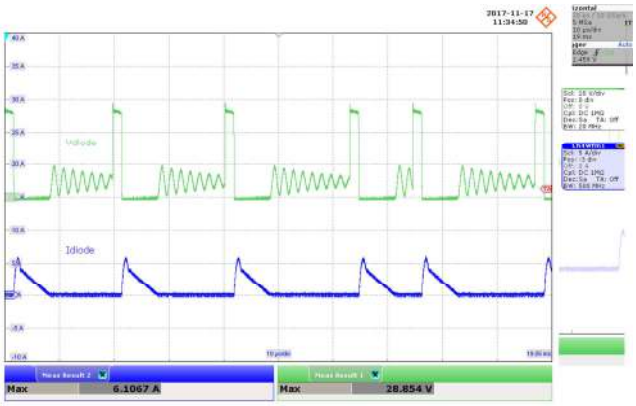

Figure 22 – 230 VAC Input, Full Load.
Upper: V_{DIODE}, 10 V / div.
Lower: I_{DIODE}, 5 A / div., 10 µs / div.
$V_{DIODE(MAX)}$: 28.854 V.
$I_{DIODE(MAX)}$: 6.1067 A.

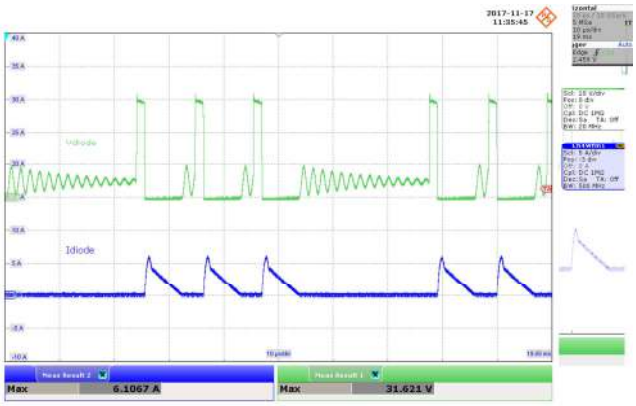

Figure 23 – 265 VAC Input, Full Load.
Upper: V_{DIODE}, 10 V / div.
Lower: I_{DIODE}, 5 A / div., 10 µs / div.
$V_{DIODE(MAX)}$: 31.621 V.
$I_{DIODE(MAX)}$: 6.1067 A.

9.4 Output Rise Time

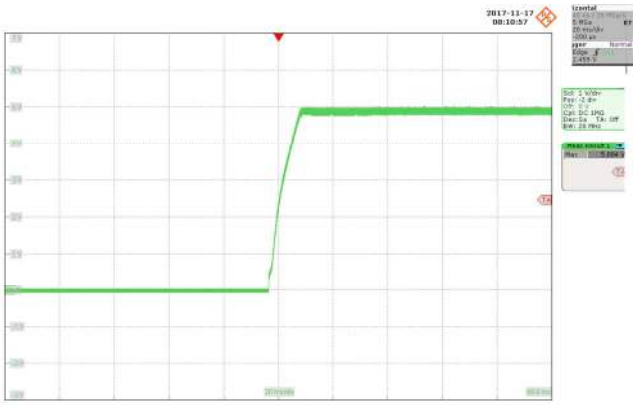

Figure 24 – 85 VAC Input, Full Load.
V_{OUT}, 1 V / div., 20 ms / div.

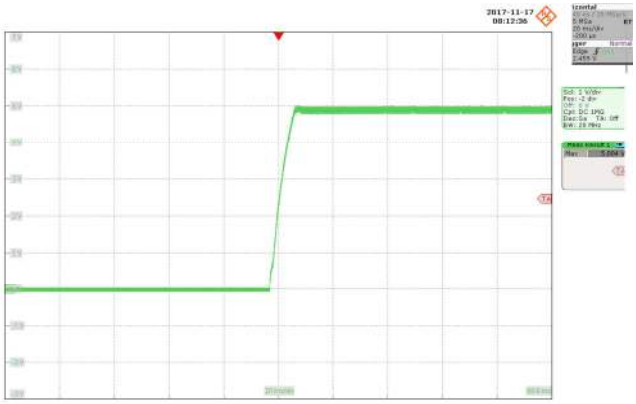

Figure 25 – 115 VAC Input, Full Load.
V_{OUT}, 1 V / div., 20 ms / div.

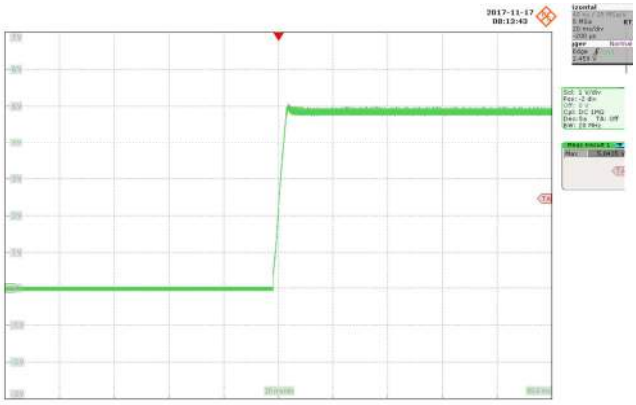

Figure 26 – 230 VAC Input, Full Load.
V_{OUT}, 1 V / div., 20 ms / div.

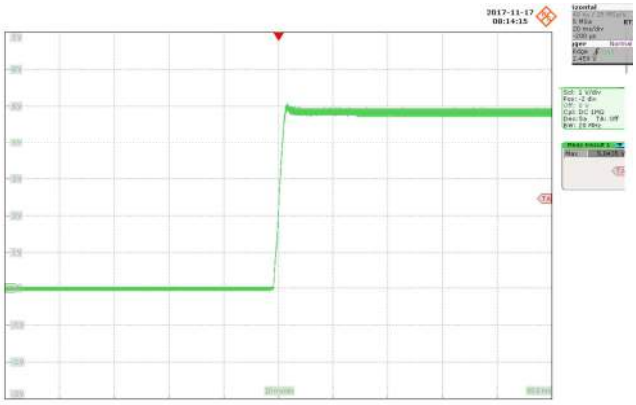

Figure 27 – 265 VAC Input, Full Load.
V_{OUT}, 1 V / div., 20 ms / div.

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9.5 Turn On Delay

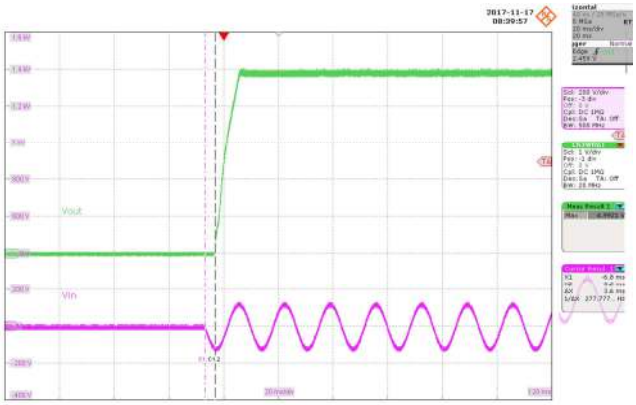

Figure 28 – 85 VAC Input, Full Load.
Upper: V_{OUT}, 2 V / div.
Lower: V_{IN}, 200 V / div., 20 ms / div.
Turn On Delay: 3.6 ms.

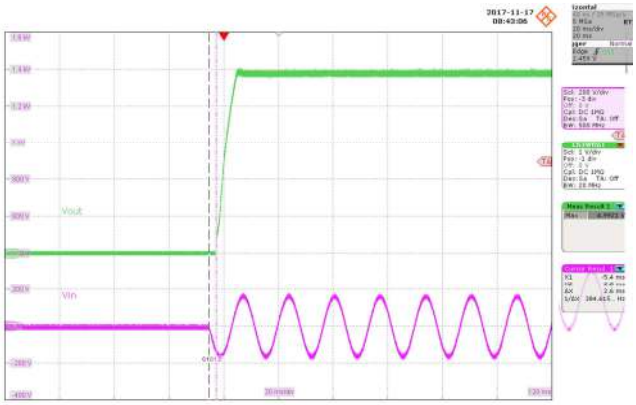

Figure 29 – 115 VAC Input, Full Load.
Upper: V_{OUT}, 2 V / div.
Lower: V_{IN}, 200 V / div., 20 ms / div.
Turn On Delay: 2.6 ms.

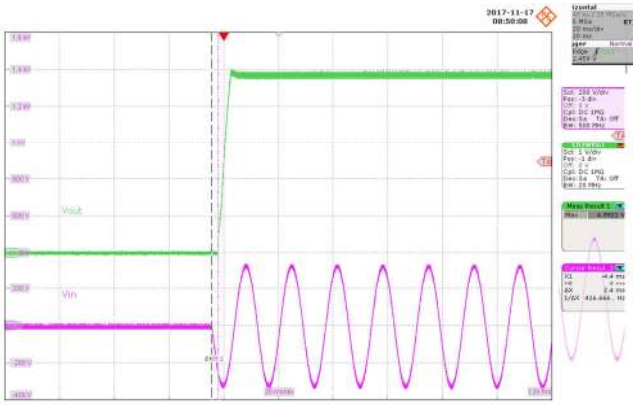

Figure 30 – 230 VAC Input, Full Load.
Upper: V_{OUT}, 2 V / div.
Lower: V_{IN}, 200 V / div., 20 ms / div.
Turn On Delay: 2.4 ms.

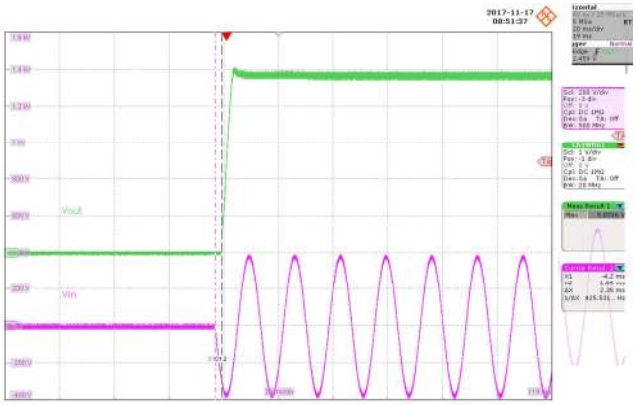

Figure 31 – 265 VAC Input, Full Load.
Upper: V_{OUT}, 2 V / div.
Lower: V_{IN}, 200 V / div., 20 ms / div.
Turn On Delay: 2.35 ms.

9.6 Output Ripple Measurements

9.6.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 µF/50 V ceramic type and one (1) 47.0 µF/16 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

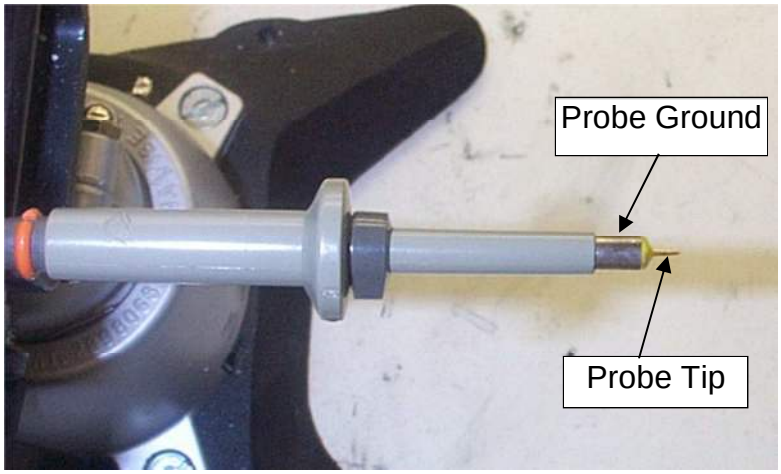

Figure 32 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 33 – Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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9.6.2 Output Ripple Measurements

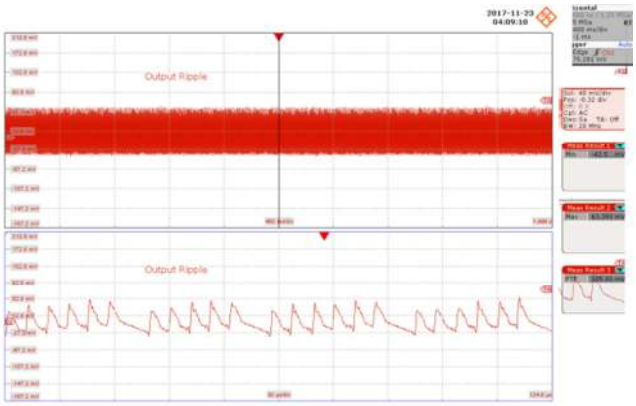

Figure 34 – 85 VAC Input, Full Load.
Upper: V_{OUT}, 40 mV / div., 400 ms / div.
Lower: $V_{OUTZOOM}$, 40 mV / div., 30 µs / div.
Output Ripple PK-PK: 105.93 mV.

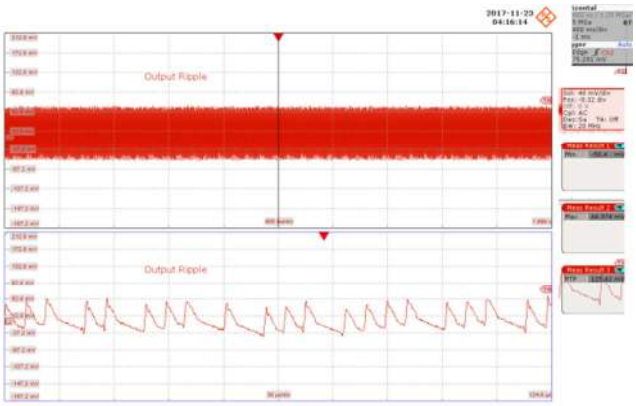

Figure 35 – 115 VAC Input, Full Load.
Upper: V_{OUT}, 40 mV / div., 400 ms / div.
Lower: $V_{OUTZOOM}$, 40 mV / div., 30 µs / div.
Output Ripple PK-PK: 115.42 mV.

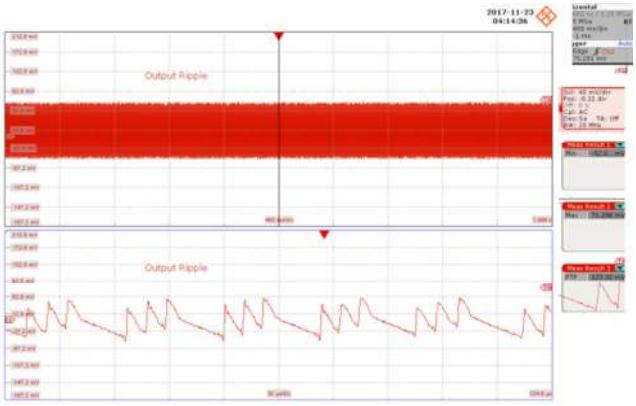

Figure 36 – 230 VAC Input, Full Load.
Upper: V_{OUT}, 40 mV / div., 400 ms / div.
Lower: $V_{OUTZOOM}$, 40 mV / div., 30 µs / div.
Output Ripple PK-PK: 123.32 mV.

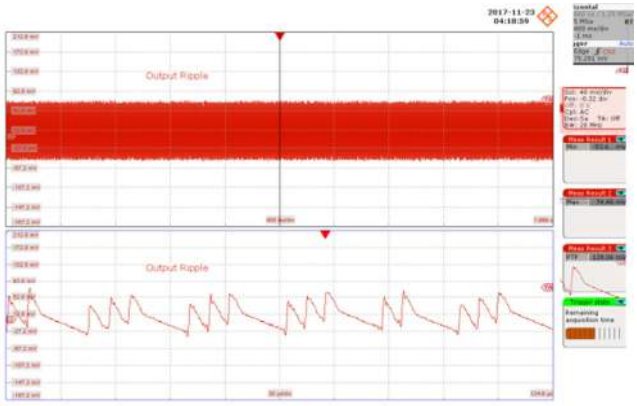

Figure 37 – 265 VAC Input, Full Load.
Upper: V_{OUT}, 40 mV / div., 400 ms / div.
Lower: $V_{OUTZOOM}$, 40 mV / div., 30 µs / div.
Output Ripple PK-PK: 128.06 mV.

10 Temperature Measurements

All measurements were taken at room temperature, full load inside an acrylic box. Unit was heat soaked for 30 minutes prior to measurement.

Input Voltage	85 VAC	265 VAC
LNK625DG	91.2	75.8
Output Diode	71.4	74.5
Transformer	69.6	65
Ambient	28	28

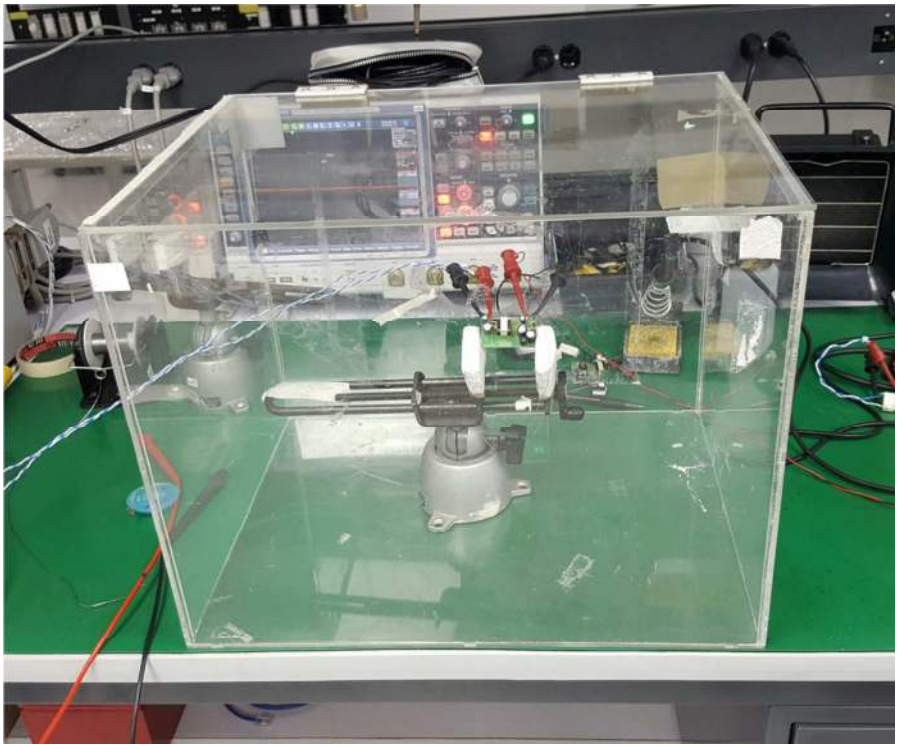

Figure 38 – Thermal Setup.

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10.1 Thermal Performance

10.1.1 Thermal Performance at 85 VAC

Ambient temperature is 28.5 ºC.

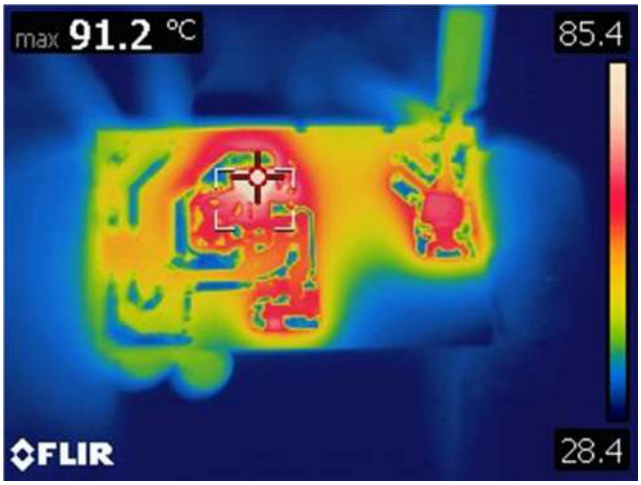

Figure 39 – U1 – LNK625DG Controller.
Spot: 91.2 ºC.

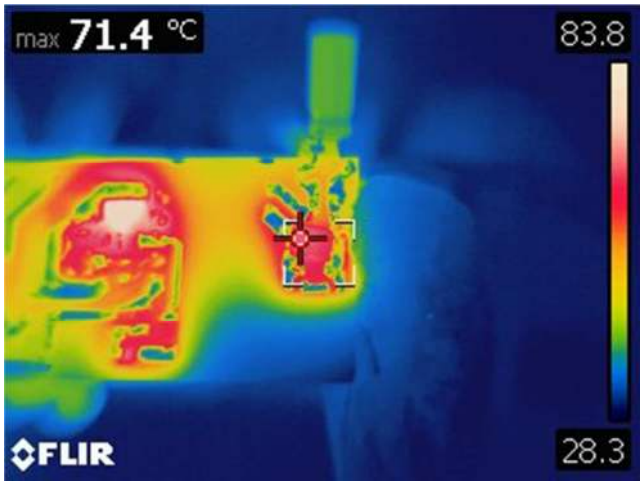

Figure 40 – D3 – Output Diode.
Spot: 71.4 ºC.

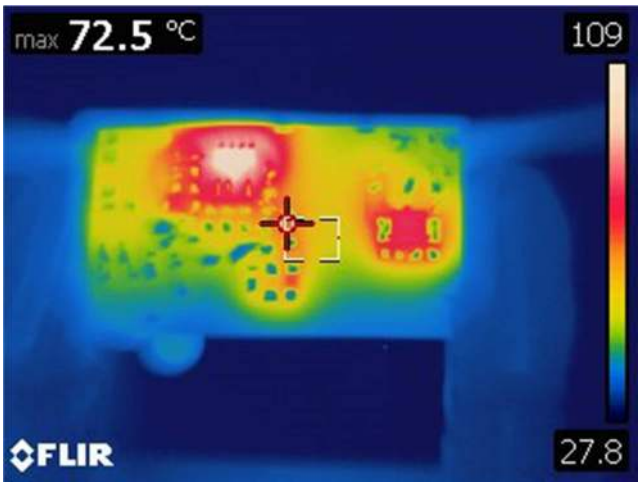

Figure 41 – D1 – Primary Snubber Diode.
Spot: 72.5 ºC.

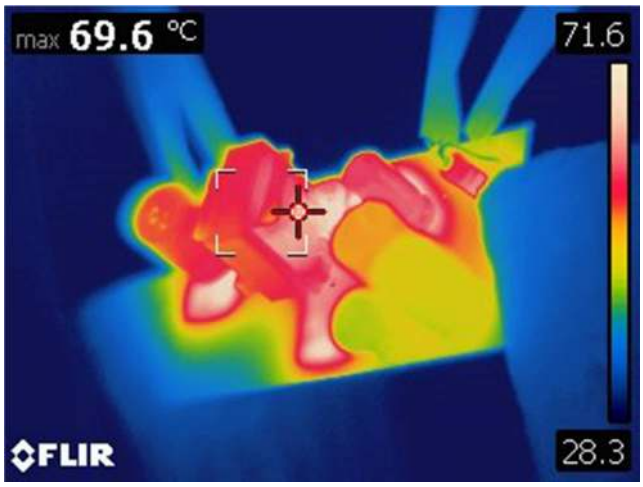

Figure 42 – T1 – Transformer.
Spot: 69.6 ºC.

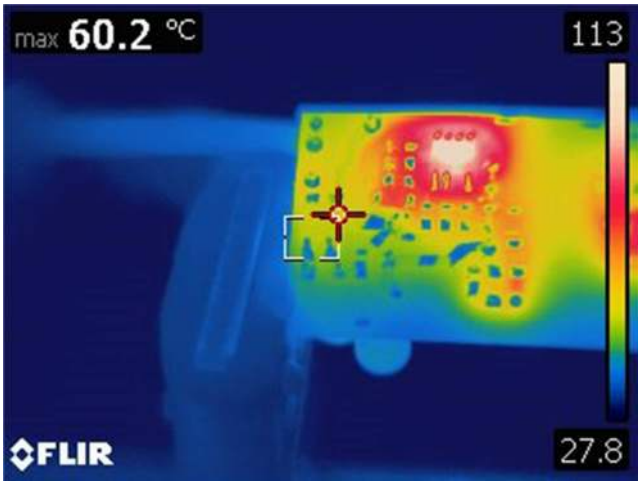

Figure 43 – BR1 – Bridge Rectifier Diode.
Spot: 60.2 ºC.

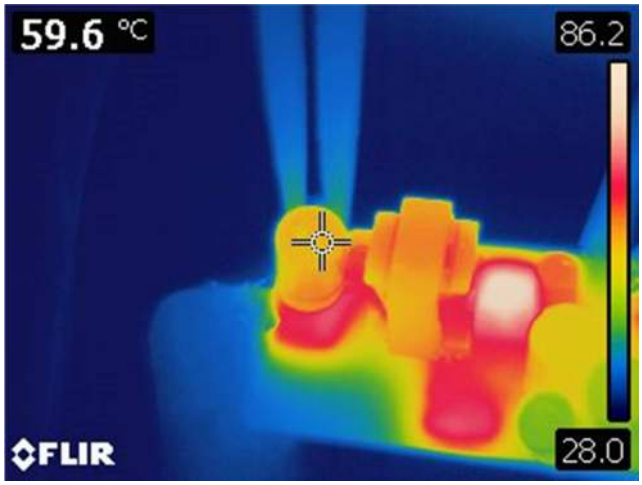

Figure 44 – C8 – Output Capacitor.
Spot: 59.6 ºC.

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10.1.2 Thermal Performance at 265 VAC

Ambient temperature is 28.5 ºC.

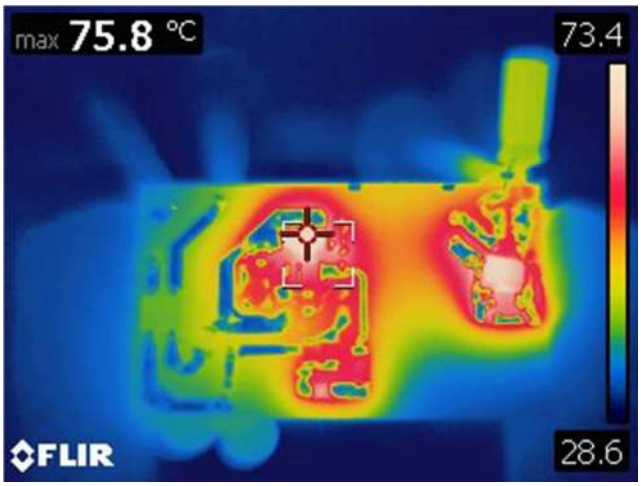

Figure 395 – U1 – LNK625DG Controller.
Spot: 75.8 ºC.

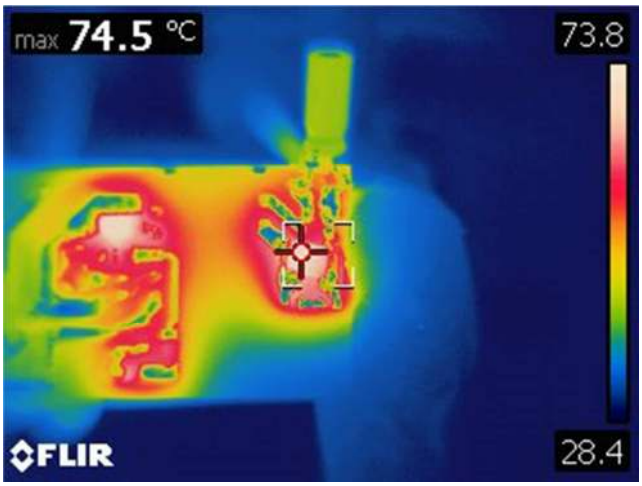

Figure 46 – D3 – Output Diode.
Spot: 74.5 ºC.

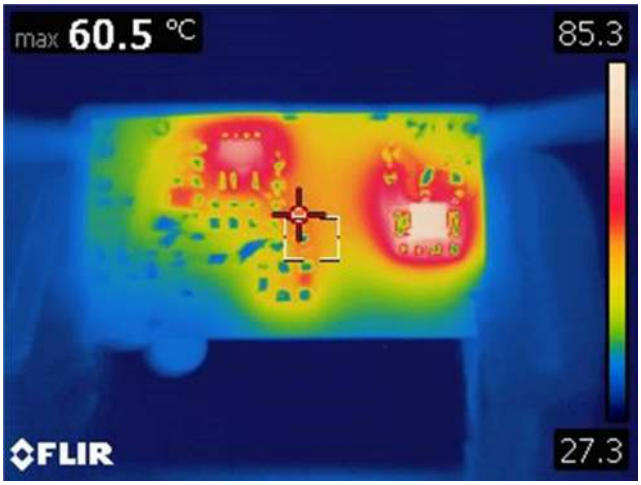

Figure 407 – D1 – Primary Snubber Diode.
Spot: 60.5 ºC.

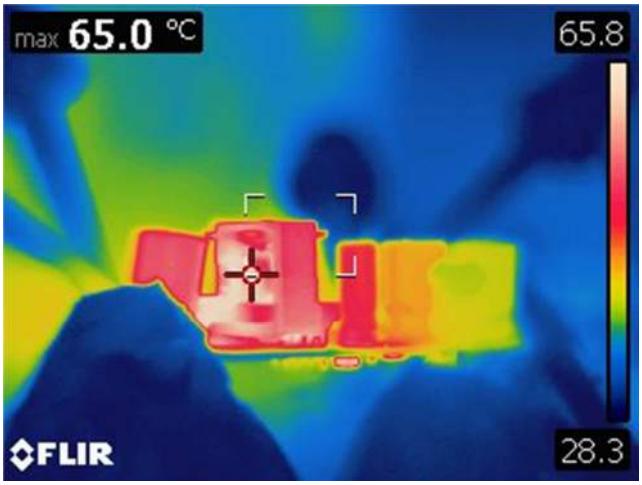

Figure 418 – T1 – Transformer.
Spot: 65ºC.

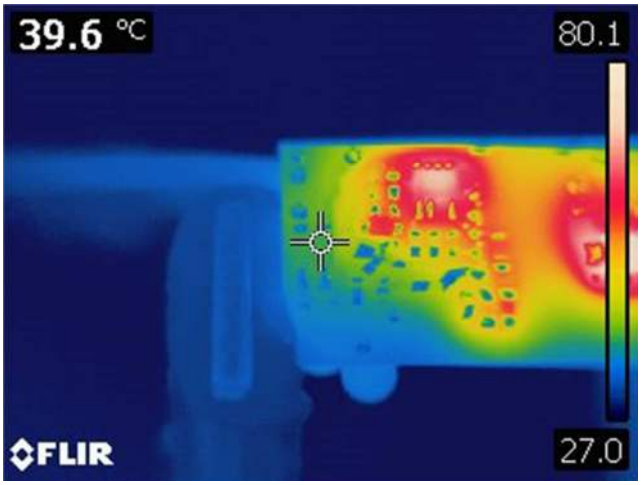

Figure 429 – BR1 – Bridge Rectifier Diode.
Spot: 39.6 ºC.

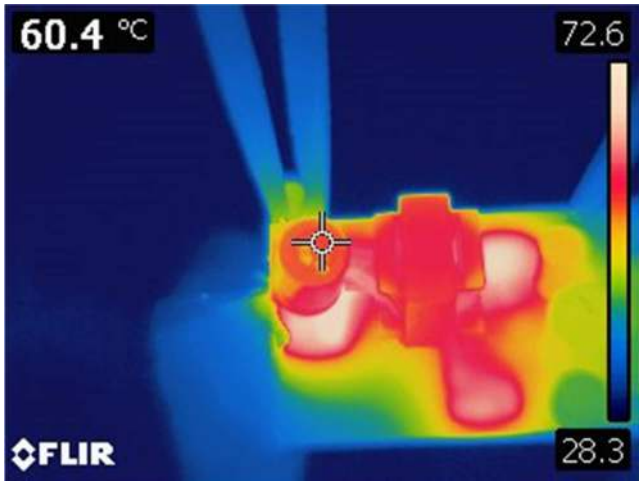

Figure 50 – C8 – Output Capacitor.
Spot: 60.4 ºC.

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10.1.3 Thermal Performance at 50 ºC

Place the test unit inside a thermal chamber. Increase chamber temperature to 50 ºC. Soak until stable. Monitor all components and ambient temperature.

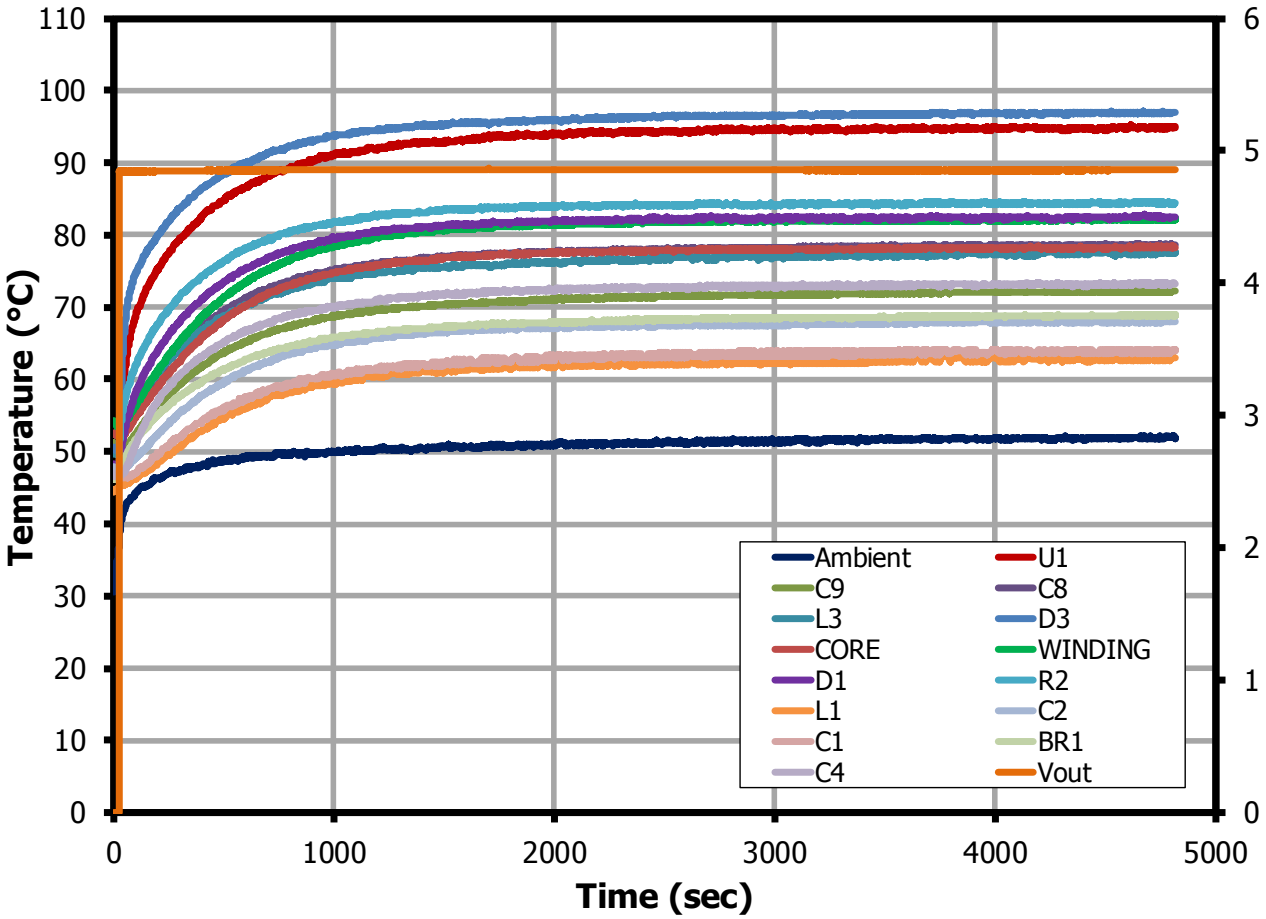
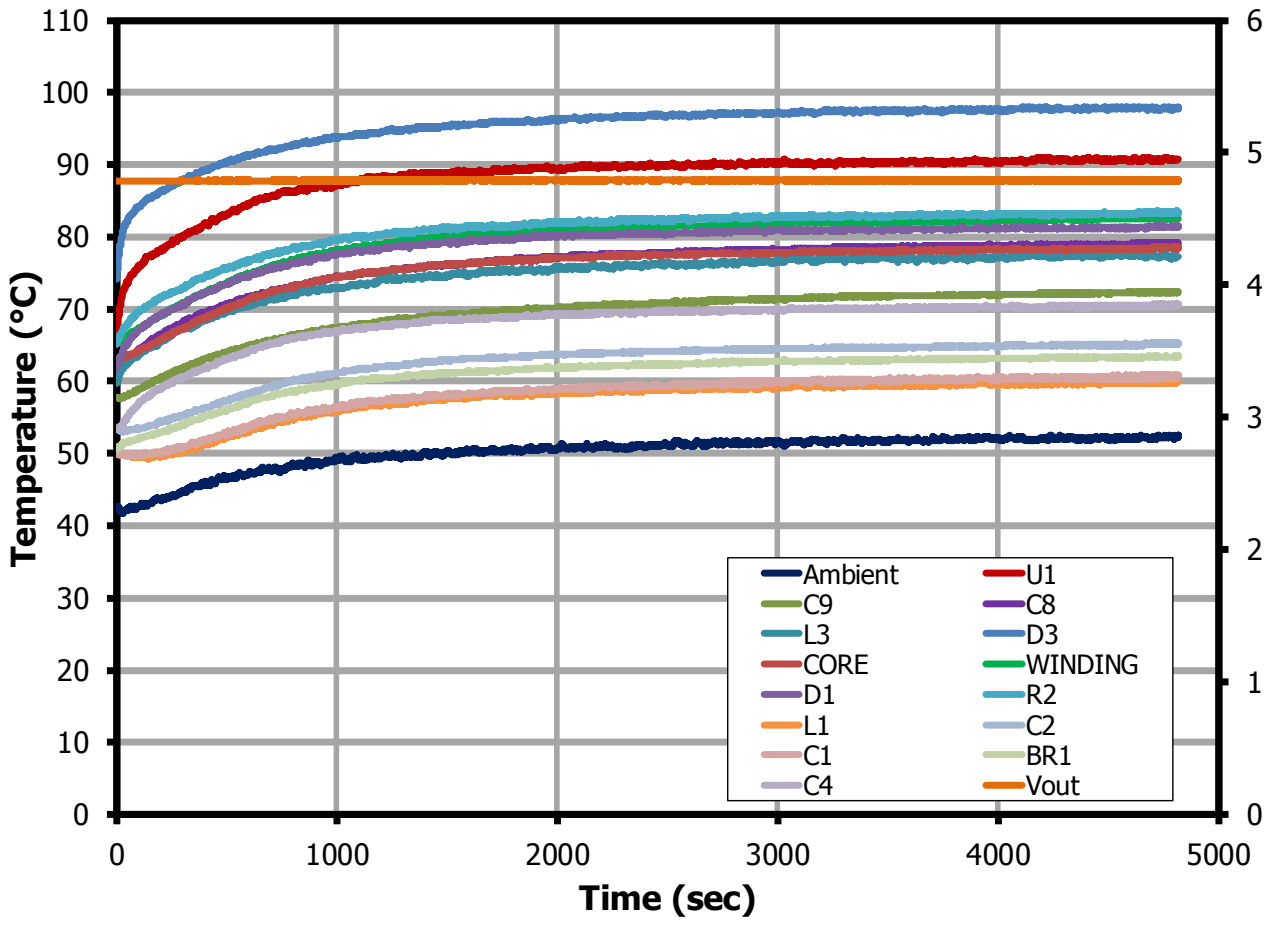


Figure 431 – 115 VAC Input, Full Load at 50 ºC Ambient.

Amb	U1	C9	C8	L3	D3	Core	Winding	D1	R2	L1	C2	C1	BR1	C4
52.2	95.2	72.3	78.8	77.9	97.1	78.4	82.3	82.8	84.7	63.2	68.2	64.2	69	73.5



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10.1.4 Thermal Performance at 40 ºC

10.1.4.1 85 VAC

Amb	U1	C9	C8	L3	D3	Core	Winding	D1	R2	L1	C2	C1	BR1	C4
43.3	106.8	64.4	71.1	71.2	90.1	72.6	76.6	78	79.2	58	64.2	60	68.2	72.6

10.1.4.2 265 VAC

Amb	U1	C9	C8	L3	D3	Core	Winding	D1	R2	L1	C2	C1	BR1	C4
43.2	84.3	64.4	71.3	69.8	90.7	70.9	74.9	73.4	75.1	51.2	56.8	52	54.6	62.6

10.2 Thermal Shutdown and Recovery

10.2.1 Shutdown and Recovery Temperature at 85 VAC, 50 ºC Ambient

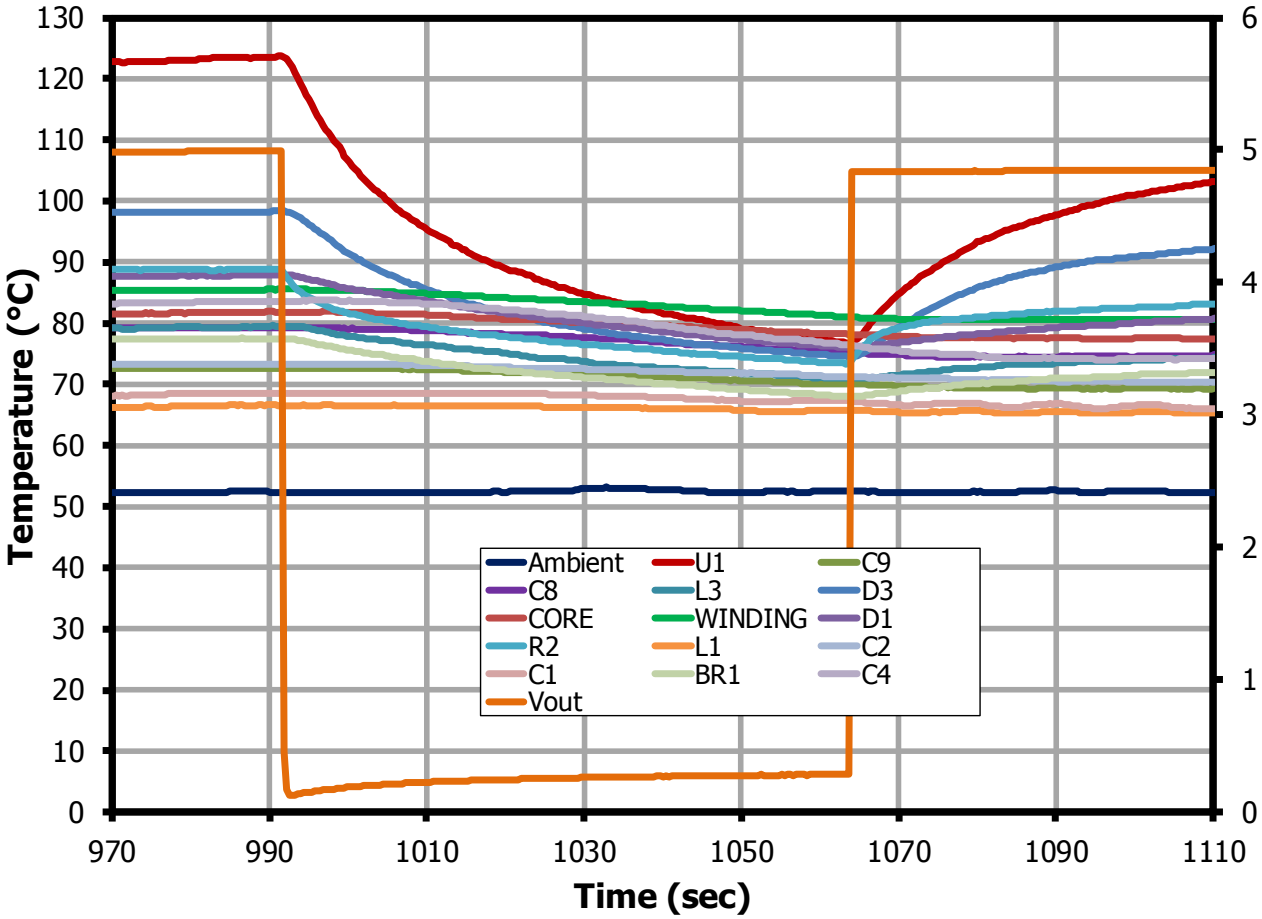

Figure 52 – 85 VAC Input.
Thermal Shutdown: U1 = 123.7 ºC.
Thermal Recovery: U1 = 76.8 ºC.

11 Conducted EMI

11.1 Test Set-up Equipment

11.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power Hi-tester.
4. Chroma measurement test fixture.
5. 5Ω resistor load.
6. Input voltage set at 115 VAC and 230 VAC.

11.2 Test Set-up

Figure 443 – EMI Set-up.

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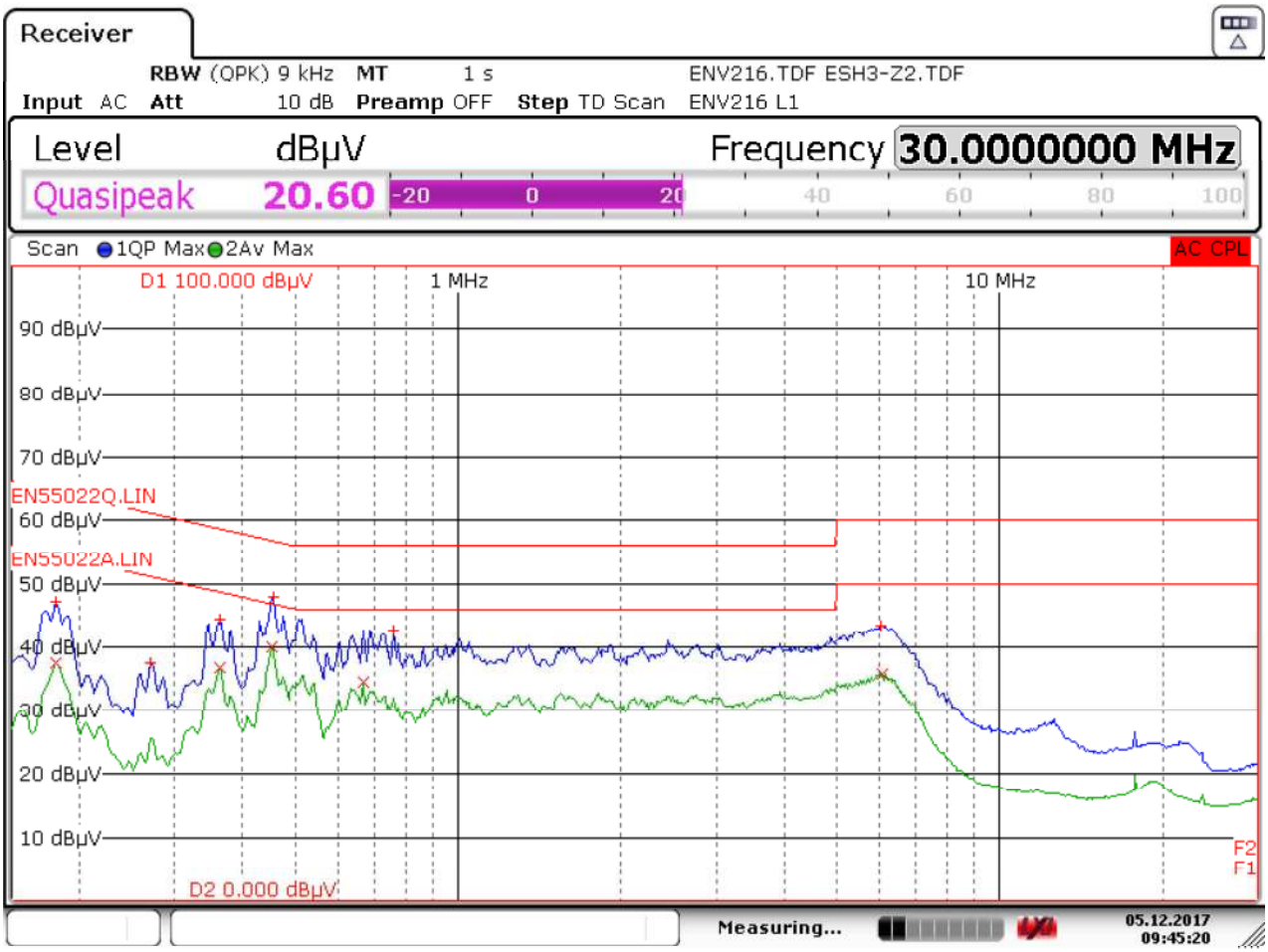
11.3 Conductive EMI with Artificial Hand Output (QP / AV)

11.3.1 115 VAC Line



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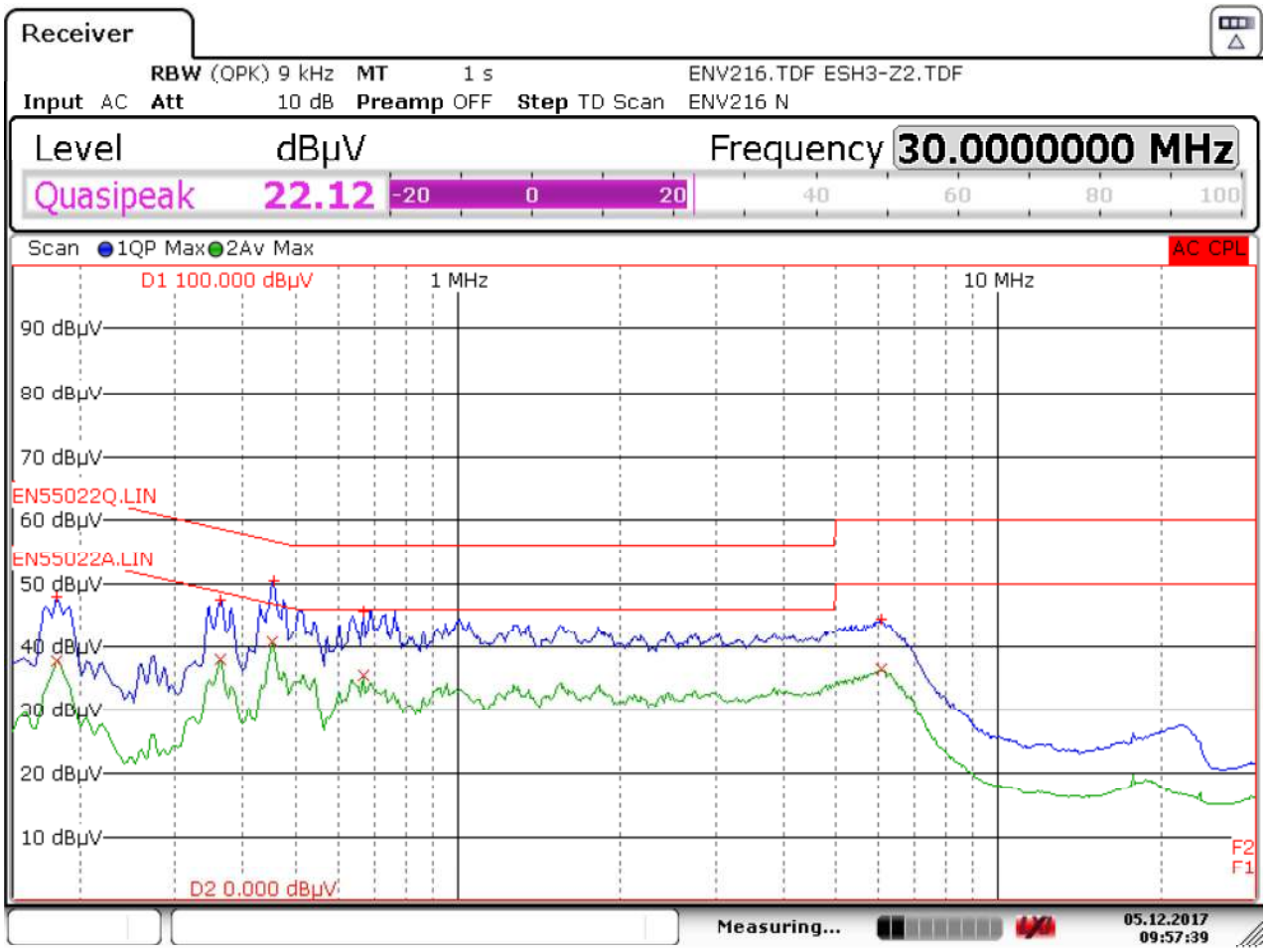
Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	453.7500 kHz	39.99 L1	-6.82 dB
1 Quasi Peak	456.0000 kHz	47.92 L1	-8.85 dB
2 Average	667.5000 kHz	34.46 L1	-11.54 dB
2 Average	363.7500 kHz	36.82 L1	-11.82 dB
1 Quasi Peak	762.0000 kHz	42.75 L1	-13.25 dB

Figure 54 – AH Connected to the Negative Output, Line.

11.3.2 115 VAC Neutral



Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	453.7500 kHz	40.79 N	-6.02 dB
1 Quasi Peak	456.0000 kHz	50.32 N	-6.45 dB
1 Quasi Peak	669.7500 kHz	45.64 N	-10.36 dB
2 Average	363.7500 kHz	38.08 N	-10.56 dB
2 Average	667.5000 kHz	35.40 N	-10.60 dB

Figure 455 – AH Connected to the Negative Output, Neutral.

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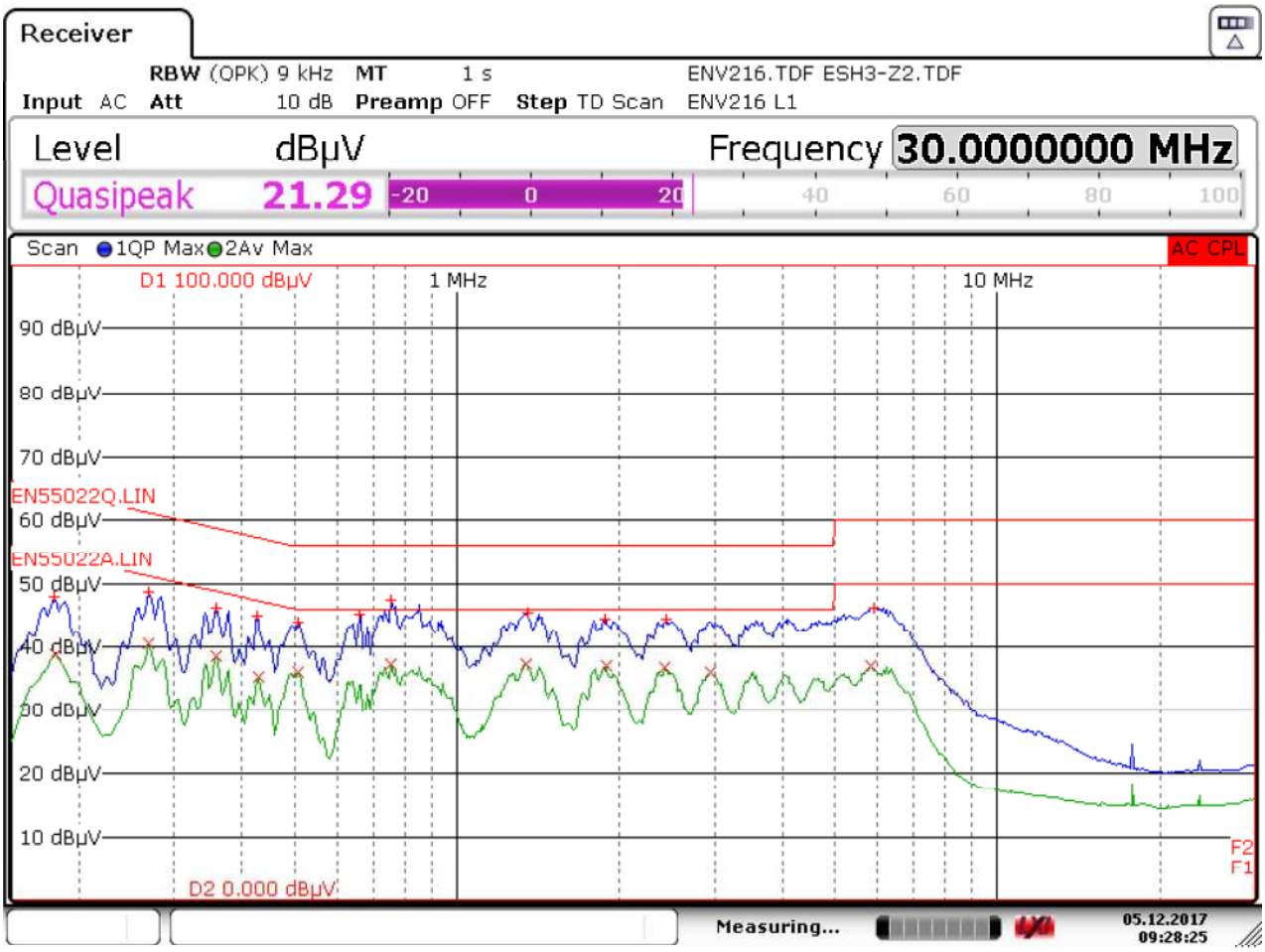
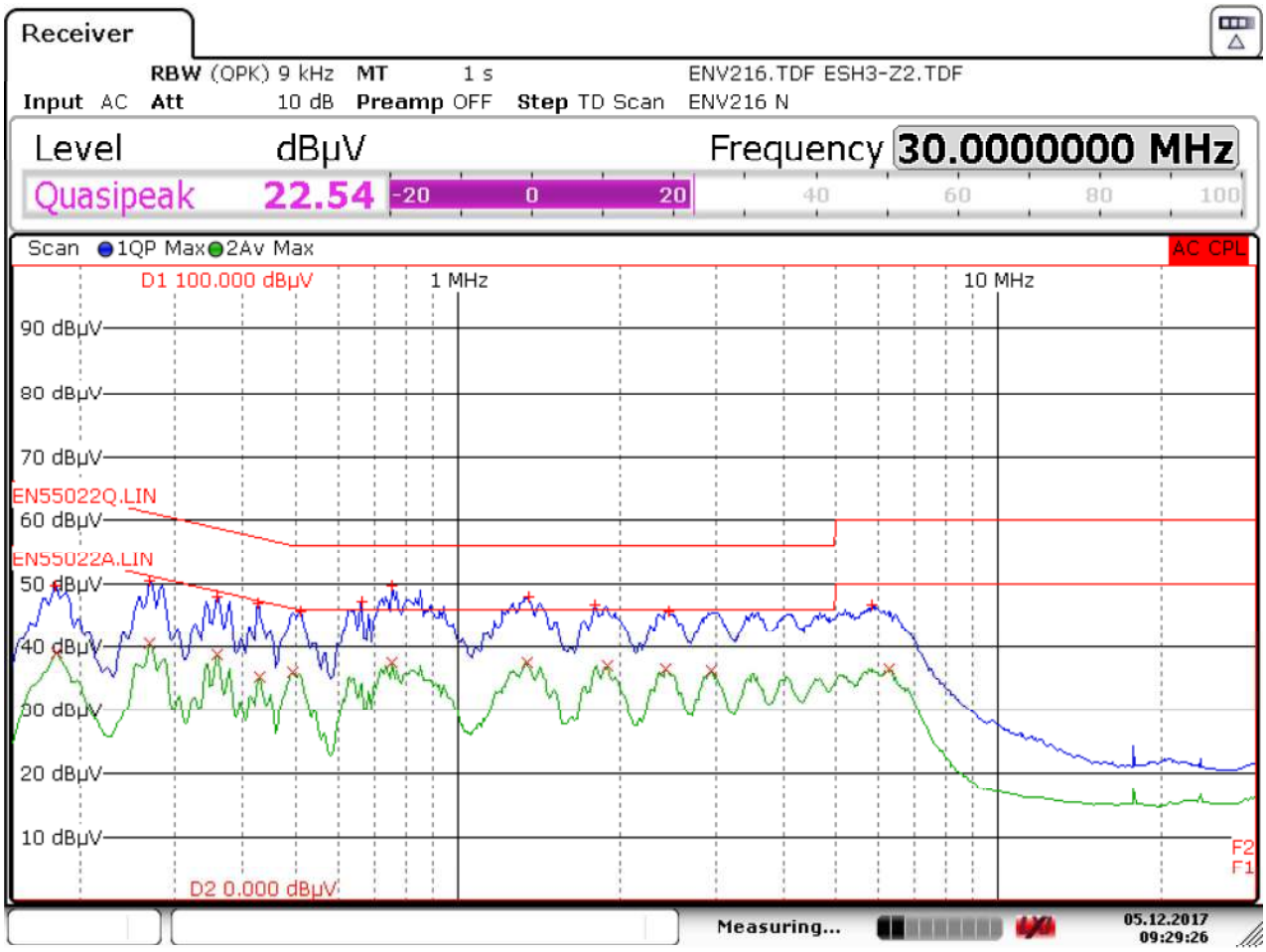
11.3.3 230 VAC Line



Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	753.0000 kHz	47.49 L1	-8.51 dB
2 Average	753.0000 kHz	37.33 L1	-8.67 dB
2 Average	1.3403 MHz	37.33 L1	-8.67 dB
2 Average	1.8960 MHz	36.97 L1	-9.03 dB
2 Average	2.4315 MHz	36.63 L1	-9.37 dB

Figure 56 – AH Connected to the Negative Output, Line.

11.3.4 230 VAC Neutral



Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	755.2500 kHz	49.60 N	-6.40 dB
1 Quasi Peak	1.3515 MHz	47.96 N	-8.04 dB
2 Average	1.3425 MHz	37.59 N	-8.41 dB
2 Average	755.2500 kHz	37.49 N	-8.51 dB
1 Quasi Peak	663.0000 kHz	47.26 N	-8.74 dB

Figure 57 – AH Connected to the Negative Output, Neutral.

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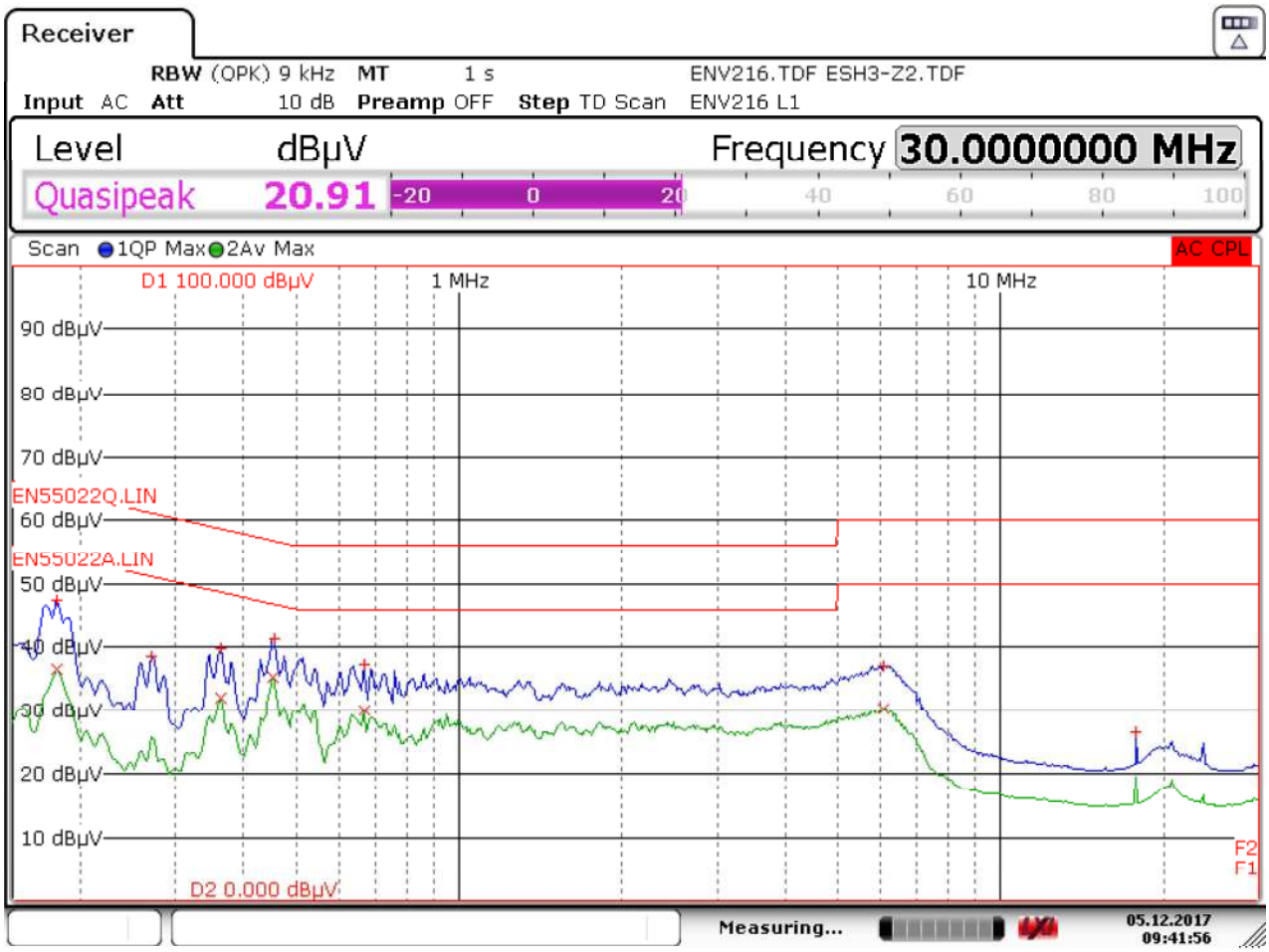
11.4 Conductive EMI with Floating Output (QP / AV)

11.4.1 115 VAC Line



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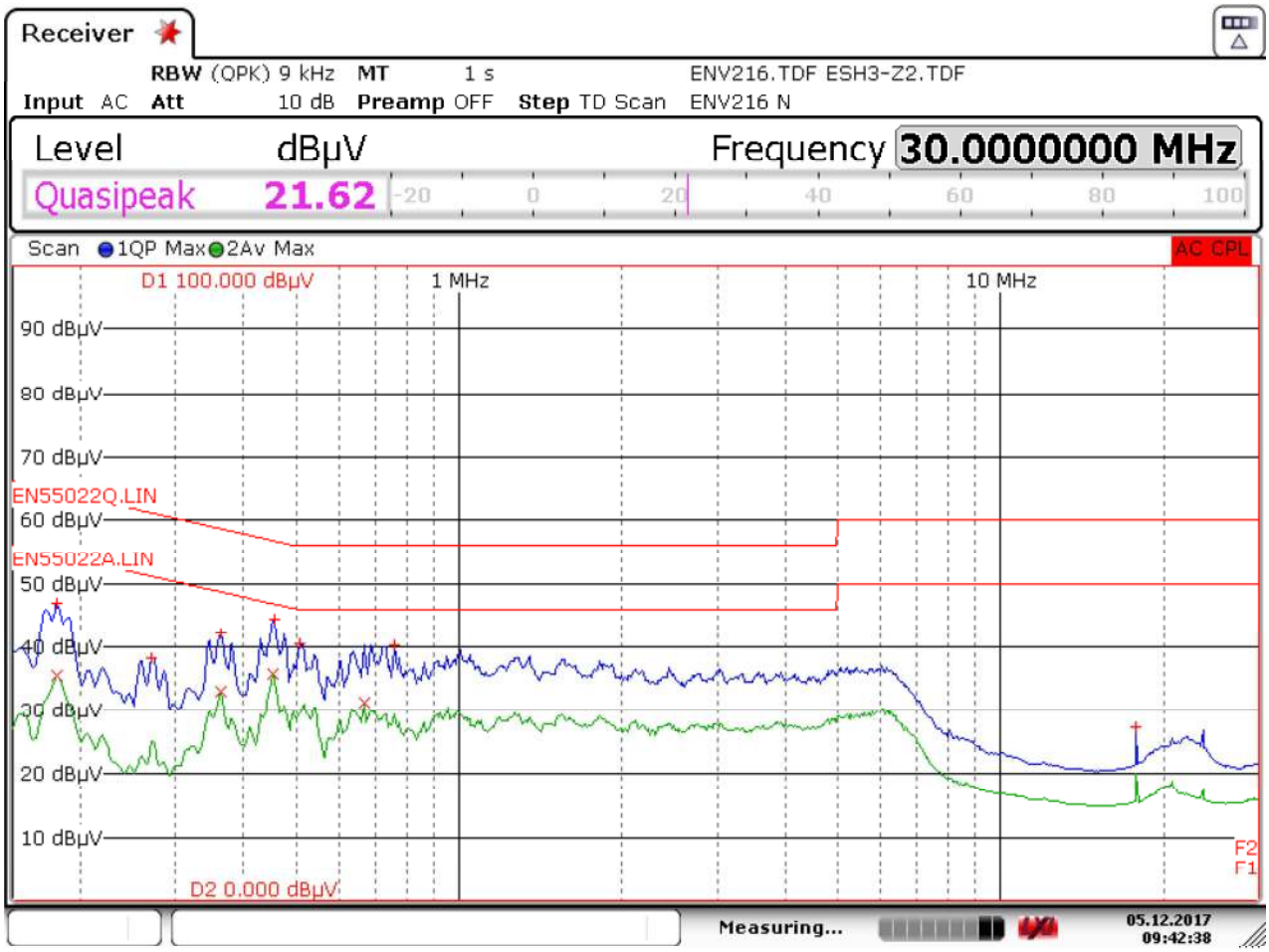
Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	453.7500 kHz	35.29 L1	-11.52 dB
1 Quasi Peak	456.0000 kHz	41.22 L1	-15.55 dB
2 Average	667.5000 kHz	30.13 L1	-15.87 dB
2 Average	363.7500 kHz	32.10 L1	-16.54 dB
1 Quasi Peak	181.5000 kHz	47.44 L1	-16.98 dB

Figure 58 – Floating Output, Line.

11.4.2 115 VAC Neutral



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Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	453.7500 kHz	35.78 N	-11.03 dB
1 Quasi Peak	456.0000 kHz	44.46 N	-12.31 dB
2 Average	667.5000 kHz	31.22 N	-14.78 dB
1 Quasi Peak	510.0000 kHz	40.49 N	-15.51 dB
1 Quasi Peak	762.0000 kHz	40.31 N	-15.69 dB

Figure 59 – Floating Output, Neutral.

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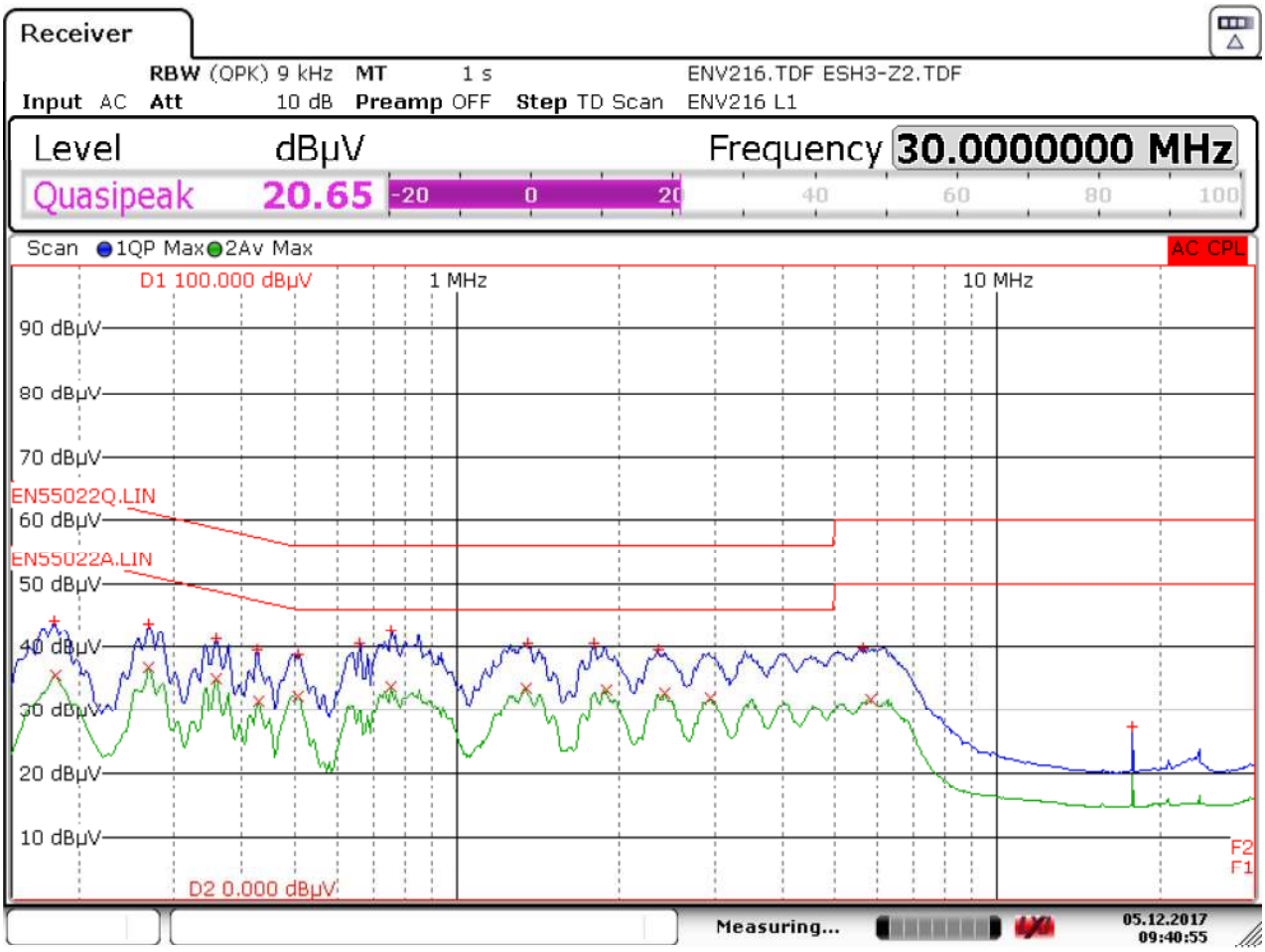
11.4.3 230 VAC Line



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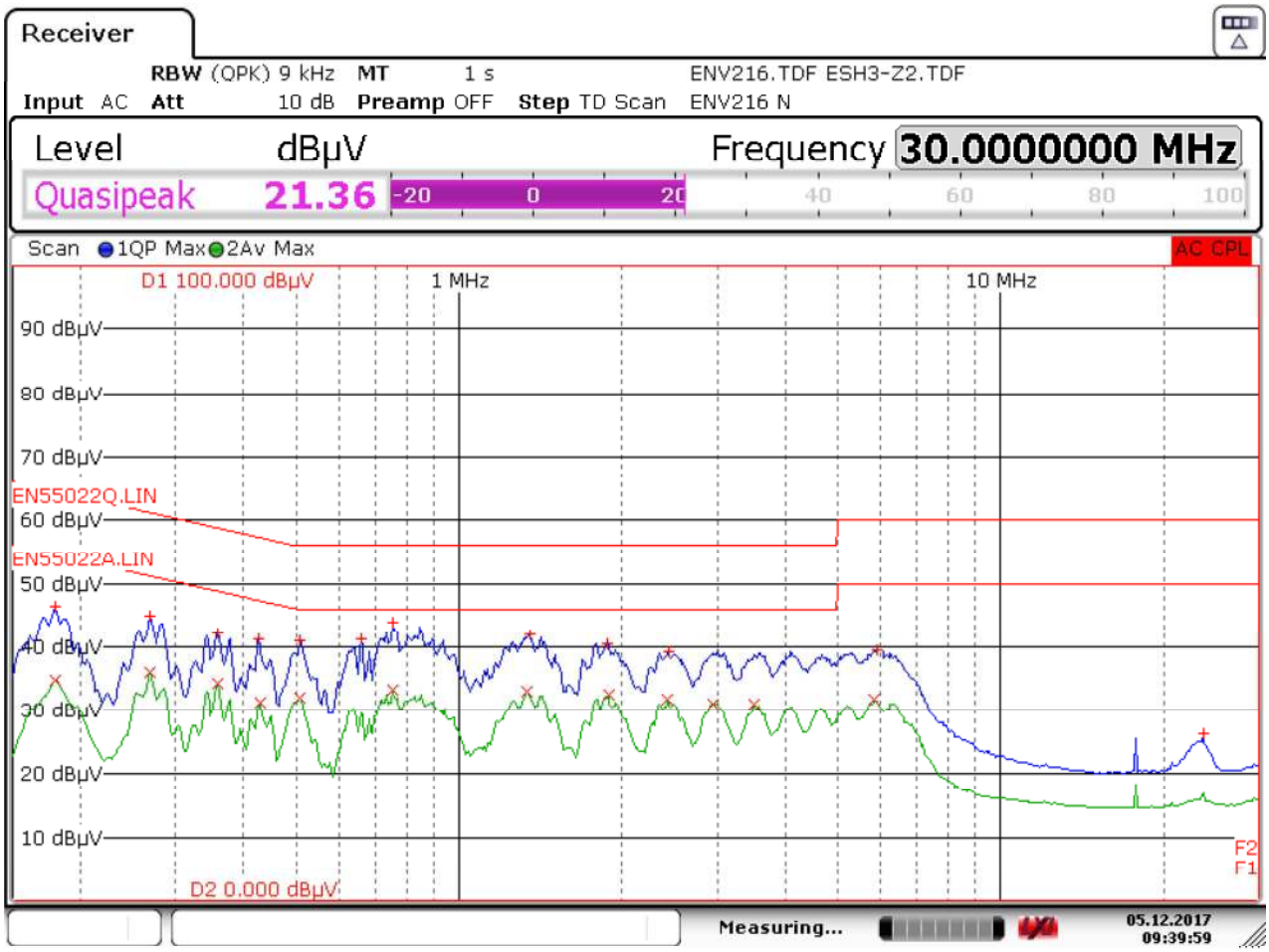
Trace/Detector	Frequency	Level dBµV	DeltaLimit
2 Average	755.2500 kHz	33.68 L1	-12.32 dB
2 Average	1.3403 MHz	33.61 L1	-12.39 dB
2 Average	1.8960 MHz	33.25 L1	-12.75 dB
2 Average	2.4315 MHz	32.74 L1	-13.26 dB
1 Quasi Peak	755.2500 kHz	42.63 L1	-13.37 dB

Figure 60 – Floating Output, Line.

11.4.4 230 VAC Neutral



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Trace/Detector	Frequency	Level dBµV	DeltaLimit
1 Quasi Peak	753.0000 kHz	43.84 N	-12.16 dB
2 Average	753.0000 kHz	33.19 N	-12.81 dB
2 Average	1.3380 MHz	33.00 N	-13.00 dB
2 Average	1.8938 MHz	32.49 N	-13.51 dB
2 Average	510.0000 kHz	32.10 N	-13.90 dB

Figure 61 – Floating Output, Neutral.

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12 Revision History

Date	Author	Revision	Description and Changes	Reviewed
22-Jan-18	MAGM	1.0	Initial Release.	Mktg and Apps
13-Feb-18	KM	1.1	Updated PCB Images.	Mktg and Apps
14-Feb-18	MAGM	1.2	Updated Waveforms.	Mktg and Apps
08-Apr-19	KM	1.3	Updated Errors in Section 7.4 and 7.5.	Mktg and Apps
23-Jun-20	KM	1.4	Converted to RDR.	Mktg and Apps
15-Jul-20	KM	1.5	Added T1 Supplier.	Mktg and Apps

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