# **N-Channel Power MOSFET** 600 V, 900 m $\Omega$

#### **Features**

- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS

## ABSOLUTE MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	600	V
Gate-to-Source Vo	ltage		$V_{GS}$	±25	V
Continuous Drain	Steady	T <sub>C</sub> = 25°C	I <sub>D</sub>	5.7	Α
Current R <sub>0JC</sub>	State	T <sub>C</sub> = 100°C		3.6	
Power Dissipation - R <sub>0</sub> JC	Steady T <sub>C</sub> = 25°C		P <sub>D</sub>	74	W
Pulsed Drain Current	t <sub>p</sub>	= 10 μs	I <sub>DM</sub>	20	Α
Operating Junction and Storage Temperature			T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C
Source Current (Body Diode)			IS	5.7	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>D</sub> = 2 A)			EAS	33	mJ
Peak Diode Recovery (Note 1)			dv/dt	15	V/ns
Lead Temperature for Soldering Leads			$T_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1.  $I_{SD} < 5.7$  A, di/dt  $\leq$  400 A/ $\mu$ s,  $V_{peak} < V_{(BR)DSS}$ 

### THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDD60N900U1	$R_{ heta JC}$	1.7	°C/W
Junction-to-Ambient Steady State           (Note 3)         NDD60N900U1           (Note 2)         NDD60N900U1-1           (Note 2)         NDD60N900U1-35	$R_{ hetaJA}$	47 99 95	°C/W

- 2. Insertion mounted
- 3. Surface mounted on FR4 board using 1" sq. pad size (Cu area = 1.127 in sq [2 oz] including traces)

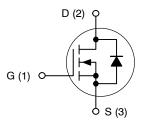


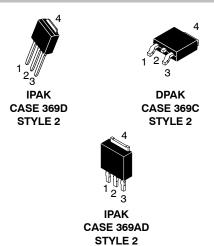
## ON Semiconductor®

### http://onsemi.com

V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX		
600 V	900 mΩ @ 10 V		

#### **N-Channel MOSFET**





#### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

## **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 r	mA	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>				550		mV/°C
Drain-to-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	T <sub>J</sub> = 25°C			1	μΑ
			T <sub>J</sub> = 125°C			100	1
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V	•			±100	nA
ON CHARACTERISTICS (Note 4)			-				
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{DS} = V_{GS}, I_{D} = 250$	Αμ Ο	2	3.2	4	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	Reference to 25°C, I <sub>D</sub> =	: 250 μA		7.2		mV/°C
Static Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.	5 A		820	900	mΩ
Forward Transconductance	9FS	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 2.	5 A		4.3		S
DYNAMIC CHARACTERISTICS			-				
Input Capacitance	C <sub>iss</sub>				360		pF
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f$	= 1 MHz		23		1
Reverse Transfer Capacitance	C <sub>rss</sub>	50 7 40			1.1		1
Effective output capacitance, energy related (Note 6)	C <sub>o(er)</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 0 to 480 V			17		]
Effective output capacitance, time related (Note 7)	C <sub>o(tr)</sub>	$I_D$ = constant, $V_{GS}$ = 0 V, $V_{DS}$ = 0 to 480 V			57		]
Total Gate Charge	$Q_{g}$				12		nC
Gate-to-Source Charge	$Q_{gs}$				2.5		1
Gate-to-Drain ("Miller") Charge	Q <sub>gd</sub>	$V_{DS} = 300 \text{ V}, I_D = 5.9 \text{ A}, V_{DS} = 5.9 \text{ A}$	' <sub>GS</sub> = 10 V		5.8		1
Plateau Voltage	$V_{GP}$				5.4		V
Gate Resistance	$R_{g}$				5		Ω
RESISTIVE SWITCHING CHARACTER	ISTICS (Note 5)		•		•	•	
Turn-on Delay Time	t <sub>d(on)</sub>				7		ns
Rise Time	t <sub>r</sub>	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 5.	9 A.		9		1
Turn-off Delay Time	t <sub>d(off)</sub>	$V_{\rm DD} = 300 \text{ V}, \text{ ip} = 5.9 \text{ A}, \\ V_{\rm GS} = 10 \text{ V}, \text{ R}_{\rm G} = 0 \Omega$			17		1
Fall Time	t <sub>f</sub>				6		1
SOURCE-DRAIN DIODE CHARACTER			<u>'</u>		-	-	
Diode Forward Voltage	$V_{SD}$	$I_S = 5.7 \text{ A}, V_{GS} = 0 \text{ V}$ $T_J = 25^{\circ}\text{C}$ $T_J = 100^{\circ}\text{C}$			0.88	1.3	V
					0.80		1
Reverse Recovery Time	t <sub>rr</sub>	$V_{GS} = 0 \text{ V}, V_{DD} = 30 \text{ V}$ $I_{S} = 5.9 \text{ A}, d_{i}/d_{t} = 100 \text{ A}/\mu\text{s}$			270		ns
Charge Time	ta				130		1
Discharge Time	t <sub>b</sub>				140		1
Reverse Recovery Charge	Q <sub>rr</sub>				1.8	<u> </u>	μС

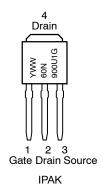
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

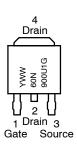
4. Pulse Width  $\leq 300~\mu$ s, Duty Cycle  $\leq 2\%$ .

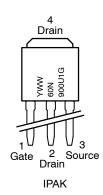
5. Switching characteristics are independent of operating junction temperatures.

6.  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{(BR)DSS}$ 7.  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{(BR)DSS}$ 

## **MARKING DIAGRAMS**







Y = Year WW = Work Week G = Pb-Free Package

DPAK

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
NDD60N900U1-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N900U1-35G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD60N900U1T4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## **TYPICAL CHARACTERISTICS**

ID, DRAIN CURRENT (A)

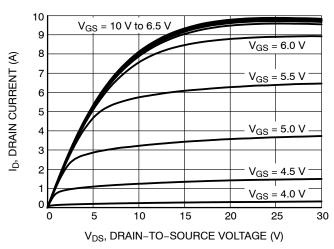
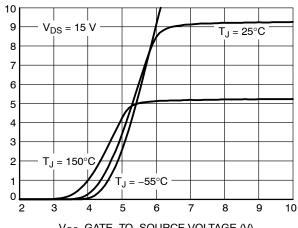


Figure 1. On-Region Characteristics



V<sub>GS</sub>, GATE-TO-SOURCE VOLTAGE (V) Figure 2. Transfer Characteristics

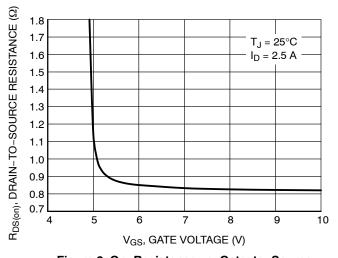


Figure 3. On-Resistance vs. Gate-to-Source Voltage

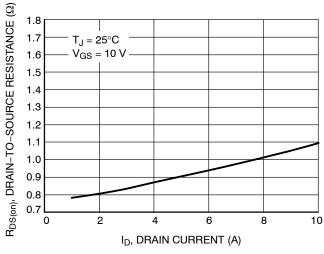


Figure 4. On–Resistance vs. Drain Current and

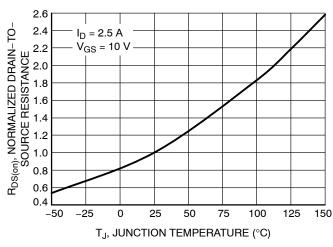


Figure 5. On–Resistance Variation with Temperature

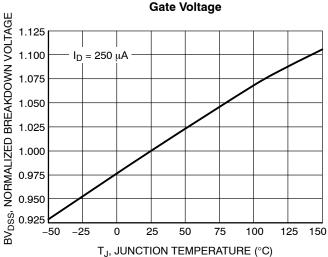
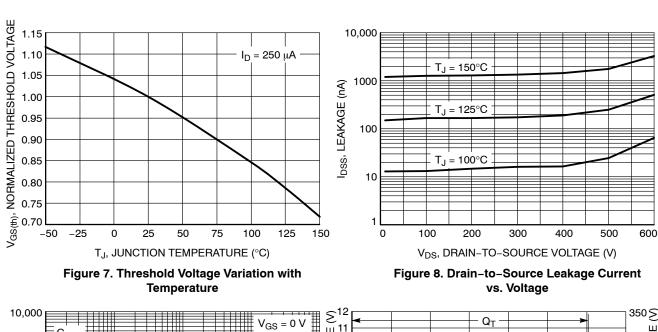


Figure 6. Breakdown Voltage Variation with Temperature

#### TYPICAL CHARACTERISTICS



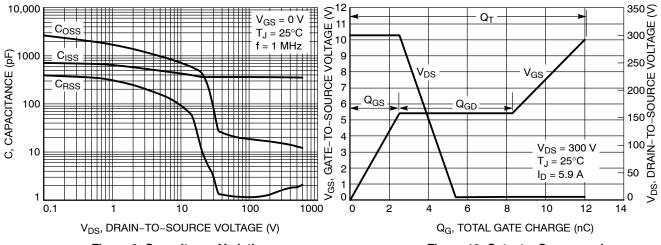


Figure 9. Capacitance Variation

Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

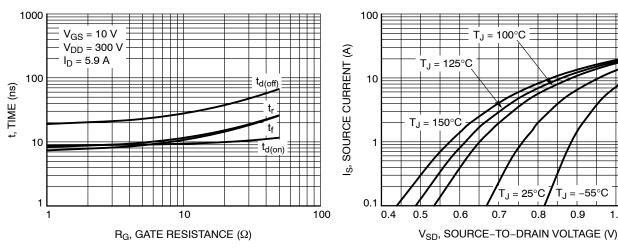


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

Figure 12. Diode Forward Voltage vs. Current

1.0

1.1

## **TYPICAL CHARACTERISTICS**

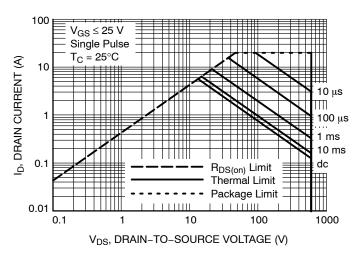


Figure 13. Maximum Rated Forward Biased **Safe Operating Area** 

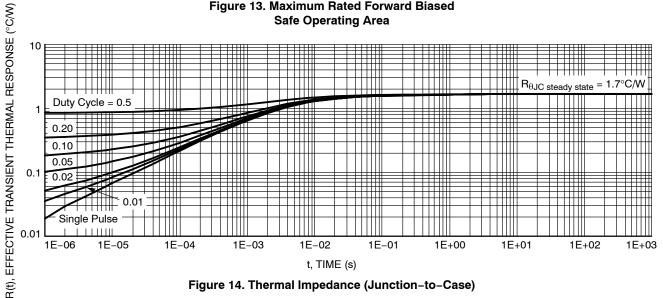
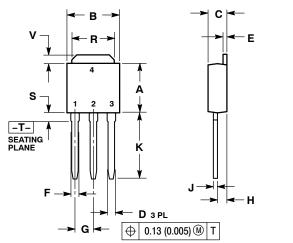
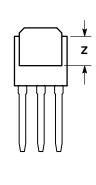


Figure 14. Thermal Impedance (Junction-to-Case)

### **PACKAGE DIMENSIONS**

**IPAK** CASE 369D-01 ISSUE C





#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIN	IETERS
DIM	MIN	MAX	MIN	MAX
Α	0.235	0.245	5.97	6.35
В	0.250	0.265	6.35	6.73
С	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
Е	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29 BSC	
Н	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
Κ	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
٧	0.035	0.050	0.89	1.27
Z	0.155		3.93	

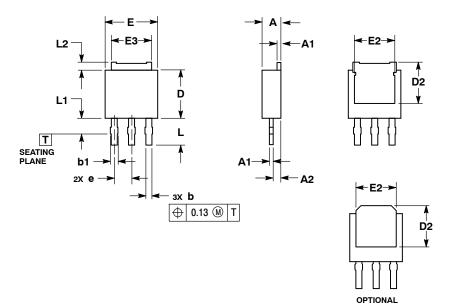
## STYLE 2:

PIN 1. GATE 2. DRAIN

- 3. SOURCE 4. DRAIN

## 3.5 MM IPAK, STRAIGHT LEAD

CASE 369AD **ISSUE B** 



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
  4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

	MILLIMETERS			
DIM	MIN	MAX		
Α	2.19	2.38		
A1	0.46	0.60		
A2	0.87	1.10		
b	0.69	0.89		
b1	0.77	1.10		
D	5.97	6.22		
D2	4.80			
Е	6.35	6.73		
E2	4.57	5.45		
E3	4.45	5.46		
е	2.28	BSC		
L	3.40	3.60		
L1	-	2.10		
L2	0.89	1.27		
L L1	3.40	3.60 2.10		

STYLE 2: PIN 1. GATE

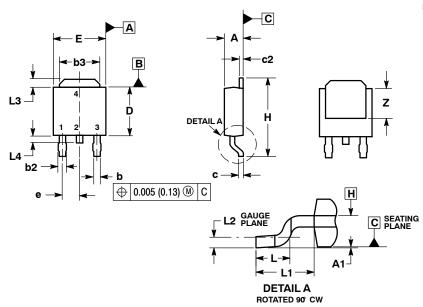
- 2. DRAIN 3. SOURCE
- 4. DRAIN

CONSTRUCTION

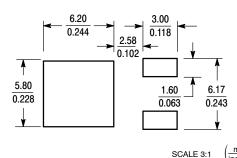
#### PACKAGE DIMENSIONS

## **DPAK (SINGLE GAUGE)**

CASE 369C ISSUE D



#### **SOLDERING FOOTPRINT\***



Mounting Techniques Reference Manual, SOLDERRM/D.

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14 5M 1994
- 2. CONTROLLING DIMENSION: INCHES.
- 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-MENSIONS b3, L3 and Z.
- 4. DIMENSIONS DAND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

	INCHES		MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.086	0.094	2.18	2.38	
A1	0.000	0.005	0.00	0.13	
b	0.025	0.035	0.63	0.89	
b2	0.030	0.045	0.76	1.14	
b3	0.180	0.215	4.57	5.46	
С	0.018	0.024	0.46	0.61	
c2	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
Е	0.250	0.265	6.35	6.73	
е	0.090	BSC	2.29 BSC		
Н	0.370	0.410	9.40	10.41	
L	0.055	0.070	1.40	1.78	
L1	0.108 REF		2.74 REF		
L2	0.020 BSC		0.51 BSC		
L3	0.035	0.050	0.89	1.27	
L4		0.040		1.01	
Z	0.155		3.93		

STYLE 2:

PIN 1. GATE 2. DRAIN 3. SOURCE

4. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and

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