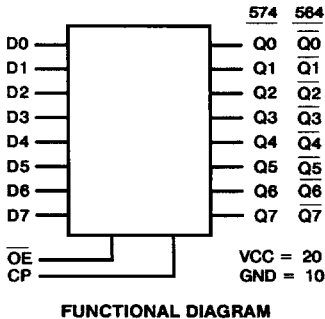


## CD54/74FCT564, CD54/74FCT564AT CD54/74FCT574, CD54/74FCT574AT

July 1990



### Octal D-Type Flip-Flops, 3-State

#### Positive-Edge Triggered

CD54/74FCT564, CD54/74FCT564AT - Inverting

CD54/74FCT574, CD54/74FCT574AT - Non-Inverting

#### Type Features:

- Buffered inputs
- Typical propagation delay:  
5.6ns @ VCC = 5V, TA = +25°C, CL = 50pF (FCT574AT)

The CD54/74FCT564, 564AT, 574, and 574AT octal D-type, 3-state, positive-edge triggered flip-flops use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The eight flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable (OE) controls the 3-state outputs and is independent of the register operation. When the Output Enable (OE) is HIGH, the outputs are in the high-impedance state. The CD54/74FCT564, 564AT and CD54/74FCT574, 574AT share the same configurations; the CD54/74FCT564, 564AT however, have inverted outputs and the CD54/74FCT574, 574AT have non-inverted outputs.

The CD54/74FCT564, 564AT, 574 and 574AT are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT564 and 574 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

#### Family Features:

- SCR-latchup-resistant BiCMOS process and circuit design
- FCTXXX Types - Speed of bipolar FAST\*/AS/S;
- FCTXXXAT Types - 30% faster than FAST/AS/S with significantly reduced power consumption
- 48/32-mA output sink current (commercial/extended industrial)
- Output voltage swing limited to 3.7V @ VCC = 5V
- Controlled output-edge rates
- Input/output isolation to VCC
- BiCMOS technology with low quiescent power

\* FAST is a registered trademark of Fairchild Semiconductor Corp.

#### TRUTH TABLE

INPUTS			OUTPUTS	
			564, 564AT	574, 574AT
OE	CP	Dn	Qn	Qn
L		H	L	H
L		L	H	L
L	L	X	Qo	Qo
H	X	X	Z	Z

H = High level (steady state)

L = Low level (steady state)

X = Don't care

= Transition from low to high level.

Qo = The level of Q before the indicated steady-state input conditions were established.

Qo = The level of Q before the indicated steady-state input conditions were established.

Z = HIGH Impedance

**MAXIMUM RATINGS, Absolute-Maximum Values:**

DC SUPPLY-VOLTAGE (VCC)	-0.5V to 6V
DC INPUT DIODE CURRENT, I <sub>IK</sub> (for V <sub>I</sub> < -0.5V)	-20mA
DC OUTPUT DIODE CURRENT, I <sub>OK</sub> (for V <sub>O</sub> < -0.5V)	-50mA
DC OUTPUT SINK CURRENT per Output Pin, I <sub>O</sub>	+70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I <sub>O</sub>	-30mA
DC VCC CURRENT (I <sub>CC</sub> )	140mA
DC GROUND CURRENT (I <sub>GND</sub> )	400mA
<b>POWER DISSIPATION PER PACKAGE (PD):</b>	
For TA = -55°C to +100°C (PACKAGE TYPE E)	500mW
For TA = +100°C to +125°C (PACKAGE TYPE E)	Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M)	400mW
For TA = +70°C to +125°C (PACKAGE TYPE M)	Derate Linearly at 8mW/°C to 70mW
<b>OPERATING-TEMPERATURE RANGE (TA):</b>	
PACKAGE TYPE E, M	-55°C to +125°C
STORAGE TEMPERATURE (T <sub>stg</sub> )	-65°C to +150°C
<b>LEAD TEMPERATURE (DURING SOLDERING):</b>	
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum	+265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only	+300°C

**RECOMMENDED OPERATING CONDITIONS:**

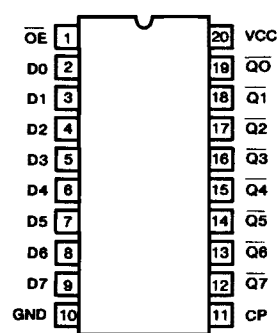
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC	LIMITS		UNITS
	MIN	MAX	
Supply-Voltage Range, VCC*: CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	4.5	5.5	V
DC Input Voltage, V <sub>I</sub>	0	VCC	V
DC Output Voltage, V <sub>O</sub>	0	≤ VCC	V
Operating Temperature, TA	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

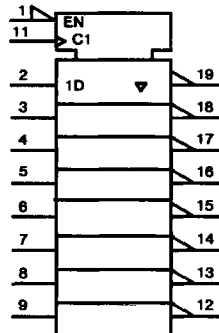
\* Unless otherwise specified, all voltages are referenced to ground.

**CD54/74FCT564, CD54/74FCT564AT TYPES**

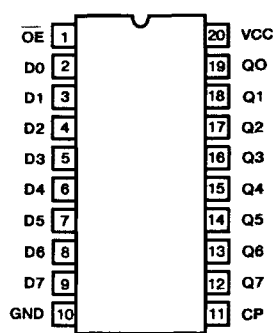
**CD54/74FCT574, CD54/74FCT574AT TYPES**



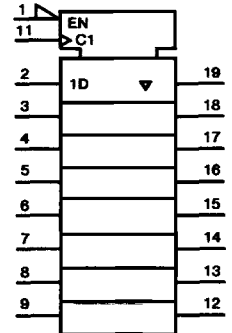
TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

TECHNICAL DATA 4

## STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V

54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS		VCC (V)	AMBIENT TEMPERATURE (TA)						UNITS
					+25°C		0°C to +70°C		-55°C to +125°C		
		VI (V)	IO (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or VIL	-15	MIN	2.4	-	2.4	-	-	-	V
			-12	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or VIL	48	MIN	-	0.55	-	0.55	-	-	V
			32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I <sub>IH</sub>	VCC		MAX	-	0.1	-	1	-	1	μA
Low-Level Input Current	I <sub>IL</sub>	GND		MAX	-	-0.1	-	-1	-	-1	μA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	μA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	μA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V <sub>IK</sub>	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V †		MAX	-	1.6	-	1.6	-	2	mA

\* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.

† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	CD54/74FCT564, 574				CD54/74FCT564/AT*, 574AT				UNITS				
			AMBIENT TEMPERATURE (T <sub>A</sub> )												
			+25°C		0°C to +70°C		-55°C to +125°C		+25°C			0°C to +70°C		-55°C to +125°C	
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX		MIN	MAX		
Clock Pulse Width	FCT574/AT	tW	5†	7	-	7	-		5	-	6	-	ns		
	FCT564/AT	tW	5	7	-	7.5	-						ns		
Setup Time Data to Clock	tSU	5		2	-	2.5	-		2	-	2	-	ns		
Data to Clock Hold Time	FCT574/AT	tH	5		2	-	2	-		1.5	-	2	-	ns	
	FCT564/AT	tH	5		2	-	2.5	-					ns		
Maximum Clock Frequency	fMAX	5		70	-	60	-						MHz		

†5V: min. is @ 4.5V  
5V: min. is @ 4.75V for 0°C to +70°C  
typ. is @ 5V

SWITCHING CHARACTERISTICS

FCT Series: tr, tf = 2.5ns, CL = 50pF, RL - See Figure 4

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	CD54/74FCT564, 574				CD54/74FCT564AT*, 574AT				UNITS				
			AMBIENT TEMPERATURE (T <sub>A</sub> )												
			+25°C		0°C to +70°C		-55°C to +125°C		+25°C			0°C to +70°C		-55°C to +125°C	
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX		MIN	MAX		
Propagation Delays:															
Clock to Q	FCT574/AT	tPLH, tPHL	5†	6.6	2	10	2	11	5.6	2	7.5	2	8.5	ns	
Clock to $\bar{Q}$	FCT564/AT	tPLH, tPHL	5	6.6	1.5	10	1.5	11					ns		
Output Disable to Q	FCT574/AT	tPLZ, tPHZ	5	6	1.5	8	1.5	8	4.2	1.5	5.5	1.5	6.5	ns	
Output Enable to Q	FCT574/AT	tPZL, tPZH	5	9	1.5	12.5	1.5	14	5.5	1.5	8	1.5	9.5	ns	
Output Disable to $\bar{Q}$	FCT564/AT	tPLZ, tPHZ	5	6	1.5	8	1.5	8					ns		
Output Enable to $\bar{Q}$	FCT564/AT	tPZL, tPZH	5	9	1.5	12.5	1.5	14					ns		
Power Dissipation Capacitance	§ CPD	-	34 Typical				34 Typical				pF				
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)	VOHV See Figure 1	5	0.5 Typical @ +25°C								V				
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)	VOLP See Figure 1	5	1 Typical @ +25°C								V				
Input Capacitance	CI	-	-	-	10	-	10	-	-	10	-	10	pF		
3-State Output Capacitance	CO	-	-	-	15	-	15	-	-	15	-	15	pF		

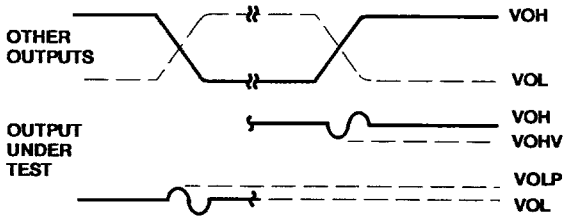
†5V: min. is @ 5.5V  
max. is @ 4.5V  
5V: min. is @ 5.25V for 0°C to +70°C  
max. is @ 4.75V for 0°C to +70°C  
typ. is @ 5V

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.  
PD (per package) = VCC ICC + Σ (VCC<sup>2</sup> fi CPD + VO<sup>2</sup> to CL + VCC ΔICC D) where:  
VCC = supply voltage  
ΔICC = flow through current x unit load  
CL = output load capacitance  
D = duty cycle of input high  
fo = output frequency  
fi = input frequency

\* Contact local Sales Office for availability

4  
TECHNICAL DATA

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics:  
PRR  $\leq$  1 MHz,  $t_r = 2.5\text{ns}$ ,  $t_f = 2.5\text{ns}$ , skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1  $\mu\text{F}$  capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

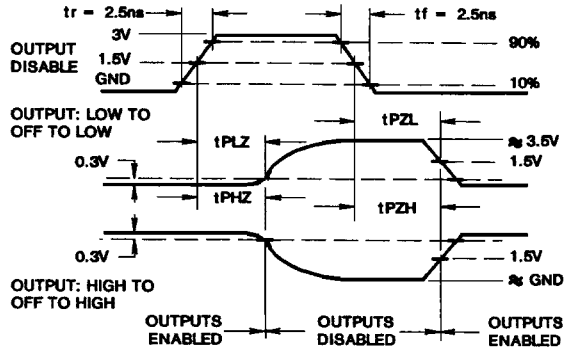
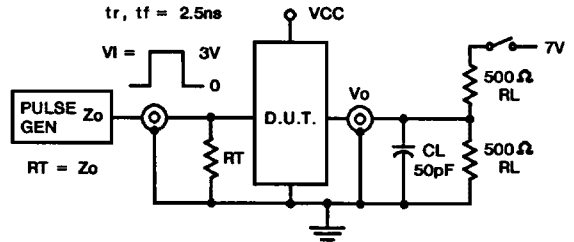


Figure 2 - Propagation delay times.



TEST	SWITCH POSITION
$t_{PLZ}$ , $t_{PZL}$ , OPEN DRAIN	CLOSED
$t_{PHZ}$ , $t_{PZH}$ , $t_{PLH}$ , $t_{PHL}$	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

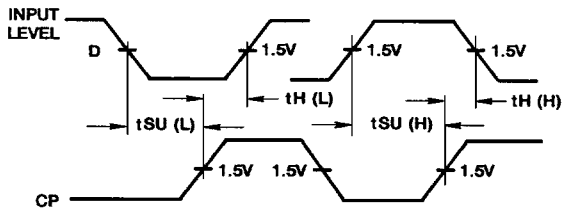


Figure 3 - Setup and hold times.