

MWCT101xSF

MWCT101XS Data Sheet

Key Features

- Operating characteristics
 - Voltage range: 2.7 V to 5.5 V
 - Ambient temperature range: -40 °C to 105 °C for HSRUN mode, -40 °C to 125 °C for RUN mode
- Arm™ Cortex-M4F core, 32-bit CPU
 - Supports up to 112 MHz frequency (HSRUN) with 1.25 Dhrystone MIPS per MHz
 - Arm Core based on the Armv7 Architecture and Thumb@-2 ISA
 - Integrated Digital Signal Processor (DSP)
 - Configurable Nested Vectored Interrupt Controller (NVIC)
 - Single Precision Floating Point Unit (FPU)
- Clock interfaces
 - 4 - 40 MHz fast external oscillator (SOSC)
 - 48 MHz Fast Internal RC oscillator (FIRC)
 - 8 MHz Slow Internal RC oscillator (SIRC)
 - 128 kHz Low Power Oscillator (LPO)
 - Up to 112 MHz (HSRUN) System Phased Lock Loop (SPLL)
 - Up to 50 MHz DC external square wave input clock
 - Real Time Counter (RTC)
- Power management
 - Low-power Arm Cortex-M4F core with excellent energy efficiency
 - Power Management Controller (PMC) with multiple power modes: HSRUN, RUN, STOP, VLPR, and VLPS. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 Mhz) to execute CSEc (Security) or EEPROM writes/erase.
 - Clock gating and low power operation supported on specific peripherals.
- Memory and memory interfaces
 - Up to 2 MB program flash memory with ECC
 - 64 KB FlexNVM for data flash memory with ECC and EEPROM emulation. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
 - Up to 256 KB SRAM with ECC
 - Up to 4 KB of FlexRAM for use as SRAM or EEPROM emulation
 - Up to 4 KB Code cache to minimize performance impact of memory access latencies
 - QuadSPI with HyperBus™ support
- Mixed-signal analog
 - Up to two 12-bit Analog-to-Digital Converter (ADC) with up to 32 channel analog inputs per module
 - One Analog Comparator (CMP) with internal 8-bit Digital to Analog Converter (DAC)
- Debug functionality
 - Serial Wire JTAG Debug Port (SWJ-DP) combines Debug Watchpoint and Trace (DWT)
 - Instrumentation Trace Macrocell (ITM)
 - Test Port Interface Unit (TPIU)
 - Flash Patch and Breakpoint (FPB) Unit
- Human-machine interface (HMI)
 - Up to 89 GPIO pins with interrupt functionality
 - Non-Maskable Interrupt (NMI)

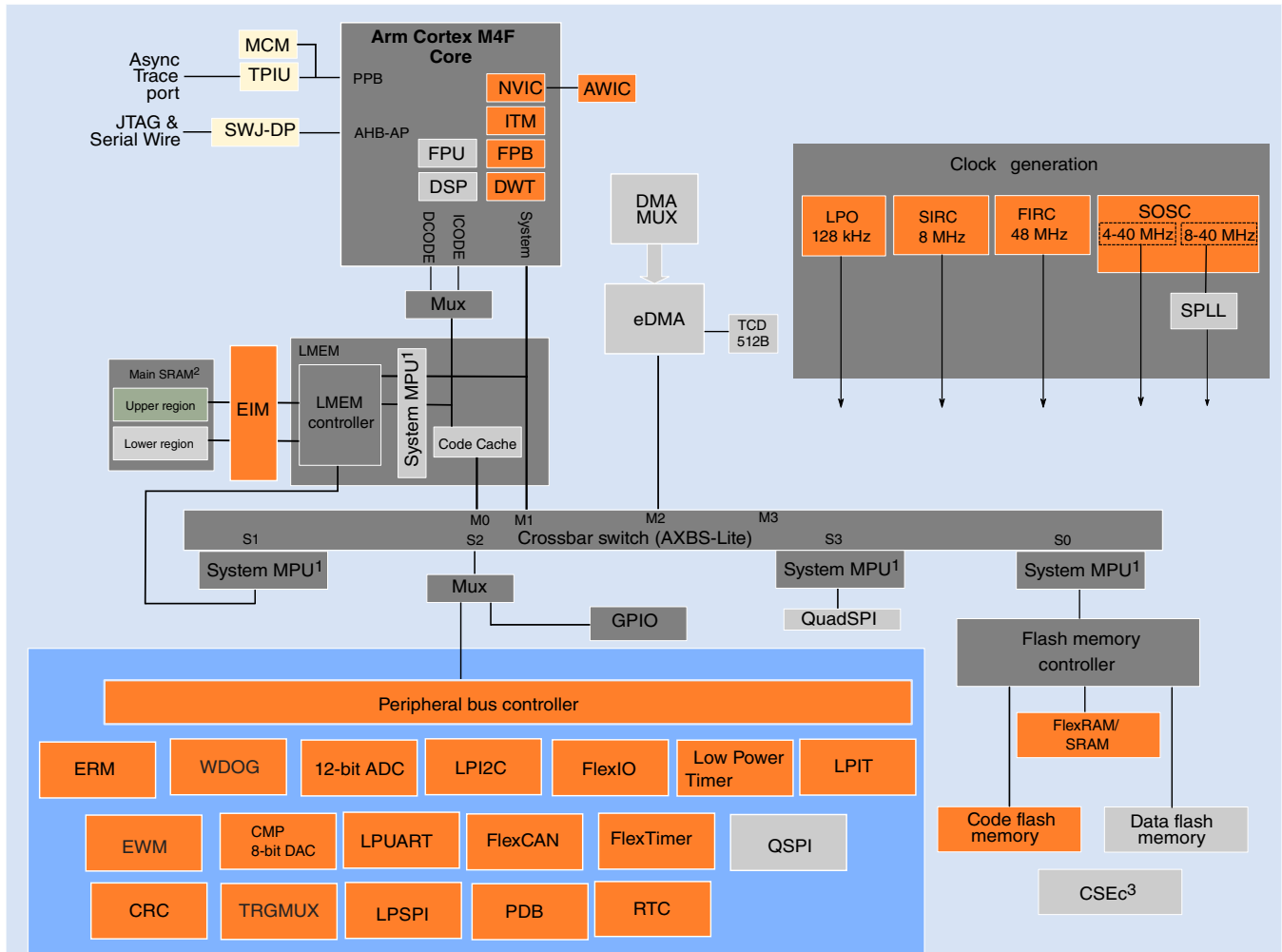
- Communications interfaces
 - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART/LIN) modules with DMA support and low power availability
 - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
 - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
 - Up to three FlexCAN modules (with optional CAN-FD support)
 - FlexIO module for emulation of communication protocols and peripherals (UART, I2C, SPI, I2S, LIN, PWM, etc).
- Safety and Security
 - Cryptographic Services Engine (CSEc) implements a comprehensive set of cryptographic functions as described in the SHE (Secure Hardware Extension) Functional Specification. Note: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device will need to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.
 - 128-bit Unique Identification (ID) number
 - Error-Correcting Code (ECC) on flash and SRAM memories
 - System Memory Protection Unit (System MPU)
 - Cyclic Redundancy Check (CRC) module
 - Internal watchdog (WDOG)
 - External Watchdog monitor (EWM) module
- Timing and control
 - Up eight independent 16-bit FlexTimers (FTM) module, offering up to 64 standard channels (IC/OC/PWM)
 - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
 - Two Programmable Delay Blocks (PDB) with flexible trigger system
 - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
 - 32-bit Real Time Counter (RTC)
- I/O and package
 - 64-pin LQFP, 100-pin LQFP, 100-pin MAPBGA package options
- 16 channel DMA with up to 63 request sources using DMAMUX

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1 Block diagram

The figure below shows a superset high level architecture block diagram of the device. Other devices within the family have a subset of the features. See [Feature comparison](#) for chip specific values.



1: On this device, NXP's system MPU implements the safety mechanisms to prevent masters from accessing restricted memory regions. This system MPU provides memory protection at the level of the Crossbar Switch. Each Crossbar master (Core, DMA) can be assigned different access rights to each protected memory region. The Arm M4 core version in this family does not integrate the Arm Core MPU, which would concurrently monitor only core-initiated memory accesses. In this document, the term MPU refers to NXP's system MPU.

2: For the device-specific sizes, see the "On-chip SRAM sizes" table in the "Memories and Memory Interfaces" chapter of the MWCT101xS Series Reference Manual.

3: CSEc (Security) or EEPROM writes/erase will trigger error flags in HSRUN mode (112 MHz) because this use case is not allowed to execute simultaneously. The device needs to switch to RUN mode (80 MHz) to execute CSEc (Security) or EEPROM writes/erase.

Key:

- Device architectural IP on all MWCT101xS devices
- Peripherals present on all MWCT101xS devices
- Peripherals present on selected MWCT101xS devices (see the "Feature Comparison" section in the RM)

Figure 1. High-level architecture diagram for the MWCT101xS family

2 Feature comparison

The following figure summarizes the memory and package options for the MWCT101xS series and demonstrates where this device fits within the overall series. All devices which share a common package are pin-to-pin compatible.

NOTE

Availability of peripherals depends on the pin availability in a particular package. For more information see IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Feature comparison

| | | MWCT101xS | | |
|---|---|--|------------------------------|--------------------------------|
| Parameter | | MWCT1014S | MWCT1015S | MWCT1016S |
| System | Core | Arm® Cortex™-M4F | | |
| | Frequency | up to 112 MHz (HSRUN) | | |
| | IEEE-754 FPU | ● | | |
| | HW security module (CSEc) ¹ | ● ² | | |
| | CRC module | 1x | | |
| | ISO 26262 | capable up to ASIL-B | | |
| | Peripheral speed | up to 112 MHz (HSRUN) | | |
| | Crossbar | ● | | |
| | DMA | ● | | |
| | EWM | ● | | |
| | Memory protection unit | ● | | |
| | FIRC CMU | ○ | | |
| | Watchdog | 1x | | |
| | Low power modes | ● | | |
| | HSRUN mode ¹ | ● | | |
| | Number of I/Os | up to 89 | up to 89 | up to 89 |
| | Single supply voltage | 2.7 - 5.5 V | | |
| Operating temperature (T _a) Temperature ambient | -40 to +105°C / +125°C | | | |
| Memory | Flash | 512 KB | 1 MB | 2 MB ³ |
| | Error correction code (ECC) | ● | | |
| | System RAM (including FlexRAM) | 64 KB | 128 KB | 256 KB |
| | FlexRAM (also available as system RAM) | 4 KB | | |
| | Cache | 4 KB | | |
| | EEPROM emulated by FlexRAM ¹ | 4 KB (up to 64 KB D-Flash) | | See footnote 4 |
| | External memory interface | ○ | | QuadSPI incl. HyperBus™ |
| Timer | Low power interrupt timer | 1x | | |
| | FlexTimer (16-bit counter) 8 channels | 4x (32) | 6x (48) | 8x (64) |
| | Low power timer (LPTMR) | 1x | | |
| | Real time counter (RTC) | 1x | | |
| | Programmable delay block (PDB) | 2x | | |
| Analog | Trigger mux (TRGMUX) | 1x (64) | 1x (73) | 1x (81) |
| | 12-bit SAR ADC (1 MSPS each) | 2x (16) | 2x (24) | 2x (32) |
| | Comparator with 8-bit DAC | 1x | | |
| Communication | Low power UART/LIN (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A and SAE J2602) | 3x | | |
| | Low power SPI | 3x | | |
| | Low power I2C | 1x | | 2x |
| | FlexCAN (CAN-FD ISO/CD 11898-1) | 3x (1x with FD) | 3x ² (2x with FD) | 3x (3x with FD) |
| | FlexIO (8 pins configurable as UART, SPI, I2C, I2S) | 1x | | |
| IDEs | Debug & trace | SWD, JTAG ⁵ (ITM, SWV, SWO) | | SWD, JTAG (ITM, SWV, SWO), ETM |
| | Ecosystem (IDE, compiler, debugger) | NXP S32 Design Studio + GCC + GHS + Lauterbach | | |
| Other | Packages ⁶ | LQFP-64 LQFP-100 | LQFP-100 BGA-100 | BGA-100 |

LEGEND:

- Not implemented
- Available on the device
- ¹ No write or erase access to Flash module, including Security (CSEc) and EEPROM commands, are allowed when device is running at HSRUN mode (112MHz) or VLPR mode.
- ² Option with No CSEc and CAN-FD is also available for MWCT1015S
- ³ Available when EEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
- ⁴ 4 KB (up to 512 KB D-Flash as a part of 2M Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.
- ⁵ Only for Boundary Scan Register
- ⁶ See Dimensions for package drawing

3 Ordering parts

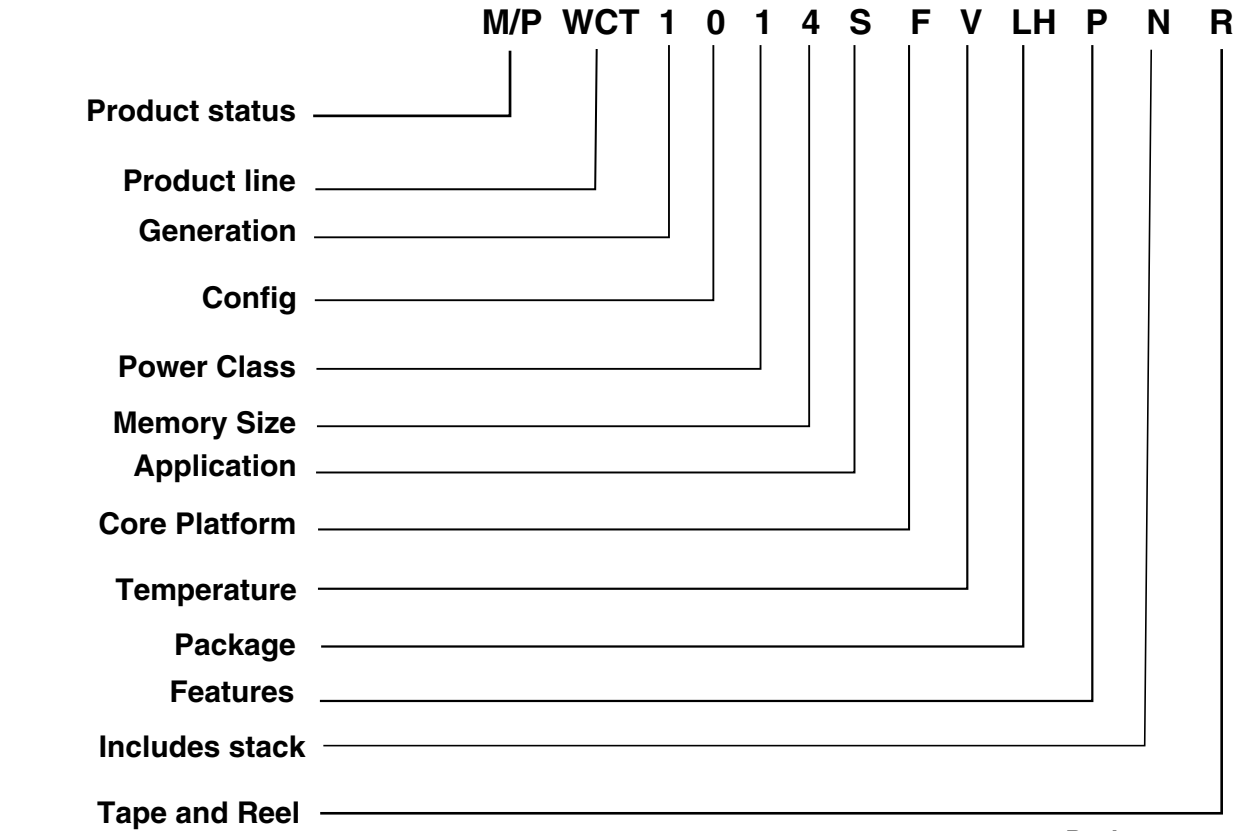
3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search.

NOTE

Not all part number combinations exist

3.2 Ordering information



| <p>Product status P: Pre Qualification M: Fully Qualified</p> | <p>Power Class 0 = 5 W 1 = 15 W 2 = 60 W 3 =200 W</p> | <p>Package</p> <table border="1"> <thead> <tr> <th>Pins</th> <th>LQFP</th> <th>BGA</th> </tr> </thead> <tbody> <tr> <td>64</td> <td>LH</td> <td>-</td> </tr> <tr> <td>100</td> <td>LL</td> <td>MH</td> </tr> </tbody> </table> | Pins | LQFP | BGA | 64 | LH | - | 100 | LL | MH |
|--|--|---|------|------|-----|-----|-------|-----|-----|---|----|
| Pins | LQFP | BGA | | | | | | | | | |
| 64 | LH | - | | | | | | | | | |
| 100 | LL | MH | | | | | | | | | |
| <p>Product line WCT: Wireless Charging Technology</p> | <p>Memory size (Flash)</p> <table border="1"> <thead> <tr> <th></th> <th>4</th> <th>5</th> <th>6</th> </tr> </thead> <tbody> <tr> <th>M4F</th> <td>512 K</td> <td>1 M</td> <td>2 M</td> </tr> </tbody> </table> | | 4 | 5 | 6 | M4F | 512 K | 1 M | 2 M | <p>Features P = No CAN-FD and CSEc</p> | |
| | 4 | 5 | 6 | | | | | | | | |
| M4F | 512 K | 1 M | 2 M | | | | | | | | |
| <p>Generation 1: 1st product Gen 2: 2nd product Gen</p> | <p>Application Blank =Customer A = Auto/Industr S = A + AUTOSAR</p> | <p>Includes stack Blank = No stack N = NFC</p> | | | | | | | | | |
| <p>Config 0 = Standard 1 = Premium</p> | <p>Core platform F: Arm Cortex M4F</p> | <p>Tape and Reel R: Tape and Reel</p> | | | | | | | | | |
| | <p>Temperature V: -40C to 105C</p> | | | | | | | | | | |

Figure 3. Ordering information

4 General

4.1 Absolute maximum ratings

NOTE

- Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions.
- Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.
- All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not guarantee desired operation.
- Unless otherwise specified, all maximum and minimum values in the datasheet are across process, voltage, and temperature.

Table 1. Absolute maximum ratings

| Symbol | Parameter | Conditions ¹ | Min | Max | Unit |
|------------------------------------|--|-------------------------|-----------|------------------|------|
| V_{DD} ² | 2.7 V - 5.5 V input supply voltage | — | -0.3 | 5.8 ³ | V |
| V_{REFH} | 3.3 V / 5.0 V ADC high reference voltage | — | -0.3 | 5.8 ³ | V |
| $I_{INJPAD_DC_ABS}$ ⁴ | Continuous DC input current (positive / negative) that can be injected into an I/O pin | — | -3 | +3 | mA |
| V_{IN_DC} | Continuous DC Voltage on any I/O pin with respect to V_{SS} | — | -0.8 | 5.8 ⁵ | V |
| $I_{INJSUM_DC_ABS}$ | Sum of absolute value of injected currents on all the pins (Continuous DC limit) | — | — | 30 | mA |
| T_{ramp} ⁶ | ECU supply ramp rate | — | 0.5 V/min | 500 V/ms | — |
| T_{ramp_MCU} ⁷ | MCU supply ramp rate | — | 0.5 V/min | 100 V/ms | — |
| T_A ⁸ | Ambient temperature | — | -40 | 125 | °C |
| T_{STG} | Storage temperature | — | -55 | 165 | °C |
| $V_{IN_TRANSIENT}$ | Transient overshoot voltage allowed on I/O pin beyond V_{IN_DC} limit | — | — | 6.8 ⁹ | V |

1. All voltages are referred to V_{SS} unless otherwise specified.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section [I/O parameters](#) and [ADC electrical specifications](#) respectively for details.
3. 60 s lifetime – No restrictions i.e. The part can switch.
10 hours lifetime – Device in reset i.e. The part cannot switch.

General

4. When input pad voltage levels are close to V_{DD} or V_{SS} , practically no current injection is possible.
5. While respecting the maximum current injection limit
6. This is the Electronic Control Unit (ECU) supply ramp rate and not directly the MCU ramp rate. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. This is the MCU supply ramp rate, and the ramp rate assumes that the HW design guidelines in [AN5426](#) are followed. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
8. T_J (Junction temperature)=135 °C. Assumes T_A =125 °C for RUN mode
 T_J (Junction temperature)=125 °C. Assumes T_A =105 °C for HSRUN mode
 - Assumes maximum θ_{JA} for 2s2p board. See [Thermal characteristics](#)
9. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

Device functionality is guaranteed up to the LVR assert level; however, electrical performance of 12-bit ADC, CMP with 8-bit DAC, IO electrical characteristics, and communication modules electrical characteristics would be degraded when voltage drops below 2.7 V

Table 2. Voltage and current operating requirements 1

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------------|---|------------------|-----------------|------|-------|
| V_{DD}^2 | Supply voltage | 2.7 ³ | 5.5 | V | 4 |
| V_{DD_OFF} | Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source. | 0 | 0.1 | V | |
| V_{DDA} | Analog supply voltage | 2.7 | 5.5 | V | 4 |
| $V_{DD} - V_{DDA}$ | V_{DD} -to- V_{DDA} differential voltage | -0.1 | 0.1 | V | 4 |
| V_{REFH} | ADC reference voltage high | 2.7 | $V_{DDA} + 0.1$ | V | 5 |
| V_{REFL} | ADC reference voltage low | -0.1 | 0.1 | V | |
| V_{ODPU} | Open drain pullup voltage level | V_{DD} | V_{DD} | V | 6 |
| $I_{INJPAD_DC_OP}^7$ | Continuous DC input current (positive / negative) that can be injected into an I/O pin | -3 | +3 | mA | |
| $I_{INJSUM_DC_OP}$ | Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules) | — | 30 | mA | |

1. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5$ V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section [I/O parameters](#) and [ADC electrical specifications](#) respectively for details.
3. MWCT1016S will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged MWCT1016S is guaranteed to operate from 2.97 V. All other MWCT101xS family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{DDA} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note [AN5032](#) for reference supply design for SAR ADC.

5. V_{REFH} should always be equal to or less than $V_{DDA} + 0.1\text{ V}$ and $V_{DD} + 0.1\text{ V}$
6. Open drain outputs must be pulled to V_{DD} .
7. When input pad voltage levels are close to V_{DD} or V_{SS} , practically no current injection is possible.

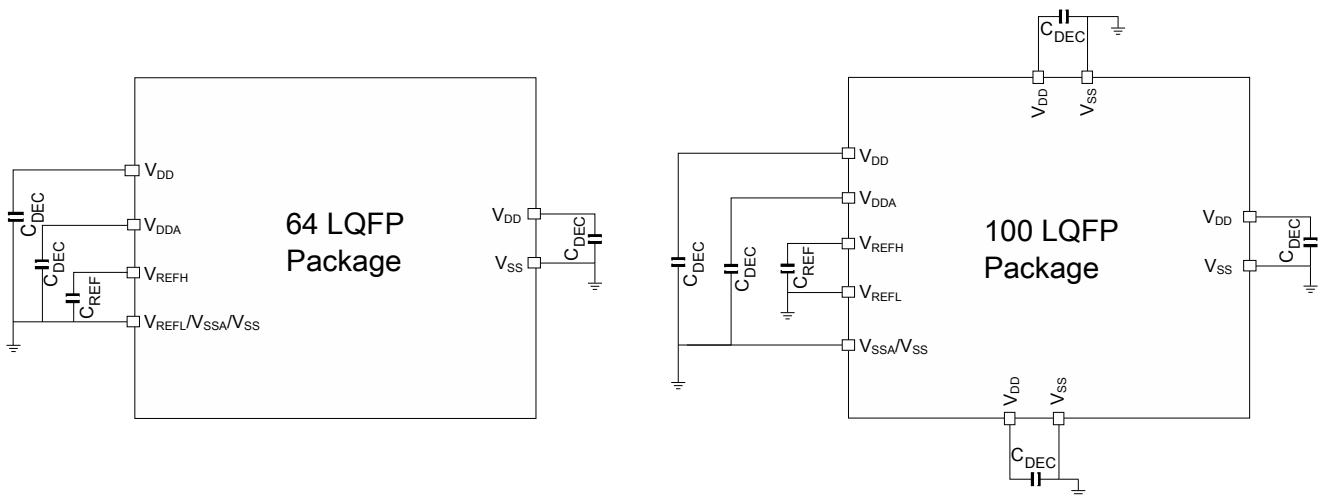
4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64-pin LQFP and 100-pin LQFP and MAPBGA packages

| Symbol | Parameter | Value | | | Unit |
|--------------------|---------------------------------|-------|------|------------------|------|
| | | Min. | Typ. | Max. | |
| T_A C-Grade Part | Ambient temperature under bias | -40 | — | 85 ¹ | °C |
| T_J C-Grade Part | Junction temperature under bias | -40 | — | 105 ¹ | °C |
| T_A V-Grade Part | Ambient temperature under bias | -40 | — | 105 ¹ | °C |
| T_J V-Grade Part | Junction temperature under bias | -40 | — | 125 ¹ | °C |
| T_A M-Grade Part | Ambient temperature under bias | -40 | — | 125 ² | °C |
| T_J M-Grade Part | Junction temperature under bias | -40 | — | 135 ² | °C |

1. Values mentioned are measured at $\leq 112\text{ MHz}$ in HSRUN mode.
2. Values mentioned are measured at $\leq 80\text{ MHz}$ in RUN mode.

4.4 Power and ground pins



NOTE: V_{DD} and V_{DDA} must be shorted to a common source on PCB

Figure 4. Pinout decoupling

Table 4. Supplies decoupling capacitors 1, 2

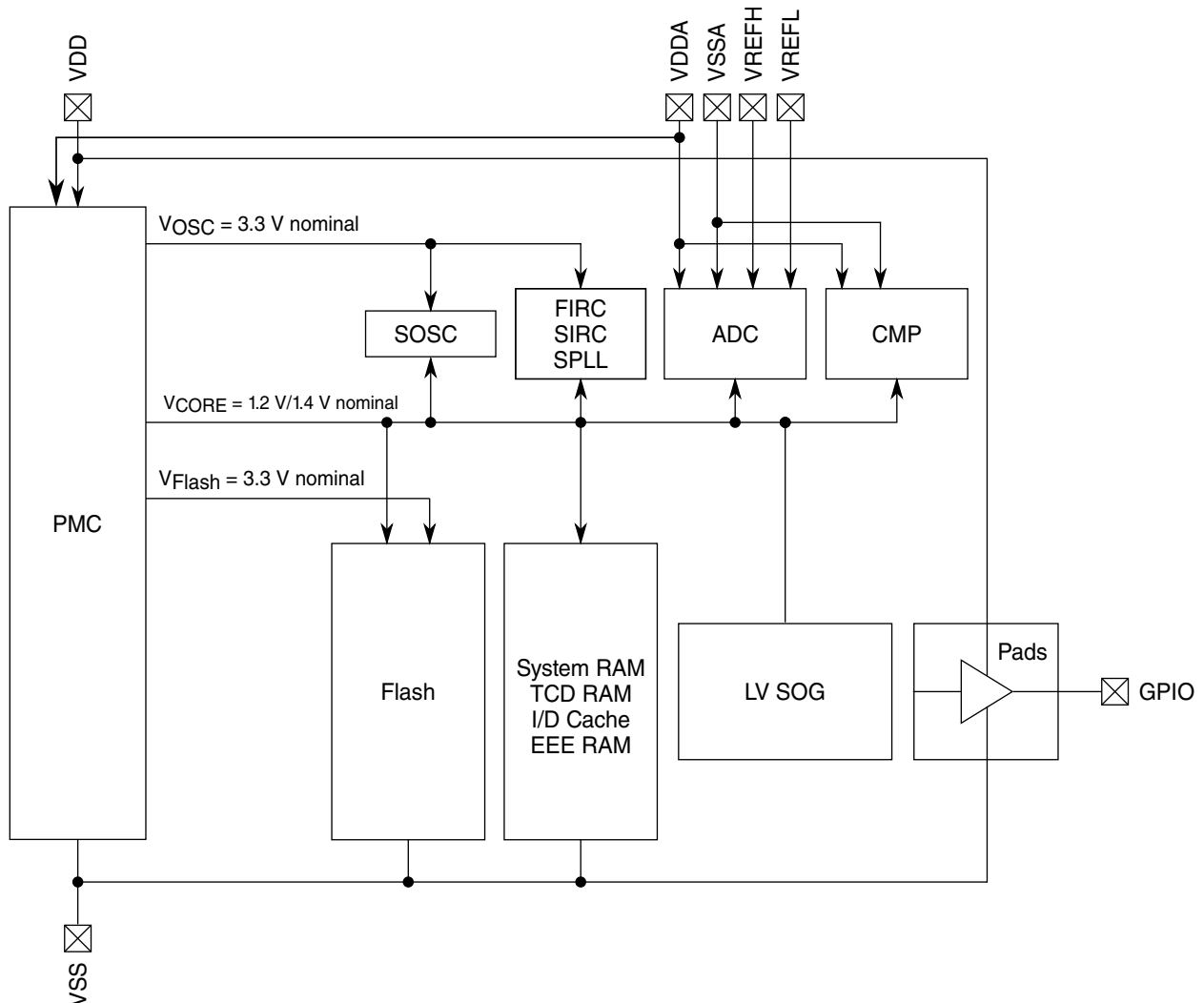
| Symbol | Description | Min. ³ | Typ. | Max. | Unit |
|---------------------------|---|-------------------|------|------|------|
| C_{REF} ^{4, 5} | ADC reference high decoupling capacitance | 70 | 100 | — | nF |

Table continues on the next page...

Table 4. Supplies decoupling capacitors 1, 2 (continued)

| Symbol | Description | Min. ³ | Typ. | Max. | Unit |
|-------------------------------------|------------------------------------|-------------------|------|------|------|
| C _{DEC} ^{5, 6, 7} | Recommended decoupling capacitance | 70 | 100 | — | nF |

- V_{DD} and V_{D_{DA}} must be shorted to a common source on PCB. The differential voltage between V_{DD} and V_{D_{DA}} is for RF-AC only. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note [AN5032](#) for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
- All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
- Minimum recommendation is after considering component aging and tolerance.
- For improved performance, it is recommended to use 10 μF, 0.1 μF and 1 nF capacitors in parallel.
- All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
- Contact your local Field Applications Engineer for details on best analog routing practices.
- The filtering used for decoupling the device supplies must comply with the following best practices rules:
 - The protection/decoupling capacitors must be on the path of the trace connected to that component.
 - No trace exceeding 1 mm from the protection to the trace or to the ground.
 - The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
 - The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.



*Note: VSSA and VSS are shorted at package level

Figure 5. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 5. V_{DD} supply LVR, LVD and POR operating requirements

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------|--|------|-------|------|------|-------|
| V_{POR} | Rising and falling V_{DD} POR detect voltage | 1.1 | 1.6 | 2.0 | V | |
| V_{LVR} | LVR falling threshold (RUN, HSRUN, and STOP modes) | 2.50 | 2.58 | 2.7 | V | |
| V_{LVR_HYST} | LVR hysteresis | — | 45 | — | mV | 1 |
| V_{LVR_LP} | LVR falling threshold (VLPS/VLPR modes) | 1.97 | 2.22 | 2.44 | V | |
| V_{LVD} | Falling low-voltage detect threshold | 2.8 | 2.875 | 3 | V | |
| V_{LVD_HYST} | LVD hysteresis | — | 50 | — | mV | 1 |
| V_{LVW} | Falling low-voltage warning threshold | 4.19 | 4.305 | 4.5 | V | |
| V_{LVW_HYST} | LVW hysteresis | — | 75 | — | mV | 1 |
| V_{BG} | Bandgap voltage reference | 0.97 | 1.00 | 1.03 | V | |

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- RUN Mode:
 - Clock source: FIRC
 - $SYS_CLK/CORE_CLK = 48$ MHz
 - $BUS_CLK = 48$ MHz
 - $FLASH_CLK = 24$ MHz
- HSRUN Mode:
 - Clock source: SPLL
 - $SYS_CLK/CORE_CLK = 112$ MHz
 - $BUS_CLK = 56$ MHz
 - $FLASH_CLK = 28$ MHz
- VLPR Mode:
 - Clock source: SIRC
 - $SYS_CLK/CORE_CLK = 4$ MHz
 - $BUS_CLK = 4$ MHz
 - $FLASH_CLK = 1$ MHz
- STOP1/STOP2 Mode:
 - Clock source: FIRC
 - $SYS_CLK/CORE_CLK = 48$ MHz

- BUS_CLK = 48 MHz
- FLASH_CLK = 24 MHz
- VLPS Mode: All clock sources disabled.

Table 6. Power mode transition operating behaviors

| Symbol | Description | Min. | Typ. | Max. | Unit |
|-----------|---|------|-------|-------|---------|
| t_{POR} | After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip. | — | 325 | — | μs |
| | VLPS → RUN | 8 | — | 17 | μs |
| | STOP1 → RUN | 0.07 | 0.075 | 0.08 | μs |
| | STOP2 → RUN | 0.07 | 0.075 | 0.08 | μs |
| | VLPR → RUN | 19 | — | 26 | μs |
| | VLPR → VLPS | 5.1 | 5.7 | 6.5 | μs |
| | VLPS → VLPR | 18.8 | 23 | 27.75 | μs |
| | RUN → Compute operation | 0.72 | 0.75 | 0.77 | μs |
| | HSRUN → Compute operation | 0.3 | 0.31 | 0.35 | μs |
| | RUN → STOP1 | 0.35 | 0.38 | 0.4 | μs |
| | RUN → STOP2 | 0.2 | 0.23 | 0.25 | μs |
| | RUN → VLPS | 0.3 | 0.35 | 0.4 | μs |
| | RUN → VLPR | 3.5 | 3.8 | 5 | μs |
| | VLPS → Asynchronous DMA Wakeup | 105 | 110 | 125 | μs |
| | STOP1 → Asynchronous DMA Wakeup | 1 | 1.1 | 1.3 | μs |
| | STOP2 → Asynchronous DMA Wakeup | 1 | 1.1 | 1.3 | μs |
| | Pin reset → Code execution | — | 214 | — | μs |

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various modes of operation. Attached *MWCT101xS_Power_Modes_Configuration.xlsx* details the modes used in gathering the power consumption data stated in the following table [Table 7](#). For full functionality refer to table: Module operation in available low power modes of the *Reference Manual*.

Table 7. Power consumption (Typicals unless stated otherwise) 1

| Chip/Device | Ambient Temperature (°C) | VLPS (μA) ^{2,3} | | VLPR (mA) | | STOP1 (mA) | STOP2 (mA) | RUN@48 MHz (mA) | | RUN@64 MHz (mA) | | RUN@80 MHz (mA) | | HSRUN@112 MHz (mA) ⁴ | | Idd/MHz ($\mu\text{A}/\text{MHz}$) ⁵ | |
|------------------------|--------------------------|---------------------------------------|---------------------|----------------------|---------------------|------------|------------|----------------------|---------------------|----------------------|---------------------|----------------------|----------------------|---------------------------------|------|---|-----|
| | | Peripherals disabled ⁶ | Peripherals enabled | Peripherals disabled | Peripherals enabled | | | Peripherals disabled | Peripherals enabled | Peripherals disabled | Peripherals enabled | Peripherals disabled | Peripherals disabled | Peripherals enabled | | | |
| MWCT1014S | 25 | Typ | 29.8 | 39.1 | 1.48 | 1.50 | 7 | 7.7 | 19.7 | 26.9 | 25.1 | 33.3 | 30.2 | 39.6 | 43.3 | 55.6 | 378 |
| | 85 | Typ | 150 | 159 | 1.72 | 1.85 | 7.2 | 8.1 | 20.4 | 27.1 | 26.1 | 33.5 | 30.5 | 40 | 43.9 | 56.1 | 381 |
| | | Max | 359 | 384 | 2.60 | 2.65 | 9.2 | 9.9 | 23.2 | 29.6 | 29.3 | 36.2 | 34.8 | 42.1 | 46.3 | 59.7 | 435 |
| | 105 | Typ | 256 | 273 | 1.80 | 2.10 | 7.8 | 8.5 | 20.6 | 27.4 | 26.6 | 33.8 | 31.2 | 40.5 | 44.8 | 57.1 | 390 |
| | | Max | 850 | 900 | 2.65 | 2.70 | 10.3 | 11.1 | 23.9 | 30.6 | 30.3 | 37.3 | 35.6 | 43.5 | 47.9 | 61.3 | 445 |
| | 125 | Max | 1960 | 1998 | 3.18 | 3.25 | 12.9 | 13.8 | 26.9 | 33.6 | 35 | 40.3 | 38.7 | 46.8 | NA | NA | 484 |
| | | | | | | | | | | | | | | | | | |
| MWCT1015S | 25 | Typ | 37 | 47 | 1.57 | 1.61 | 8 | 9.2 | 23.4 | 31.4 | 30.5 | 40.2 | 36.2 | 47.6 | 52 | 68.3 | 452 |
| | 85 | Typ | 207 | 209 | 1.79 | 1.83 | 8.9 | 10.1 | 24.4 | 32.4 | 31.5 | 41.3 | 37.2 | 48.7 | 53.3 | 69.8 | 465 |
| | | Max | 974 | 981 | 3.32 | 3.38 | 12.7 | 13.9 | 29.3 | 37.9 | 36.7 | 47 | 42.4 | 54.4 | 60.3 | 78 | 530 |
| | 105 | Typ | 419 | 422 | 1.99 | 2.04 | 9.8 | 11 | 25.3 | 33.4 | 32.5 | 42.2 | 38.1 | 49.6 | 54.4 | 70.8 | 477 |
| | | Max | 2004 | 2017 | 4.06 | 4.13 | 17.1 | 18.3 | 34.1 | 42.6 | 41.3 | 51.4 | 46.9 | 58.8 | 65.7 | 82.8 | 587 |
| | 125 | Max | 3358 | 3380 | 5.28 | 5.38 | 22.6 | 23.7 | 40.2 | 48.8 | 47.3 | 57.4 | 52.8 | 64.8 | NA | NA | 660 |
| | | | | | | | | | | | | | | | | | |
| MWCT1016S ⁷ | 25 | Typ | 38 | 54 | 2.17 | 2.20 | 8.5 | 9.6 | 27.6 | 34.9 | 35.5 | 45.3 | 42.1 | 57.7 | 60.3 | 83.3 | 526 |
| | 85 | Typ | 336 | 357 | 2.30 | 2.35 | 10.1 | 11.1 | 29.1 | 37.0 | 36.8 | 46.6 | 43.4 | 59.9 | 62.9 | 88.7 | 543 |
| | | Max | 1660 | 1736 | 3.48 | 3.55 | 14.5 | 15.6 | 34.8 | 43.6 | 41.9 | 53.9 | 48.7 | 65.1 | 70.4 | 96.1 | 609 |
| | 105 | Typ | 560 | 577 | 2.49 | 2.54 | 10.9 | 11.9 | 29.8 | 37.8 | 37.6 | 47.5 | 45.2 | 61.5 | 63.8 | 89.1 | 565 |
| | | Max | 2945 | 2970 | 4.40 | 4.47 | 18.0 | 19.0 | 38.4 | 46.8 | 44.9 | 55.3 | 51.6 | 66.8 | 73.6 | 97.4 | 645 |
| | 125 | Max | 3990 | 4166 | 6.00 | 6.08 | 23.4 | 24.5 | 44.3 | 52.5 | 50.9 | 61.3 | 57.5 | 71.6 | NA | NA | 719 |
| | | | | | | | | | | | | | | | | | |

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration. Typical conditions assumes $V_{DD} = V_{DDA} = V_{REFH} = 5\text{ V}$, temperature = 25 °C and typical silicon process unless otherwise stated. All output pins are floating and On-chip pull-down is enabled for all unused input pins.

General

2. This is an average based on the use case described in the Comparator section, whereby the analog sampling is taking place periodically, with a mechanism to only enable the DAC as required. The numbers quoted assumes that only a single ANL_CMP is active and the others are disabled
3. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
4. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
5. Values mentioned are measured at RUN@80 MHz with peripherals disabled.
6. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
7. The MWCT1016S data points assume that QuadSPI etc. are inactive.

4.8 ESD handling ratings

| Symbol | Description | Min. | Max. | Unit | Notes |
|------------------|---|--------|------|------|-------|
| V_{HBM} | Electrostatic discharge voltage, human body model | - 4000 | 4000 | V | 1 |
| V_{CDM} | Electrostatic discharge voltage, charged-device model | | | | 2 |
| | All pins except the corner pins | - 500 | 500 | V | |
| | Corner pins only | - 750 | 750 | V | |
| I_{LAT} | Latch-up current at ambient temperature of 125 °C | - 100 | 100 | mA | 3 |

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

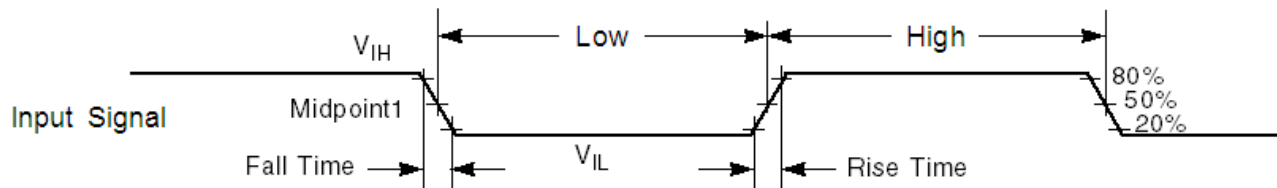
4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{\text{IL}} + (V_{\text{IH}} - V_{\text{IL}})/2$.

Figure 6. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 8. General switching specifications

| Symbol | Description | Min. | Max. | Unit | Notes |
|--------|--|---------------------------------------|------|------------------|-------|
| | GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path | 1.5 | — | Bus clock cycles | 1, 2 |
| | GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path | 50 | — | ns | 3 |
| WFRST | $\overline{\text{RESET}}$ input filtered pulse | — | 10 | ns | 4 |
| WNFRST | $\overline{\text{RESET}}$ input not filtered pulse | Maximum of (100 ns, bus clock period) | — | ns | 5 |

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Maximum length of $\overline{\text{RESET}}$ pulse which will be filtered by internal filter.
5. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter. This number depends on bus clock period also. For example, in VLPR mode bus clock is 4 MHz, which make clock period of 250 ns. In this case, minimum pulse width which will cause reset is 250 ns. For faster bus clock frequencies which have clock period less than 100 ns, the minimum pulse width not filtered will be 100 ns.

5.3 DC electrical specifications at 3.3 V Range

NOTE

For details on the pad types defined in [Table 9](#) and [Table 10](#), see Reference Manual section *IO Signal Table* and IO Signal Description Input Multiplexing sheet(s) attached with Reference Manual.

Table 9. DC electrical specifications at 3.3 V Range

| Symbol | Parameter | Value | | | Unit | Notes |
|-----------------|---|----------------------|------|---------------------|------|-------|
| | | Min. | Typ. | Max. | | |
| V_{DD} | I/O Supply Voltage | 2.7 | 3.3 | 4 | V | 1 |
| V_{ih} | Input Buffer High Voltage | $0.7 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | 2 |
| V_{il} | Input Buffer Low Voltage | $V_{SS} - 0.3$ | — | $0.3 \times V_{DD}$ | V | 3 |
| V_{hys} | Input Buffer Hysteresis | $0.06 \times V_{DD}$ | — | — | V | |
| $I_{oh_{GPIO}}$ | I/O current source capability measured when pad $V_{oh} = (V_{DD} - 0.8 \text{ V})$ | 3.5 | — | — | mA | |

Table continues on the next page...

Table 9. DC electrical specifications at 3.3 V Range (continued)

| Symbol | Parameter | Value | | | Unit | Notes | |
|---|---|-------|------|-------|------------|-------|---------------|
| | | Min. | Typ. | Max. | | | |
| loh _{GPIO-HD_DSE_0} | | | | | | | |
| lol _{GPIO} lol _{GPIO-HD_DSE_0} | I/O current sink capability measured when pad $V_{ol} = 0.8\text{ V}$ | 3 | — | — | mA | | |
| loh _{GPIO-HD_DSE_1} | I/O current source capability measured when pad $V_{oh} = (V_{DD} - 0.8\text{ V})$ | 14 | — | — | mA | 4 | |
| lol _{GPIO-HD_DSE_1} | I/O current sink capability measured when pad $V_{ol} = 0.8\text{ V}$ | 12 | — | — | mA | 4 | |
| loh _{GPIO-FAST_DSE_0} | I/O current sink capability measured when pad $V_{oh} = V_{DD} - 0.8\text{ V}$ | 9.5 | — | — | mA | 5 | |
| lol _{GPIO-FAST_DSE_0} | I/O current sink capability measured when pad $V_{ol} = 0.8\text{ V}$ | 10 | — | — | mA | 5 | |
| loh _{GPIO-FAST_DSE_1} | I/O current sink capability measured when pad $V_{oh} = V_{DD} - 0.8\text{ V}$ | 16 | — | — | mA | 5 | |
| lol _{GPIO-FAST_DSE_1} | I/O current sink capability measured when pad $V_{ol} = 0.8\text{ V}$ | 15.5 | — | — | mA | 5 | |
| IOHT | Output high current total for all ports | — | — | 100 | mA | | |
| IIN | Input leakage current (per pin) for full temperature range at $V_{DD} = 3.3\text{ V}$ | | | | | 6 | |
| | All pins other than high drive port pins | | | 0.005 | 0.5 | | μA |
| | High drive port pins | | | 0.010 | 0.5 | | μA |
| R _{PU} | Internal pullup resistors | 20 | | 60 | k Ω | 7 | |
| R _{PD} | Internal pulldown resistors | 20 | | 60 | k Ω | 8 | |

- MWCT1016S will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged MWCT1016S is guaranteed to operate from 2.97 V. All other MWCT101xS family devices operate from 2.7 V in all modes.
- For reset pads, same V_{ih} levels are applicable
- For reset pads, same V_{il} levels are applicable
- The value given is measured at high drive strength mode. For value at low drive strength mode see the loh_Standard value given above.
- For reference only. Run simulations with the IBIS model and custom board for accurate results.
- Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *MWCT101xS_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
- Measured at input $V = V_{SS}$
- Measured at input $V = V_{DD}$

5.4 DC electrical specifications at 5.0 V Range

Table 10. DC electrical specifications at 5.0 V Range

| Symbol | Parameter | Value | | | Unit | Notes |
|----------|---------------------------|----------------------|------|----------------|------|-------|
| | | Min. | Typ. | Max. | | |
| V_{DD} | I/O Supply Voltage | 4 | — | 5.5 | V | |
| V_{ih} | Input Buffer High Voltage | $0.65 \times V_{DD}$ | — | $V_{DD} + 0.3$ | V | 1 |

Table continues on the next page...

Table 10. DC electrical specifications at 5.0 V Range (continued)

| Symbol | Parameter | Value | | | Unit | Notes |
|--------------|--|----------------------|-------|----------------------|---------------|-------|
| | | Min. | Typ. | Max. | | |
| V_{il} | Input Buffer Low Voltage | $V_{SS} - 0.3$ | — | $0.35 \times V_{DD}$ | V | 2 |
| V_{hys} | Input Buffer Hysteresis | $0.06 \times V_{DD}$ | — | — | V | |
| Ioh_Standard | I/O current source capability measured when pad $V_{oh} = (V_{DD} - 0.8 \text{ V})$ | 5 | — | — | mA | |
| Iol_Standard | I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$ | 5 | — | — | mA | |
| Ioh_Strong | I/O current source capability measured when pad $V_{oh} = V_{DD} - 0.8 \text{ V}$ | 20 | — | — | mA | 3, 4 |
| Iol_Strong | I/O current sink capability measured when pad $V_{ol} = 0.8 \text{ V}$ | 20 | — | — | mA | 4, 5 |
| IOHT | Output high current total for all ports | — | — | 100 | mA | |
| IIN | Input leakage current (per pin) for full temperature range at $V_{DD} = 5.5 \text{ V}$ | | | | | 6 |
| | All pins other than high drive port pins | | 0.005 | 0.5 | μA | |
| | High drive port pins | | 0.010 | 0.5 | μA | |
| R_{PU} | Internal pullup resistors | 20 | | 50 | k Ω | 7 |
| R_{PD} | Internal pulldown resistors | 20 | | 50 | k Ω | 8 |

- For reset pads, same V_{ih} levels are applicable
- For reset pads, same V_{il} levels are applicable
- The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
- The strong pad I/O pin is capable of switching a 50 pF load at up to 40 MHz.
- The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
- Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *MWCT101xS_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
- Measured at input $V = V_{SS}$
- Measured at input $V = V_{DD}$

5.5 AC electrical specifications at 3.3 V range

Table 11. AC electrical specifications at 3.3 V Range

| Symbol | DSE | Rise time (nS) ¹ | | Fall time (nS) ¹ | | Capacitance (pF) ² |
|-------------------|-----|-----------------------------|------|-----------------------------|------|-------------------------------|
| | | Min. | Max. | Min. | Max. | |
| t_{RF_GPIO} | NA | 3.2 | 14.5 | 3.4 | 15.7 | 25 |
| | | 5.7 | 23.7 | 6.0 | 26.2 | 50 |
| | | 20.0 | 80.0 | 20.8 | 88.4 | 200 |
| $t_{RF_GPIO-HD}$ | 0 | 3.2 | 14.5 | 3.4 | 15.7 | 25 |

Table continues on the next page...

Table 11. AC electrical specifications at 3.3 V Range (continued)

| Symbol | DSE | Rise time (nS) ¹ | | Fall time (nS) ¹ | | Capacitance (pF) ² |
|--------------------------|-----|-----------------------------|------|-----------------------------|------|-------------------------------|
| | | Min. | Max. | Min. | Max. | |
| | | 5.7 | 23.7 | 6.0 | 26.2 | 50 |
| | | 20.0 | 80.0 | 20.8 | 88.4 | 200 |
| | | 1.5 | 5.8 | 1.7 | 6.1 | 25 |
| | 1 | 2.4 | 8.0 | 2.6 | 8.3 | 50 |
| | | 6.3 | 22.0 | 6.0 | 23.8 | 200 |
| | | 0.6 | 2.8 | 0.5 | 2.8 | 25 |
| tRF _{GPIO-FAST} | 0 | 3.0 | 7.1 | 2.6 | 7.5 | 50 |
| | | 12.0 | 27.0 | 10.3 | 26.8 | 200 |
| | | 0.4 | 1.3 | 0.38 | 1.3 | 25 |
| | 1 | 1.5 | 3.8 | 1.4 | 3.9 | 50 |
| | | 7.4 | 14.9 | 7.0 | 15.3 | 200 |

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 12. AC electrical specifications at 5 V Range

| Symbol | DSE | Rise time (nS) ¹ | | Fall time (nS) ¹ | | Capacitance (pF) ² |
|--------------------------|-----|-----------------------------|-------|-----------------------------|------|-------------------------------|
| | | Min. | Max . | Min. | Max. | |
| tRF _{GPIO} | NA | 2.8 | 9.4 | 2.9 | 10.7 | 25 |
| | | 5.0 | 15.7 | 5.1 | 17.4 | 50 |
| | | 17.3 | 54.8 | 17.6 | 59.7 | 200 |
| tRF _{GPIO-HD} | 0 | 2.8 | 9.4 | 2.9 | 10.7 | 25 |
| | | 5.0 | 15.7 | 5.1 | 17.4 | 50 |
| | | 17.3 | 54.8 | 17.6 | 59.7 | 200 |
| | 1 | 1.1 | 4.6 | 1.1 | 5.0 | 25 |
| | | 2.0 | 5.7 | 2.0 | 5.8 | 50 |
| | | 5.4 | 16.0 | 5.0 | 16.0 | 200 |
| tRF _{GPIO-FAST} | 0 | 0.42 | 2.2 | 0.37 | 2.2 | 25 |
| | | 2.0 | 5.0 | 1.9 | 5.2 | 50 |
| | | 9.3 | 18.8 | 8.5 | 19.3 | 200 |
| | 1 | 0.37 | 0.9 | 0.35 | 0.9 | 25 |
| | | 1.2 | 2.7 | 1.2 | 2.9 | 50 |
| | | 6.0 | 11.8 | 6.0 | 12.3 | 200 |

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 13. Standard input pin capacitance

| Symbol | Description | Min. | Max. | Unit |
|-------------|---------------------------------|------|------|------|
| C_{IN_D} | Input capacitance: digital pins | — | 7 | pF |

NOTE

Please refer to [External System Oscillator electrical specifications](#) for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 14. Device clock specifications 1

| Symbol | Description | Min. | Max. | Unit |
|---|--------------------------|------|-----------------|------|
| High Speed run mode ² | | | | |
| f_{SYS} | System and core clock | — | 112 | MHz |
| f_{BUS} | Bus clock | — | 56 | MHz |
| f_{FLASH} | Flash clock | — | 28 | MHz |
| Normal run mode (MWCT101xS series) ³ | | | | |
| f_{SYS} | System and core clock | — | 80 | MHz |
| f_{BUS} | Bus clock | — | 40 ⁴ | MHz |
| f_{FLASH} | Flash clock | — | 26.67 | MHz |
| VLPR mode ⁵ | | | | |
| f_{SYS} | System and core clock | — | 4 | MHz |
| f_{BUS} | Bus clock | — | 4 | MHz |
| f_{FLASH} | Flash clock | — | 1 | MHz |
| f_{ERCLK} | External reference clock | — | 16 | MHz |

1. Refer to the section [Feature comparison](#) for the availability of modes and other specifications.
2. Only available on some devices. See section [Feature comparison](#).
3. With SPLL as system clock source.
4. 48 MHz when f_{SYS} is 48 MHz
5. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

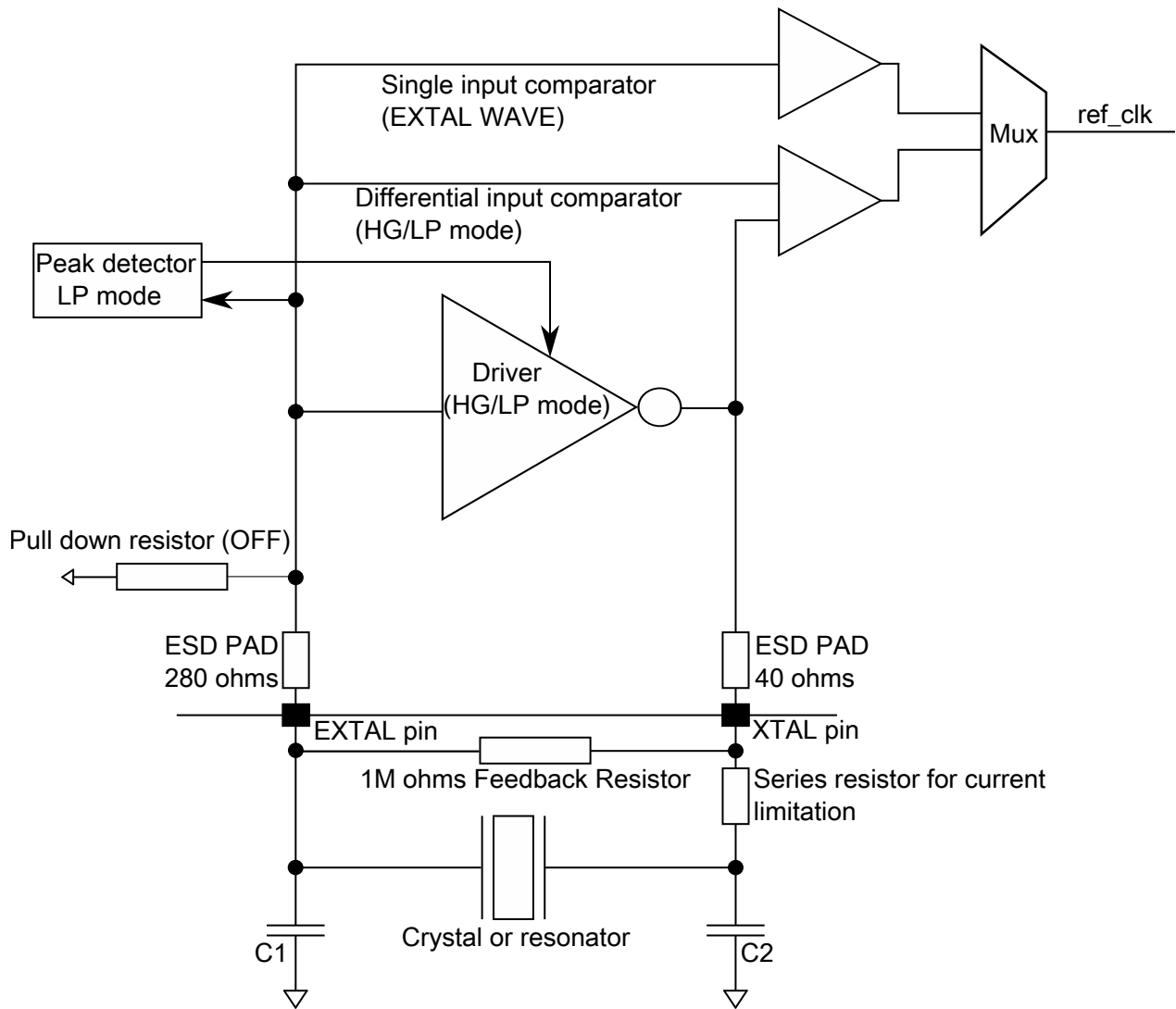


Figure 7. Oscillator connections scheme

Table 15. External System Oscillator electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|--------------------|---|-----------------------|------|------------------------|------|-------|
| g _{mXOSC} | Crystal oscillator transconductance | | | | | |
| | 4-8 MHz | 2.2 | — | 13.7 | mA/V | |
| | 8-40 MHz | 16 | — | 47 | mA/V | |
| V _{IL} | Input low voltage — EXTAL pin in external clock mode | V _{SS} | — | 0.35 * V _{DD} | V | |
| V _{IH} | Input high voltage — EXTAL pin in external clock mode | 0.7 * V _{DD} | — | V _{DD} | V | |
| C ₁ | EXTAL load capacitance | — | — | — | | 1 |
| C ₂ | XTAL load capacitance | — | — | — | | 1 |
| R _F | Feedback resistor | | | | | 2 |
| | Low-gain mode (HGO=0) | — | — | — | MΩ | |

Table continues on the next page...

Table 15. External System Oscillator electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------|---|------|------|------|------|-------|
| | High-gain mode (HGO=1) | — | 1 | — | MΩ | |
| R _S | Series resistor | | | | | |
| | Low-gain mode (HGO=0) | — | 0 | — | kΩ | |
| | High-gain mode (HGO=1) | — | 0 | — | kΩ | |
| V _{pp} | Peak-to-peak amplitude of oscillation (oscillator mode) | | | | | 3 |
| | Low-gain mode (HGO=0) | — | 1.0 | — | V | |
| | High-gain mode (HGO=1) | — | 3.3 | — | V | |

1. Crystal oscillator circuit provides stable oscillations when $g_{mXOSC} > 5 * gm_crit$. The gm_crit is defined as:

$$gm_crit = 4 * ESR * (2\pi F)^2 * (C_0 + C_L)^2$$

where:

- g_{mXOSC} is the transconductance of the internal oscillator circuit
- ESR is the equivalent series resistance of the external crystal
- F is the external crystal oscillation frequency
- C_0 is the shunt capacitance of the external crystal
- C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2 / (C_1 + C_2)]$
- C_s is stray or parasitic capacitance on the pin due to any PCB traces
- C_1, C_2 external load capacitances on EXTAL and XTAL pins

See manufacture datasheet for external crystal component values

2. • When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
• When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Table 16. External System Oscillator frequency specifications

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|-----------------------|--|------|------|------|------|-------|
| f _{osc_hi} | Oscillator crystal or resonator frequency | 4 | — | 40 | MHz | |
| f _{ec_extal} | Input clock frequency (external clock mode) | — | — | 50 | MHz | 1 |
| t _{dc_extal} | Input clock duty cycle (external clock mode) | 48 | 50 | 52 | % | 1 |
| t _{cst} | Crystal Start-up Time | | | | | 2 |
| | 8 MHz low-gain mode (HGO=0) | — | 1.5 | — | ms | |
| | 8 MHz high-gain mode (HGO=1) | — | 2.5 | — | | |
| | 40 MHz low-gain mode (HGO=0) | — | 2 | — | | |
| | 40 MHz high-gain mode (HGO=1) | — | 2 | — | | |

1. Frequencies below 40 MHz can be used for degraded duty cycle up to 40-60%
2. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 System Clock Generation (SCG) specifications

6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 17. Fast internal RC Oscillator electrical specifications

| Symbol | Parameter ¹ | Value | | | Unit |
|-------------------------------|--|-------|------|------|--------------------|
| | | Min. | Typ. | Max. | |
| F _{FIRC} | FIRC target frequency | — | 48 | — | MHz |
| ΔF | Frequency deviation across process, voltage, and temperature < 105°C | — | ±0.5 | ±1 | %F _{FIRC} |
| ΔF125 | Frequency deviation across process, voltage, and temperature < 125°C | — | ±0.5 | ±1.1 | %F _{FIRC} |
| T _{Startup} | Startup time | | 3.4 | 5 | μs ² |
| T _{JIT} ³ | Cycle-to-Cycle jitter | — | 250 | 500 | ps |
| T _{JIT} ³ | Long term jitter over 1000 cycles | — | 0.04 | 0.1 | %F _{FIRC} |

1. With FIRC regulator enable
2. Startup time is defined as the time between clock enablement and clock availability for system use.
3. FIRC as system clock

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 18. Slow internal RC oscillator (SIRC) electrical specifications

| Symbol | Parameter | Value | | | Unit |
|----------------------|--|-------|------|------|--------------------|
| | | Min. | Typ. | Max. | |
| F _{SIRC} | SIRC target frequency | — | 8 | — | MHz |
| ΔF | Frequency deviation across process, voltage, and temperature < 105°C | — | — | ±3 | %F _{SIRC} |
| ΔF125 | Frequency deviation across process, voltage, and temperature < 125°C | — | — | ±3.3 | %F _{SIRC} |
| T _{Startup} | Startup time | — | 9 | 12.5 | μs ¹ |

1. Startup time is defined as the time between clock enablement and clock availability for system use.

6.2.4 Low Power Oscillator (LPO) electrical specifications

Table 19. Low Power Oscillator (LPO) electrical specifications

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|----------------------|---|------|------|------|------|
| F _{LPO} | Internal low power oscillator frequency | 113 | 128 | 139 | kHz |
| T _{startup} | Startup Time | — | — | 20 | μs |

6.2.5 SPLL electrical specifications

Table 20. SPLL electrical specifications

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|--------------------------------------|--|--------|------|--|------|
| F _{SPLL_REF} ¹ | PLL Reference Frequency Range | 8 | — | 16 | MHz |
| F _{SPLL_Input} ² | PLL Input Frequency | 8 | — | 40 | MHz |
| F _{VCO_CLK} | VCO output frequency | 180 | — | 320 | MHz |
| F _{SPLL_CLK} | PLL output frequency | 90 | — | 160 | MHz |
| J _{CYC_SPLL} | PLL Period Jitter (RMS) ³ | | | | |
| | at F _{VCO_CLK} 180 MHz | — | 120 | — | ps |
| | at F _{VCO_CLK} 320 MHz | — | 75 | — | ps |
| J _{ACC_SPLL} | PLL accumulated jitter over 1μs (RMS) ³ | | | | |
| | at F _{VCO_CLK} 180 MHz | — | 1350 | — | ps |
| | at F _{VCO_CLK} 320 MHz | — | 600 | — | ps |
| D _{UNL} | Lock exit frequency tolerance | ± 4.47 | — | ± 5.97 | % |
| T _{SPLL_LOCK} | Lock detector detection time ⁴ | — | — | 150 × 10 ⁻⁶ + 1075(1/F _{SPLL_REF}) | s |

1. F_{SPLL_REF} is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLL_CFG register of Reference Manual.
2. F_{SPLL_Input} is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

6.3 Memory and memory interfaces

6.3.1 Flash memory module (FTFC) electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — commands

Table 21. Flash command timing specifications

| Symbol | Description ¹ | | MWCT1014S | | MWCT1015S | | MWCT1016S | | Unit | Notes |
|-----------------------|---|---------------------|-----------|------|-----------|-------|-----------|-------|------|-------|
| | | | Typ | Max | Typ | Max | Typ | Max | | |
| t _{rd1blk} | Read 1 Block execution time | 32 KB flash | — | — | — | — | — | — | ms | |
| | | 64 KB flash | — | 0.5 | — | 0.5 | — | — | | |
| | | 128 KB flash | — | — | — | — | — | — | | |
| | | 256 KB flash | — | — | — | — | — | — | | |
| | | 512 KB flash | — | 1.8 | — | 2 | — | 2 | | |
| t _{rd1sec} | Read 1 Section execution time | 2 KB flash | — | 75 | — | 75 | — | 75 | μs | |
| | | 4 KB flash | — | 100 | — | 100 | — | 100 | | |
| t _{pgmchk} | Program Check execution time | — | — | 95 | — | 95 | — | 100 | μs | |
| t _{pgm8} | Program Phrase execution time | — | 90 | 225 | 90 | 225 | 90 | 225 | μs | |
| t _{ersblk} | Erase Flash Block execution time | 32 KB flash | — | — | — | — | — | — | ms | 2 |
| | | 64 KB flash | 30 | 550 | 30 | 550 | — | — | | |
| | | 128 KB flash | — | — | — | — | — | — | | |
| | | 256 KB flash | — | — | — | — | — | — | | |
| | | 512 KB flash | 250 | 4250 | 250 | 4250 | 250 | 4250 | | |
| t _{ersscr} | Erase Flash Sector execution time | — | 12 | 130 | 12 | 130 | 12 | 130 | ms | 2 |
| t _{pgmsec1k} | Program Section execution time (1KB flash) | — | 5 | — | 5 | — | 5 | — | ms | |
| t _{rd1all} | Read 1s All Block execution time | — | — | 2.3 | — | 5.2 | — | 8.2 | ms | |
| t _{rdonce} | Read Once execution time | — | — | 30 | — | 30 | — | 30 | μs | |
| t _{pgmonce} | Program Once execution time | — | 90 | — | 90 | — | 90 | — | μs | |
| t _{ersall} | Erase All Blocks execution time | — | 400 | 4900 | 700 | 10000 | 1400 | 17000 | ms | 2 |
| t _{vykey} | Verify Backdoor Access Key execution time | — | — | 35 | — | 35 | — | 35 | μs | |
| t _{ersallu} | Erase All Blocks Unsecure execution time | — | 400 | 4900 | 700 | 10000 | 1400 | 17000 | ms | 2 |
| t _{pgmpart} | Program Partition for EEPROM execution time | 32 KB EEPROM backup | 70 | — | 70 | — | — | — | ms | 3 |
| | | 64 KB EEPROM backup | 71 | — | 71 | — | 150 | — | | |

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

| Symbol | Description ¹ | | MWCT1014S | | MWCT1015S | | MWCT1016S | | Unit | Notes |
|-------------------------|---|---|-----------|------|-----------|------|-----------|------|------|-------|
| | | | Typ | Max | Typ | Max | Typ | Max | | |
| t _{setram} | Set FlexRAM Function execution time | Control Code 0xFF | 0.08 | — | 0.08 | — | 0.08 | — | ms | 3 |
| | | 32 KB EEPROM backup | 0.8 | 1.2 | 0.8 | 1.2 | — | — | | |
| | | 48 KB EEPROM backup | 1 | 1.5 | 1 | 1.5 | — | — | | |
| | | 64 KB EEPROM backup | 1.3 | 1.9 | 1.3 | 1.9 | 1.3 | 1.9 | | |
| t _{eewr8b} | Byte write to FlexRAM execution time | 32 KB EEPROM backup | 385 | 1700 | 385 | 1700 | — | — | μs | 3-4 |
| | | 48 KB EEPROM backup | 430 | 1850 | 430 | 1850 | — | — | | |
| | | 64 KB EEPROM backup | 475 | 2000 | 475 | 2000 | 475 | 4000 | | |
| t _{eewr16b} | 16-bit write to FlexRAM execution time | 32 KB EEPROM backup | 385 | 1700 | 385 | 1700 | — | — | μs | 3-4 |
| | | 48 KB EEPROM backup | 430 | 1850 | 430 | 1850 | — | — | | |
| | | 64 KB EEPROM backup | 475 | 2000 | 475 | 2000 | 475 | 4000 | | |
| t _{eewr32bers} | 32-bit write to erased FlexRAM location execution time | — | 360 | 2000 | 360 | 2000 | 360 | 2000 | μs | |
| t _{eewr32b} | 32-bit write to FlexRAM execution time | 32 KB EEPROM backup | 630 | 2000 | 630 | 2000 | — | — | μs | 3-4 |
| | | 48 KB EEPROM backup | 720 | 2125 | 720 | 2125 | — | — | | |
| | | 64 KB EEPROM backup | 810 | 2250 | 810 | 2250 | 810 | 4500 | | |
| t _{quickwr} | 32-bit Quick Write execution time: Time from CCIF clearing (start the write) until CCIF setting (32-bit write | 1st 32-bit write | 200 | 550 | 200 | 550 | 200 | 1100 | μs | 4-5-6 |
| | | 2nd through Next to Last (Nth-1) 32-bit write | 150 | 550 | 150 | 550 | 150 | 550 | | |

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

| Symbol | Description ¹ | | MWCT1014S | | MWCT1015S | | MWCT1016S | | Unit | Notes |
|---------------------------|--|--|-----------|----------------------------|-----------|----------------------------|-----------|----------------------------|------|-------|
| | | | Typ | Max | Typ | Max | Typ | Max | | |
| | complete, ready for next 32-bit write) | Last (Nth) 32-bit write (time for write only, not cleanup) | 200 | 550 | 200 | 550 | 200 | 550 | | |
| $t_{\text{quickwrClnup}}$ | Quick Write Cleanup execution time | — | — | (# of Quick Writes) * 2.0 | — | (# of Quick Writes) * 2.0 | — | (# of Quick Writes) * 2.0 | ms | 7 |

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record cleanup has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 1st time EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. Only after the Nth write completes will any data be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power on reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write times may take up to 550 μ s, as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

6.3.1.2 Reliability specifications**Table 22. NVM reliability specifications**

| Symbol | Description | Min. | Typ. | Max. | Unit | Notes |
|---|---|-------|------|------|--------|---------|
| When using as Program and Data Flash | | | | | | |
| $t_{\text{nmwretp1k}}$ | Data retention after up to 1 K cycles | 20 | — | — | years | 1 |
| η_{nmwrcycp} | Cycling endurance | 1 K | — | — | cycles | 2, 3 |
| When using FlexMemory feature: FlexRAM as Emulated EEPROM | | | | | | |
| t_{nmwretee} | Data retention | 5 | — | — | years | 4 |
| η_{nmwree16} | Write endurance | 100 K | — | — | writes | 5, 6, 7 |
| $\eta_{\text{nmwree256}}$ | • EEPROM backup to FlexRAM ratio = 16 • EEPROM backup to FlexRAM ratio = 256 | 1.6 M | — | — | writes | |

1. Data retention period per block begins upon initial user factory programming or after each subsequent erase.
2. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
3. Cycling endurance is per DFlash or PFlash Sector.
4. Data retention period per block begins upon initial user factory programming or after each subsequent erase. Background maintenance operations during normal FlexRAM usage extend effective data retention life beyond 5 years.

5. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across product temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
6. For usage of any EEE driver other than the FlexMemory feature, the endurance spec will fall back to the specified endurance value of the D-Flash specification (1K).
7. [FlexMemory calculator tool](#) is available at NXP web site for help in estimation of the maximum write endurance achievable at specific EEPROM/FlexRAM ratios. The “In Spec” portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- QuadSPI trace length should be 3 inches.
- For non-Quad mode of operation if external device doesn't have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

Table 23. QuadSPI electrical specifications

| FLASH PORT | Sym | Unit | FLASH A | | | | | | | | | | | | FLASH B | | | | | | | | |
|---------------------|------------------|------|--------------------|------|--------------------|--------------|--------------------|-------------------|--------------------|------|--------------------|------|--------------------|--------------|------------------------|------|-------------------|------------------|------|------|--------------|------|------|
| | | | RUN ¹ | | | | | | HSRUN ¹ | | | | | | RUN/HSRUN ² | | | | | | | | |
| | | | SDR | | | Internal DQS | | | Internal Sampling | | | SDR | | | Internal Sampling | | | DDR ³ | | | | | |
| | | | Internal Sampling | N1 | Min | Max | PAD Loopback | Internal Loopback | Min | Max | N1 | Min | Max | PAD Loopback | Internal Loopback | Min | Max | N1 | Min | Max | External DQS | Min | Max |
| Register Settings | | | | | | | | | | | | | | | | | | | | | | | |
| MCR[DDR_EN] | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| MCR[DQS_EN] | | - | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| MCR[SCLKCFG[0]] | | - | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| MCR[SCLKCFG[1]] | | - | - | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| MCR[SCLKCFG[2]] | | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 0 |
| MCR[SCLKCFG[3]] | | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 0 |
| MCR[SCLKCFG[5]] | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| SMPR[FSPHS] | | - | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SMPR[FSPLY] | | - | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| SOCRR | | - | - | 0 | 23 | - | - | - | - | - | 0 | 0 | 30 | - | - | - | - | - | - | - | - | - | - |
| [SOCCFG[7:0]] | | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | 30 |
| SOCCR[SOCCFG[15:8]] | | - | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x00 | 0x01 | 0x01 |
| Timing Parameters | | | | | | | | | | | | | | | | | | | | | | | |
| SCK Clock Frequency | f _{sck} | MHZ | - | 38 | - | 64 | - | 48 | - | 40 | - | 80 | - | 50 | - | 20 | - | 20 ⁴ | | | | | |
| SCK Clock Period | t _{sck} | ns | 1/f _{sck} | - | 1/f _{sck} | - | 1/f _{sck} | - | 1/f _{sck} | - | 1/f _{sck} | - | 1/f _{sck} | - | 50.0 | - | 50.0 ⁴ | - | - | - | - | - | - |

Table continues on the next page...

Table 23. QuadSPI electrical specifications (continued)

| FLASH PORT | Sym | Unit | FLASH A | | | | | | | | | | | | FLASH B | | | |
|-----------------------------|--------------------|------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|----------------------------|----------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| | | | RUN ¹ | | | | HSRUN ¹ | | | | SDR | | | | SDR | | DDR ³ | |
| QuadSPI Mode | | | Internal Sampling | | | | Internal DQS | | | | Internal DQS | | | | Internal Sampling | | External DQS | |
| | | | N1 | | Internal Loopback | | N1 | | PAD Loopback | | Internal Loopback | | N1 | | External DQS | | External DQS | |
| | | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max |
| SCK Duty Cycle | t _{SDC} | ns | t _{SCK/2} - 1.5 | t _{SCK/2} + 1.5 | t _{SCK/2} - 1.5 | t _{SCK/2} + 1.5 | t _{SCK/2} - 1.5 | t _{SCK/2} + 1.5 | t _{SCK/2} - 0.750 | t _{SCK/2} - 0.750 | t _{SCK/2} - 1.5 | t _{SCK/2} + 1.5 | t _{SCK/2} - 2.5 | t _{SCK/2} - 2.5 | t _{SCK/2} - 2.5 | t _{SCK/2} + 2.5 | t _{SCK/2} - 2.5 | t _{SCK/2} + 2.5 |
| Data Input Setup Time | t _{IS} | ns | 15 | - | 2.5 | - | 10 | - | 1.6 | - | 9 | - | 25 | - | 2 | - | - | - |
| Data Input Hold Time | t _{IH} | ns | 0 | - | 1 | - | 1 | - | 1 | - | 1 | - | 0 | - | 20 | - | - | - |
| Data Output Valid Time | t _{OV} | ns | - | 4.5 | - | 4.5 | - | 4.5 | - | 4 | - | 4 | - | 10 | - | 10 | - | 10 |
| Data Output In-Valid Time | t _{IV} | ns | - | 5 | - | 5 | - | 5 | - | 3 ⁵ | - | 5 | - | 5 | - | 5 | - | - |
| CS to SCK Time ⁶ | t _{CSCK} | ns | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 10 | - | 10 | - | - | - |
| SCK to CS Time ⁷ | t _{CSCKS} | ns | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - |
| Output Load | | pf | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 | 25 |

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz, Output invalid time is 5 ns.
6. Program register value QuadSPI_FLASHCR[TCSS] = 4'h2
7. Program register value QuadSPI_FLASHCR[TCSH] = 4'h1

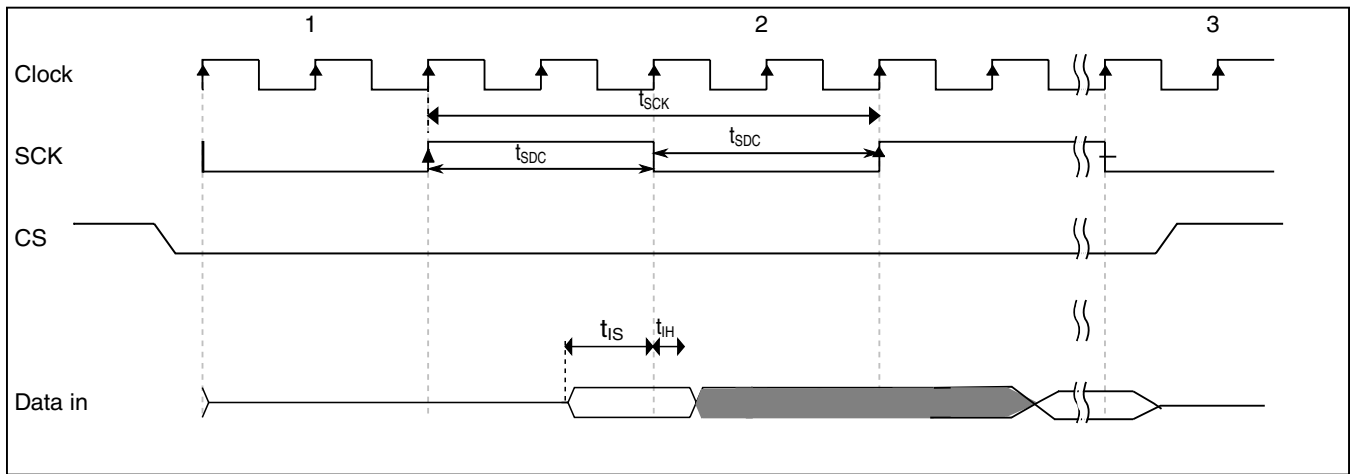


Figure 8. QuadSPI input timing (SDR mode) diagram

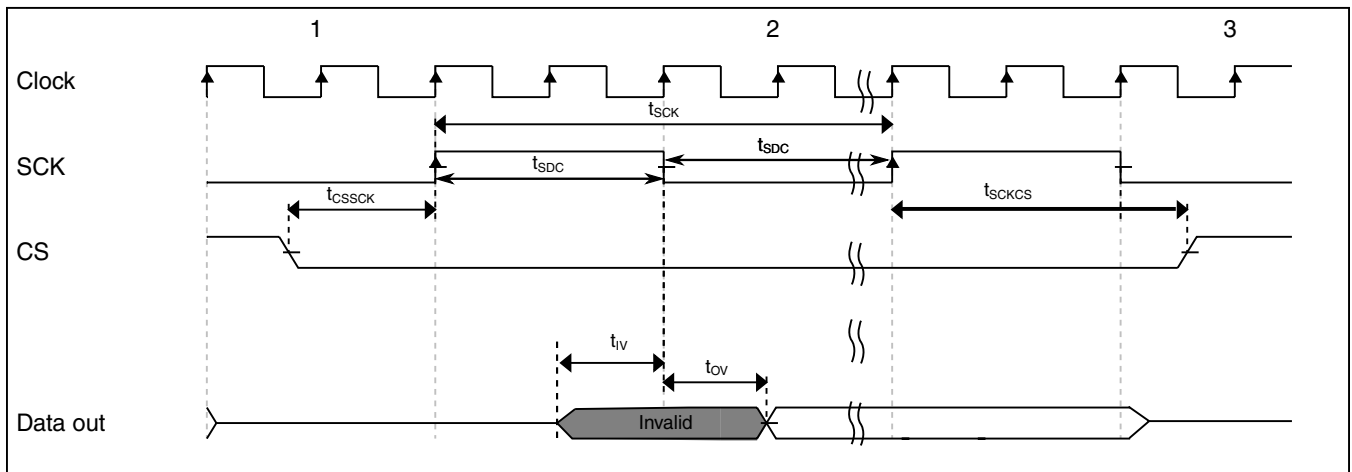
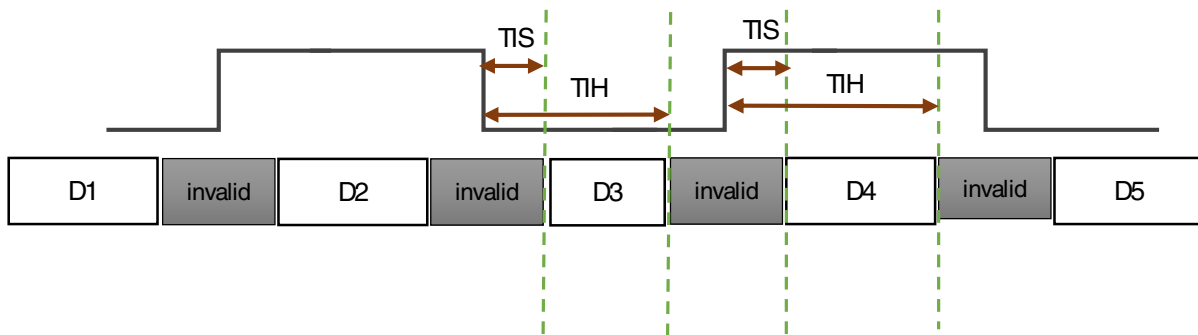


Figure 9. QuadSPI output timing (SDR mode) diagram



TIS – Setup Time
 TIH – Hold Time

Figure 10. QuadSPI input timing (HyperRAM mode) diagram

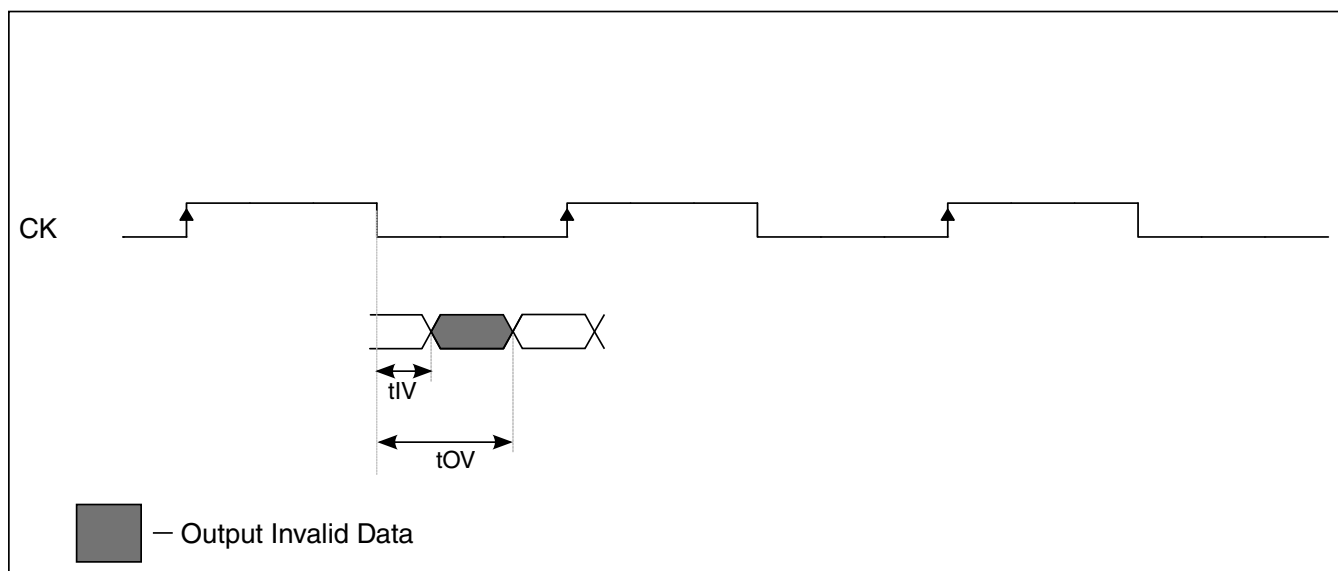


Figure 11. QuadSPI output timing (HyperRAM mode) diagram

6.4 Analog modules

6.4.1 ADC electrical specifications

6.4.1.1 12-bit ADC operating conditions

Table 24. 12-bit ADC operating conditions

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|------------|------------------------------------|--------------------|---|-------------------|---|------------|-------|
| V_{REFH} | ADC reference voltage high | | See Voltage and current operating requirements for values | V_{DDA} | See Voltage and current operating requirements for values | V | 2 |
| V_{REFL} | ADC reference voltage low | | See Voltage and current operating requirements for values | 0 | See Voltage and current operating requirements for values | mV | 2 |
| V_{ADIN} | Input voltage | | V_{REFL} | — | V_{REFH} | V | |
| R_S | Source impedence | $f_{ADCK} < 4$ MHz | — | — | 5 | k Ω | |
| R_{SW1} | Channel Selection Switch Impedance | | — | 0.75 | 1.2 | k Ω | |
| R_{AD} | Sampling Switch Impedance | | — | 2 | 5 | k Ω | |
| C_{P1} | Pin Capacitance | | — | 10 | — | pF | |
| C_{P2} | Analog Bus Capacitance | | — | — | 4 | pF | |
| C_S | Sampling capacitance | | — | 4 | 5 | pF | |

Table continues on the next page...

Table 24. 12-bit ADC operating conditions (continued)

| Symbol | Description | Conditions | Min. | Typ. ¹ | Max. | Unit | Notes |
|-------------------|--------------------------------|---|------|-------------------|-------|------|-------|
| f _{ADCK} | ADC conversion clock frequency | Normal usage | 2 | 40 | 50 | MHz | 3, 4 |
| f _{CONV} | ADC conversion frequency | No ADC hardware averaging. ⁵ Continuous conversions enabled, subsequent conversion time | 46.4 | 928 | 1160 | Ksps | 6, 7 |
| | | ADC hardware averaging set to 32. ⁵ Continuous conversions enabled, subsequent conversion time | 1.45 | 29 | 36.25 | Ksps | 6, 7 |

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
3. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual*.
4. ADC conversion will become less reliable above maximum frequency.
5. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
6. Numbers based on the minimum sampling time of 275 ns.
7. For guidelines and examples of conversion rate calculation, see the *Reference Manual* or download the ADC calculator tool.

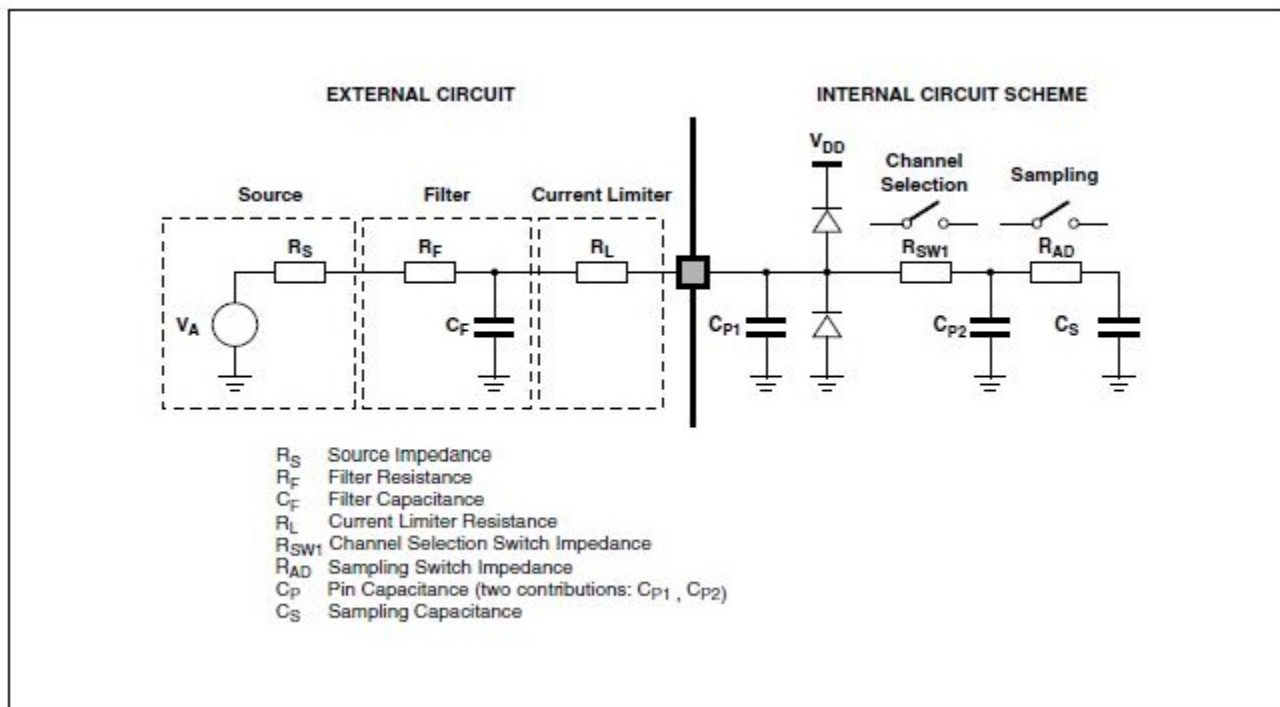


Figure 12. ADC input impedance equivalency diagram

6.4.1.2 12-bit ADC electrical characteristics

NOTE

- ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.
- On reduced pin packages where ADC reference pins are shared with supply pins, ADC analog performance characteristics may be impacted. The amount of variation will be directly impacted by the external PCB layout and hence care must be taken with PCB routing. See [AN5426](#) for details

Table 25. 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|------------------|----------------------------|-------------------------|------|-------------------|--------------------------------------|------------------|------------|
| V_{DDA} | Supply voltage | | 2.7 | — | 3 | V | |
| I_{DDA_ADC} | Supply current per ADC | | — | 0.6 | — | mA | 3 |
| SMPLTS | Sample Time | | 275 | — | Refer to the <i>Reference Manual</i> | ns | |
| TUE ⁴ | Total unadjusted error | | — | ±4 | ±8 | LSB ⁵ | 6, 7, 8, 9 |
| DNL | Differential non-linearity | | — | ±1.0 | — | LSB ⁵ | 6, 7, 8, 9 |
| INL | Integral non-linearity | | — | ±2.0 | — | LSB ⁵ | 6, 7, 8, 9 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}=V_{DD}$, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume $V_{DDA} = 3\text{ V}$, $\text{Temp} = 25\text{ }^{\circ}\text{C}$, $f_{ADCK} = 40\text{ MHz}$, $R_{AS}=20\text{ }\Omega$, and $C_{AS}=10\text{ nF}$.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. $1\text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

Table 26. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

| Symbol | Description | Conditions ¹ | Min. | Typ. ² | Max. | Unit | Notes |
|------------------|----------------------------|-------------------------|------|-------------------|--------------------------------------|------------------|------------|
| V_{DDA} | Supply voltage | | 3 | — | 5.5 | V | |
| I_{DDA_ADC} | Supply current per ADC | | — | 1 | — | mA | 3 |
| SMPLTS | Sample Time | | 275 | — | Refer to the <i>Reference Manual</i> | ns | |
| TUE ⁴ | Total unadjusted error | | — | ±4 | ±8 | LSB ⁵ | 6, 7, 8, 9 |
| DNL | Differential non-linearity | | — | ±0.7 | — | LSB ⁵ | 6, 7, 8, 9 |
| INL | Integral non-linearity | | — | ±1.0 | — | LSB ⁵ | 6, 7, 8, 9 |

1. All accuracy numbers assume the ADC is calibrated with $V_{REFH}=V_{DDA}=V_{DD}$, with the calibration frequency set to less than or equal to half of the maximum specified ADC clock frequency.
2. Typical values assume $V_{DDA} = 5.0$ V, Temp = 25 °C, $f_{ADCK} = 40$ MHz, $R_{AS}=20$ Ω, and $C_{AS}=10$ nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. $1 \text{ LSB} = (V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

- Due to triple bonding in lower pin packages like the 64-LQFP, degradation might be seen in ADC parameters.
- When using high speed interfaces such as the QuadSPI, there may be some ADC degradation on the adjacent analog input paths. See following table for details.

| Pin name | TGATE purpose |
|----------|--------------------|
| PTE8 | CMP0_IN3 |
| PTC3 | ADC0_SE11/CMP0_IN4 |
| PTC2 | ADC0_SE10/CMP0_IN5 |
| PTD7 | CMP0_IN6 |
| PTD6 | CMP0_IN7 |
| PTD28 | ADC1_SE22 |
| PTD27 | ADC1_SE21 |

6.4.2 CMP with 8-bit DAC electrical specifications

Table 28. Comparator with 8-bit DAC electrical specifications

| Symbol | Description | Min. | Typ. | Max. | Unit |
|--------------------|--|------|----------------------|------------------|------|
| I _{DDHS} | Supply current, High-speed mode ¹ | | | | μA |
| | -40 - 125 °C | — | 230 | 300 | |
| I _{DDL} | Supply current, Low-speed mode ¹ | | | | μA |
| | -40 - 105 °C | — | 6 | 11 | |
| | -40 - 125 °C | | 6 | 13 | |
| V _{AIN} | Analog input voltage | 0 | 0 - V _{DDA} | V _{DDA} | V |
| V _{AIO} | Analog input offset voltage, High-speed mode | | | | mV |
| | -40 - 125 °C | -25 | ±1 | 25 | |
| V _{AIO} | Analog input offset voltage, Low-speed mode | | | | mV |
| | -40 - 125 °C | -40 | ±4 | 40 | |
| t _{DHSB} | Propagation delay, High-speed mode ² | | | | ns |
| | -40 - 105 °C | — | 35 | 200 | |
| | -40 - 125 °C | | 35 | 300 | |
| t _{DLSB} | Propagation delay, Low-speed mode ² | | | | μs |
| | -40 - 105 °C | — | 0.5 | 2 | |
| | -40 - 125 °C | — | 0.5 | 3 | |
| t _{DHSS} | Propagation delay, High-speed mode ³ | | | | ns |
| | -40 - 105 °C | — | 70 | 400 | |
| | -40 - 125 °C | — | 70 | 500 | |
| t _{DLSS} | Propagation delay, Low-speed mode ³ | | | | μs |
| | -40 - 105 °C | — | 1 | 5 | |
| | -40 - 125 °C | — | 1 | 5 | |
| t _{IDHS} | Initialization delay, High-speed mode ⁴ | | | | μs |
| | -40 - 125 °C | — | 1.5 | 3 | |
| t _{IDLS} | Initialization delay, Low-speed mode ⁴ | | | | μs |
| | -40 - 125 °C | — | 10 | 30 | |
| V _{HYST0} | Analog comparator hysteresis, Hyst0 | | | | mV |
| | -40 - 125 °C | — | 0 | — | |
| V _{HYST1} | Analog comparator hysteresis, Hyst1, High-speed mode | | | | mV |
| | -40 - 125 °C | — | 19 | 66 | |
| | Analog comparator hysteresis, Hyst1, Low-speed mode | | | | |
| | -40 - 125 °C | — | 15 | 40 | |
| V _{HYST2} | Analog comparator hysteresis, Hyst2, High-speed mode | | | | mV |
| | -40 - 125 °C | — | 34 | 133 | |

Table continues on the next page...

Table 28. Comparator with 8-bit DAC electrical specifications (continued)

| Symbol | Description | Min. | Typ. | Max. | Unit | |
|--------------------|--|-------|------|------|------------------|----|
| | Analog comparator hysteresis, Hyst2, Low-speed mode | | | | | |
| | -40 - 125 °C | — | 23 | 80 | | |
| V _{HYST3} | Analog comparator hysteresis, Hyst3, High-speed mode | | | | mV | |
| | -40 - 125 °C | — | 46 | 200 | | |
| | Analog comparator hysteresis, Hyst3, Low-speed mode | | | | | |
| | -40 - 125 °C | — | 32 | 120 | | |
| I _{DAC8b} | 8-bit DAC current adder (enabled) | | | | | |
| | 3.3V Reference Voltage | — | 6 | 9 | | μA |
| | 5V Reference Voltage | — | 10 | 16 | | μA |
| INL ⁵ | 8-bit DAC integral non-linearity | -0.75 | — | 0.75 | LSB ⁶ | |
| DNL | 8-bit DAC differential non-linearity | -0.5 | — | 0.5 | LSB ⁶ | |
| t _{DDAC} | Initialization and switching settling time | — | — | 30 | μs | |

1. Difference at input > 200mV
2. Applied ± (100 mV + V_{HYST0/1/2/3}+ max. of V_{AIO}) around switch point.
3. Applied ± (30 mV + 2 × V_{HYST0/1/2/3}+ max. of V_{AIO}) around switch point.
4. Applied ± (100 mV + V_{HYST0/1/2/3}).
5. Calculation method used: Linear Regression Least Square Method
6. 1 LSB = V_{reference}/256

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

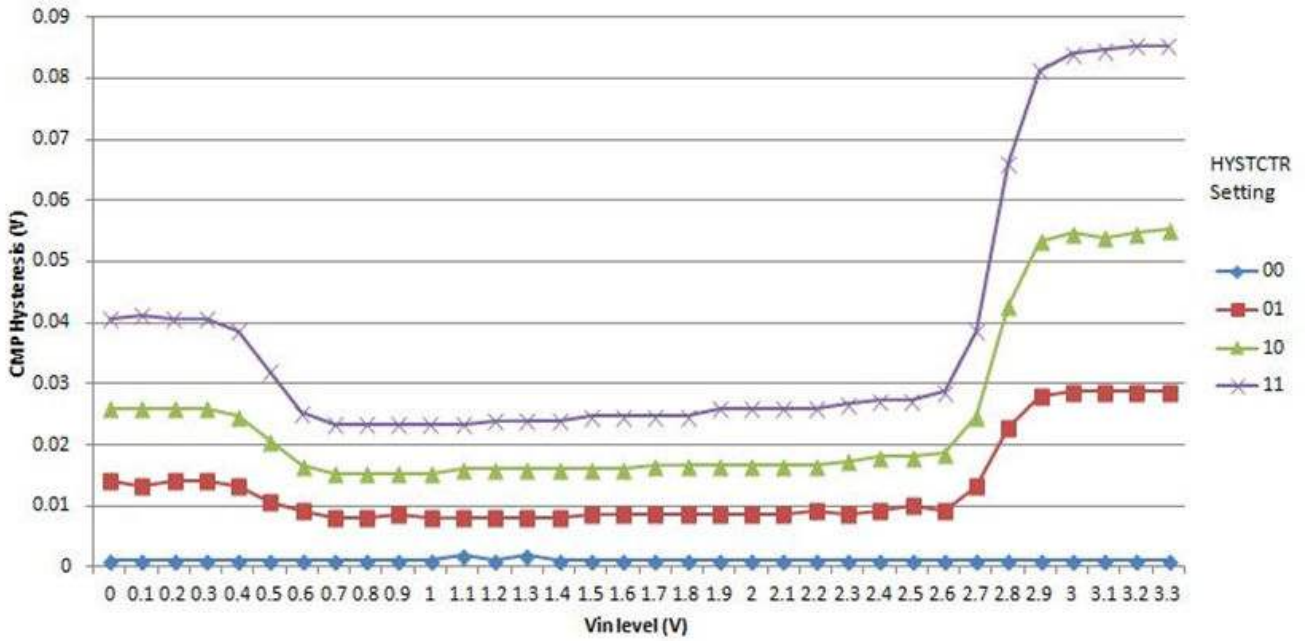


Figure 13. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)

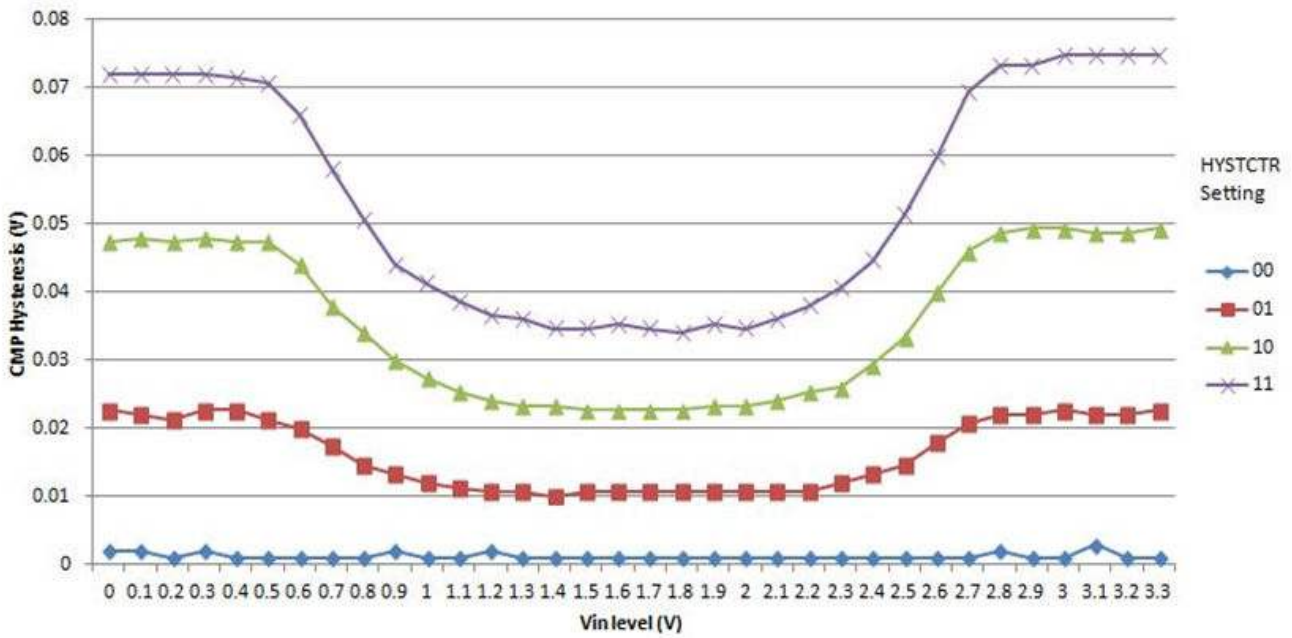


Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

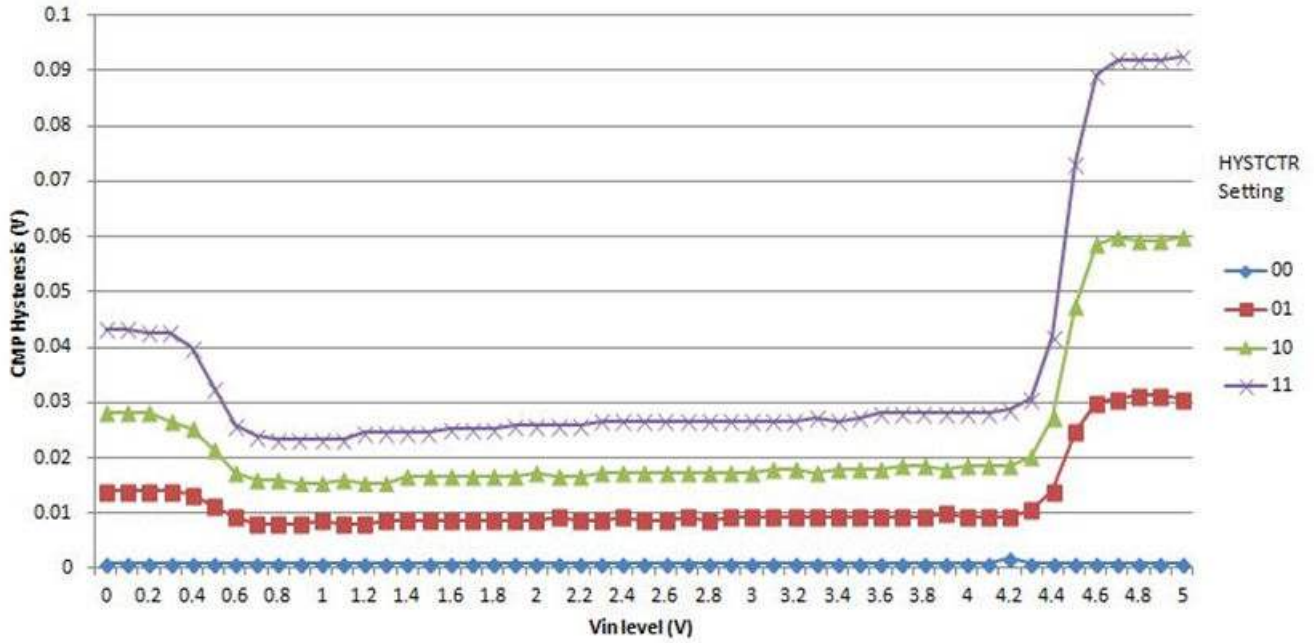


Figure 15. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 0)

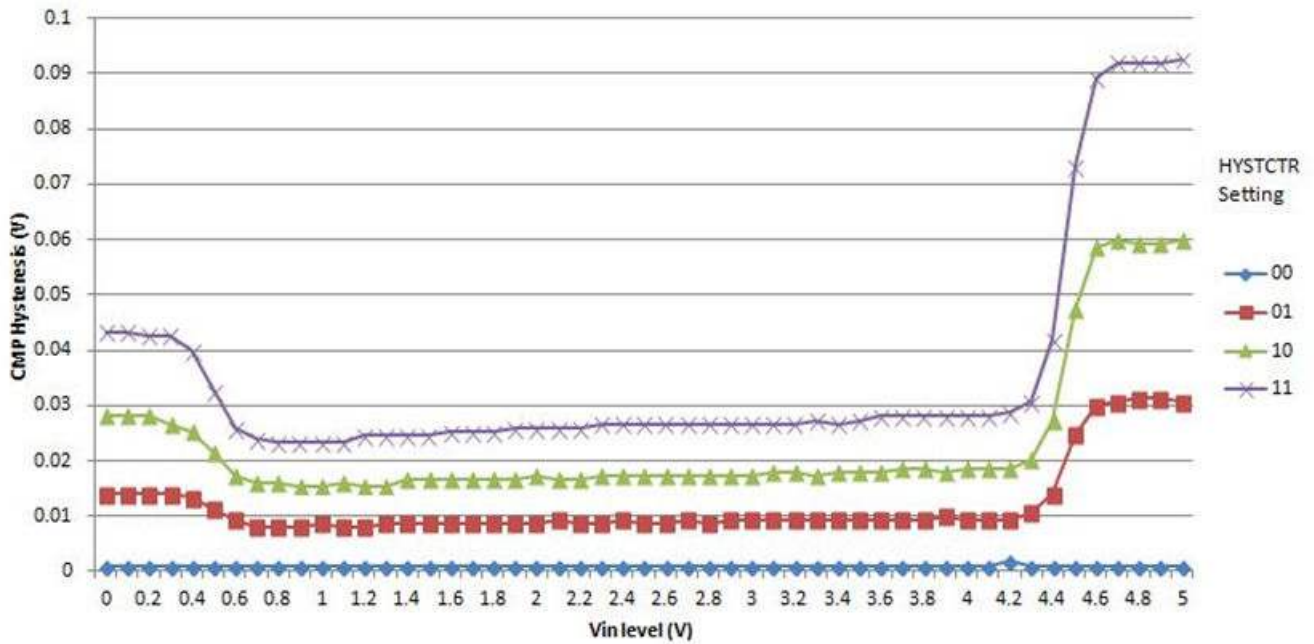


Figure 16. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 1)

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to [General AC specifications](#) for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 29. LPSPi electrical specifications¹

| Num | Symbol | Description | Conditions | Run Mode ² | | | | HSRUN Mode ² | | | | VLPR Mode | | | | Unit |
|-----|------------------------------------|---------------------------------------|------------------------------------|------------------------------------|------|------------------------------------|------|------------------------------------|------|------------------------------------|-----------------|------------------------------------|------|------------------------------------|------|------|
| | | | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | |
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| | f_{periph} ^{3,4} | Peripheral Frequency | Slave | - | 40 | - | 40 | - | 56 | - | 56 | - | 4 | - | 4 | MHz |
| | | | Master | - | 40 | - | 40 | - | 56 | - | 56 | - | 4 | - | 4 | |
| | | | Master Loopback ⁵ | - | 40 | - | 48 | - | 48 | - | 48 | - | 4 | - | 4 | |
| | | | Master Loopback(slow) ⁶ | - | 48 | - | 48 | - | 48 | - | 48 | - | 4 | - | 4 | |
| 1 | f_{op} | Frequency of operation | Slave | - | 10 | - | 10 | - | 14 | - | 14 ⁷ | - | 2 | - | 2 | MHz |
| | | | Master | - | 10 | - | 10 | - | 14 | - | 14 ⁷ | - | 2 | - | 2 | |
| | | | Master Loopback ⁵ | - | 20 | - | 12 | - | 24 | - | 12 | - | 2 | - | 2 | |
| | | | Master Loopback(slow) ⁶ | - | 12 | - | 12 | - | 12 | - | 12 | - | 2 | - | 2 | |
| 2 | t_{SPSCK} | SPSCK period | Slave | 100 | - | 100 | - | 72 | - | 72 | - | 500 | - | 500 | - | ns |
| | | | Master | 100 | - | 100 | - | 72 | - | 72 | - | 500 | - | 500 | - | |
| | | | Master Loopback ⁵ | 50 | - | 83 | - | 42 | - | 83 | - | 500 | - | 500 | - | |
| | | | Master Loopback(slow) ⁶ | 83 | - | 83 | - | 83 | - | 83 | - | 500 | - | 500 | - | |
| 3 | t_{Lead} ⁸ | Enable lead time (PCS to SPSCK delay) | Slave | - | - | - | - | - | - | - | - | - | - | - | - | ns |
| | | | Master | - | - | - | - | - | - | - | - | - | - | - | - | |
| | | | Master Loopback ⁵ | (PCSSCK+1)* $t_{\text{periph-25}}$ | - | (PCSSCK+1)* $t_{\text{periph-25}}$ | - | (PCSSCK+1)* $t_{\text{periph-25}}$ | - | (PCSSCK+1)* $t_{\text{periph-25}}$ | - | (PCSSCK+1)* $t_{\text{periph-50}}$ | - | (PCSSCK+1)* $t_{\text{periph-50}}$ | - | |
| | | | Master Loopback(slow) ⁶ | (PCSSCK+1)* $t_{\text{periph-25}}$ | - | (PCSSCK+1)* $t_{\text{periph-25}}$ | - | (PCSSCK+1)* $t_{\text{periph-25}}$ | - | (PCSSCK+1)* $t_{\text{periph-25}}$ | - | (PCSSCK+1)* $t_{\text{periph-50}}$ | - | (PCSSCK+1)* $t_{\text{periph-50}}$ | - | |

Table continues on the next page...

Table 29. LPSPi electrical specifications¹ (continued)

| Num | Symbol | Description | Conditions | Run Mode ² | | | | HSRUN Mode ² | | | | VLPR Mode | | | | Unit | |
|-----|---------------|--|------------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|------|---------------------------------|
| | | | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | | |
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 4 | t_{Lag}^9 | Enable lag time (After SPSPCK delay) | Slave | - | - | - | - | - | - | - | - | - | - | - | - | ns | |
| | | | Master | - | - | - | - | - | - | - | - | - | - | - | - | | - |
| | | | Master Loopback ⁵ | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | | (SCKPCS+1)* t_{periph}^6 - 25 |
| | | | Master Loopback(slow) ⁶ | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | (SCKPCS+1)* t_{periph}^6 - 25 | | (SCKPCS+1)* t_{periph}^6 - 25 |
| 5 | $t_{wSPSPCK}$ | Clock(SPSPCK) high or low time (SPSPCK duty cycle) | Slave | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | t_{SPSPCK}^{2+3} | ns | |
| | | | Master | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | | |
| | | | Master Loopback ⁵ | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | | |
| | | | Master Loopback(slow) ⁶ | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | t_{SPSPCK}^{2-3} | | |
| | | | Slave | 3 | 5 | 3 | 5 | 3 | 5 | 3 | 5 | 3 | 5 | 3 | 5 | | |
| 6 | t_{su} | Data setup time(inputs) | Slave | 29 | 38 | 26 | 37 ¹⁰ | 18 | 72 | 18 | 78 | 18 | 78 | 18 | 78 | ns | |
| | | | Master | 7 | 8 | 5 | 32 ¹¹ | 20 | 20 | 20 | 20 | 20 | 20 | 20 | | | |
| | | | Master Loopback ⁵ | 8 | 10 | 7 | 9 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | | | |
| | | | Master Loopback(slow) ⁶ | 3 | 3 | 3 | 3 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | | | |
| | | | Slave | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| 7 | t_{HI} | Data hold time(inputs) | Slave | 3 | 3 | 3 | 3 | 14 | 14 | 14 | 14 | 14 | 14 | 14 | ns | | |
| | | | Master | 3 | 3 | 2 | 3 | 11 | 11 | 11 | 11 | 11 | 11 | 11 | | | |
| | | | Master Loopback ⁵ | 3 | 3 | 3 | 3 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | | | |
| | | | Master Loopback(slow) ⁶ | 3 | 3 | 3 | 3 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | | | |
| | | | Slave | 3 | 3 | 3 | 3 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | | | |

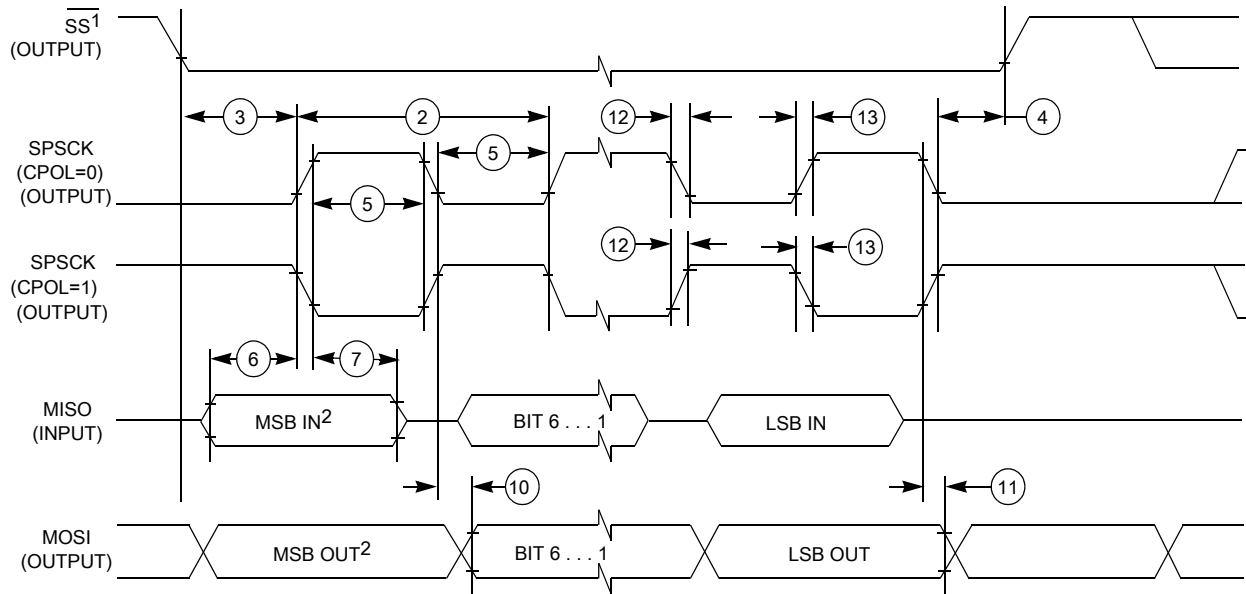
Table continues on the next page...

Table 29. LPSPi electrical specifications¹ (continued)

| Num | Symbol | Description | Conditions | Run Mode ² | | | | | | HSRUN Mode ² | | | | | | VLPR Mode | | | | | | Unit |
|-----|-------------|--------------------------------|------------------------------------|-----------------------|------|----------|------|----------|------|-------------------------|--------------------------------------|----------|------|----------|------|-----------|------|----------|------|-----|----|------|
| | | | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | | | |
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | | |
| 8 | t_a | Slave access time | Slave | - | 50 | - | 50 | - | 50 | - | 50 | - | 50 | - | 100 | - | 100 | - | 100 | ns | | |
| 9 | t_{dis} | Slave MISO (SOUT) disable time | Slave | - | 50 | - | 50 | - | 50 | - | 50 | - | 50 | - | 100 | - | 100 | - | 100 | ns | | |
| 10 | t_v | Data valid (after SPSCK edge) | Slave | - | 30 | - | 39 | - | 26 | - | 36 ¹⁰ 31 ¹¹ | - | 92 | - | 96 | - | 96 | - | 96 | ns | | |
| | | | Master | - | 12 | - | 16 | - | 11 | - | 15 | - | 47 | - | 48 | - | 48 | - | 48 | | | |
| | | | Master Loopback ⁵ | - | 12 | - | 16 | - | 11 | - | 15 | - | 47 | - | 48 | - | 48 | - | 48 | | | |
| 11 | t_{HO} | Data hold time(outputs) | Master Loopback(slow) ⁶ | - | 8 | - | 10 | - | 7 | - | 9 | - | 44 | - | 44 | - | 44 | - | 44 | | | |
| | | | Slave | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | 4 | ns | |
| | | | Master | -15 | - | -22 | - | -15 | - | -23 | - | -22 | - | -29 | - | -29 | - | -29 | - | -29 | | |
| | | | Master Loopback ⁵ | -10 | - | -14 | - | -10 | - | -14 | - | -14 | - | -19 | - | -19 | - | -19 | - | -19 | | |
| | | | Master Loopback(slow) ⁶ | -15 | - | -22 | - | -15 | - | -22 | - | -22 | - | -27 | - | -27 | - | -27 | - | -27 | | |
| | | | Slave | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | ns |
| 12 | $t_{RI/FI}$ | Rise/Fall time input | Master | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | | |
| | | | Master Loopback ⁵ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | |
| | | | Master Loopback(slow) ⁶ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | |
| | | | Slave | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | ns |
| | | | Master | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| | | | Master Loopback ⁵ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| 13 | $t_{RO/FO}$ | Rise/Fall time output | Master Loopback(slow) ⁶ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | | | |
| | | | Slave | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | ns |
| | | | Master | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |
| | | | Master Loopback ⁵ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | |

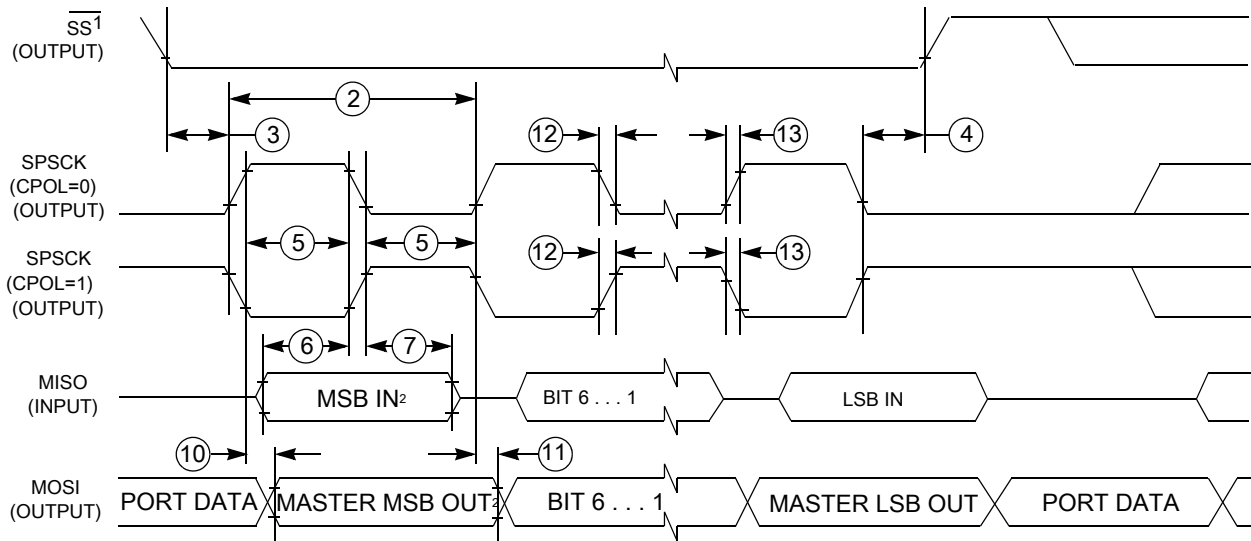
1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPi output clock should not be more than 14 MHz.
3. $f_{\text{periph}} = \text{LPSPi peripheral clock}$
4. $t_{\text{periph}} = 1/f_{\text{periph}}$
5. Master Loopback mode - In this mode LPSPi_SCK clock is delayed for sampling the input data which is enabled by setting LPSPi_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPi0.
6. Master Loopback (slow) - In this mode LPSPi_SCK clock is delayed for sampling the input data which is enabled by setting LPSPi_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPi0.
7. This is the maximum operating frequency (f_{op}) for LPSPi0 with medium PAD type only. Otherwise, the maximum operating frequency (f_{op}) is 12 Mhz.
8. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPi baud rate clock, where PCSSCK ranges from 0 to 255.
9. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPi baud rate clock, where SCKPCS ranges from 0 to 255.
10. Maximum operating frequency (f_{op}) is 12 MHz irrespective of PAD type and LPSPi instance.
11. Applicable for LPSPi0 only with medium PAD type, with maximum operating frequency (f_{op}) as 14 MHz.

Communication modules



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. LPSPI master mode timing (CPHA = 0)



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. LPSPI master mode timing (CPHA = 1)

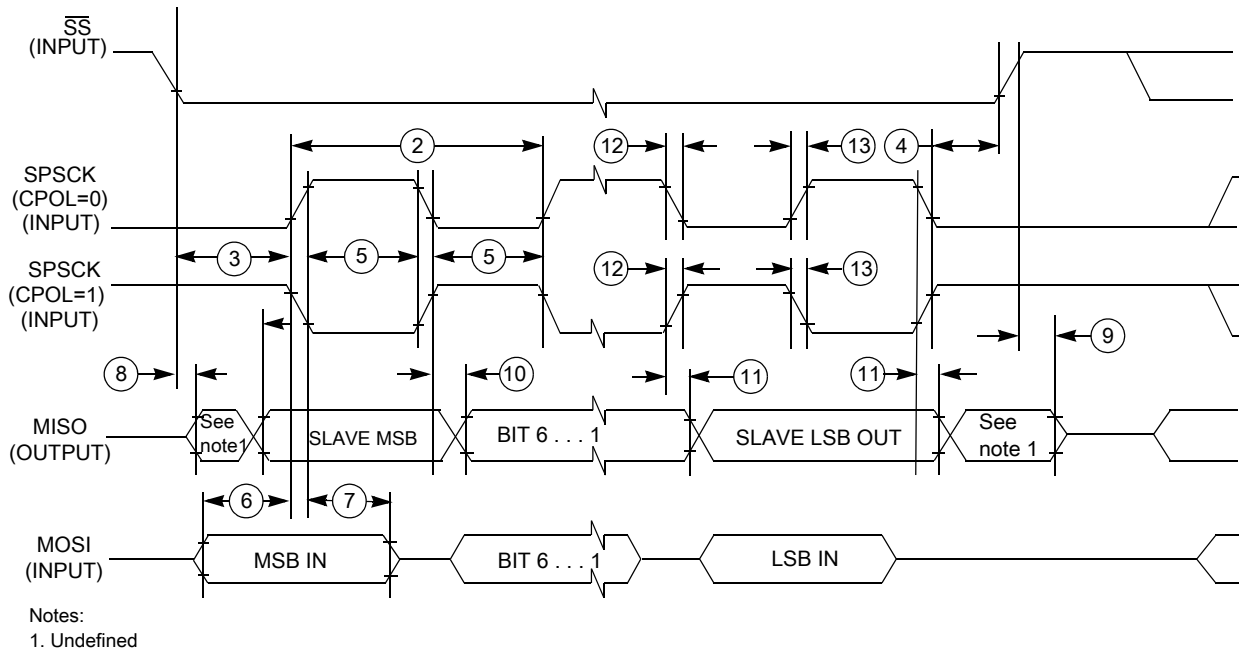


Figure 19. LPSPI slave mode timing (CPHA = 0)

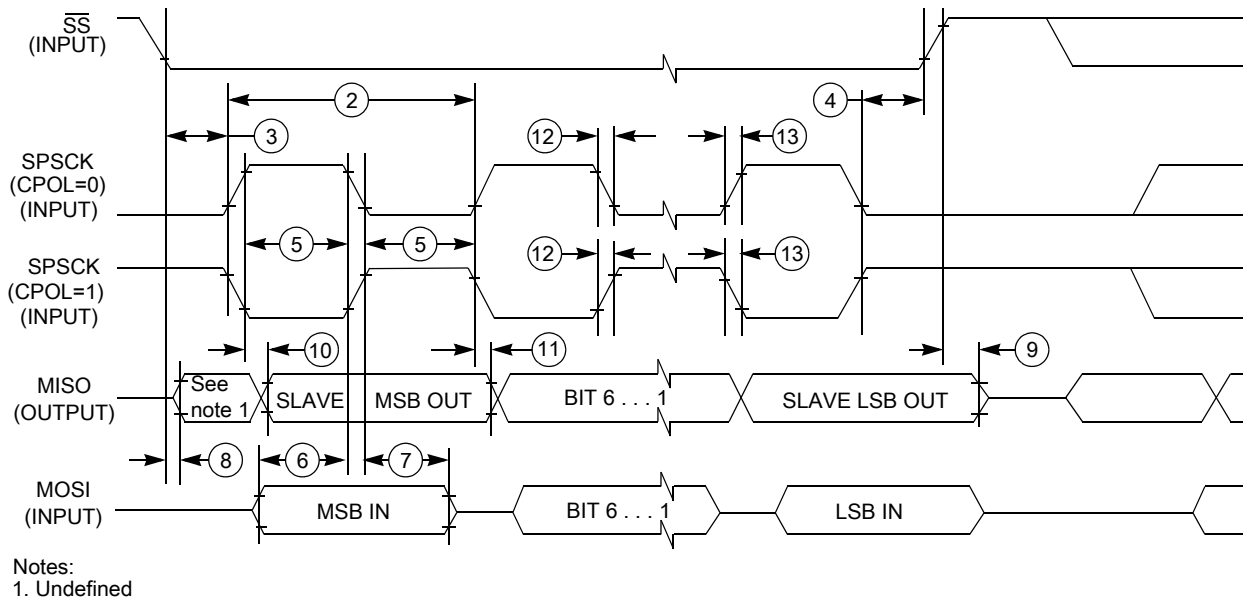


Figure 20. LPSPI slave mode timing (CPHA = 1)

6.5.3 LPI2C electrical specifications

See [General AC specifications](#) for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual*.

6.5.4 FlexCAN electrical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

6.5.5 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specifications

Table 30. SWD electrical specifications

| Symbol | Description | Run Mode | | | | | | HSRUN Mode | | | | | | VLPR Mode | | | | | | Unit |
|--------|---|----------|----------|----------|----------|----------|----------|------------|----------|----------|----------|----------|----------|-----------|----------|----------|----------|-----|--|------|
| | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | | |
| S1 | SWD_CLK frequency of operation | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 25 | - | 10 | - | 10 | MHz | | |
| S2 | SWD_CLK cycle period | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | 1/S1 | - | ns | | |
| S3 | SWD_CLK clock pulse width | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | S2/2 - 5 | S2/2 + 5 | ns | | |
| S4 | SWD_CLK rise and fall times | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | ns | | |
| S9 | SWD_DIO input data setup time to SWD_CLK rise | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | 4 | - | 16 | - | 16 | - | ns | | |
| S10 | SWD_DIO input data hold time after SWD_CLK rise | 3 | - | 3 | - | 3 | - | 3 | - | 3 | - | 3 | - | 10 | - | 10 | - | ns | | |
| S11 | SWD_CLK high to SWD_DIO data valid | - | 28 | - | 38 | - | 28 | - | 28 | - | 38 | - | 28 | - | 70 | - | 77 | ns | | |
| S12 | SWD_CLK high to SWD_DIO high-Z | - | 28 | - | 38 | - | 28 | - | 28 | - | 38 | - | 28 | - | 70 | - | 77 | ns | | |
| S13 | SWD_CLK high to SWD_DIO data invalid | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns | | |

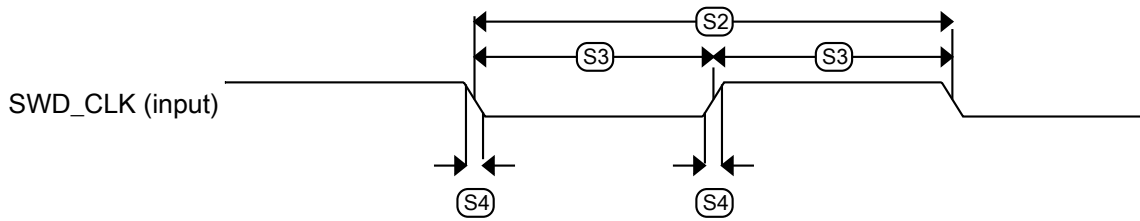


Figure 21. Serial wire clock input timing

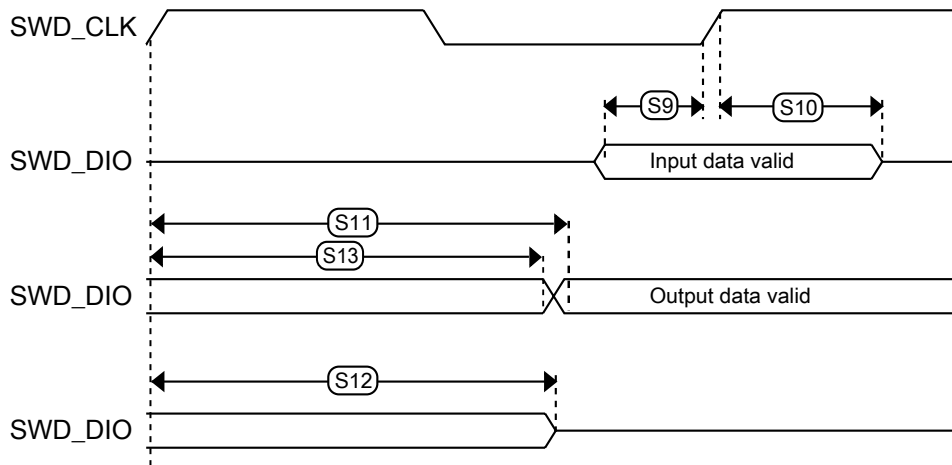


Figure 22. Serial wire data timing

6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 31. Trace specifications

| | Symbol | Description | RUN Mode | | | HSRUN Mode | | VLPR Mode | Unit |
|---|--------|------------------|----------|----|----|------------|----|-----------|------|
| | | | 80 | 48 | 40 | 112 | 80 | | |
| — | Fsys | System frequency | 80 | 48 | 40 | 112 | 80 | 4 | MHz |

Table continues on the next page...

Table 31. Trace specifications (continued)

| | Symbol | Description | RUN Mode | | | HSRUN Mode | | VLPR Mode | Unit |
|--------------------|-------------|---------------------|----------|----|----|------------|-------|-----------|------|
| Trace on fast pads | f_{TRACE} | Max Trace frequency | 80 | 48 | 40 | 74.667 | 80 | 4 | MHz |
| | t_{DVO} | Data Output Valid | 4 | 4 | 4 | 4 | 4 | 20 | ns |
| | t_{DIV} | Data Output Invalid | -2 | -2 | -2 | -2 | -2 | -10 | ns |
| Trace on slow pads | f_{TRACE} | Max Trace frequency | 22.86 | 24 | 20 | 22.4 | 22.86 | 4 | MHz |
| | t_{DVO} | Data Output Valid | 8 | 8 | 8 | 8 | 8 | 20 | ns |
| | t_{DIV} | Data Output Invalid | -4 | -4 | -4 | -4 | -4 | -10 | ns |

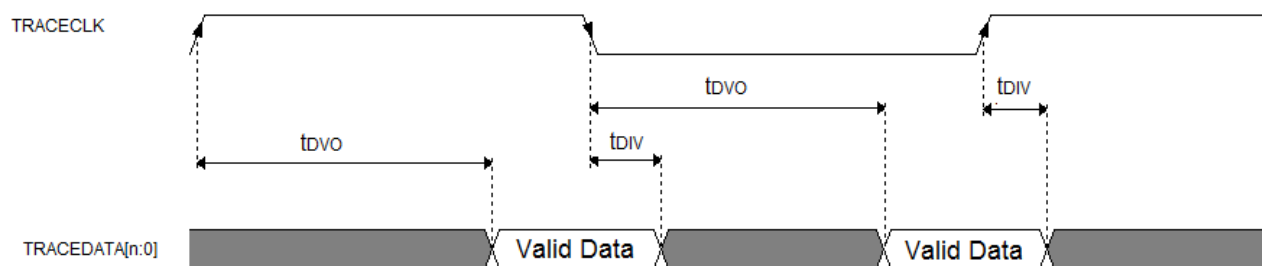


Figure 23. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

Table 32. JTAG electrical specifications

| Symbol | Description | Run Mode | | | | HSRUN Mode | | | | VLPR Mode | | | | Unit | | |
|--------|--|----------|---------|----------|---------|------------|---------|----------|---------|-----------|---------|----------|---------|---------|---------|----|
| | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | 5.0 V IO | | 3.3 V IO | | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | | |
| J1 | TCLK frequency of operation | | | | | | | | | | | | | MHz | | |
| | Boundary Scan | - | 20 | - | 20 | - | 20 | - | 20 | - | 20 | - | 10 | - | 10 | |
| | JTAG | - | 20 | - | 20 | - | 20 | - | 20 | - | 20 | - | 10 | - | 10 | |
| J2 | TCLK cycle period | 1/J1 | - | 1/J1 | - | 1/J1 | - | 1/J1 | - | 1/J1 | - | 1/J1 | - | 1/J1 | - | ns |
| J3 | TCLK clock pulse width | | | | | | | | | | | | | ns | | |
| | Boundary Scan | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | |
| | JTAG | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | J12 - 5 | J12 + 5 | |
| J4 | TCLK rise and fall times | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | - | 1 | ns |
| J5 | Boundary scan input data setup time to TCLK rise | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 15 | - | ns |
| J6 | Boundary scan input data hold time after TCLK rise | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 5 | - | 8 | - | ns |
| J7 | TCLK low to boundary scan output data valid | - | 28 | - | 32 | - | 28 | - | 32 | - | 28 | - | 80 | - | 80 | ns |
| J8 | TCLK low to boundary scan output data invalid | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | |
| J9 | TCLK low to boundary scan output high-Z | - | 28 | - | 32 | - | 28 | - | 32 | - | 28 | - | 80 | - | 80 | ns |
| J10 | TMS, TDI input data setup time to TCLK rise | 3 | - | 3 | - | 3 | - | 3 | - | 3 | - | 3 | - | 15 | - | ns |
| J11 | TMS, TDI input data hold time after TCLK rise | 2 | - | 2 | - | 2 | - | 2 | - | 2 | - | 2 | - | 8 | - | ns |
| J12 | TCLK low to TDO data valid | - | 28 | - | 32 | - | 28 | - | 32 | - | 28 | - | 80 | - | 80 | ns |
| J13 | TCLK low to TDO data invalid | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | 0 | - | ns |
| J14 | TCLK low to TDO high-Z | - | 28 | - | 32 | - | 28 | - | 32 | - | 28 | - | 80 | - | 80 | ns |

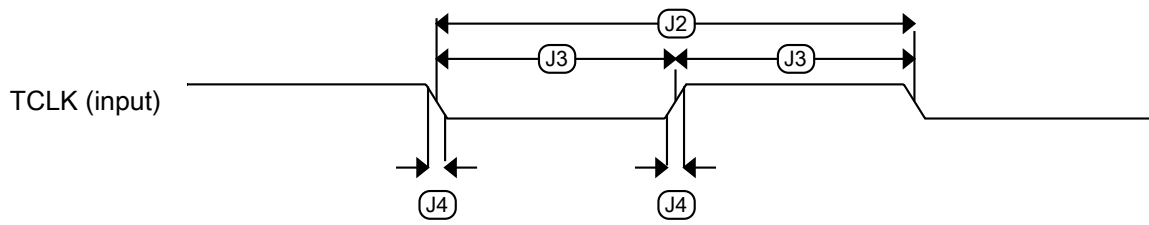


Figure 24. Test clock input timing

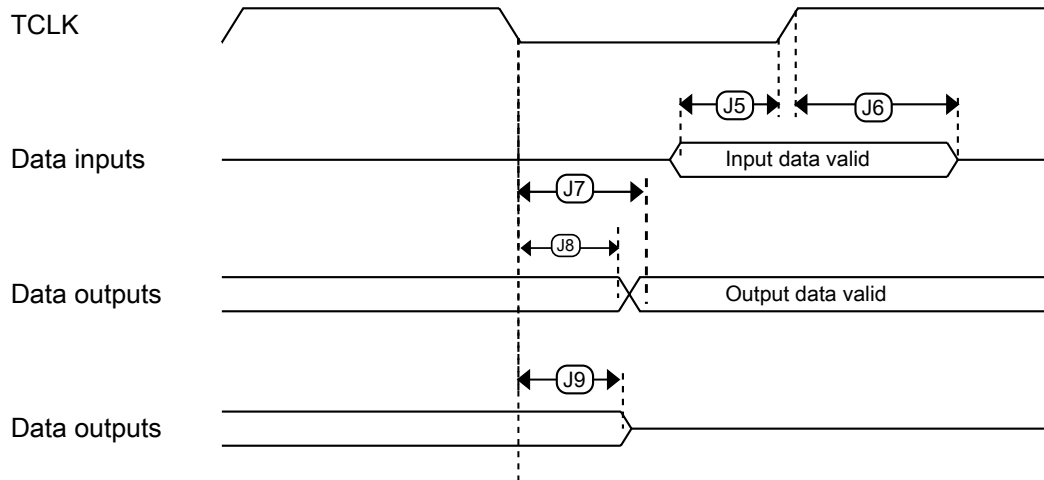


Figure 25. Boundary scan (JTAG) timing

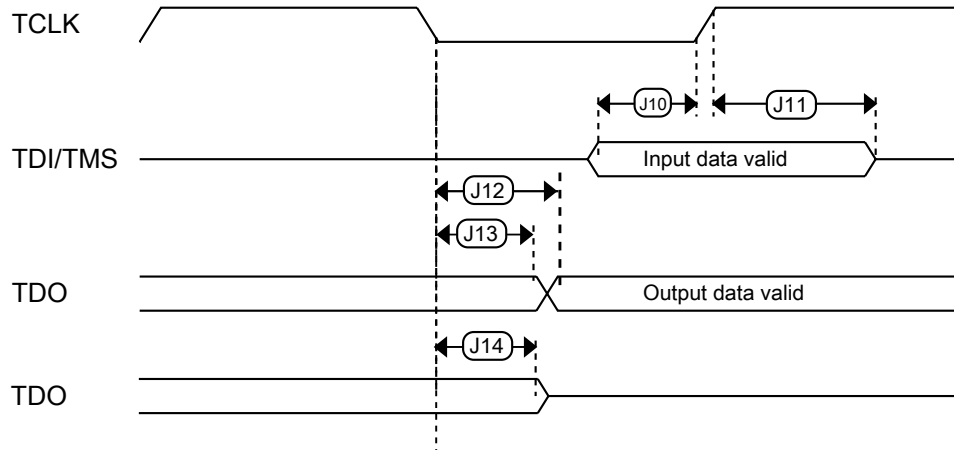


Figure 26. Test Access Port timing

7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

Table 33. Thermal characteristics for the 64/100-pin LQFP package

| Rating | Conditions | Symbol | Packages | Values | | | Unit |
|---|-------------------------|------------------|----------|-----------|-----------|-----------|------|
| | | | | MWCT1014S | MWCT1015S | MWCT1016S | |
| Thermal resistance, Junction to Ambient (Natural Convection) ^{1,2} | Single layer board (1s) | $R_{\theta JA}$ | 64 | 61 | 59 | NA | °C/W |
| | | | 100 | 52 | 21 | NA | °C/W |
| Thermal resistance, Junction to Ambient (Natural Convection) ¹ | Two layer board (1s1p) | $R_{\theta JA}$ | 64 | 45 | 44 | NA | °C/W |
| | | | 100 | 42 | 40 | NA | °C/W |
| Thermal resistance, Junction to Ambient (Natural Convection) ^{1,2} | Four layer board (2s2p) | $R_{\theta JA}$ | 64 | 43 | 41 | NA | °C/W |
| | | | 100 | 40 | 39 | NA | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min) ^{1,3} | Single layer board (1s) | $R_{\theta JMA}$ | 64 | 49 | 48 | NA | °C/W |
| | | | 100 | 42 | 41 | NA | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min) ¹ | Two layer board (1s1p) | $R_{\theta JMA}$ | 64 | 38 | 37 | NA | °C/W |
| | | | 100 | 35 | 34 | NA | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min) ^{1,3} | Four layer board (2s2p) | $R_{\theta JMA}$ | 64 | 36 | 35 | NA | °C/W |
| | | | 100 | 34 | 33 | NA | °C/W |
| Thermal resistance, Junction to Board ⁴ | — | $R_{\theta JB}$ | 64 | 25 | 23 | NA | °C/W |
| | | | 100 | 25 | 24 | NA | °C/W |
| Thermal resistance, Junction to Case ⁵ | — | $R_{\theta JC}$ | 64 | 12 | 11 | NA | °C/W |
| | | | 100 | 12 | 11 | NA | °C/W |
| Thermal resistance, Junction to Package Top ⁶ | Natural Convection | ψ_{JT} | 64 | 2 | 2 | NA | °C/W |
| | | | 100 | 2 | 2 | NA | °C/W |

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
- Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 34. Thermal characteristics for the 100 MAPBGA package

| Rating | Conditions | Symbol | Values | | | Unit |
|--|-------------------------|------------------|-----------|-----------|-----------|------|
| | | | MWCT1015S | MWCT1014S | MWCT1016S | |
| Thermal resistance, Junction to Ambient (Natural Convection) 1, 2 | Single layer board (1s) | $R_{\theta JA}$ | 57.2 | 61.0 | 52.5 | °C/W |
| Thermal resistance, Junction to Ambient (Natural Convection) 1, 2, 3 | Four layer board (2s2p) | $R_{\theta JA}$ | 32.1 | 35.6 | 27.5 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 2, 3} | Single layer board (1s) | $R_{\theta JMA}$ | 44.1 | 46.6 | 39.0 | °C/W |
| Thermal resistance, Junction to Ambient (@200 ft/min) ^{1, 3} | Two layer board (2s2p) | $R_{\theta JMA}$ | 27.2 | 30.9 | 22.8 | °C/W |
| Thermal resistance, Junction to Board ⁴ | — | $R_{\theta JB}$ | 15.3 | 18.9 | 11.2 | °C/W |
| Thermal resistance, Junction to Case ⁵ | — | $R_{\theta JC}$ | 10.2 | 14.2 | 7.5 | °C/W |
| Thermal resistance, Junction to Package Top outside center ⁶ | — | ψ_{JT} | 0.2 | 0.4 | 0.2 | °C/W |
| Thermal resistance, Junction to Package Bottom outside center ⁷ | — | ψ_{JB} | 12.2 | 15.9 | 18.3 | °C/W |

- Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
- Per JEDEC JESD51-6 with the board horizontal.
- Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.
- Thermal characterization parameter indicating the temperature difference between package bottom center and the junction temperature per JEDEC JESD51-12. When Greek letters are not available, the thermal characterization parameter is written as Psi-JB.

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J , can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package ($^{\circ}\text{C}$)
- $R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)
- $R_{\theta JC}$ = junction to case thermal resistance ($^{\circ}\text{C}/\text{W}$)
- $R_{\theta CA}$ = case to ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

Dimensions

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package ($^{\circ}\text{C}$)
- Ψ_{JT} = thermal characterization parameter ($^{\circ}\text{C}/\text{W}$)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to <http://www.nxp.com> and perform a keyword search for the drawing's document number:

| Package option | Document Number |
|----------------|-----------------|
| 64-pin LQFP | 98ASS23234W |
| 100-pin LQFP | 98ASS23308W |
| 100-pin MAPBGA | 98ASA00802D |

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 35. Revision History

| Rev. No. | Date | Substantial Changes |
|----------|----------|---|
| Rev. 0 | May 2017 | <ul style="list-style-type: none"> Initial release. |
| Rev. 1 | Dec 2017 | <ul style="list-style-type: none"> In "Feature comparison" section, updated the "MWCT101xS product series comparison" figure. In Table 1, <ul style="list-style-type: none"> Updated note 'All the limits defined ... ' Updated parameter 'I_{INJPAD_DC_ABS}', 'V_{IN_DC}', I_{INJSUM_DC_ABS}. In Table 2, <ul style="list-style-type: none"> Updated min. value of V_{DD_OFF} Added parameter I_{INJPAD_DC_OP} and I_{INJSUM_DC_OP}. Updated footnote to T_{SPLL_LOCK} and removed I_{DDSPLL} in "SPLL electrical specifications" table. In "12-bit ADC electrical characteristics" section, <ul style="list-style-type: none"> Updated table: 12-bit ADC characteristics (2.7 V to 3 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS}) <ul style="list-style-type: none"> Added typ. value to I_{DDA_ADC}, T_{UE}, D_{NL}, and I_{NL} Added min. value to S_{MPLTS} Removed footnote 'All the parameters in this table ... ' Updated table: 12-bit ADC characteristics (3 V to 5.5 V) (V_{REFH} = V_{DDA}, V_{REFL} = V_{SS}) <ul style="list-style-type: none"> Added typ. value to I_{DDA_ADC} Removed footnote 'All the parameters in this table ... ' In "Flash command timing specifications" table, updated Max. value of t_{vykey} to 35 μs Updated "MWCT101xS product series comparison" figure. In Table 5, updated TBDs for V_{LVR_HYST}, V_{LVD_HYST}, and V_{LWV_HYST} In Power mode transition operating behaviors, <ul style="list-style-type: none"> Added VLPR → VLPS Added VLPS → VLPR Updated TBDs for VLPS → Asynchronous DMA Wakeup, STOP1 → Asynchronous DMA Wakeup, and STOP2 → Asynchronous DMA Wakeup In Table 7, updated the specifications for MWCT1014S. Updated the attachment <i>MWCT101xS_Power_Modes_Configuration.xlsx</i>. In "Standard input pin capacitance" table, removed C_{IN_A}. In "External System Oscillator electrical specifications" table, |

Table continues on the next page...

Table 35. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|----------|-----------|---|
| | | <ul style="list-style-type: none"> • Updated specifications for g_{mXOSC}. • Removed I_{DDOSC} • In "Fast internal RC Oscillator (FIRC) electrical specifications" section, <ul style="list-style-type: none"> • Added parameter ΔF_{125}. • Removed I_{DDFIRC} • In "Slow internal RC oscillator (SIRC) electrical specifications" section, <ul style="list-style-type: none"> • Added parameter ΔF_{125}. • Removed $I_{DDSIIRC}$ • In "Low Power Oscillator (LPO) electrical specifications" section, removed I_{LPPO} • Updated section: "Flash memory module (FTFC) electrical specifications" • In section: "12-bit ADC electrical characteristics", <ul style="list-style-type: none"> • Updated TBDs in Table 25. • Updated TBDs in Table 26. • In section: QuadSPI AC specifications, updated figure 'QuadSPI output timing (HyperRAM mode) diagram'. • In section: "ADC electrical specifications", updated Table 24. • In section: "CMP with 8-bit DAC electrical specifications", added note 'For comparator IN signals adjacent ...' • In table: "LPSPi electrical specifications", minor update in footnote 6. • In table: Table 33, updated specifications for MWCT1015S. |
| Rev. 2 | July 2018 | <ul style="list-style-type: none"> • Global update: removed Ethernet and SAI • Updated the attachment <i>MWCT101xS_Power_Modes_Configuration.xlsx</i> • In 'Key features': <ul style="list-style-type: none"> • Added a note under 'Power management', 'Memory and memory interfaces', and 'Safety and security' • Updated FlexIO under Communications interfaces • Updated Cryptographic Services Engine (CSEc) under 'Safety and security' • Updated package information • In High-level architecture diagram for the MWCT101xS family, added footnote 3 • In "Feature comparison" section, updated the "MWCT101xS product series comparison" figure: <ul style="list-style-type: none"> • Updated the "System RAM" row • Added support for LIN protocol version 2.2 A • Updated the Ecosystem information • Updated the Package information • Updated the Legend notes • Updated Ordering information • In Absolute maximum ratings : <ul style="list-style-type: none"> • Updated the NOTE section • Added parameter 'T_{ramp_MCU}' • Updated footnote for 'T_{ramp}' • Updated Voltage and current operating requirements • In Power and ground pins <ul style="list-style-type: none"> • Removed the 144-pin LQFP package • Updated footnote 'V_{DD} and V_{DDA} must be shorted ...' • Updated the "Power diagram" figure • In Power mode transition operating behaviors updated numbers for: <ul style="list-style-type: none"> • VLPR → VLPS |

Table continues on the next page...

Table 35. Revision History

| Rev. No. | Date | Substantial Changes |
|----------|------|--|
| | | <ul style="list-style-type: none"> • VLPS → VLPR • RUN → VLPS • RUN → VLPR • In Power consumption : <ul style="list-style-type: none"> • Updated specs • Removed section 'Modes configuration', and moved its content under the first paragraph. • Updated footnote 'Typical current numbers are indicative ...' • Updated footnote 'The MWCT1016S data ...' • Removed footnote 'Above MWCT1016S data is preliminary targets only' • In General AC specifications : <ul style="list-style-type: none"> • Updated max value and footnote of WFRST • Updated symbol for not filtered pulse to 'WNFRST', updated min value, removed max. value, and added footnote • Fixed naming conventions to align with DS in DC electrical specifications at 3.3 V Range and DC electrical specifications at 5.0 V Range • Updated specs for AC electrical specifications at 3.3 V range and AC electrical specifications at 5 V range • In Device clock specifications : <ul style="list-style-type: none"> • Added footnote to f_{BUS} • In External System Oscillator frequency specifications : <ul style="list-style-type: none"> • Updated 't_{dc_extal}' • Added footnote 'Frequencies below ...' to 'f_{ec_extal}' and 't_{dc_extal}' • Updated Flash timing specifications — commands • In Reliability specifications : <ul style="list-style-type: none"> • Updated footnotes • In QuadSPI AC specifications : <ul style="list-style-type: none"> • Updated 'MCR[SCLKCFG[5]]' value to 0 • Updated 'Data Input Setup Time' HSRUN Internal DQS PAD Loopback value to 1.6 • Updated 'Data Input Setup Time' DDR External DQS min. value to 2 • Updated 'Data Input Hold Time' DDR External DQS min. value to 20 • Updated t_{IV} • Updated figure 'QuadSPI output timing (SDR mode) diagram' and 'QuadSPI input timing (HyperRAM mode) diagram' • In 12-bit ADC operating conditions : <ul style="list-style-type: none"> • Fixed the typo in R_{SW1} • Removed parameter 'ΔV_{DDA}' • In 12-bit ADC electrical characteristics : <ul style="list-style-type: none"> • Added note 'On reduced pin packages where ...' • Removed max. value of 'I_{DDA_ADC}' • Added note 'Due to triple ...' • In CMP with 8-bit DAC electrical specifications : <ul style="list-style-type: none"> • Updated Typ. and Max. values of 'I_{DDL5}' • Updated Typ. value of 't_{DHSB}' • Updated Typ. value of 'V_{HYST1}', 'V_{HYST2}', and 'V_{HYST3}' • In LPSPI electrical specifications : <ul style="list-style-type: none"> • Updated 'f_{periph}' and 'f_{op}', and 't_{SPSCK}' • Updated 3.3 V numbers and added footnote against f_{op}, t_{SU}, and t_V in HSRUN Mode • Added footnote to 't_{WSPSCK}' |

Table continues on the next page...

Table 35. Revision History (continued)

| Rev. No. | Date | Substantial Changes |
|----------|----------|--|
| | | <ul style="list-style-type: none"> • Updated t_{Lead} and t_{Lag} • Added footnote in Figure: LPSPI slave mode timing (CPHA = 0) and Figure: LPSPI slave mode timing (CPHA = 1) • In Thermal characteristics : <ul style="list-style-type: none"> • Updated table name for the LQFP packages • Added table for the BGA package • Updated Obtaining package dimensions |
| Rev. 3 | Dec 2019 | <ul style="list-style-type: none"> • Updated Ordering Information in Ordering information • Updated CAN-FD and CSec information for MWCT1015SF in Feature Comparison figure |
| Rev. 4 | Aug 2020 | <ul style="list-style-type: none"> • Removed Trays and Tubes from the Ordering information |

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Document Number MWCT101xSF
Revision 4, 08/2020

