

MMFT2N25E



Product Preview

High Energy Power FET N-Channel Enhancement-Mode Silicon Gate

ON Semiconductor®

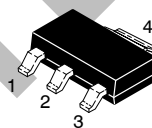
<http://onsemi.com>

POWER FET
2.0 AMPERES, 250 VOLTS

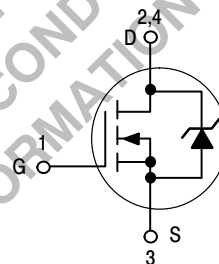
$R_{DS(on)} = 3.5 \Omega$

This advanced high voltage MOSFET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor – Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



CASE 318E-04, STYLE 3
TO-261AA



MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	250	Vdc
Drain-to-Gate Voltage, $R_{GS} = 1.0 \text{ m}\Omega$	V_{DGR}	250	Vdc
Gate-to-Source Voltage — Continuous	V_{GS}	± 20	Vdc
Gate-to-Source Voltage — Single Pulse ($t_p \leq 50 \mu\text{s}$)	V_{GSM}	± 40	Vdc
Drain Current — Continuous @ $T_C = 25^\circ\text{C}$	I_D	2.0	Adc
— Continuous @ $T_C = 100^\circ\text{C}$	I_D	0.6	
— Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_{DM}	7.0	Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	0.77	Watts
Derate above 25°C		6.2	mW/ $^\circ\text{C}$
Total P_D @ $T_A = 25^\circ\text{C}$ mounted on 1" Sq. Drain Pad on FR-4 Bd. Material		1.0	Watts
Total P_D @ $T_A = 25^\circ\text{C}$ mounted on 0.7" Sq. Drain Pad on FR-4 Bd. Material		1.2	
Total P_D @ $T_A = 25^\circ\text{C}$ mounted on min. Drain Pad on FR-4 Bd. Material		0.8	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS ($T_J < 150^\circ\text{C}$)

Single Pulse Drain-to-Source Avalanche Energy — Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 80 \text{ V}$, $V_{GS} = 10 \text{ V}$, Peak $I_L = 4.0 \text{ Apk}$, $L = 3.0 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	26	mJ
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THERMAL CHARACTERISTICS

— Junction-to-Ambient on 1" Sq. Drain Pad on FR-4 Bd. Material	$R_{\theta JA}$	90	$^\circ\text{C}/\text{W}$
— Junction-to-Ambient on 0.7" Sq. Drain Pad on FR-4 Bd. Material		103	
— Junction-to-Ambient on min. Drain Pad on FR-4 Bd. Material		162	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0, I _D = 0.25 mA) Temperature Coefficient (Positive)	BV _{DSS}	250 —	— 324	— —	Vdc V/°C
Zero Gate Voltage Drain Current (V _{DS} = 250 V, V _{GS} = 0) (V _{DS} = 250 V, V _{GS} = 0, T _J = 125°C)	I _{DSS}	— —	— —	10 100	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 V, V _{DS} = 0)	I _{GSS}	—	—	100	nAdc

ON CHARACTERISTICS (1)

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 0.25 mA) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	2.0 —	2.8 5.7	4.0 —	Vdc mV/°C
Static Drain-to-Source On-Resistance (V _{GS} = 10 V, I _D = 1.0 Adc)	R _{DS(on)}	—	2.1	3.5	Ohms
Drain-to-Source On-Voltage (V _{GS} = 10 V, I _D = 2.0 A) (V _{GS} = 10 V, I _D = 1.0 A, T _J = 125°C)	V _{DS(on)}	— —	— —	8.40 7.35	Vdc
Forward Transconductance (V _{DS} = 8.0 V, I _D = 2.0 Adc)	g _{FS}	0.44	1.2	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 V, V _{GS} = 0, f = 1.0 MHz)	C _{iSS}	—	137	190	pF
Output Capacitance		C _{oSS}	—	30	40	
Transfer Capacitance		C _{rSS}	—	7.0	10	

SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V _{DS} = 125 V, I _D = 2.0 A, R _G = 9.1 Ohms, V _{GS} = 10 V)	t _{d(on)}	—	9.2	20	ns
Rise Time		t _r	—	6.6	10	
Turn-Off Delay Time		t _{d(off)}	—	13	30	
Fall Time		t _f	—	8.5	20	
Gate Charge	(V _{DS} = 200 V, I _D = 2.0 A, V _{GS} = 10 V)	Q _T	—	4.7	10	nC
		Q ₁	—	1.3	—	
		Q ₂	—	3.2	—	
		Q ₃	—	2.3	—	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	I _S = 2.0 A, V _{GS} = 0 V	V _{SD}	—	0.94	2.0	Vdc
	I _S = 2.0 A, V _{GS} = 0 V, T _J = 125°C	V _{SD}	—	0.83	—	
Reverse Recovery Time	(I _S = 2.0 A, di _S /dt = 100 A/μs)	t _{rr}	—	104	—	nS
		t _a	—	63	—	
		t _b	—	41	—	
Reverse Recovery Stored Charge		q _{rr}	—	0.365	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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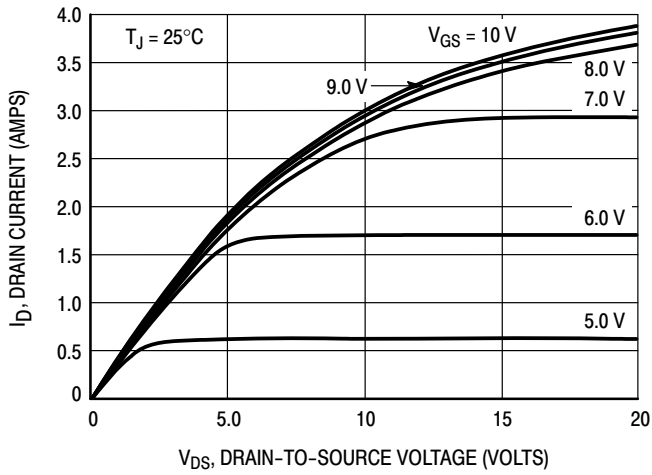


Figure 1. On-Region Characteristics

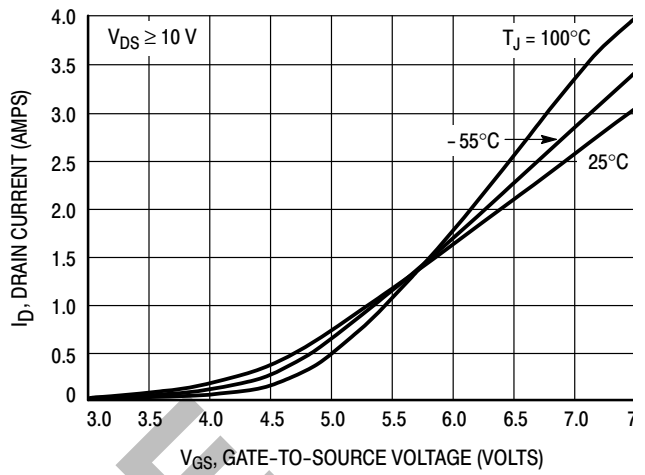


Figure 2. Transfer Characteristics

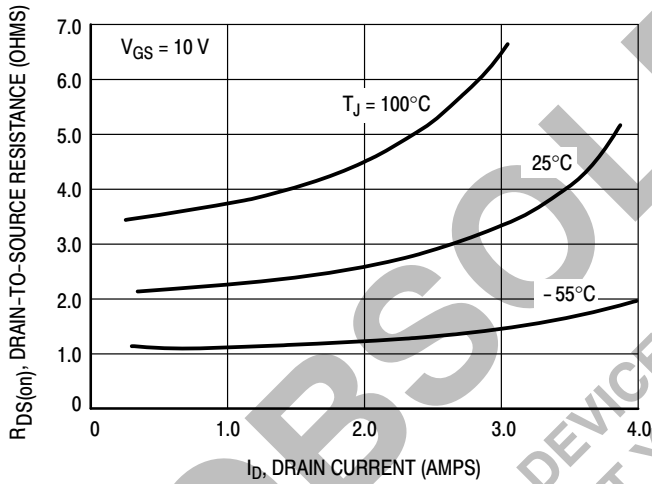


Figure 3. On-Resistance versus Drain Current and Temperature

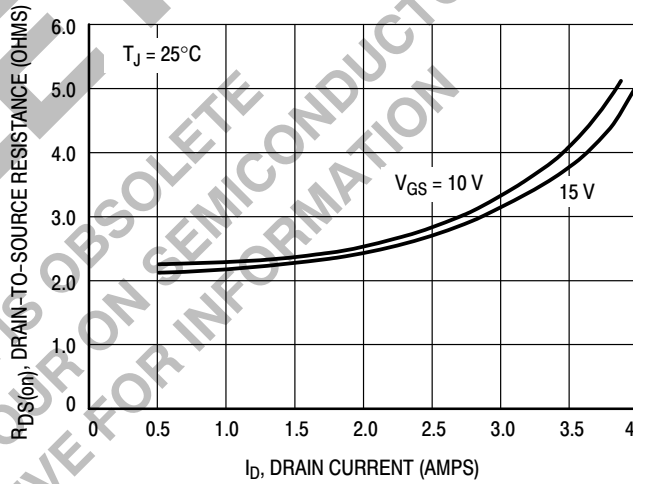


Figure 4. On-Resistance versus Drain Current and Gate Voltage

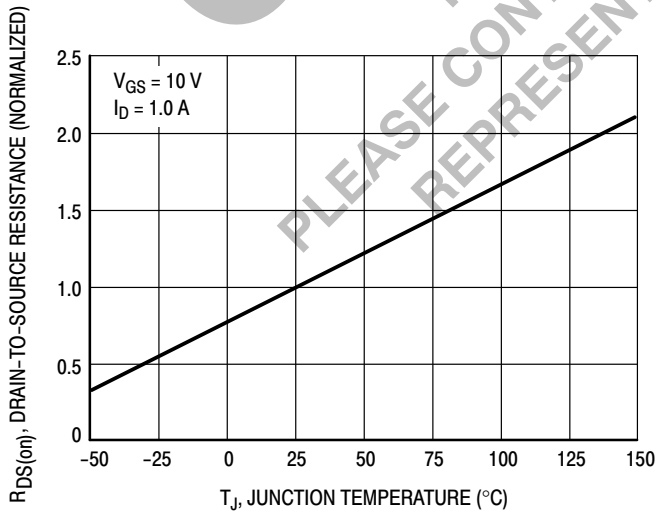


Figure 5. On-Resistance Variation versus Temperature

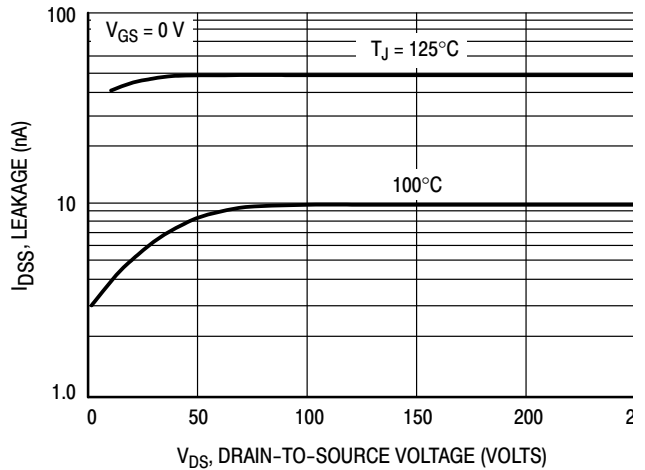


Figure 6. Drain-to-Source Leakage Current versus Voltage

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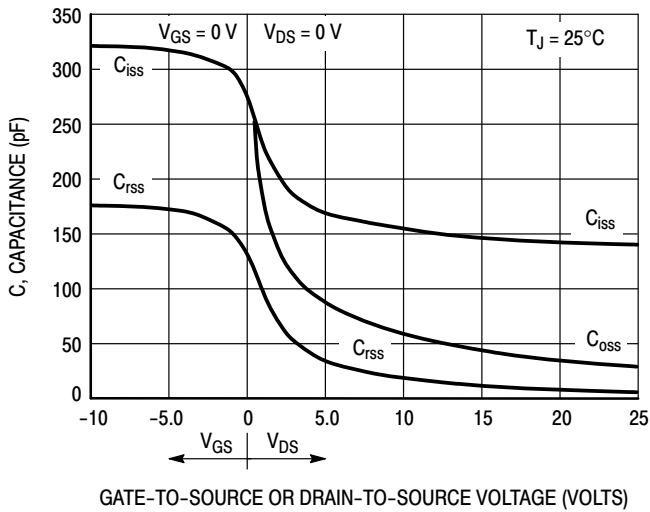


Figure 7. Capacitance Variation

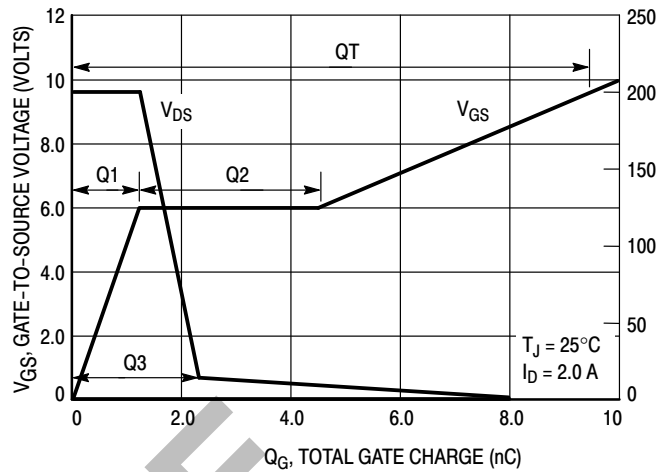


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

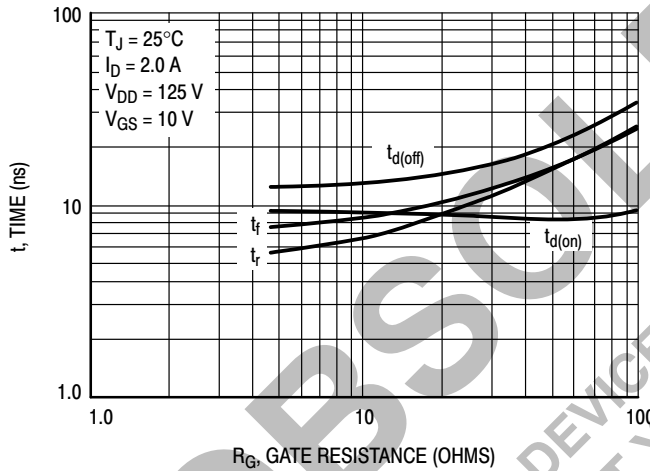


Figure 9. Resistive Switching Time Variation versus Gate Resistance

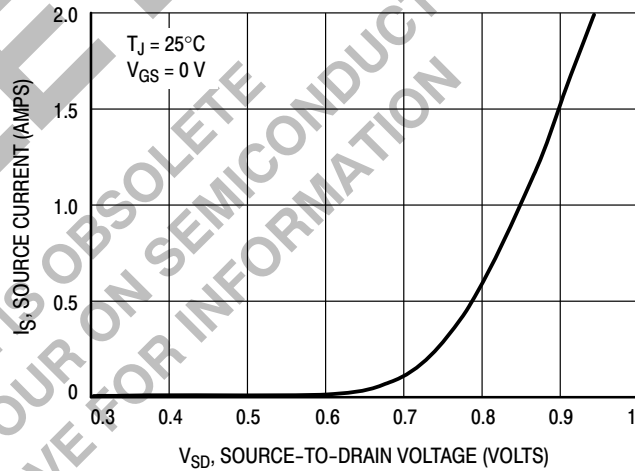


Figure 10. Diode Forward Voltage versus Current

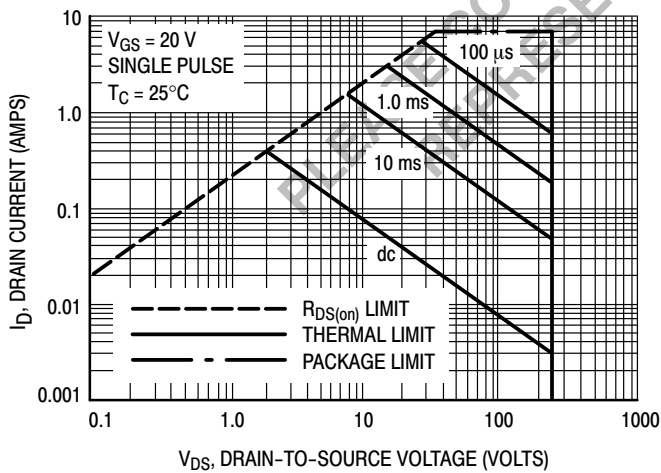


Figure 11. Maximum Rated Forward Biased Safe Operating Area

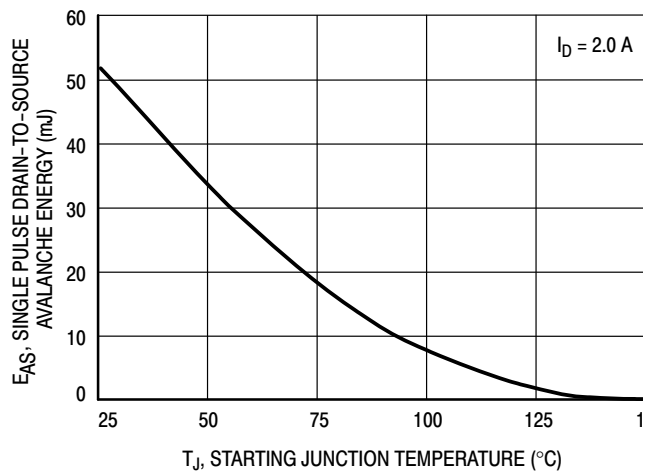


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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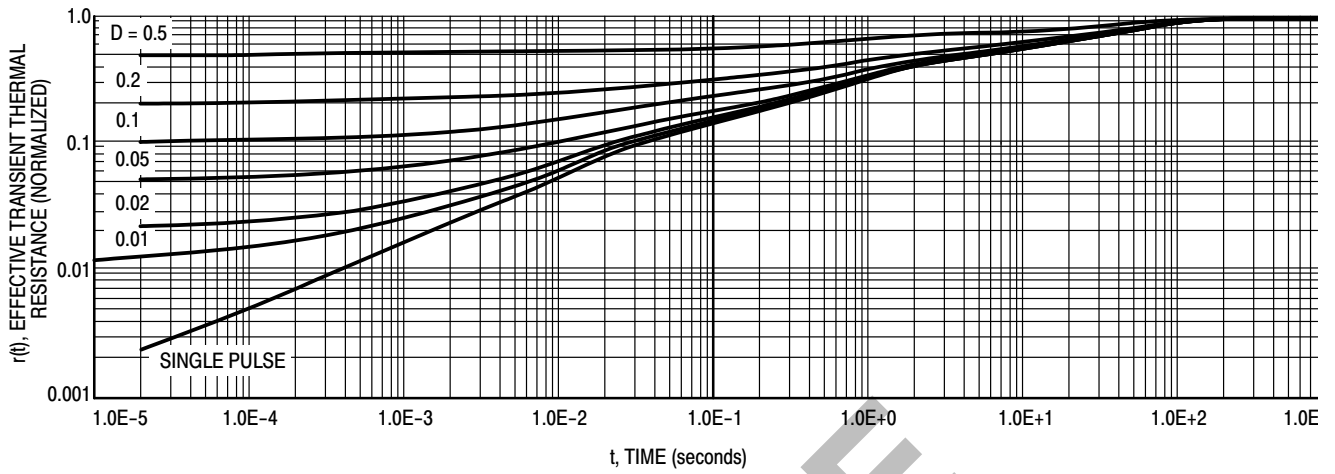


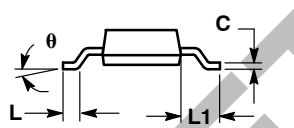
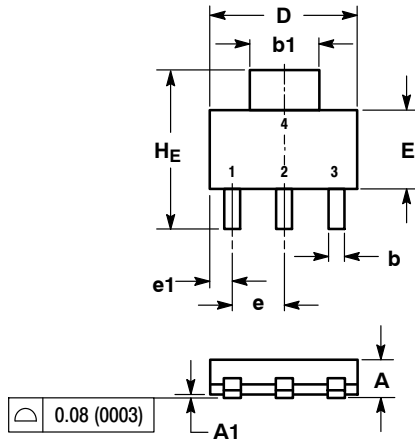
Figure 13. Thermal Response

OBSOLETE
THIS DEVICE IS OBSOLETE
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PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE N

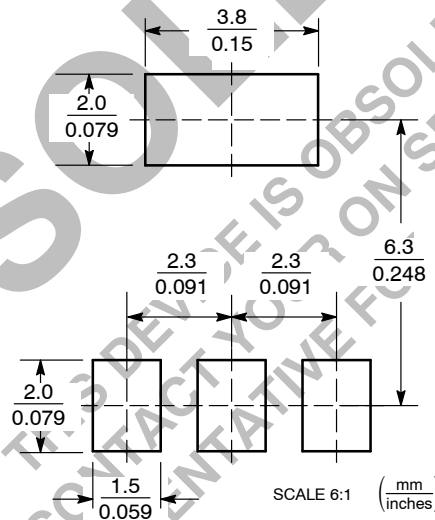


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	-	10°	0°	-	10°

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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