CSD25485F5 –20-V P-Channel FemtoFET™ MOSFET

1 Features

- Low-on resistance
- Low Q_g and Q_{gd}
- Ultra-small footprint
  - 1.53 mm × 0.77 mm
  - 0.50-mm pad pitch
- Low profile
  - 0.36-mm height
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for industrial load switch applications
- Optimized for general purpose switching applications

3 Description

This 29.7-mΩ, –20-V, P-Channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing a significant reduction in footprint size.

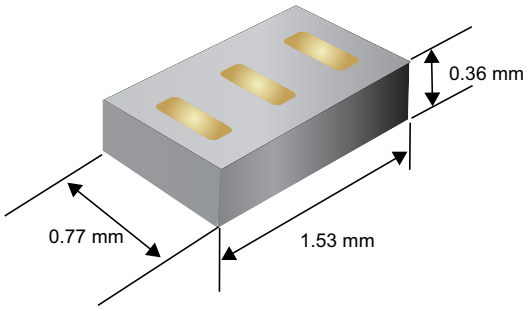

Figure 3-1. Typical Part Dimensions

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	–20		V
Q_g	Gate Charge Total (–4.5 V)	2.7		nC
Q_{gd}	Gate Charge Gate-to-Drain	0.56		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	V_{GS} = –1.8 V	89	mΩ
		V_{GS} = –2.5 V	51	
		V_{GS} = –4.5 V	35	
		V_{GS} = –8 V	29.7	
$V_{GS(th)}$	Threshold Voltage	–0.95		V

Device Information(1)

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD25485F5	3000	7-Inch Reel	Femto 1.53-mm × 0.77-mm SMD Leadless	Tape and Reel
CSD25485F5T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	–20	V
V_{GS}	Gate-to-Source Voltage	–12	V
I_D	Continuous Drain Current(1)	–3.2	A
	Continuous Drain Current(2)	–5.3	
I_{DM}	Pulsed Drain Current(1) (3)	–31	A
P_D	Power Dissipation(1)	0.5	W
	Power Dissipation(2)	1.4	
$V_{(ESD)}$	Human-Body Model (HBM)	4000	V
	Charged-Device Model (CDM)	2000	
T_J, T_{stg}	Operating Junction, Storage Temperature	–55 to 150	°C

(1) Min Cu, typical $R_{\theta JA}$ = 245°C/W.
(2) Max Cu, typical $R_{\theta JA}$ = 90°C/W.
(3) Pulse duration ≤ 100 µs, duty cycle ≤ 1%.

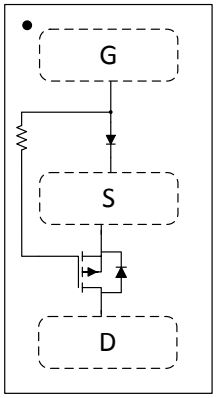

Figure 3-2. Top View

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4 Revision History

Changes from Revision A (January 2017) to Revision B (February 2022) **Page**

- Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height.... 1
- Updated ultra-low profile image height from 0.35 mm to 0.36 mm.... 1
- Changed ultra-low profile image height from 0.35 mm to 0.36 mm.... 7
- Added FemtoFET Surface Mount Guide note.... 8

Changes from Revision * (August 2016) to Revision A (January 2017) **Page**

- Changed Min Cu $R_{\theta JA}$ from 90°C/W : to 245°C/W in Figure 5-11 3
- Added Table 7-1 in the *Mechanical Dimensions* section.... 7

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_{DS} = –250 µA	–20			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = –16 V			–100	nA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = –12 V			–25	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_{DS} = –250 µA	–0.7	–0.95	–1.3	V
$R_{DS(on)}$	Drain-to-source on resistance	V_{GS} = –1.8 V, I_{DS} = –0.1 A		89	250	mΩ
		V_{GS} = –2.5 V, I_{DS} = –0.9 A		51	70	
		V_{GS} = –4.5 V, I_{DS} = –0.9 A		35	42	
		V_{GS} = –8 V, I_{DS} = –0.9 A		29.7	35	
g_{fs}	Transconductance	V_{DS} = –2 V, I_{DS} = –0.9 A		7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = –10 V, f = 1 MHz		410	533	pF
C_{oss}	Output capacitance			212	276	pF
C_{rss}	Reverse transfer capacitance			17	23	pF
R_G	Series gate resistance			20		Ω
Q_g	Gate charge total (–4.5 V)	V_{DS} = –10 V, I_{DS} = –0.9 A		2.7	3.5	nC
Q_{gd}	Gate charge gate-to-drain			0.56		nC
Q_{gs}	Gate charge gate-to-source			0.67		nC
$Q_{g(th)}$	Gate charge at V_{th}			0.40		nC
Q_{oss}	Output charge	V_{DS} = –10 V, V_{GS} = 0 V		4.4		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = –10 V, V_{GS} = –4.5 V, I_{DS} = –0.9 A, R_G = 2 Ω		14		ns
t_r	Rise time			6		ns
$t_{d(off)}$	Turnoff delay time			27		ns
t_f	Fall time			14		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = –0.9 A, V_{GS} = 0 V		–0.75	–1	V

5.2 Thermal Information

T_A = 25°C (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		90		°C/W
	Junction-to-ambient thermal resistance(2)		245		

(1) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise stated)

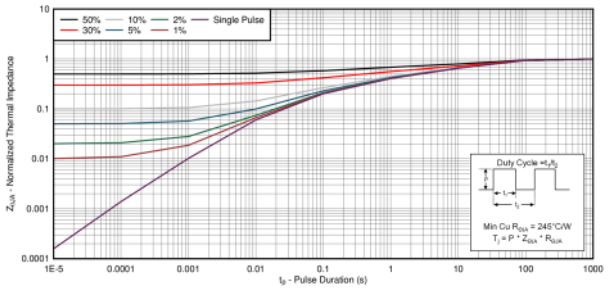


Figure 5-1. Transient Thermal Impedance

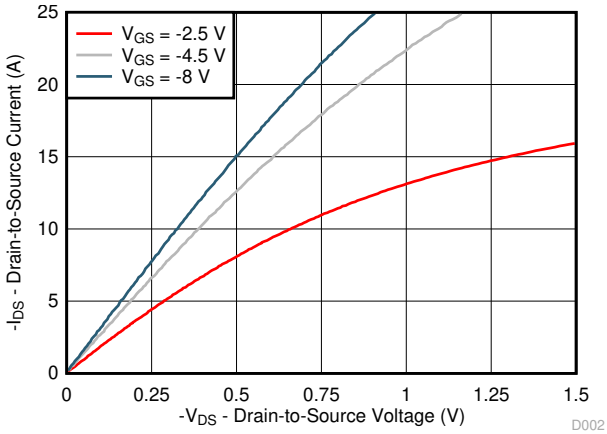
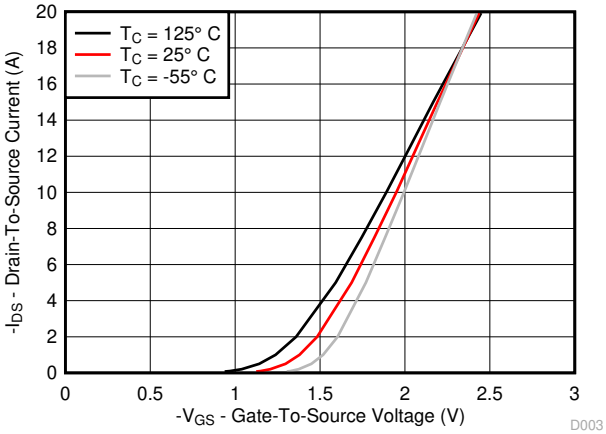
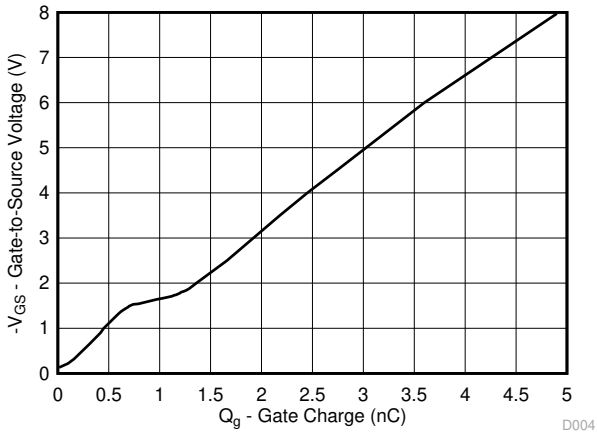


Figure 5-2. Saturation Characteristics



V_{DS} = –5 V

Figure 5-3. Transfer Characteristics



I_D = –0.9 A V_{DS} = –10 V

Figure 5-4. Gate Charge

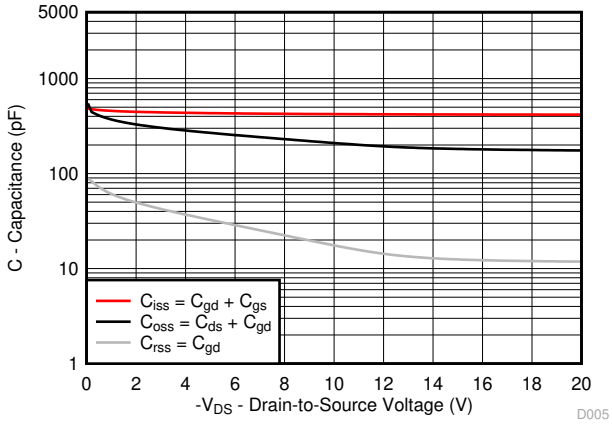
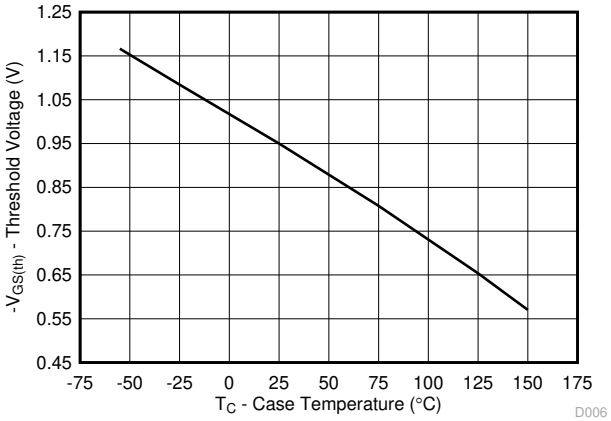


Figure 5-5. Capacitance



I_D = –250 µA

Figure 5-6. Threshold Voltage vs Temperature

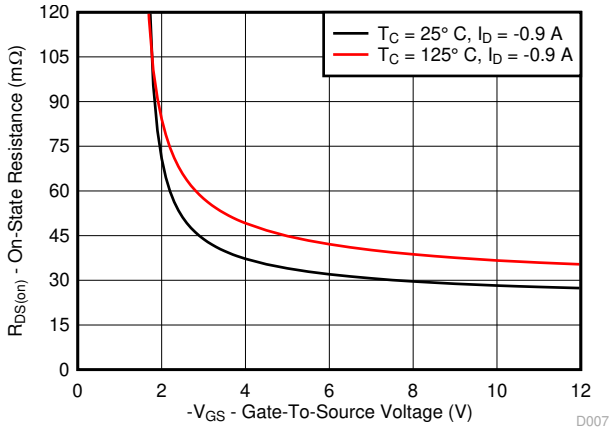
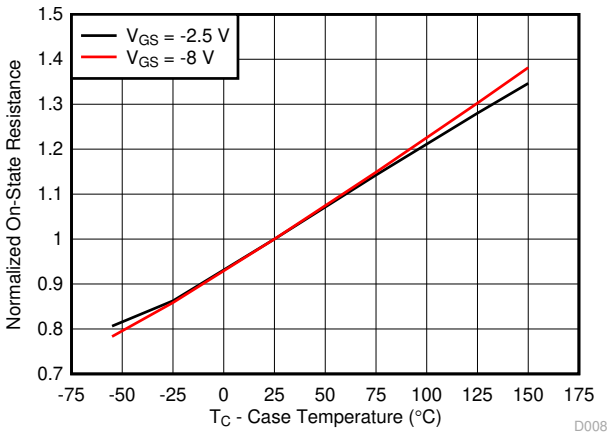


Figure 5-7. On-State Resistance vs Gate-to-Source Voltage



I_D = –0.9 A

Figure 5-8. Normalized On-State Resistance vs Temperature

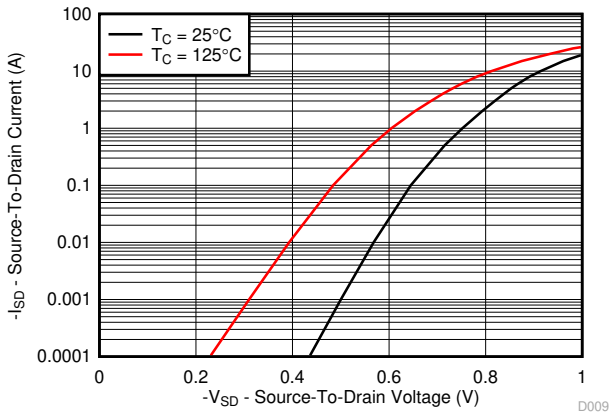
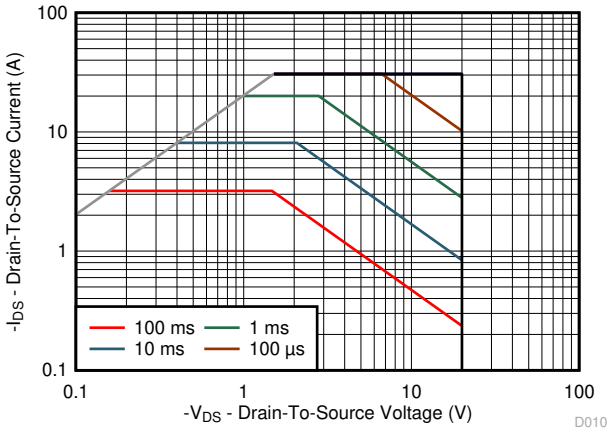
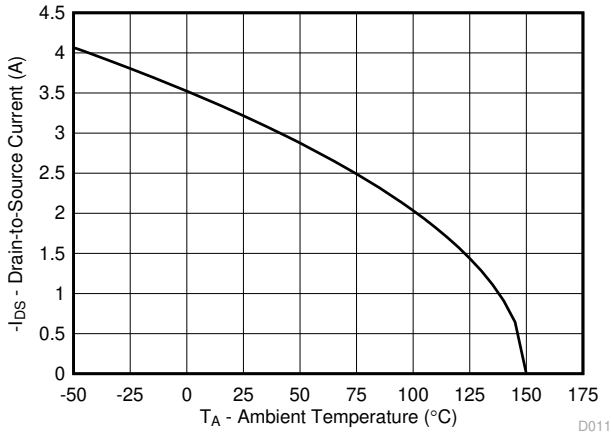


Figure 5-9. Typical Diode Forward Voltage



Single pulse, typ min Cu $R_{\theta JA}$ = 245°C/W

Figure 5-10. Maximum Safe Operating Area (SOA)



Typ min Cu $R_{\theta JA}$ = 245°C/W

Figure 5-11. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

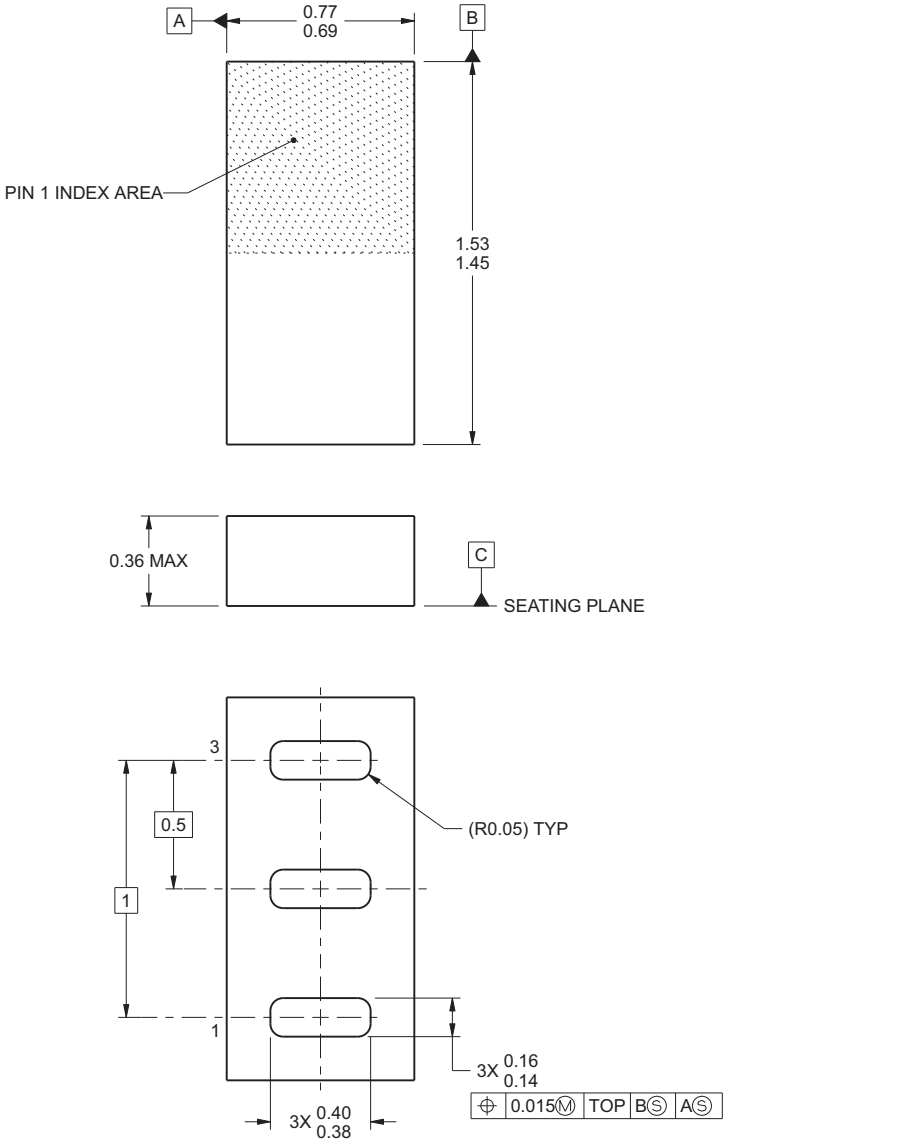
6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



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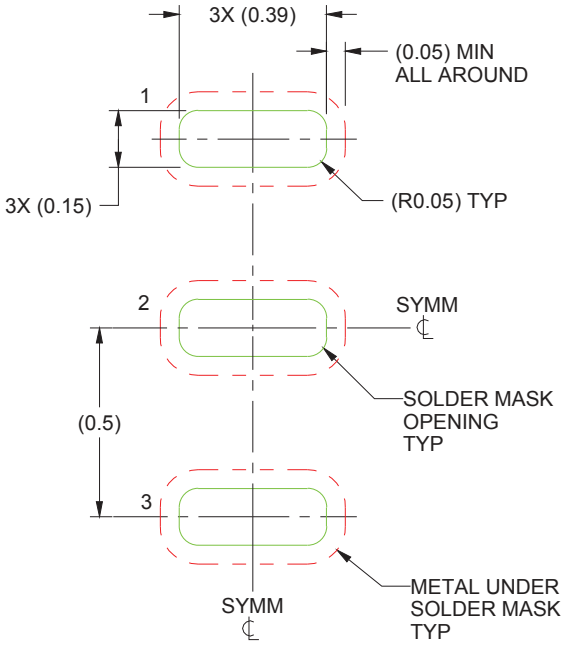
A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a PB-free solder land design.

Table 7-1. Pin Configuration

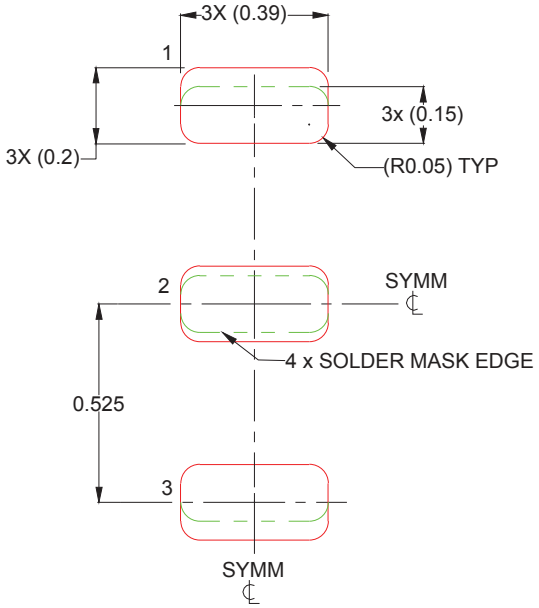
POSITION	DESIGNATION
Pin 1	Gate
Pin 2	Source
Pin 3	Drain

7.2 Recommended Minimum PCB Layout



A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern



A. All dimensions are in millimeters.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD25485F5	ACTIVE	PICOSTAR	YJK	3	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	3H	Samples
CSD25485F5T	ACTIVE	PICOSTAR	YJK	3	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	3H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

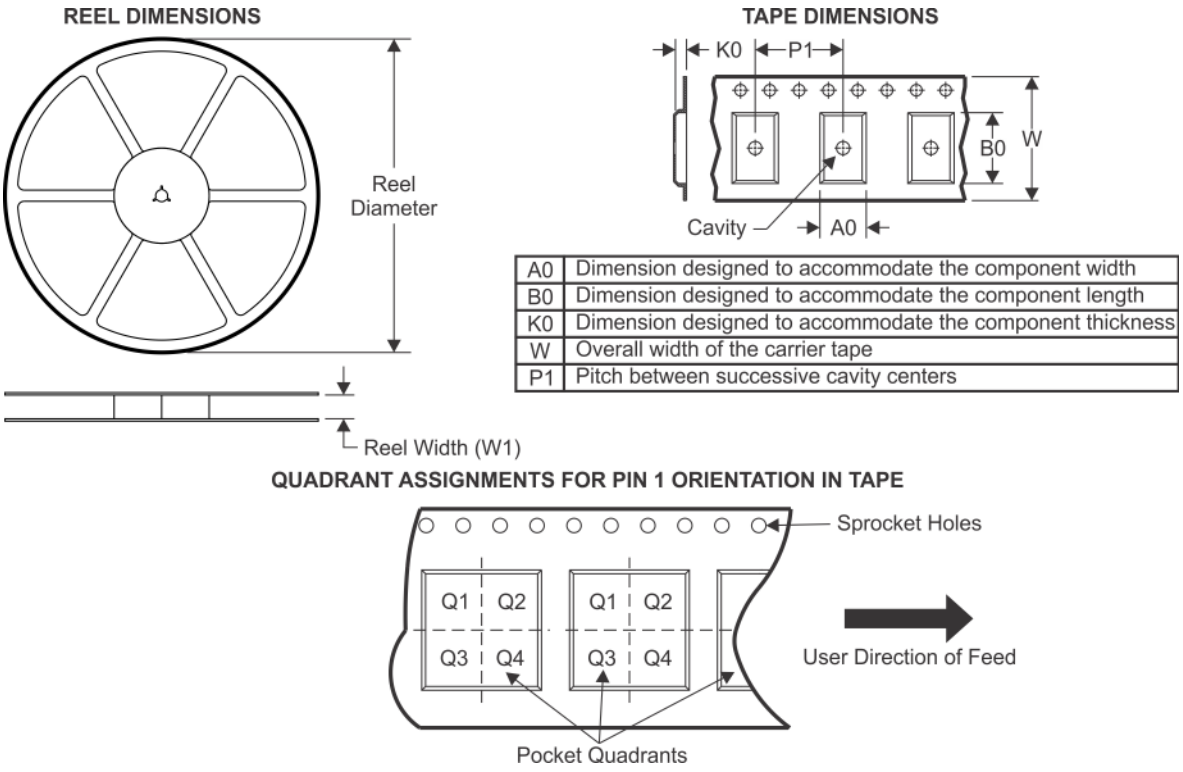
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

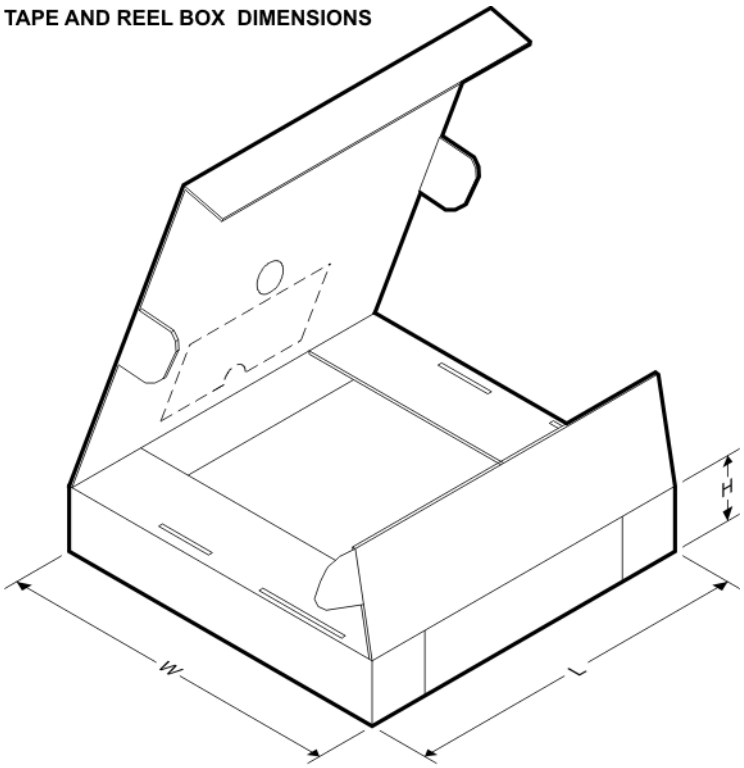


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD25485F5	PICOSTAR	YJK	3	3000	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1
CSD25485F5T	PICOSTAR	YJK	3	250	180.0	8.4	0.92	1.68	0.42	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

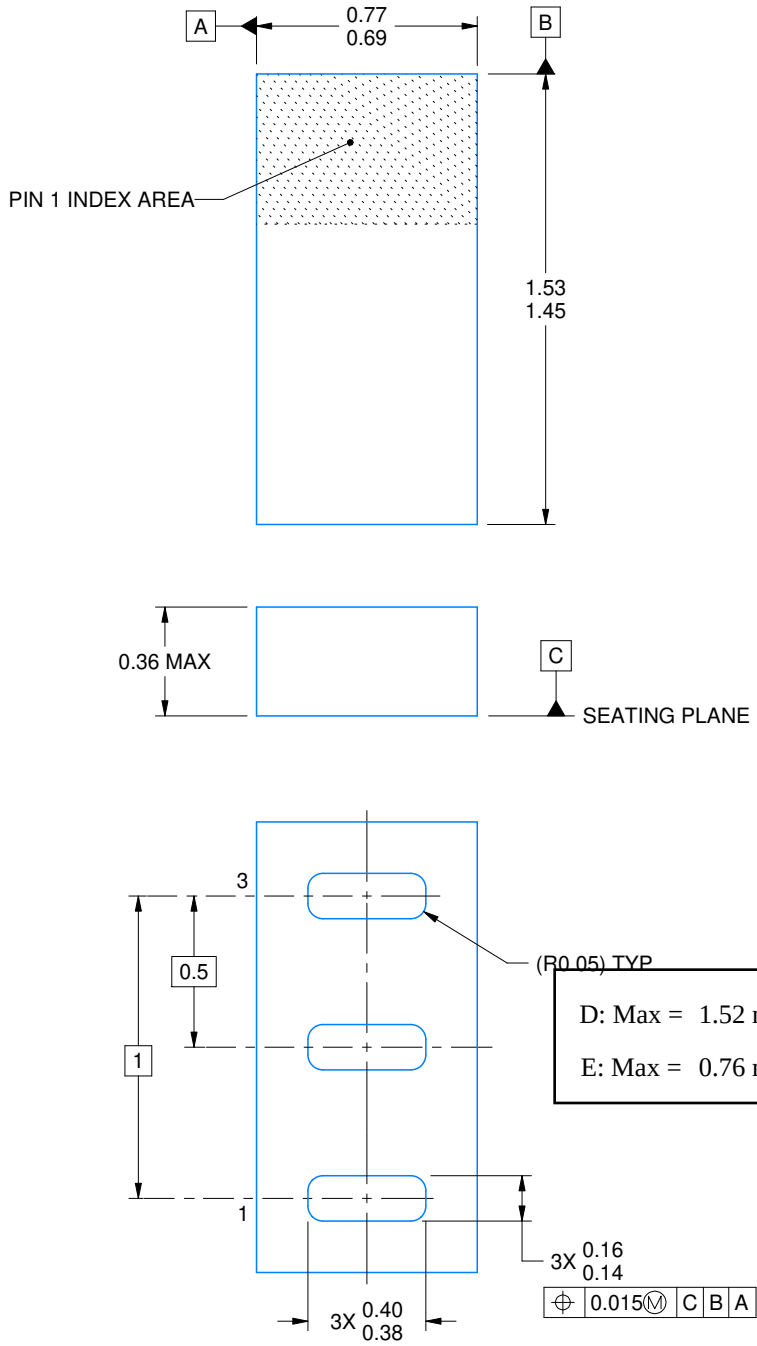
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD25485F5	PICOSTAR	YJK	3	3000	182.0	182.0	20.0
CSD25485F5T	PICOSTAR	YJK	3	250	182.0	182.0	20.0

PACKAGE OUTLINE

YJK0003A

PicoStar™ - 0.36 mm max height

PicoStar™



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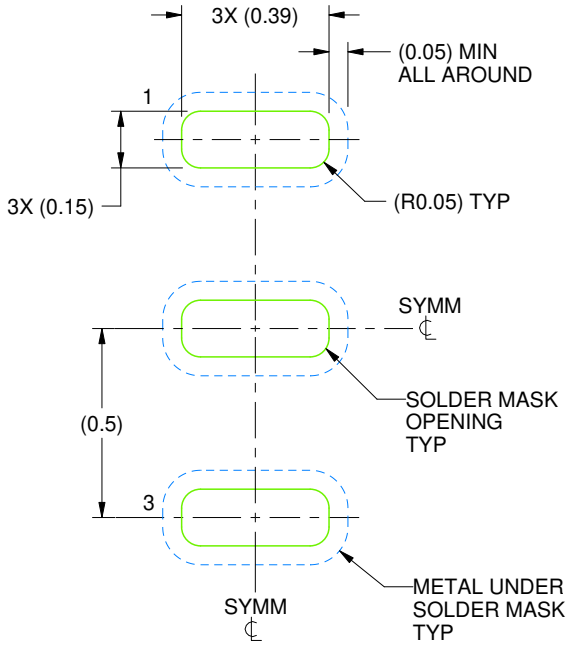
PicoStar is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:50X

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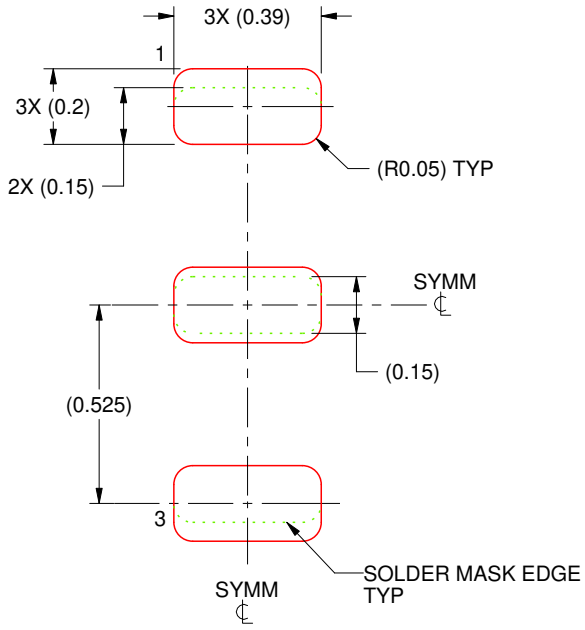
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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