ISO8200AQ

Datasheet

Galvanic isolated octal high side smart power solid state relay with SPI interface

TFQFPN32

Product status link
ISO8200AQ

Product summary		
Order code	ISO8200AQ	ISO8200AQTR
Package	TFQFPN32	
Packing	Tube	Tape & Reel

Product label
SUSTAINABLE TECHNOLOGY

Features

- V_{CC} operating range: 10.5 V to 45 V
- I_{OUT} operating range: ≤ 0.7 A (per channel)
- $R_{DS(\ on)}$ = 0.120 Ω (per channel)
- 20MHz SPI interface with daisy chaining
- 5 V and 3.3 V TTL/CMOS and MCU compatible I/Os
- Common output enable/disable pin
- Fast demagnetization of inductive loads ($V_{DEMAG(TYP)}$ = V_{CC} - 50 V
- Reset function for IC outputs disable
- Very low supply current
- Undervoltage shutdown with auto restart and hysteresis
- Short-circuit protection
- Per-channel overtemperature protection
- Thermal independence of separate channels
- Case overtemperature protection
- Loss of Ground and Supply protections
- Overvoltage protection (V_{CC} clamping)
- Common OVT fault open drain output
- Power GOOD open drain output
- High common mode transient immunity
- ESD protection
- Designed to meet IEC 61000-4-2, IEC 61000- 4-4, IEC 61000-4-5 and IEC 61000-4-8
- UL1577 and UL508 certified

Applications

- Programmable logic control
- Industrial PC peripheral input/output
- Numerical control machines
- Drivers for all type of loads (resistive, capacitive, inductive)

1 Description

The ISO8200AQ is a galvanic isolated 8-channel driver featuring a very low supply current. It contains 2 independent galvanic isolated voltage domains (V_{CC} and V_{DD} for the Process and Control Logic stages, respectively). The IC is intended for driving any kind of load with one side connected to ground.

The Control Logic Stage features an 8-bit Output Status Register (where the microcontroller sets the ON/OFF status of the output channels in the Process Stage) and an 8-bit Fault Register (where the OVT faults of each channel are stored). The two stages communicate through the galvanic isolation channel via an ST proprietary protocol.

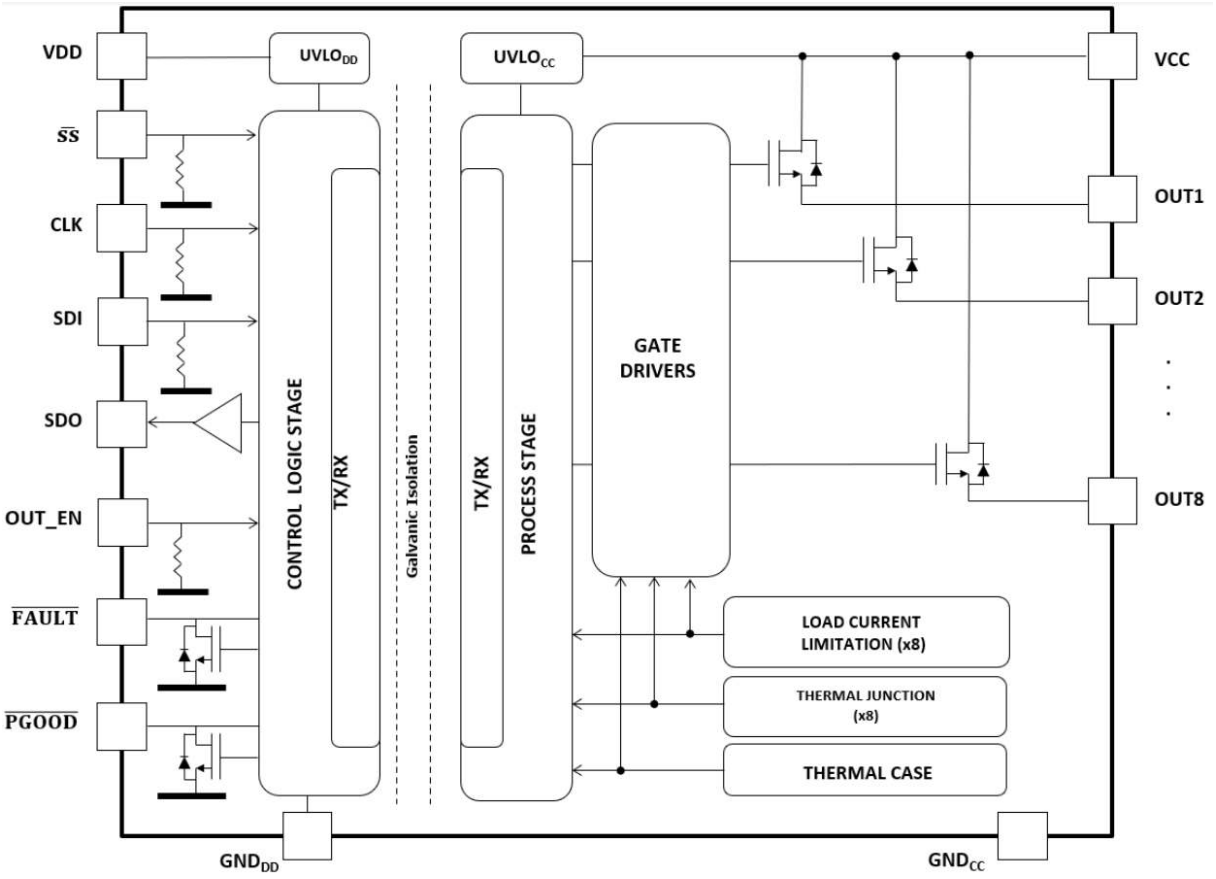
Active channel current limitation (OVL) combined with thermal shutdown (OVT), independent for each channel, protects the device against overload and overtemperature.

Additional embedded functions include loss of ground protection, V_{CC} and V_{DD} UVLOs (with hysteresis), watchdog and V_{CC} Power GOOD.

An internal circuit provides an OR-wired not latched common ($\overline{FAULT}$) indicator signaling the channel OVT. The ($\overline{PGOOD}$) diagnostic pin is activated if V_{CC} falls below the power good internal threshold. Both ($\overline{FAULT}$) and ($\overline{PGOOD}$) pins are open drain, active low, fault indication pins.

2 Block diagram

Figure 1. **Block diagram**



3 Pin connection

Figure 2. **Pin connection (top through view)**

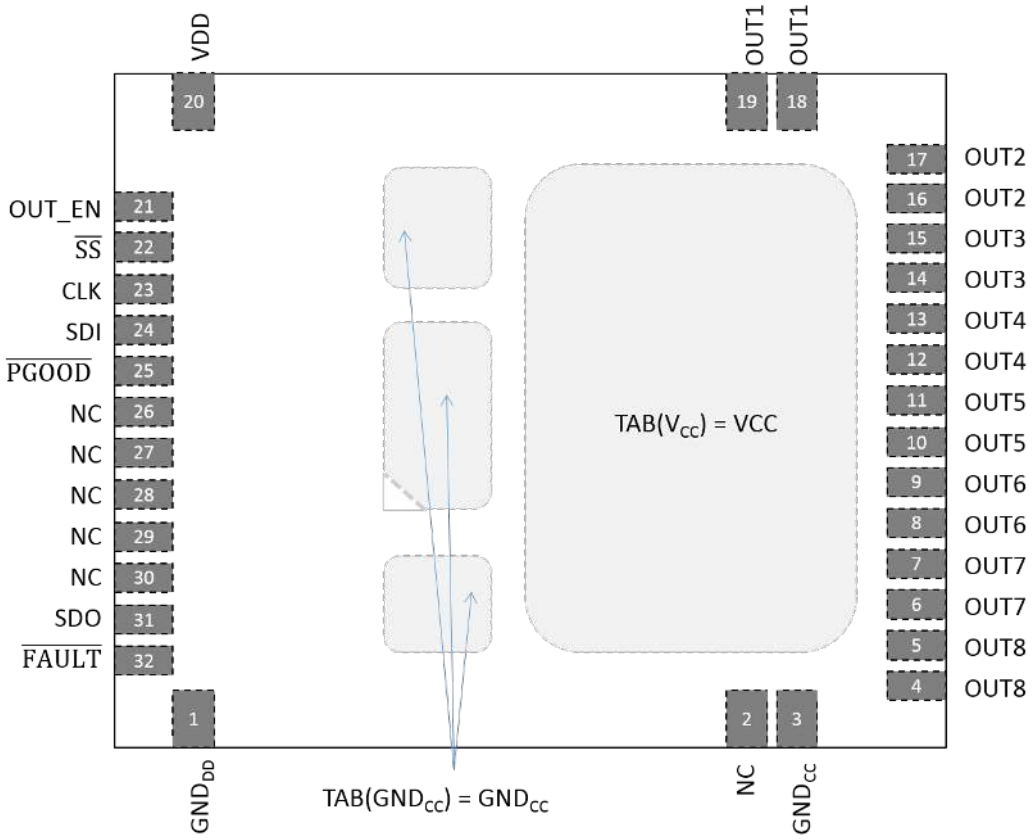


Table 1. **Pin description**

Pin	Name	Description
1	GND_{DD}	Input Control Logic Stage ground, negative logic supply
2	NC	Not connected
3	GNDCC	Output power ground
4	OUT8	Channel 8 power output
5	OUT8	
6	OUT7	Channel 7 power output
7	OUT7	
8	OUT6	Channel 6 power output
9	OUT6	
10	OUT5	Channel 5 power output
11	OUT5	
12	OUT4	Channel 4 power output
13	OUT4	
14	OUT3	Channel 3 power output

Pin	Name	Description
15	OUT3	Channel 3 power output
16	OUT2	Channel 2 power output
17	OUT2	
18	OUT1	Channel 1 power output
19	OUT1	
20	VDD	Positive Control Logic Stage supply
21	OUT_EN	Output enable
22	$\overline{SS}$	Chip select
23	CLK	Serial Clock Digital Input
24	SDI (MOSI)	SPI device Input
25	$\overline{PGOOD}$	Power Good diagnostic pin - active low
26	NC	Not connected
27	NC	Not connected
28	NC	Not connected
29	NC	Not connected
30	NC	Not connected
31	SDO (MISO)	SPI device Output
32	$\overline{FAULT}$	Common fault diagnostic pin - active low
TAB(V_{CC})	VCC	Exposed tab internally connected to V_{CC}, positive Process Stage supply voltage
TAB(GND_{CC})	GND_{CC}	Exposed tab internally connected to GNDcc (ground of Process Stage)

4 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Process Stage supply voltage	-0.3	+45	V
V_{DD}	Control Logic Stage supply voltage	-0.3	+6.5	V
V_{IN}	DC Input pins voltage (INx, SS, CLK, SDI, OUT_EN)	-0.3	+6.5	V
V_{FAULT}, V_{PGOOD}	$\overline{FAULT}$ and $\overline{PGOOD}$ pins voltage	-0.3	+6.5	V
I_{GNDdd}	DC digital ground reverse current	-	-25	mA
I_{OUT}	Channel Output Current (continuous)	-	Internally limited	A
I_{GNDcc}	DC power ground reverse current	-	-250	mA
I_{RX}	Single channel reverse output current (from OUTX pins to V_{CC})	-	-5	A
I_{RT}	Total reverse output current (from OUTX pins to V_{CC}) @ T_{AMB} 25°C	-	-12	A
I_{IN}	DC Input pins current (INx, SS, CLK, SDI, OUT_EN)	-10	+10	mA
I_{FAULT}, I_{PGODD}	$\overline{FAULT}$ and $\overline{PGOOD}$ pins current	-10	+10	mA
V_{ESD}	Electrostatic discharge with Human Body Model (R = 1.5K Ω; C = 100 pF)	-	2000	V
EAS	Single pulse avalanche energy per channel not simultaneously @T_{AMB}= 125 °C, I_{OUT} = 0.5 A	-	1.8	J
	Single pulse avalanche energy per channel, all channels driven simultaneously @T_{AMB}= 125 °C, I_{OUT} = 0.5 A	-	0.35	
P_{TOT}	Power dissipation at T_c = 25 °C	-	Internally limited (1)	W
T_J	Junction operating temperature	-	Internally limited (1)	°C
T_{STG}	Storage temperature	-	-55 to 150	°C

1. *Protection functions are intended to avoid IC damage in fault conditions and are not intended for continuous operation. Continuous or repetitive operation of protection functions may reduce the IC lifetime.*

5 Thermal data

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance, junction-to-case(1)	1	°C/W
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient (2)	25	
$R_{th\ j\text{-}amb}$	Thermal resistance, junction-to-ambient (3)	15	

1. *Rth between the die and the bottom case surface measured by cold plate as per JESD51.*
2. *JESD51-7.*
3. *IC mounted on the product evaluation board (FR4, 4 layers, 8 cm² for each layer, copper thickness 35 mm).*

6 Electrical characteristics

10.5 V < V_{CC} < 36 V; -40 °C < T_J < 125 °C, unless otherwise specified.

Table 4. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{CC(THON)}$	V_{CC} undervoltage turn-on threshold			9.5	10.5	V
$V_{CC(THOFF)}$	V_{CC} undervoltage turn-off threshold		8	9		V
$V_{CC(HYS)}$	V_{CC} undervoltage hysteresis		0.25	0.5		V
$V_{CCclamp}$	Clamp on VCC pin	I_{clamp} = 20 mA	45	50	52	V
$V_{CC(PGON)}$	V_{CC} Power Good turn-on threshold	V_{DD} = 3.3 V, VCC increasing		17.5	18.4	V
$V_{CC(PGOFF)}$	V_{CC} Power Good turn-off threshold	V_{DD} = 3.3 V, VCC decreasing	15.2	16.5		V
$V_{CC(PG- HYS)}$	V_{CC} Power Good hysteresis			1		V
$R_{DS(ON)}$	ON state resistance	I_{OUT} = 0.5 A, T_J = 25 °C		0.12		Ω
		I_{OUT} = 0.5 A, T_J = 125 °C			0.24	
R_{PD}	Output pull-down resistor			210		kΩ
I_{CC}	Power supply current	All channels in OFF state		5		mA
		All channels in ON state		9		
I_{LGND}	Ground disconnection output current	V_{CC} = VGND = 0 V V_{OUT} = -24 V			500	µA
$V_{OUT(OFF)}$	OFF state output voltage	Channel OFF and I_{OUT} = 0 A			1	V
$I_{OUT(OFF)}$	OFF state output current	Channel OFF and V_{OUT} = 0 V			5	µA

Table 5. Digital supply voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operating voltage range	-	2.75	-	5.5	V
$V_{DD(THON)}$	V_{DD} undervoltage turn-on threshold	-	2.55	-	2.75	V
$V_{DD(THOFF)}$	V_{DD} undervoltage turn-off threshold	-	2.45	-	2.65	V
$V_{DD(HYS)}$	V_{DD} undervoltage hysteresis	-	0.04	0.1	-	V
I_{DD}	V_{DD} supply current	V_{DD} = 5 V and SPI not transmitting	-	4.5	6	mA
		V_{DD} = 3.3 V and SPI not transmitting	-	4.4	5.9	mA

Table 6. Diagnostic pin and output protection function

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{FAULT}	$\overline{FAULT}$ pin open drain voltage output low	I_{FAULT} = 5 mA			0.4	V
I_{LFAULT}	$\overline{FAULT}$ output leakage current	V_{FAULT} = 5 V			1	µA
V_{PGOOD}	$\overline{PGOOD}$ pin open drain voltage output low	I_{PGOOD} = 5 mA			0.4	V
I_{LPGOOD}	$\overline{PGOOD}$ output leakage current	V_{PGOOD} = 5 V			1	µA
I_{PEAK}	Maximum DC output current before limitation	V_{CC} = 24 V R_{LOAD} = 0 Ω		1.6		A

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{LIM}	Short-circuit current limitation	V_{CC} = 24 V R_{LOAD} = 0 Ω	0.7	1.3	1.9	A
Hyst	ILIM tracking limits			0.3		A
T_{JSD}	Junction shutdown temperature		150	170		°C
T_{JR}	Junction reset temperature			150		°C
T_{JHYST}	Junction thermal hysteresis			20		°C
T_{CSD}	Case shutdown temperature		115	130	145	°C
T_{CR}	Case reset temperature			110		°C
T_{CHYST}	Case thermal hysteresis			20		°C
V_{DEMAG}	Output voltage at turn-off	I_{OUT} = 0.5 A; I_{LOAD} >= 1 mH	V_{CC}-45	V_{CC}-50	V_{CC}-52	V

Table 7. Power switching characteristics (V_{CC} = 24 V; -40°C < T_J < 125°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
dV/dt(ON)	Turn-on voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5.6	-	V/µs
dV/dt(OFF)	Turn-off voltage slope	I_{OUT} = 0.5 A, resistive load 48 Ω	-	2.81	-	V/µs
td(ON)	Turn-on delay time (see Figure 5)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	17	22	µs
td(OFF)	Turn-off delay time (see Figure 5)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	22	40	µs
tf	Fall time (see Figure 4)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5	-	µs
tr	Rise time (see Figure 4)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	5	-	µs
$t_{w(OUT\_EN)}$	OUT_EN pulse width (see Figure 10, Figure 11)	I_{OUT} = 0.5 A, resistive load 48 Ω	150	-	-	ns
$t_{p(OUT\_EN)}$	OUT_EN propagation delay (see Figure 10, Figure 11)	I_{OUT} = 0.5 A, resistive load 48 Ω	-	22	40	µs

Figure 3. $R_{DS(on)}$ measurement

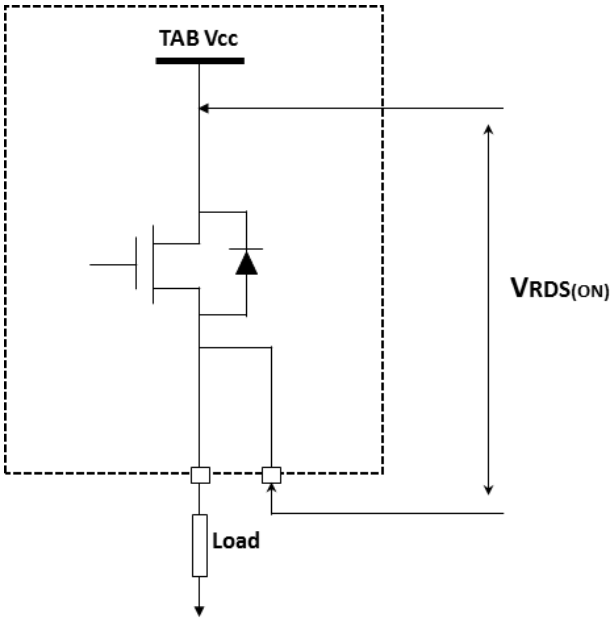


Figure 4. dV/dT definition

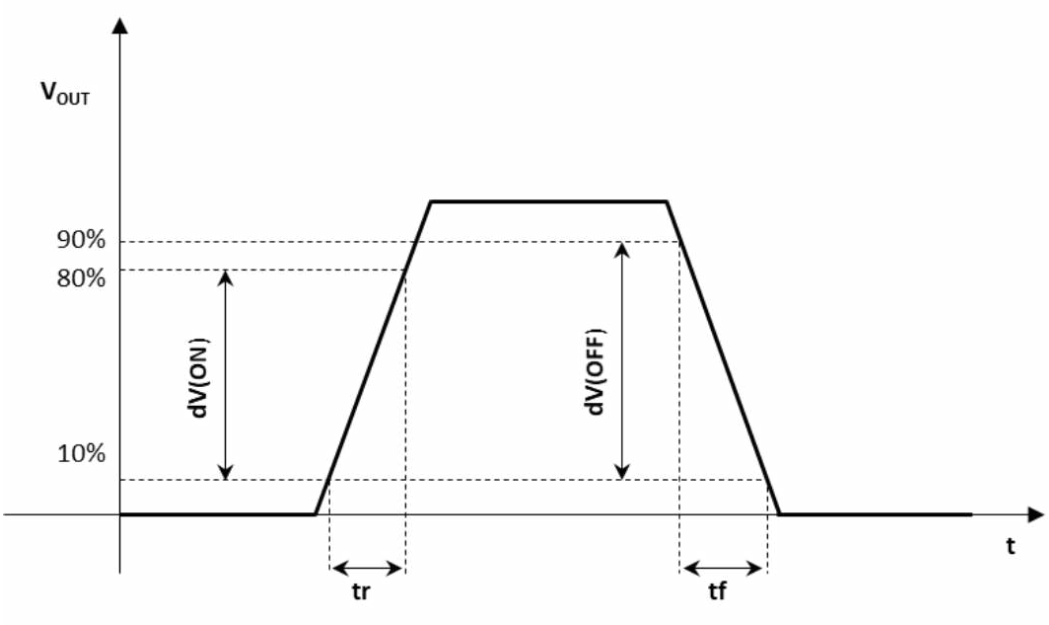


Figure 5. td(ON)-td(OFF) definition

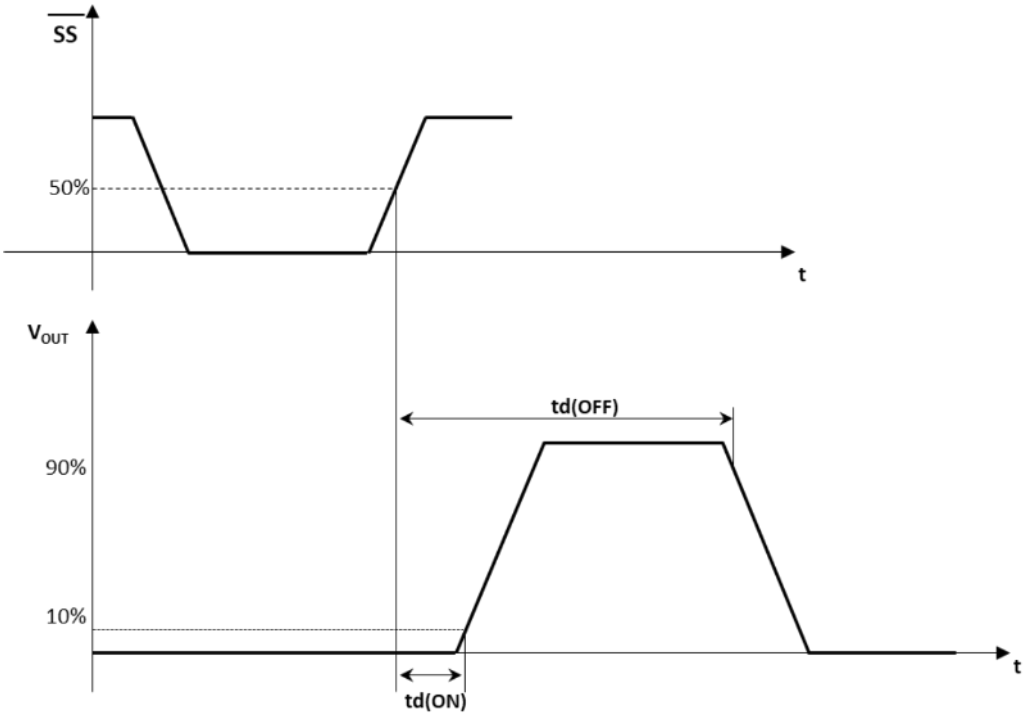


Table 8. Logic inputs and output

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	$\overline{SS}$, CLK, SDI and OUT_EN low level voltage	-	-0.3	-	0.3 x V_{DD}	V
V_{IH}	$\overline{SS}$, CLK, SDI and OUT_EN high level voltage	-	0.7 x V_{DD}	-	V_{DD} +0.3	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{I(HYST)}$	$\overline{SS}$, CLK, SDI and OUT_EN hysteresis	V_{DD} = 5 V	-	100	-	mV
I_{IN}	$\overline{SS}$, CLK, SDI and OUT_EN current	V_{IN} = 5 V	10	-	-	µA
V_{SDOH}	SDO high level voltage	I_{SDO} = -1 mA	V_{DD}-0.2	-	-	V
V_{SDOL}	SDO low level voltage	I_{SDO} = +2 mA	-	-	0.2	V

Table 9. Serial interface timings (V_{DD} = 5 V; V_{CC} = 24 V; -40°C < T_J < 125°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
fCLK	SPI clock frequency	-	-	-	20	MHz
T_{CLK}	SPI clock period	-	50	-	-	ns
tr(CLK) tf(CLK)	SPI clock rise/fall time (see Figure 7, Figure 8)	-	-	-	5	ns
tsu(SS)	SS setup time (see Figure 7, Figure 8)	-	80	-	-	ns
th(SS)	SS hold time (see Figure 7, Figure 8)	-	80	-	-	ns
tc(SS)	SS disable time (see Figure 7, Figure 8)	-	20	-	-	µs
tw(CLK)	CLK high time (see Figure 7, Figure 8)	-	15	-	-	ns
tsu(SDI)	Data input setup time (see Figure 7, Figure 8)	-	6	-	-	ns
th(SDI)	Data input hold time (see Figure 7, Figure 8)	-	6	-	-	ns
ta(SDO)	Data output access time (see Figure 7, Figure 8)	$R_{PULL-DOWN}$ = 300 Ω C_{LOAD} = 50 pF	-	-	25	ns
tdis(SDO)	Data output disable time (see Figure 7, Figure 8)		-	-	20	ns
tv(SDO)	Data output valid time (see Figure 7, Figure 8)		-	-	20	ns
t_{JITTER}	Jitter on single channel $t_{CYCLE\ (SS)}$ = 20 µs	-	-	-	6	µs
	Jitter on single channel $t_{CYCLE\ (SS)}$ < 20 µs	-	-	-	20	

Table 10. Internal communication timings (V_{DD} = 5 V; V_{CC} = 24 V; -40°C < T_J < 125°C)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$f_{refresh}$	Refresh delay	-	-	15	-	kHz
t_{WD}	Watchdog time	-	272	320	400	µs

Table 11. Insulation and safety-related specifications

Symbol	Parameter	Test conditions	Value	Unit
CLR	Clearance (minimum external air gap)	Measured from input terminals to output terminals, shortest distance through air	3.3	mm
CPG	Creepage (minimum external tracking)	Measured from input terminals to output terminals, shortest distance path along body	3.3	mm
CTI	Comparative tracking index (tracking resistance)	DIN IEC 112/VDE 0303 part 1	≥600	V
	Isolation group	Material group (DIN VDE 0110, 1/89, Table 1)	I	-

Table 12. Insulation characteristics

Symbol	Parameter	Test condition	Value	Unit
IEC 60747-5-5				
V_{IORM}	Maximum working isolation	-	937	V_{PEAK}
V_{PR}	Input-to-output test voltage	Method a, type test, V_{PR} = V_{IORM} x 1.6, tm = 10s partial discharge < 5 pC	1500	V_{PEAK}
		Method b, 100% production test, V_{PR} = V_{IORM} x 1.875, tm = 1s partial discharge < 5 pC	1758	V_{PEAK}
V_{IOTM}	Transient overvoltage	Type test; t_{ini} = 60 s	4245	V_{PEAK}
V_{IOSM}	Maximum surge insulation voltage	Type test	4245	V_{PEAK}
R_{IO}	Insulation resistance	V_{IO} = 500 V at ts	$>10^9$	Ω
UL1577				
V_{ISO}	Insulation withstand voltage	1 min. type test	2500/3536	V_{rms}/V_{PEAK}
V_{ISO} test	Insulation withstand test	1 sec. 100% production	3000/4245	V_{rms}/V_{PEAK}

Table 13. Safety limits

Symbol	Parameter	Test conditions	Value	Unit
Input safety, Logic side				
T_{SI}	Safety temperature of Logic side	-	150	°C
P_{SI}	Safety power of Logic side	VDD ≤ 6.5V, $V_{LOGIC(x)}$ ≤ 6.5V, $I_{LOGIC(x)}$ ≤ 10mA, T_J ≤ T_{SI}	0.9	W
Output safety, Process side				
T_{SO}	Safety temperature of Process side	-	150	°C
P_{SO}	Safety power of Logic side	VCC ≤ 36V, $I_{OUT(x)}$ ≤ 1.5mA, T_J ≤ T_{SO}	5	W

The above limits are measured according to VDE 0884-11. Respecting the above limits prevents potential damage to the isolation barrier upon failure on logic or process side circuitry. The user should apply these values to protect the IC and ensure the safety of the embedded isolation barrier. LOGIC(x) stands for any pin on the logic side; OUT(x) stands for any of the 8 output pins on the process side.

7 Serial interface

7.1 Functional description

An integrated SPI peripheral provides a fast communication interface between an external microcontroller and the IC to drive the Power Stage outputs and monitor the per-channel OVT diagnostic information of the device. Daisy chaining is supported.

It follows the timing requirement established by the synchronous serial communication standard and works up to 20 MHz communication speed.

The communication implemented expects 8-bit data communication; the frame sent by the microcontroller only contains the status of the channels (ON or OFF), while the frame received by the microcontroller contains information regarding channel fault status (bit “0” for a running channel represents normal operation; bit 1 represents a fault condition).

Table 14. SDI frame

MSB							LSB
IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0

Table 15. SDO frame

MSB							LSB
F7	F6	F5	F4	F3	F2	F1	F0

7.2 Serial data in (SDI)

This pin is the IC input of the serial command frame (MOSI). SDI reads on CLK rising edges and so the microcontroller changes SDI state during CLK falling edges.

The bits sent through the SDI line are shifted in the internal Output Status Register. In daisy chain communication, the microcontroller keeps the $\overline{SS}$ low after the 8th bit to allow the shift of the Output Status Register to the SDO line. The bits in the Output Status Register are frozen by the internal logic when the $\overline{SS}$ goes high.

7.3 Serial data out (SDO)

This pin is the IC output of the serial fault frame (MISO). The information on SDO is updated on CLK falling edges, whereas the microcontroller reads the SDO frame on CLK rising edges, as established by standard. At communication startup, when the $\overline{SS}$ falling edge is arriving, only the first bit of the frame is available.

SDO pin is tri-stated when the $\overline{SS}$ signal is high.

In daisy chain communication and OUT_EN driven high, the SDO line transfers the content of the internal Output Status Register after the 8th CLK pulse.

7.4 Serial data clock (CLK)

The CLK line is the IC input clock for serial data sampling. SDO is updated on CLK falling edges, and then sampled on the rising edge. The SDI line is sampled on SCK rising edges.

When the $\overline{SS}$ signal is high (slave not selected), the microcontroller should drive the CLK low (settings for MCU SPI port are CPHA = 0 and CPOL = 0).

7.5 Slave select ($\overline{SS}$)

The slave select $\overline{SS}$ signal is used to enable the ISO8200AQ serial communication shift register. Data is flushed in through the SDI pin and out from the SDO pin only when the $\overline{SS}$ pin is low. On the $\overline{SS}$ pin falling edge, the Fault Register (containing IC fault conditions) is frozen, so any change on the channel status is latched until the next $\overline{SS}$ falling edge event, the SDO is enabled and the internal refresh is simultaneously disabled. On the $\overline{SS}$ pin rising edge event, the 8 bits in the Output Status Register are frozen and the outputs of the Process Stage are driven accordingly. If more than 8 bits are flushed into the IC, only the last 8 are evaluated, the other bits are flushed out from the SDO pin after fault condition bits. This method allows proper communication even in daisy chain configuration.

Figure 6. SPI mode diagram

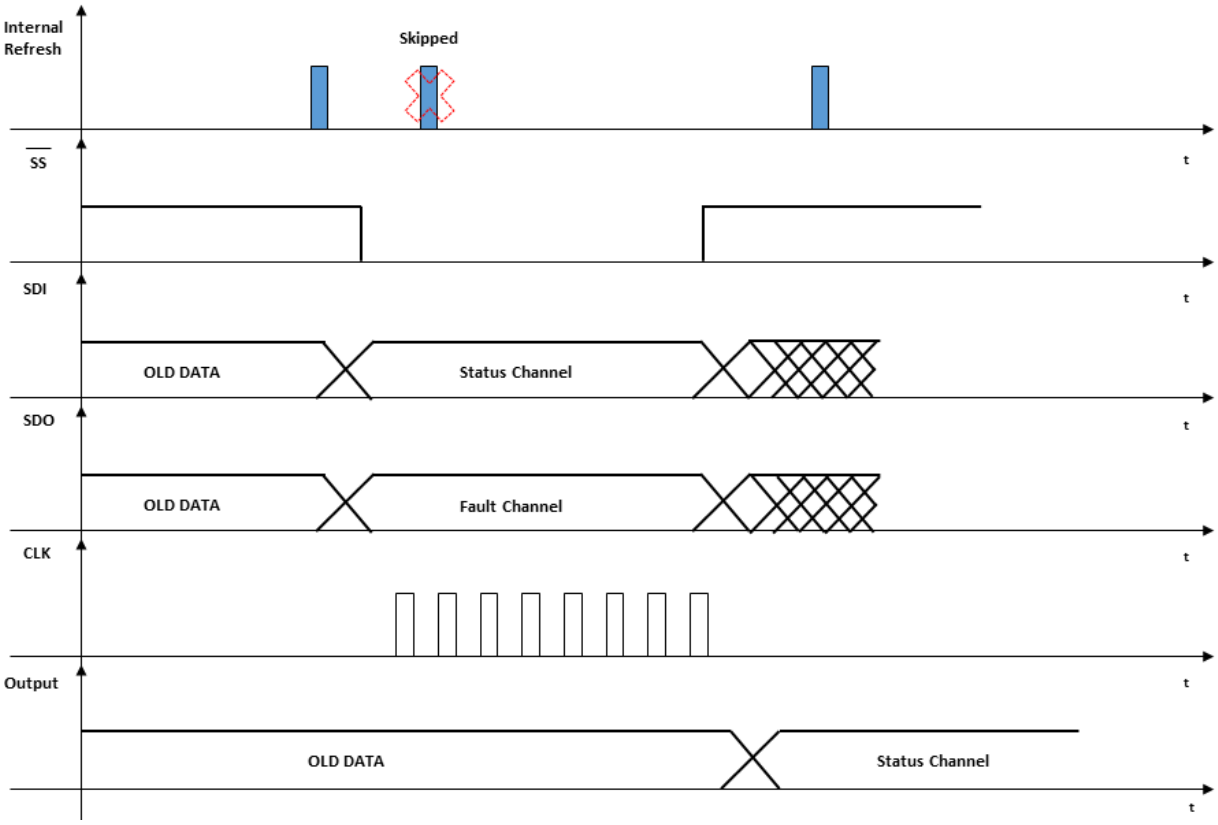


Figure 7. SPI input timing diagram

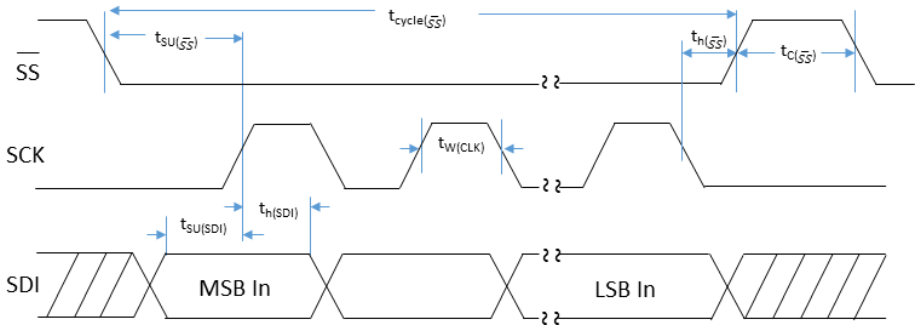
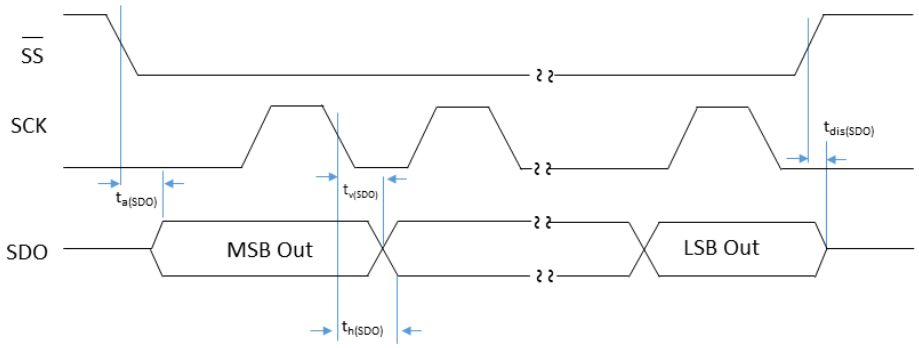


Figure 8. **SPI output timing diagram**



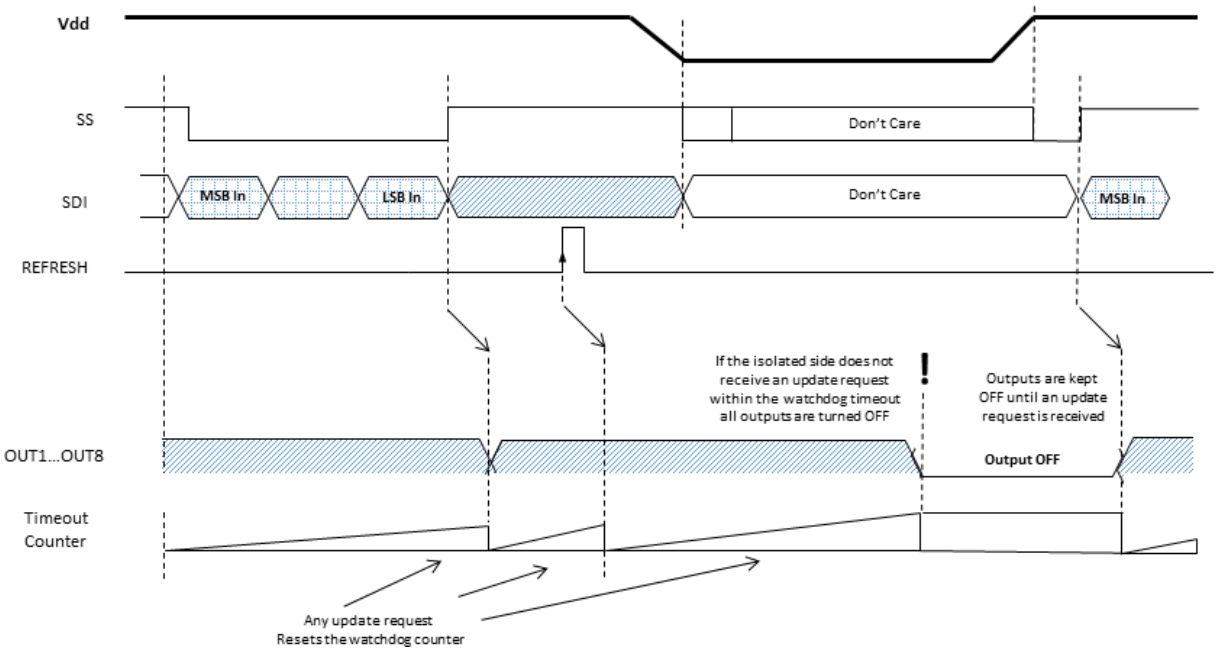
7.5.1 Watchdog

The IC consists of two chips (Logic Stage and Process Stage) supplied by two independent and galvanic isolated sources (V_{DD}/GND_{DD} and V_{CC}/GND_{CC} pins, respectively).

The IC provides a watchdog function in order to ensure a safe condition for the Process Stage when V_{DD} (or GND_{DD}) supply voltage is missing. At the end of each SPI communication, the channel status register on Logic Stage is ready to be transferred to the Process Stage: the IC resets the internal watchdog counter and turns ON/OFF the outputs accordingly only when the new output status configuration has been received at Process Stage. If the Logic Stage does not update the output status within t_{WD}, all the outputs of the Process Stage are disabled until a new update request is received (this also happens if $\overline{SS}$ stays low for longer than t_{WD}).

Independent of the SPI communication, the Logic Stage chip periodically sends a refresh signal to the Process Stage chip. The refresh signal is also considered a valid update signal to reset the timeout counter on the Process Stage, so the isolated side watchdog does not protect the system from a failure of the host controller (e.g., MCU freezing).

Figure 9. **Watchdog behavior**



7.5.2 Output enable (OUT_EN)

This pin provides a fast way to disable all the outputs simultaneously. When the OUT_EN pin is driven low for at least $t_{W\ (\ OUT\_EN)}$, all eight outputs are disabled. This timing execution is compatible with an external reset push from the operator and/or safety requirements.

Note that the OUT_EN signal acts as a reset for the internal data register driving the output switches: when the OUT_EN is low, SDO is pulled down and the output stage is forced OFF. To re-enable SDO, it is necessary to raise the OUT_EN pin; to enable the output stage again, it is then necessary to raise the OUT_EN pin and send the desired output configuration by an SPI command.

Figure 10. OUT_EN without effect on output

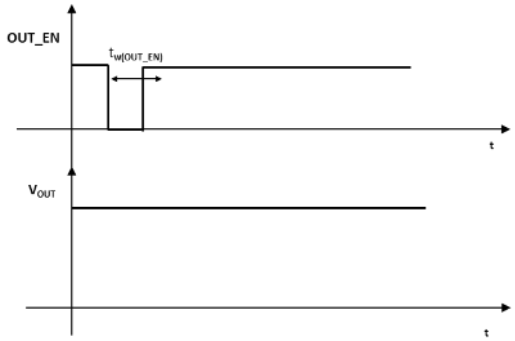
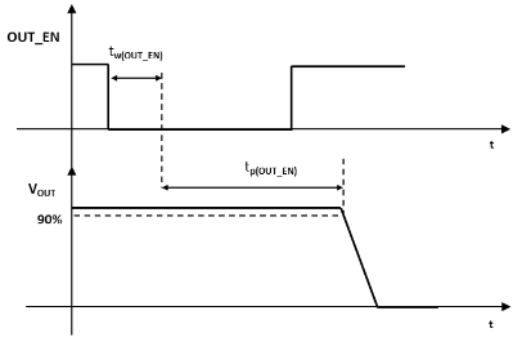


Figure 11. OUT_EN effective on output channel



7.6 FAULT and PGOOD indications

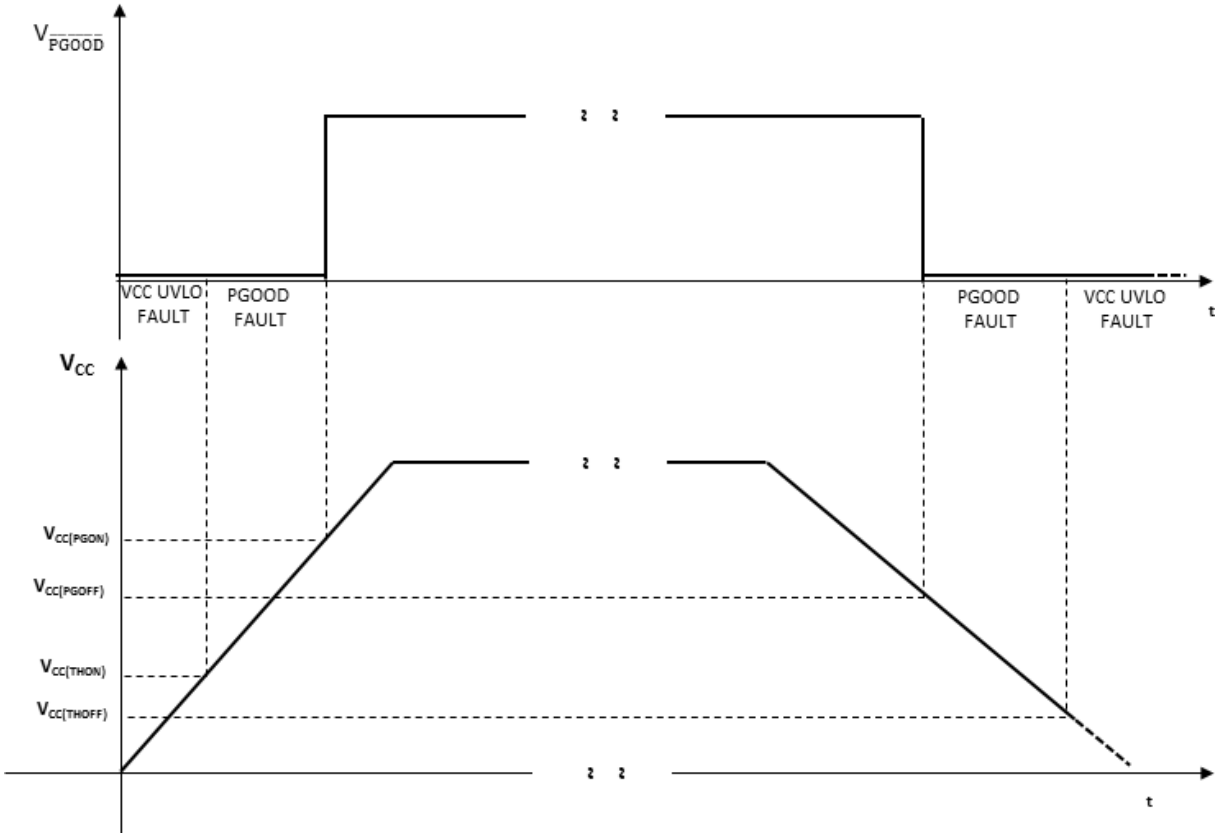
The $\overline{\text{FAULT}}$ pin is an active low open drain output indicating fault conditions. This pin is activated when at least one of the following conditions occurs:

- Junction overtemperature (TJX >TJSD) of one or more channels of the Process Stage. The MISO signal can be used to detect which channels are in thermal fault (per-channel OVT diagnostic)
- No module-8 SPI communication (the number of bits sent through the SDI is not a multiple of 8)
- Internal communication error. In fact, the IC is able to identify (and report to the microcontroller) if any errors occur in the data transmission between isolation. When it occurs, the output stage maintains the previous ON/OFF status.

The $\overline{\text{PGOOD}}$ pin is an active low open drain output indicating whether the supply voltage of the Process Stage chip is lower than the internal threshold (see Figure 12).

Note: When $\overline{SS}$ signal is low the transmission between Control Logic Stage and Process Stage is inhibited and the status of $\overline{PGOOD}$ is not refreshed ($\overline{PGOOD}$ refresh time < 120 µs).

Figure 12. **Power GOOD pin behavior**



7.7 Truth table

Table 16. **Truth table**

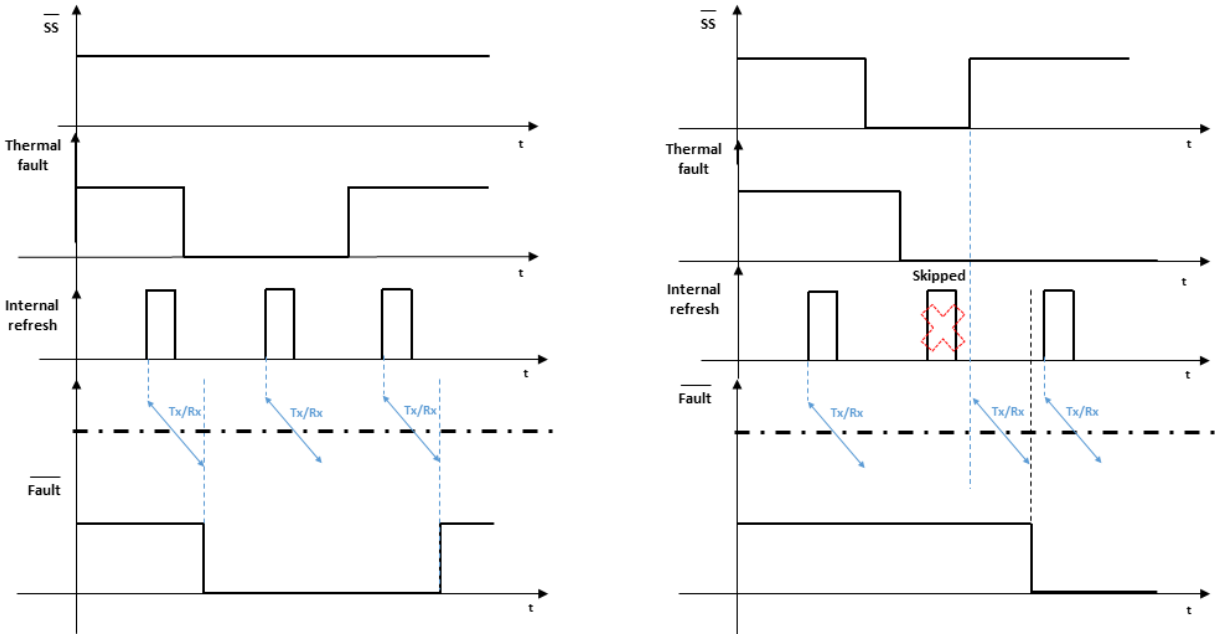
x = maintain the previous condition.

Condition	Status register BIT_x	OUT_x	Fault register BIT_x	FAULT	PGOOD
Normal operation	1	ON	0	H (not active)	H (not active)
	0	OFF	0		
Thermal Junction (T_{JX}> T_{JSD})	1	OFF	1	L (active)	Don‘t care
	0	OFF	1	H (not active)	
Thermal Case T_C > T_{CSD}	See Figure 20			Don‘t care	Don‘t care
V_{CC} UVLO FAULT (Figure 12)	0	OFF	X	X	L (active)
	1				
POWER GOOD FAULT (Figure 12)	1	ON	Don‘t care	Don‘t care	L (active)
	0	OFF			
V_{DD} UVLO (Watchdog)	X	OFF	X	H (not active)	H (not active)
SPI FAULT (module-8 violation)	X	X	Don‘t care	L (active)	Don‘t care
Internal communication error	X	X	X	L (active)	Don‘t care

7.7.1 Junction overtemperature

The thermal status of the device is updated during each transmission sequence between the two isolated stages. When $\overline{SS}$ is low, the communication between the two stages is disabled. In this case, the thermal status of the device cannot be updated, and the $\overline{FAULT}$ indication may be different to the actual status. In any case, the thermal protections of the channel outputs in the Process Stage are always operative.

Figure 13. Thermal status update



8 Power section

8.1 Current limitation

The current limitation process is activated when the current sense connected on the output stage measures a current value higher than a fixed threshold. When this condition is verified, the gate voltage is modulated to avoid output current increasing over the limitation value.

The following figures (where BIT_X is intended as Xth bit of the Output Status Register) show typical output current waveforms with different load conditions.

Figure 14. Switching on resistive load

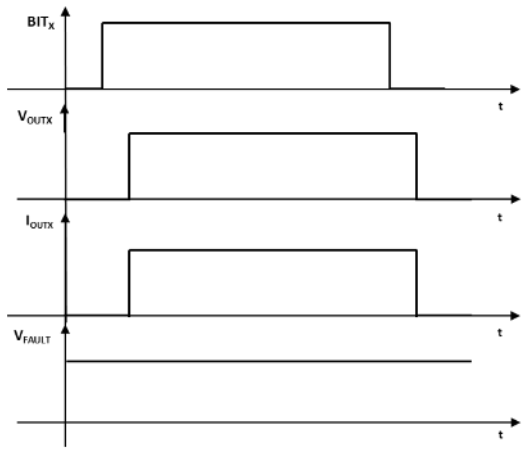


Figure 15. Switching on bulb lamp

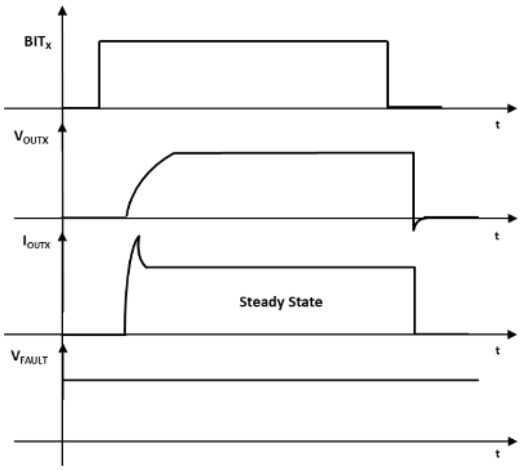


Figure 16. Switching on light inductive load

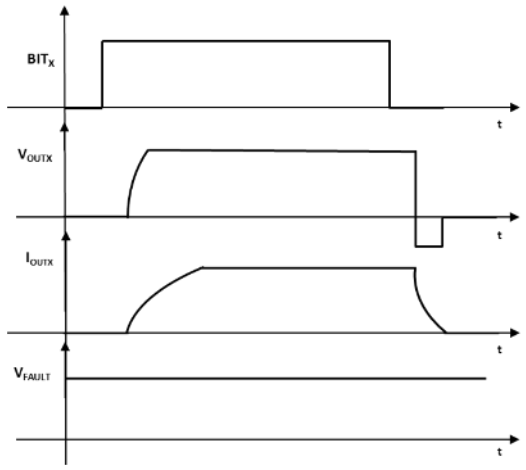


Figure 17. Switching on heavy inductive load

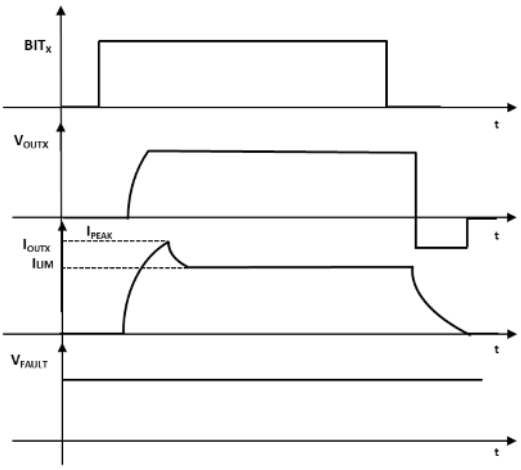


Figure 18. **Short-circuit (with OVT) during ON state**

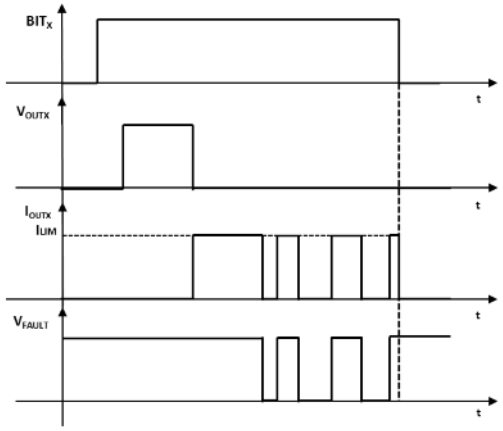
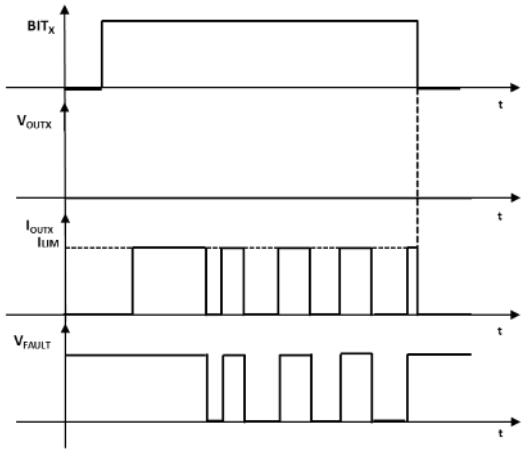


Figure 19. **Switching on short-circuit (with OVT)**



8.2 Thermal protection

The device is protected against overheating due to overload conditions. During driving period, if the output is overloaded, the device suffers two different thermal stresses, the first one related to the junction, and the second related to the case.

The two faults have different trigger thresholds: the junction protection threshold (T_{JSD}) is higher than that of the case protection (T_{CSD}). Generally, the first protection that is activated in thermal stress conditions is the junction thermal shutdown. The output is turned off when the temperature is higher than the related threshold and turned back on when it falls below the reset threshold (T_{JR}). This behavior continues while the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection is activated, and the output is switched off and back on when the junction temperature of each channel in fault and case temperature are below the respective reset thresholds.

Figure 20. **Thermal protection flowchart**

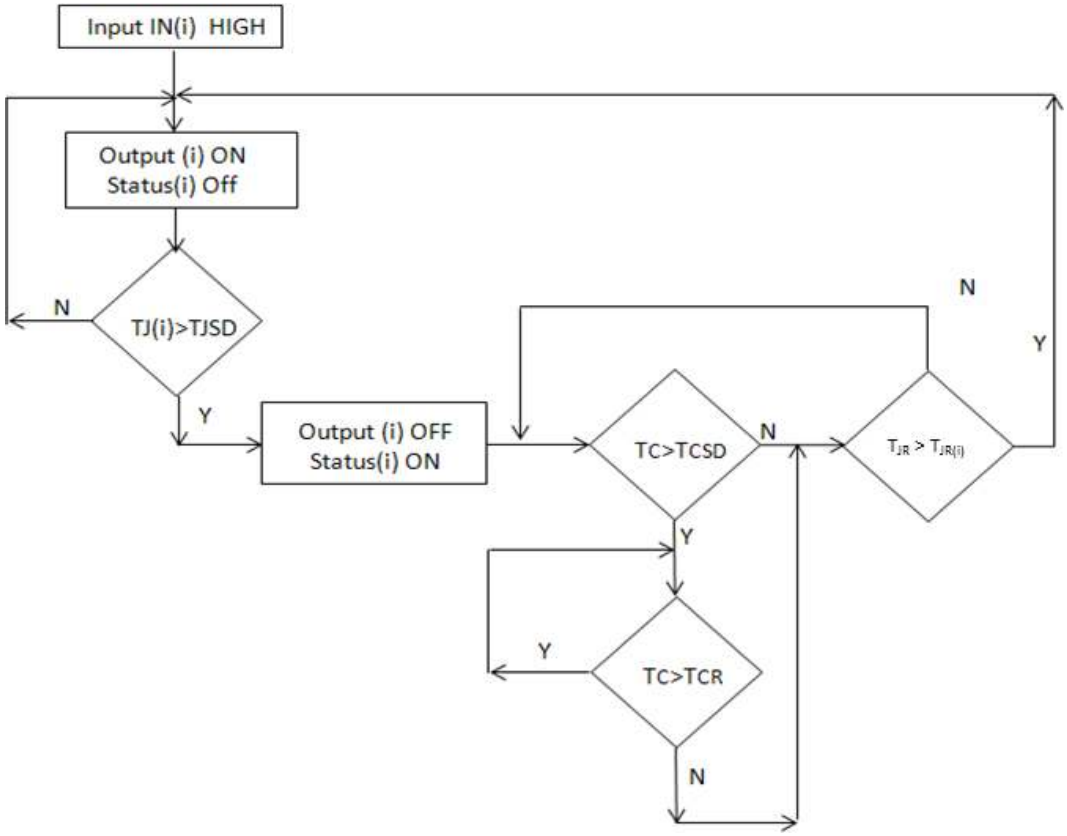


Figure 21. **Thermal protection and fault behavior (T_{JSD} triggered before T_{CSD})**

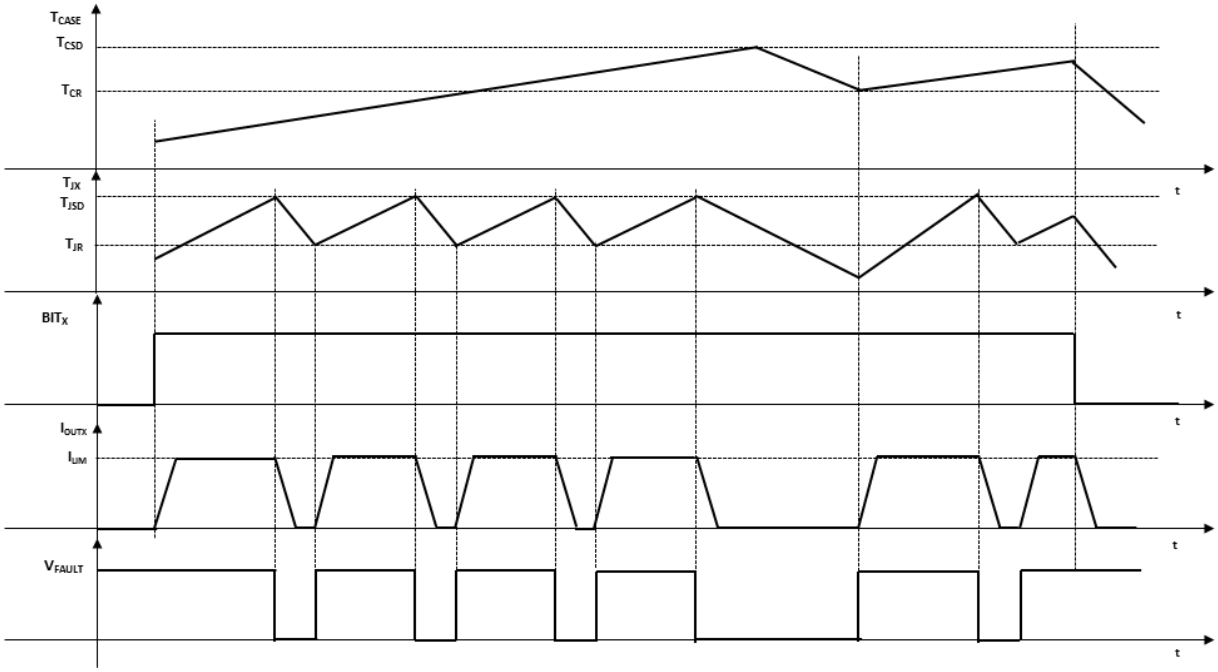
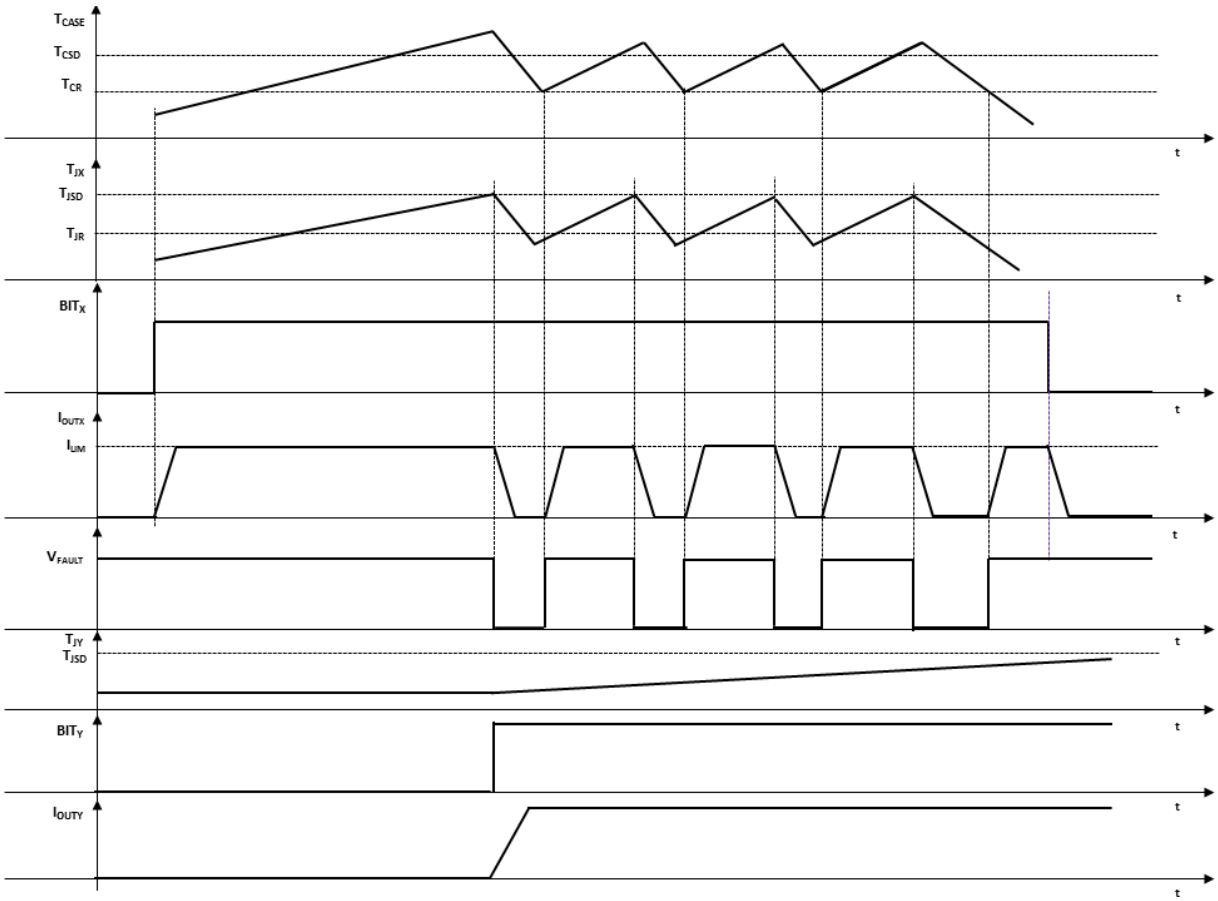


Figure 22. Thermal protection and fault behavior (T_{CSD} triggered before T_{JSD})



9 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions (or both, which is recommended):

1. Placing a resistor (R_{GND}) between IC GND pin and load GND
2. Placing a diode in parallel to a resistor between IC GND pin and load GND

If option 1 is selected, the minimum resistance value must be selected according to the following equation:

$$R_{GND} \geq \frac{V_{CC}}{I_{GND_{CC}}} \quad (1)$$

where $I_{GND_{CC}}$ is the DC reverse ground pin current and can be found in Table 2.

The power dissipated by R_{GND} during reverse polarity is:

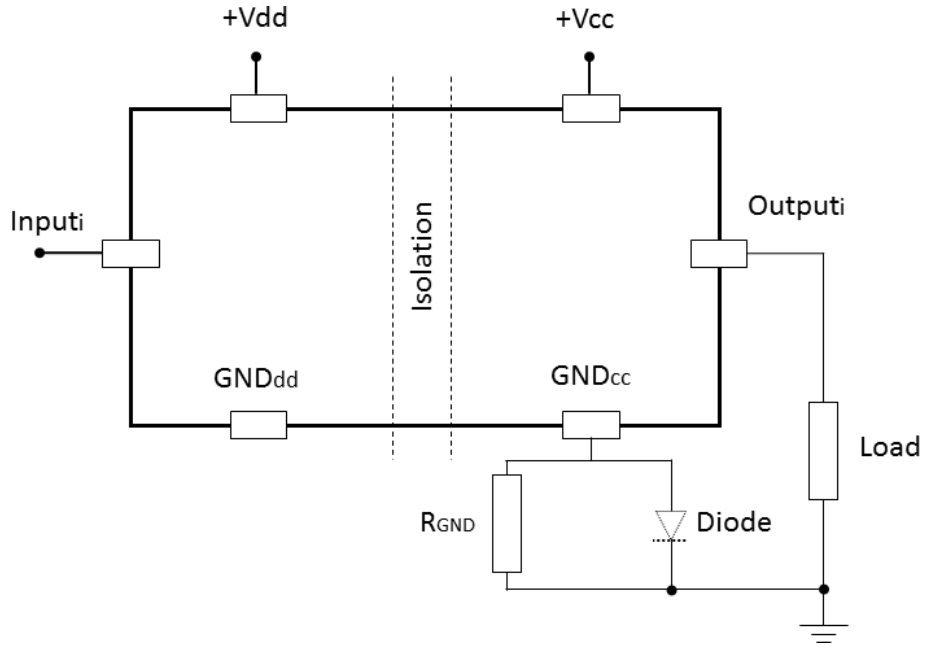
$$P_D = \frac{(V_{CC})^2}{R_{GND}} \quad (2)$$

If option 2 is selected, the diode has to be chosen by taking into account VRRM > $|V_{CC}|$ and its power dissipation capability:

$$P_D \geq I_S \times V_F \quad (3)$$

*Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the system. Using option 1, ΔV = Rgnd * Icc. Using option 2, ΔV = VF@(IF).*

Figure 23. Reverse polarity protection



Note: Input(i) is intended as any input pin on logic side.
This schematic can be used with any type of load.

10 Reverse polarity on VDD

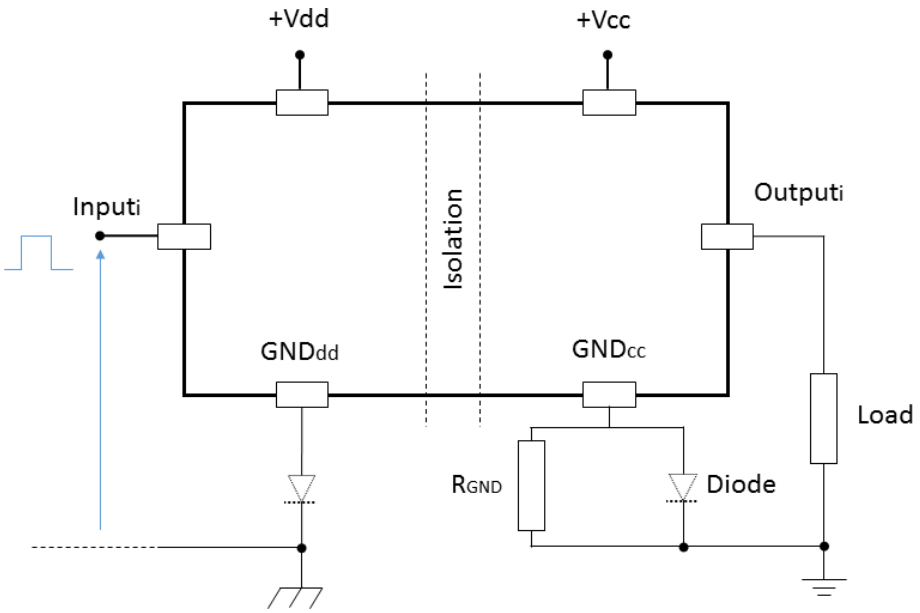
The reverse polarity on V_{DD} can be implemented on board by placing a diode between the GND_{DD} pin and GND digital ground.

The diode must be chosen by taking into account VRRM >$|V_{DD}|$ and its power dissipation capability:

$$P_D \geq I_{DD} \times V_F \quad (4)$$

Note: In normal operation (no reverse polarity), there is a voltage drop (ΔV = VF@(Idd)) between GND_{DD} of the device and digital ground of the system. In order to guarantee to proper
triggering of the input signal, ΔV(max.) must result lower than $V_{IH(MIN)}$.

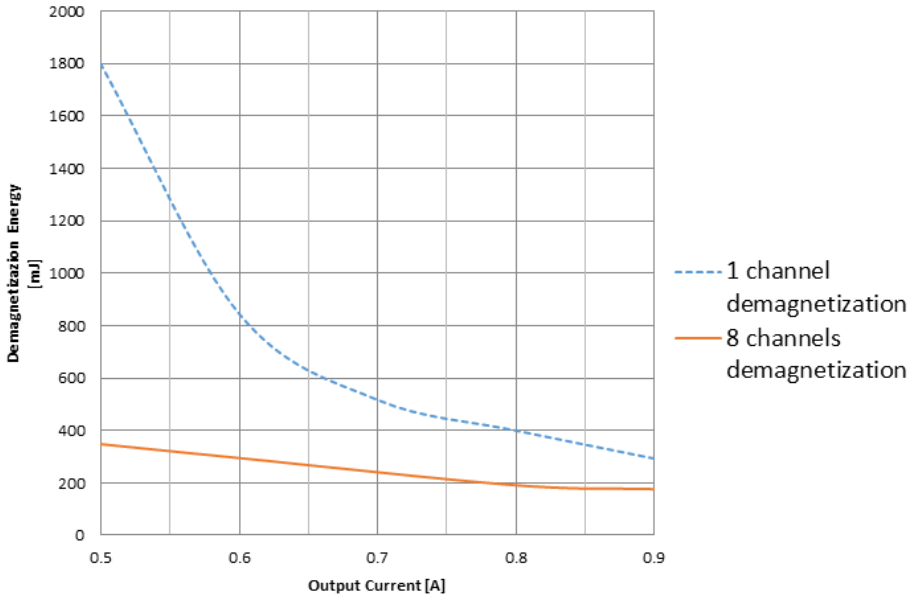
Figure 24. V_{DD} reverse polarity protection



Note: Input(i) is intended as any input pin on logic side.

11 Demagnetization energy

Figure 25. **Single pulse demagnetization energy vs. load current (Typical values at T_{AMB} = 125°C)**

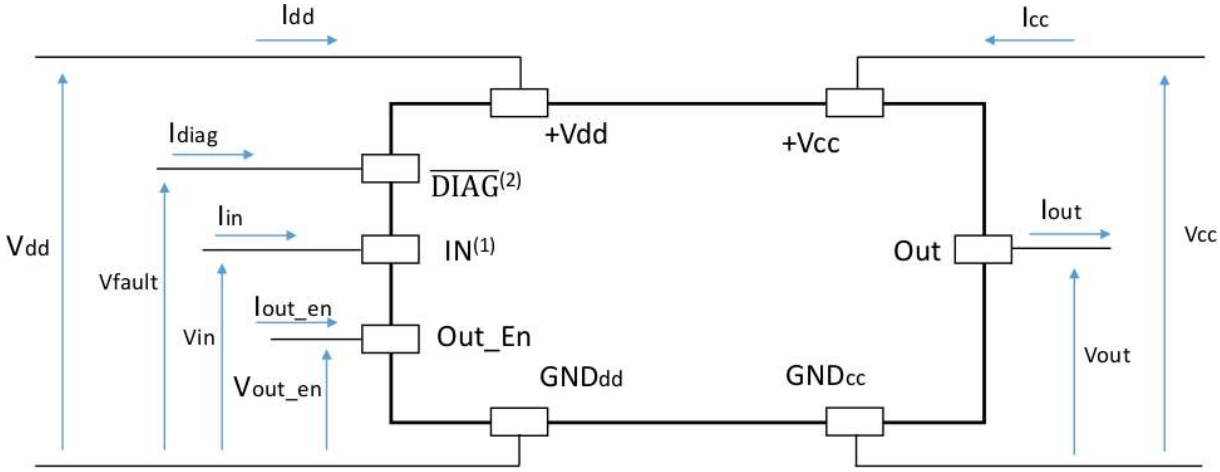


12 Conventions

12.1 Supply voltage and power output conventions

Figure 26. Supply voltage and power output conventions

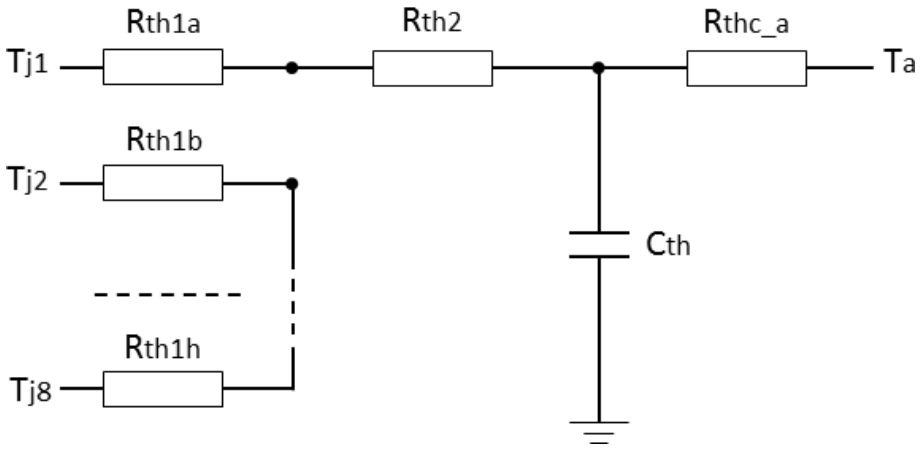
(1): intended as any input pin on logic side
(2): intended as any open drain pin on logic side



13 Thermal information

13.1 Thermal impedance

Figure 27. **Simplified thermal model of the process stage**

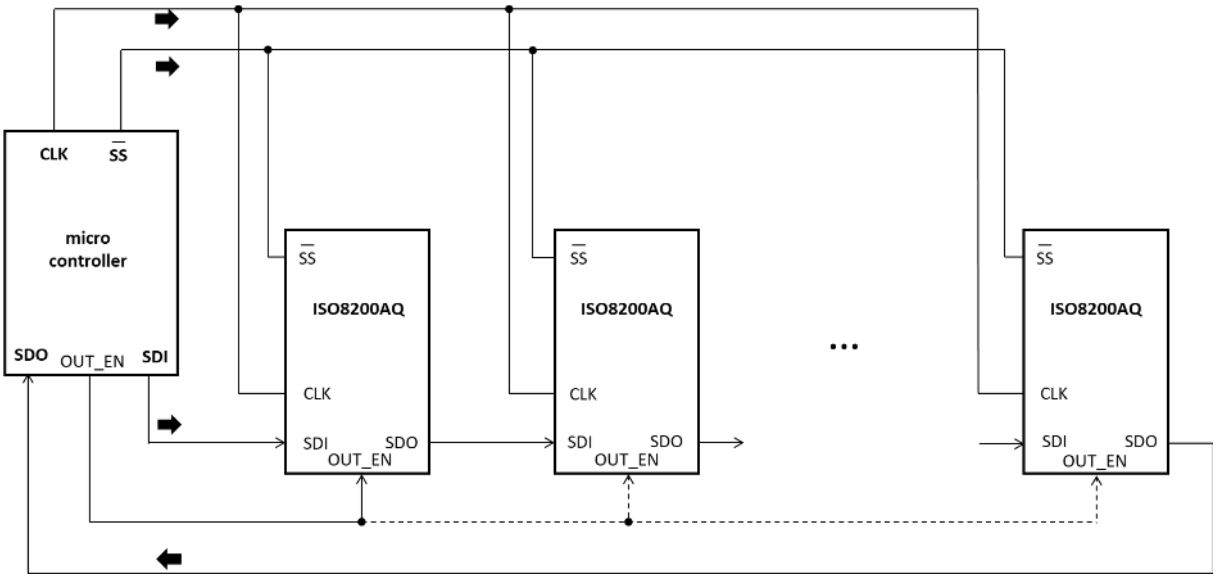


14 Daisy chaining

The ISO8200AQ can be daisy-chained by connecting the MOSI port of the micro-controller to the SDI pin of the first IC of the chain; the SDO pin of the first IC of the chain to the SDI pin of the second (and similarly for the next ICs of chain); the SDO pin of the last IC of the chain to the MISO port of the micro-controller. See an example in figure Figure 28. Example of daisy chaining connection.

The $t_{cycle(\overline{SS})}$ (Figure 7. SPI input timing diagram) must take into account of the internal communication timing ($f_{refresh}$ and t_{WD}): it is recommended $t_{cycle(\overline{SS})}$ (max) < 136µs. The maximum number of ICs that can be daisy chained depends on the SPI clock frequency set by the micro-controller.

Figure 28. Example of daisy chaining connection



15 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

15.1 TFQFPN32 package information

Figure 29. TFQFPN32 package outline

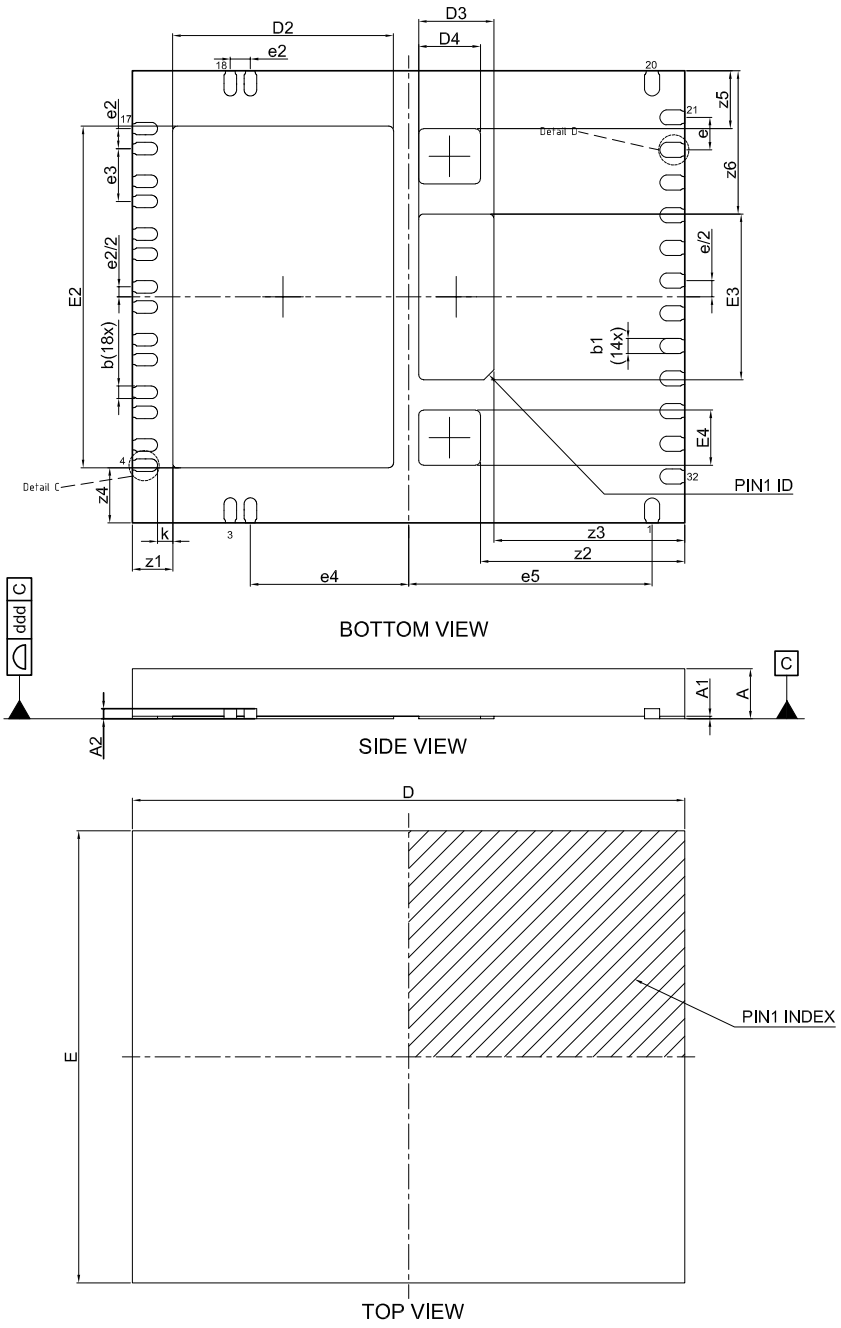


Figure 30. **TFQFPN32 package detail outline**

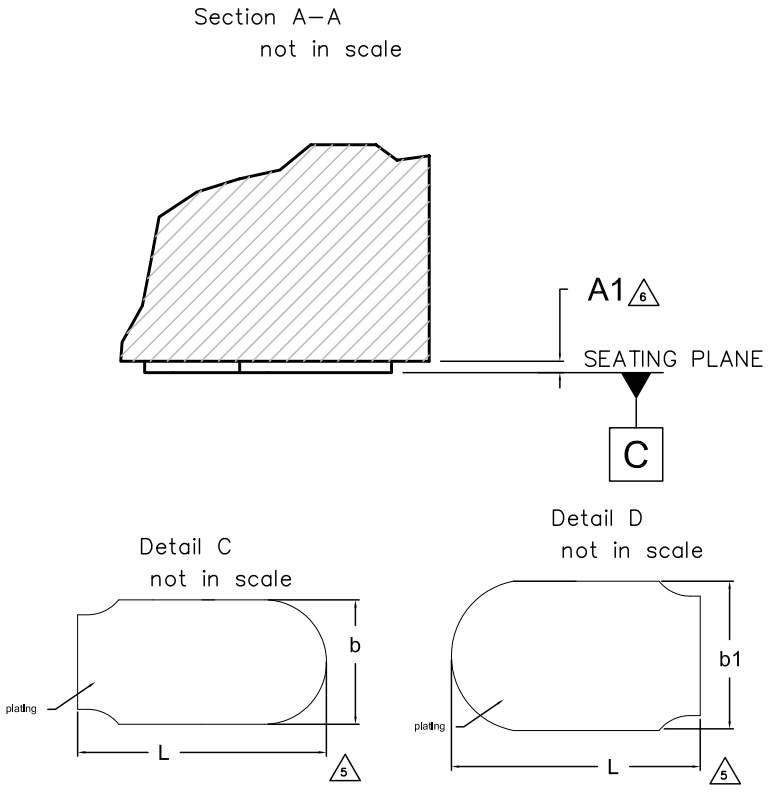


Table 17. **TFQFPN32 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	0.95	1.00	1.05
A1	0	-	0.05
A2	-	0.20 REF	-
b (1)	0.20	0.25	0.30
b1(1)	0.25	0.30	0.35
D	10.90	11.0	11.10
E(1)	8.90	9.00	9.10
D2	4.30	4.40	4.50
E2	6.70	6.80	6.90
D3	1.40	1.50	1.60
E3	3.20	3.30	3.40
D4	1.13	1.23	1.33
E4	1.00	1.10	1.20
e	-	0.65	-
e2	-	0.40	-
e3	-	1.05	-
e4	-	3.15	-
e5	-	4.85	-

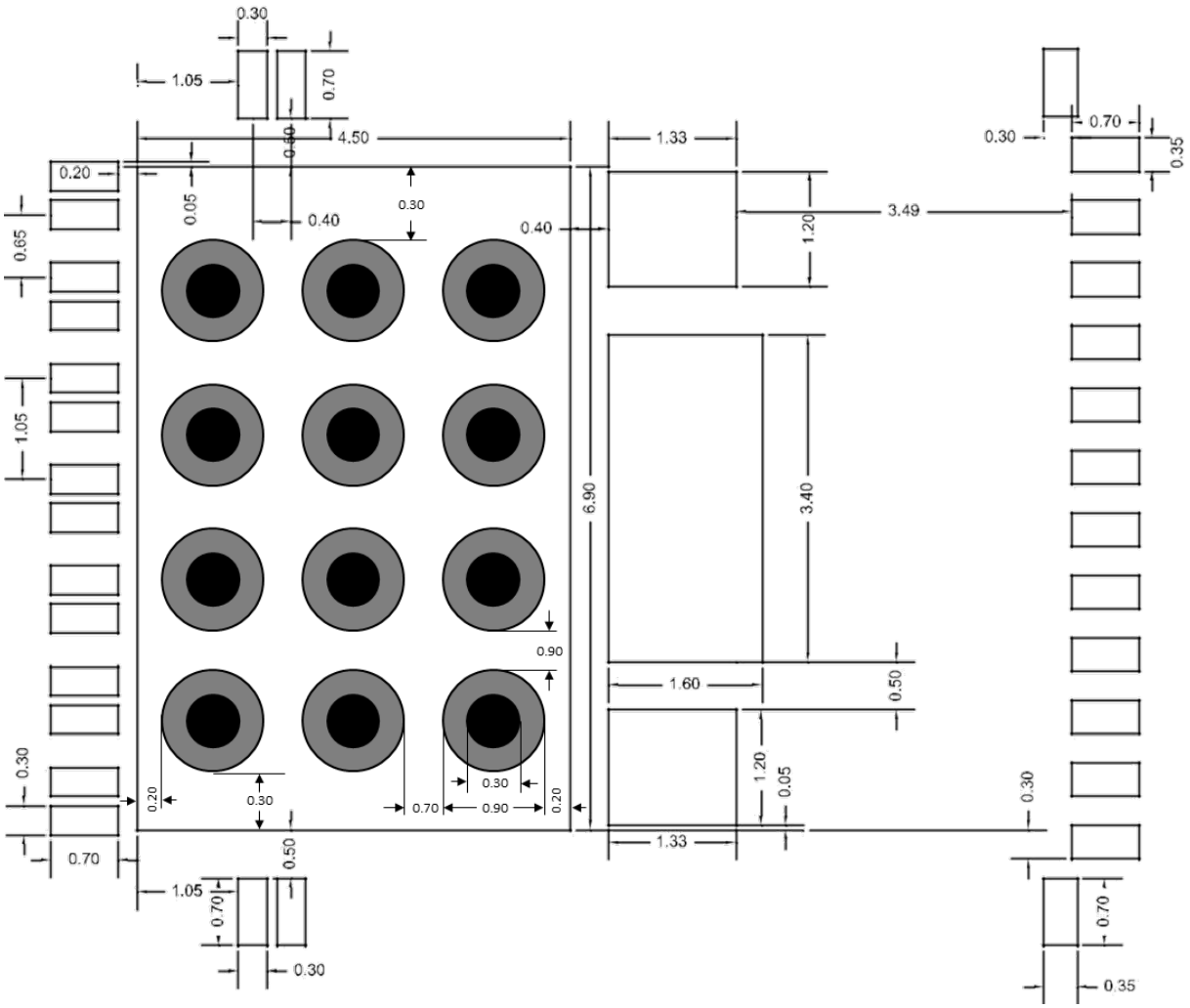
Dim.	mm		
	Min.	Typ.	Max.
k	0	0.30	-
z1	-	0.80	-
z2	-	4.07	-
z3	-	3.80	-
z4	-	1.10	-
z5	-	1.15	-
z6	-	2.85	-
L(1)	0.45	0.50	0.55

1. *Dimensions “b” and “L” are measured on terminal plating surface.*

Table 18. Tolerance of form and position

Symbol	Tolerance of form and position	Definition	Notes
Aaa	0.15	The bilateral profile tolerance that controls the position of the plastic body sides. The centers of the profile zones are defined by the basic dimensions D and E.	-
Bbb	0.10	The tolerance that controls the position of the entire terminal pattern with respect to datums A and B. The center of the tolerance zone for each terminal is defined by the basic dimension "e" as related to datum's A and B.	-
Ccc	0.10	The tolerance located parallel to the seating plane in which the top surface of the package must be located.	-
ddd	0.08	The tolerance that controls the position of the terminals to each other. The centers of the profile zones are defined by basic dimension "e".	This tolerance is normally compounded with tolerance zone defined by bbb.
eee	0.08	The unilateral tolerance located above the seating plane where in the bottom surface of all terminals must be located.	This tolerance is commonly known as the "coplanarity" of the package terminals.
fff	0.10	Thetolerance that controls the position of the exposed metal heat feature. The center of the tolerance zone will be datum's defined by the centerlines of the package body.	-
REF	-	-	No tolerance for A2

Figure 31. **TFQFPN32 suggested footprint (measured in mm)**



16 Packing information

16.1 TFQFPN32 packing information

16.1.1 TFQFPN32 packing method concept

Figure 32. **TFQFPN32 packing method concept**

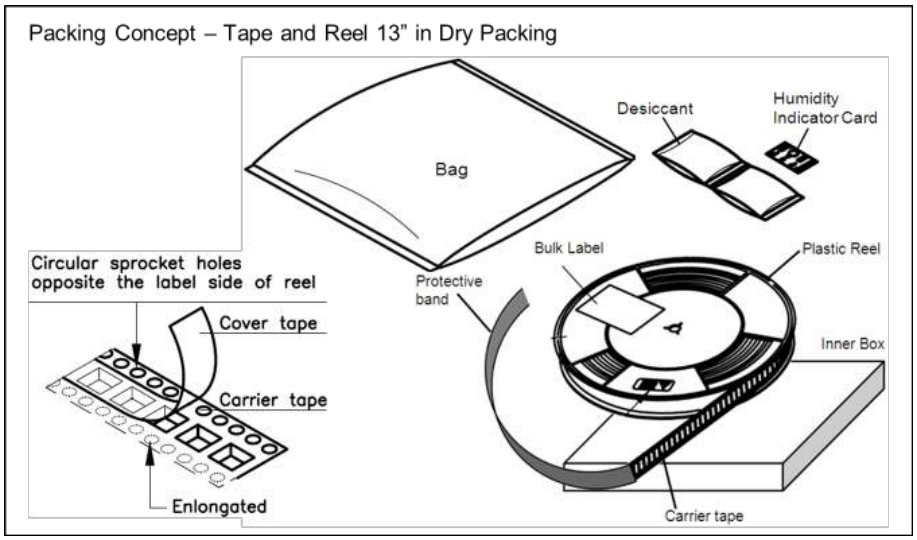


Figure 33. **TFQFPN32 carrier tape**

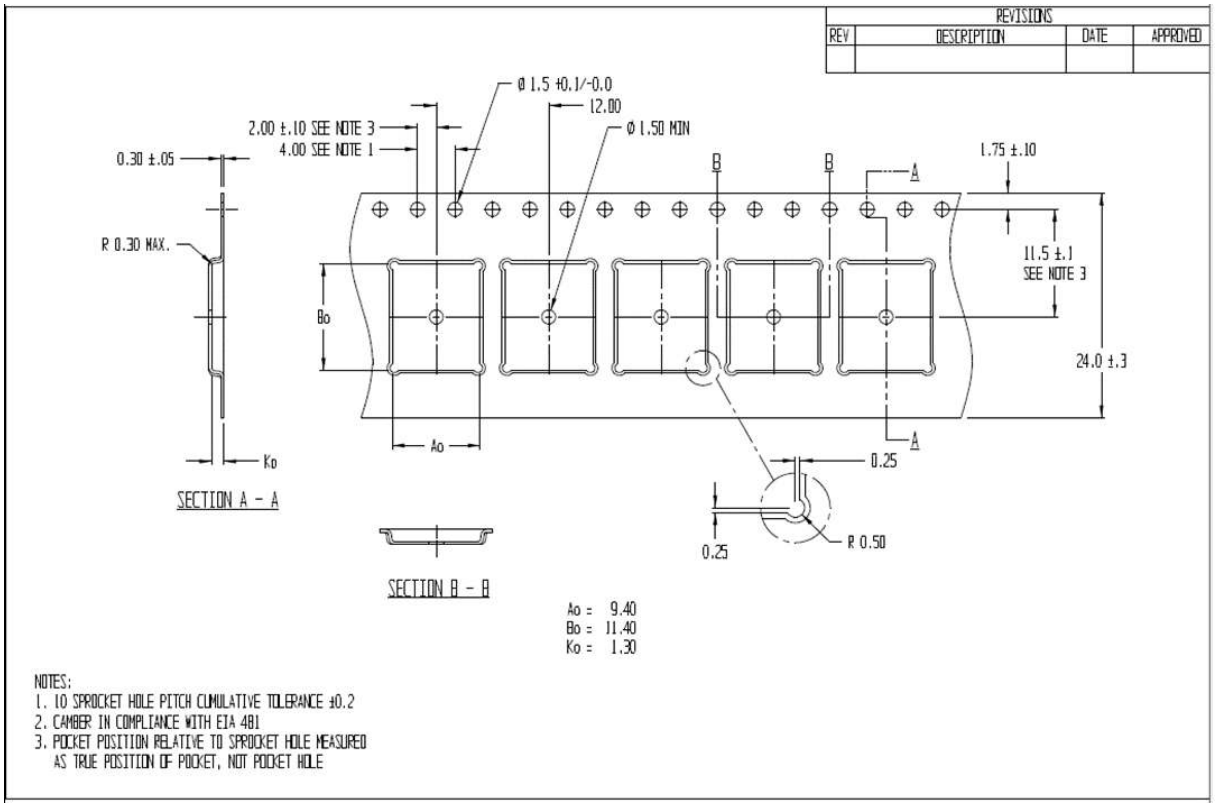
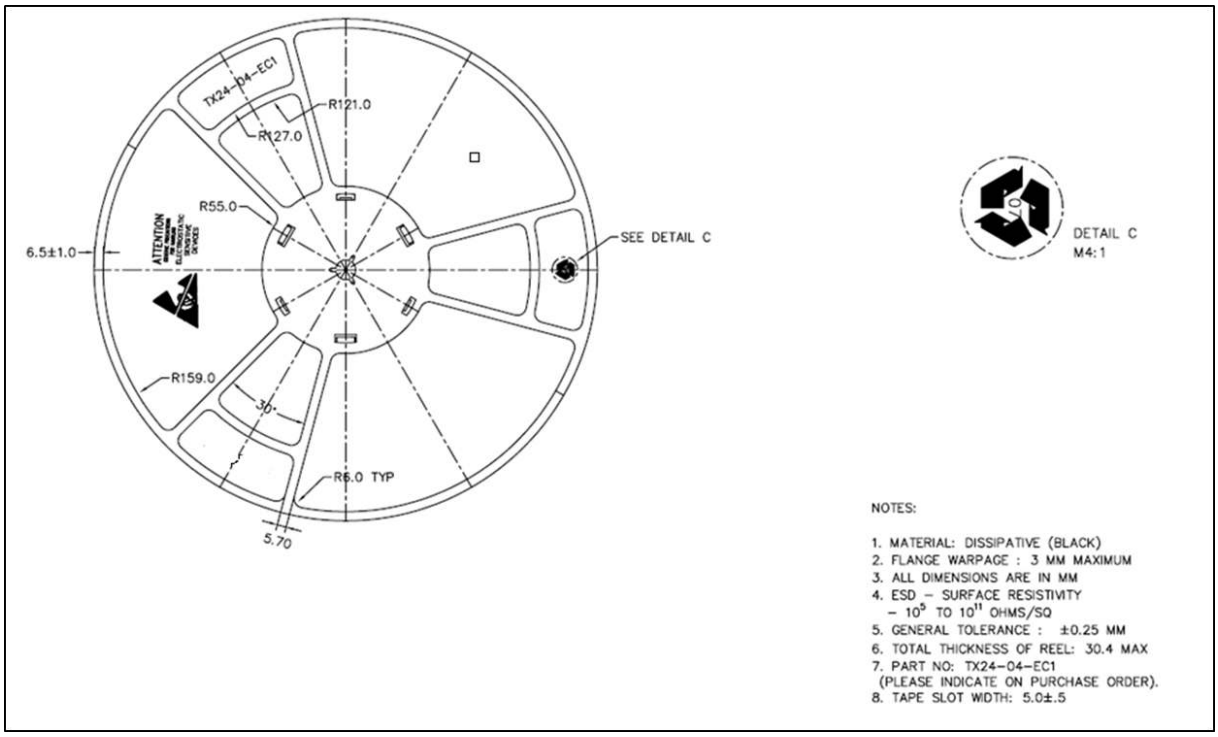


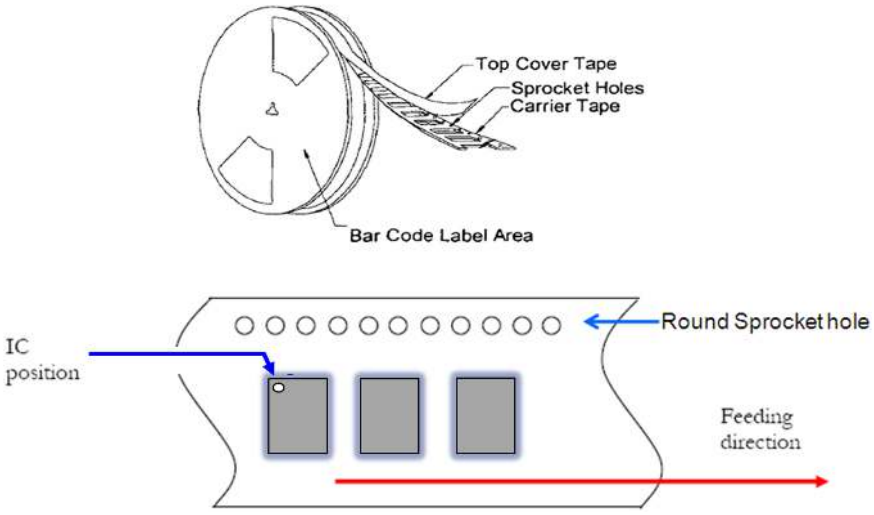
Figure 34. **TFQFPN32 reel**



Reel – 330 mm diameter x 101 mm hub x 24 mm width.

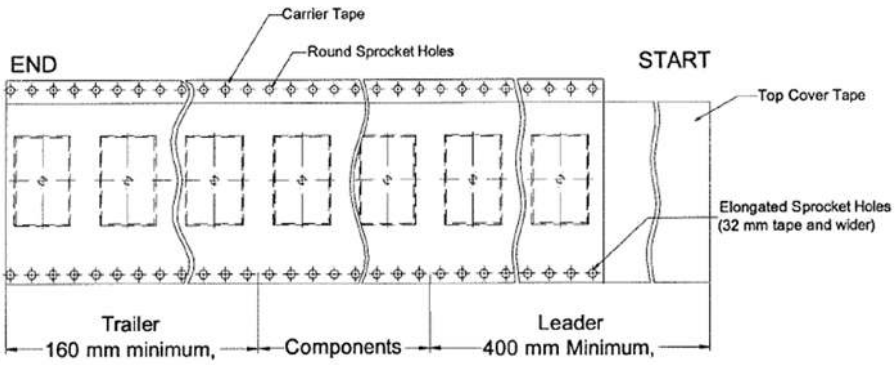
16.1.2 TFQFPN32 winding direction

Figure 35. **TFQFPN32 winding direction**



16.1.3 TFQFPN32 leader and trailer

Figure 36. **TFQFPN32 leader and trailer**



Note: Leader and trailer length as per EAI-481specification.

17 Ordering information

Table 19. **Ordering information**

Part number	Package	Packaging
ISO8200AQ	TFQFPN32	Tube
ISO8200AQTR	TFQFPN32	Tape and reel

Revision history

Table 20. **Document revision history**

Date	Version	Changes
31-Oct-2018	1	Initial release.
3-Dec-2018	2	Updated Figure 1 and Figure 28, amended Table 8
2-Jun-2019	3	Features updated. Table 1 & Table 2 modified. Figure replaced. Small changes to the text.
23-Apr-2020	4	Table 12 and 14 updated. Figure 29 replaced and Table 15 added.
11-Oct-2020	5	Throughout document: - Updated template, with minor content rearrangement and text edits In Section 6 Electrical characteristics: - added Table 13. Safety limits Updated Section 7.2 Serial data in (SDI)
17-Dec-2020	6	Updated Values in Table 7, 9, and 10
30-Jul-2021	7	Mentioned UL508 certification in the front page. Rephrased the logic and process stages synchronization in chapter Section 7.5.1 Watchdog. Rephrased chapter Section 14 Daisy chaining and added limitations on $t_{cycle(\overline{SS})}$.

Contents

1 **Description** 2
2 **Block diagram** 3
3 **Pin connection** 4
4 **Absolute maximum ratings** 6
5 **Thermal data** 7
6 **Electrical characteristics** 8
7 **Serial interface** 13
7.1 Functional description 13
7.2 Serial data in (SDI) 13
7.3 Serial data out (SDO) 13
7.4 Serial data clock (CLK) 13
7.5 Slave select ($\overline{SS}$) 14
7.5.1 Watchdog 15
7.5.2 Output enable (OUT_EN) 15
7.6 FAULT and PGOOD indications 16
7.7 Truth table 17
7.7.1 Junction overtemperature 18
8 **Power section** 19
8.1 Current limitation 19
8.2 Thermal protection 20
9 **Reverse polarity protection** 23
10 **Reverse polarity on VDD** 24
11 **Demagnetization energy** 25
12 **Conventions** 26
12.1 Supply voltage and power output conventions 26
13 **Thermal information** 27
13.1 Thermal impedance 27
14 **Daisy chaining** 28
15 **Package information** 29

15.1 TFQFPN32 package information 29
16 Packing information 33
16.1 TFQFPN32 packing information 33
16.1.1 TFQFPN32 packing method concept 33
16.1.2 TFQFPN32 winding direction 34
16.1.3 TFQFPN32 leader and trailer 35
17 Ordering information 36
Revision history 37

List of figures

Figure 1. Block diagram . . . 3
Figure 2. Pin connection (top through view) . . . 4
Figure 3. $R_{DS(on)}$ measurement . . . 9
Figure 4. dV/dT definition . . . 10
Figure 5. td(ON)-td(OFF) definition . . . 10
Figure 6. SPI mode diagram . . . 14
Figure 7. SPI input timing diagram . . . 14
Figure 8. SPI output timing diagram . . . 15
Figure 9. Watchdog behavior . . . 15
Figure 10. OUT_EN without effect on output . . . 16
Figure 11. OUT_EN effective on output channel . . . 16
Figure 12. Power GOOD pin behavior . . . 17
Figure 13. Thermal status update . . . 18
Figure 14. Switching on resistive load . . . 19
Figure 15. Switching on bulb lamp . . . 19
Figure 16. Switching on light inductive load . . . 19
Figure 17. Switching on heavy inductive load . . . 19
Figure 18. Short-circuit (with OVT) during ON state . . . 20
Figure 19. Switching on short-circuit (with OVT) . . . 20
Figure 20. Thermal protection flowchart . . . 21
Figure 21. Thermal protection and fault behavior (T_{JSD} triggered before T_{CSD}) . . . 21
Figure 22. Thermal protection and fault behavior (T_{CSD} triggered before T_{JSD}) . . . 22
Figure 23. Reverse polarity protection . . . 23
Figure 24. V_{DD} reverse polarity protection . . . 24
Figure 25. Single pulse demagnetization energy vs. load current (Typical values at T_{AMB} = 125°C) . . . 25
Figure 26. Supply voltage and power output conventions . . . 26
Figure 27. Simplified thermal model of the process stage . . . 27
Figure 28. Example of daisy chaining connection . . . 28
Figure 29. TFQFPN32 package outline . . . 29
Figure 30. TFQFPN32 package detail outline . . . 30
Figure 31. TFQFPN32 suggested footprint (measured in mm) . . . 32
Figure 32. TFQFPN32 packing method concept . . . 33
Figure 33. TFQFPN32 carrier tape . . . 33
Figure 34. TFQFPN32 reel . . . 34
Figure 35. TFQFPN32 winding direction . . . 34
Figure 36. TFQFPN32 leader and trailer . . . 35

List of tables

Table 1. Pin description . . . 4
Table 2. Absolute maximum ratings . . . 6
Table 3. Thermal data . . . 7
Table 4. Power section . . . 8
Table 5. Digital supply voltage . . . 8
Table 6. Diagnostic pin and output protection function . . . 8
Table 7. Power switching characteristics (V_{CC} = 24 V; -40°C < T_J < 125°C) . . . 9
Table 8. Logic inputs and output . . . 10
Table 9. Serial interface timings (V_{DD} = 5 V; V_{CC} = 24 V; -40°C < T_J < 125°C) . . . 11
Table 10. Internal communication timings (V_{DD} = 5 V; V_{CC} = 24 V; -40°C < T_J < 125°C) . . . 11
Table 11. Insulation and safety-related specifications . . . 11
Table 12. Insulation characteristics . . . 12
Table 13. Safety limits . . . 12
Table 14. SDI frame . . . 13
Table 15. SDO frame . . . 13
Table 16. Truth table . . . 17
Table 17. TFQFPN32 package mechanical data . . . 30
Table 18. Tolerance of form and position . . . 31
Table 19. Ordering information . . . 36
Table 20. Document revision history . . . 37