Using the LMG5200EVM-02 GaN Half-Bridge Power Stage EVM

User's Guide

Texas Instruments

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Contents

List of Figures

List of Tables

General TI High Voltage Evaluation User Safety Guidelines

WARNING

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed-circuit board assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments. If you are not suitably qualified, you should immediately stop from further use of the HV EVM.

- **Work Area Safety:**
  - Maintain a clean and orderly work area.
  - Qualified observer(s) must be present anytime circuits are energized.
  - Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
  - All interface circuits, power supplies, evaluation modules, instruments, meters, scopes, and other related apparatus used in a development environment exceeding 50 V_{RMS}/75 VDC must be electrically located within a protected Emergency Power Off (EPO) protected power strip.
  - Use a stable and non-conductive work surface.
  - Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
- **Electrical Safety:**

  As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
  - De-energize the TI HV EVM and all its inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
  - With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups, and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
  - When EVM readiness is complete, energize the EVM as intended.

  WARNING: While the EVM is energized, never touch the EVM or its electrical circuits as they could be at high voltages capable of causing electrical shock hazard.

- **Personal Safety:**
  - Wear personal protective equipment, for example, latex gloves and/or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.
- **Limitation for Safe Use:**
  - EVMs are not to be used as all or part of a production unit.

Safety and Precautions

The EVM is designed for professionals who have received the appropriate technical training, and is designed to operate from an AC power supply or a high-voltage DC supply. Please read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION

Do not leave the EVM powered when unattended.

WARNING

Hot surface! Contact may cause burns. Do not touch!

WARNING

High Voltage! Electric shock is possible when connecting board to live wire. Board should be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

Using the LMG5200EVM-02 GaN Half-Bridge Power Stage EVM

The LMG5200 device is an 80-V Gallium Nitride (GaN) half-bridge power module with an integrated driver. It provides an integrated power stage solution using enhancement-mode GaN FETs. The LMG5200 device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration. The guide shows a circuit and the list of materials describing how to power the board up and how to set the board up for a certain regulation voltage. The EVM board is designed to accelerate the evaluation of the LMG5200. This board is not intended to be used as a standalone product, but it intended to evaluate the switching performance of LMG5200.

1 Description

The LMG5200 evaluation module is a small, easy-to-use power stage with an external PWM signal. The board can be configured as a buck converter, boost converter, or other converter topology using a half bridge. Because this is an open-loop board with an external PWM signal, do not use it to evaluate transient response. It can be used to evaluate the performance of the LMG5200 as a hard-switched converter to sample measurements such as efficiency, switching speed and dv/dt. The EVM features a LMG5200 half-bridge power module with two 15-mΩ GaN FETs and a half-bridge driver. The module can deliver up to 10 A of current if the application includes adequate thermal management (monitor case temperature and ensure adequate airflow is present if required). The thermal management considerations include forced air, heat sink, and lower operating frequency to minimize the power dissipation in the module.

1.1 Featured Application

LMG5200EVM-02 features include:

- Input voltage operates up to 80 V DC
- Integrated 80-V, 15-mΩ GaN FETs with driver
- Single-input, onboard for PWM signal with 8-ns dead time
- Configurable onboard dead-time adjustment by simple resistance change
- Onboard LDO for generating 5-V VCC supply from a poorly regulated supply between 5.5 V and 10 V
- Kelvin sense capability for efficiency measurements for input and output voltage

CAUTION

High-voltage levels are present on the evaluation module whenever it is energized. Proper precautions must be taken when working with the EVM.

1.2 Typical Applications

The LMG5200 is suited for use in high-frequency DC-DC converters. It is simple to use and requires few external components.

- High-speed, synchronous buck converters
- Class D amplifiers for audio
- 48-V point-of-load converters for industrial, computing, and telecom

2 Schematic

Figure 1 shows the schematic of the EVM.

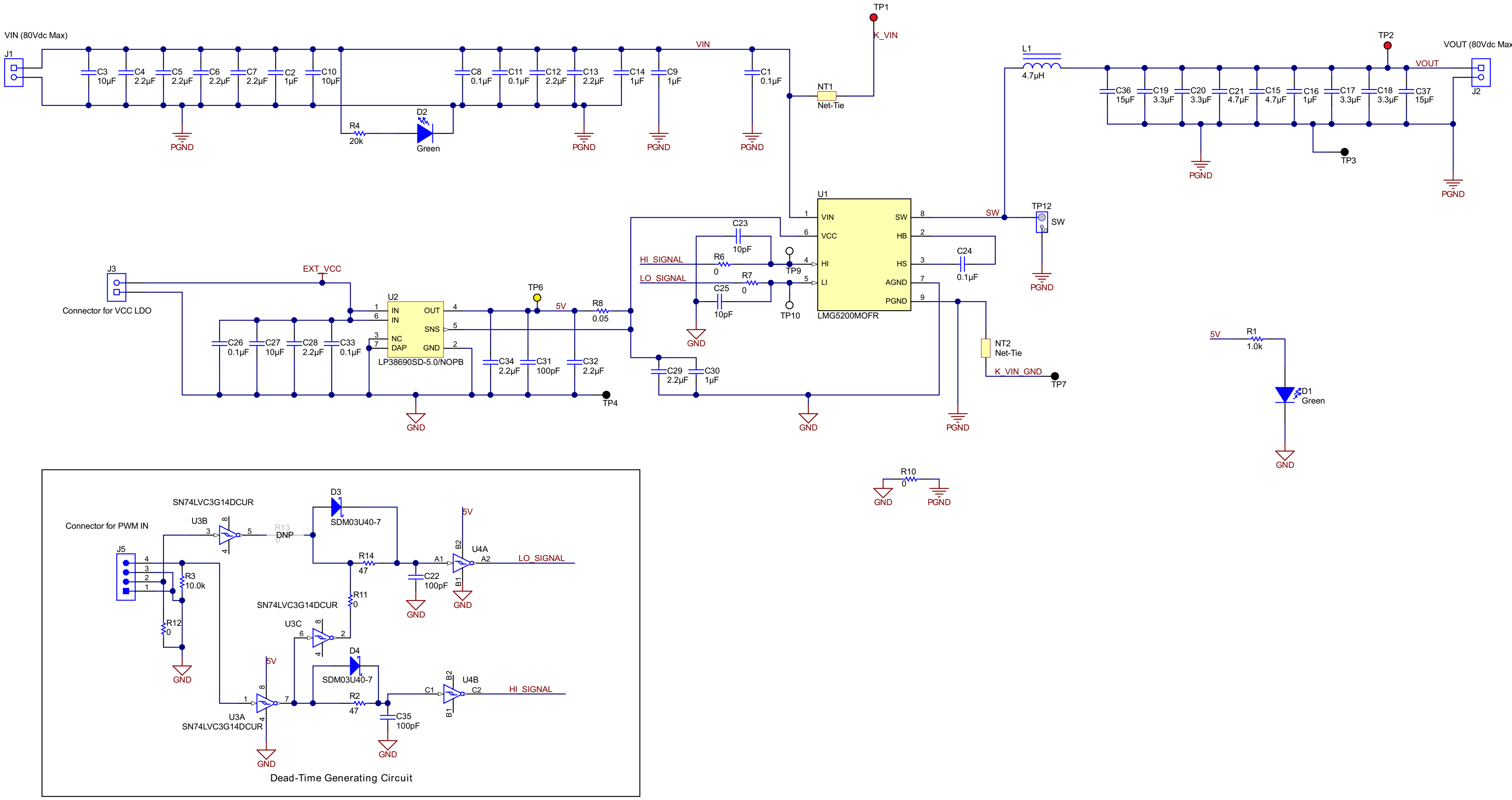

Figure 1. LMG5200EVM-02 Schematic

3 EVM Kit Contents

The kit contains the following:

- Safety instructions
- LMG5200EVM-02 Circuit Board

4 Electrical Performance Specifications

The inductor used in this EVM is a 4.7-µH inductor. The switching frequency is set by an external PWM signal (between 0 V and 5 V). The duty cycle of this PWM signal sets the duty cycle of the half-bridge module.

4.1 Test Setup

This section describes the EVM hardware and outlines the procedure to set it up for evaluation. Figure 2 and Figure 3 show the top and bottom views of the LMG5200EVM-02, respectively.

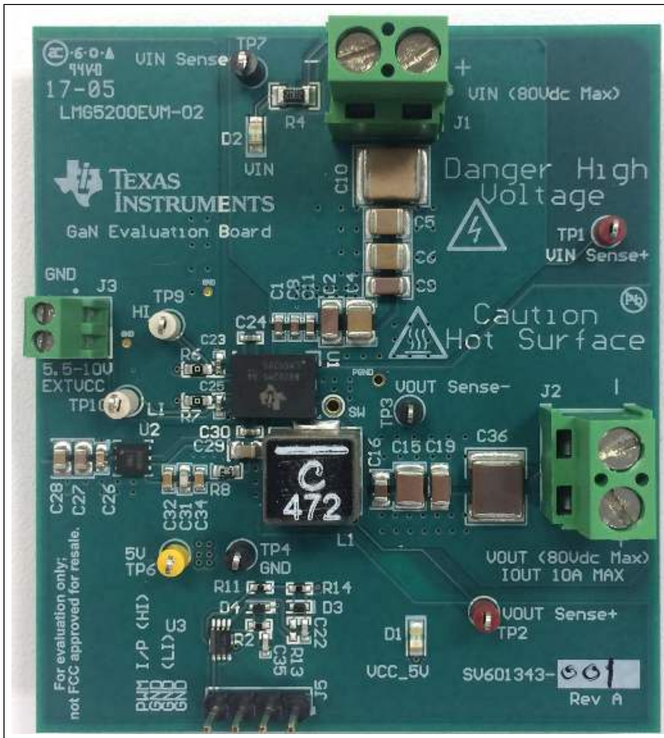

Figure 2. LMG5200EVM-02 Board Top View

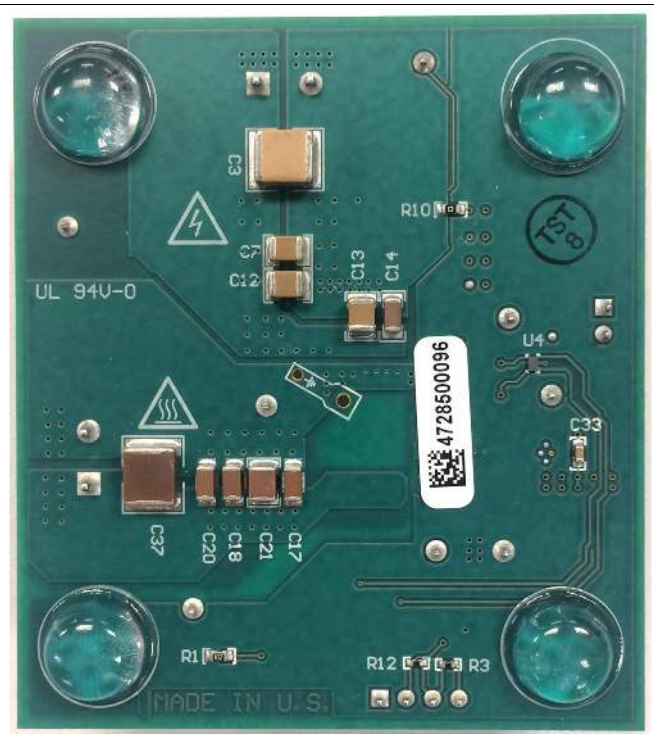

Figure 3. LMG5200EVM-02 Board Bottom View

WARNING

High voltages that may cause injury exist on this evaluation module (EVM). Please ensure all safety procedures are followed when working on this EVM. Never leave a powered EVM unattended.

4.1.1 List of Test Points

Table 1. Test Point Functional Description

TEST POINT	NAME	DESCRIPTION
TP1	TP1	Sense connection for the input supply
TP2	TP2	Sense connection for output voltage
TP3	TP3	Sense connection for output ground
TP4	TP4	Analog Ground sense connection
TP6	TP6	5-V sense connection for LDO output
TP7	TP7	Sense connection for the input supply ground
TP9	TP9	HI input to LMG5200
TP10	TP10	LI input to LMG5200
TP12	TP12	SW node, designed for use with oscilloscope probe and spring-type ground connection for better measurements
J1	J1	VIN power connector (80-V DC maximum)
J2	J2	VOUT power connector (80-V DC maximum)
J3	J3	EXTVCC connection (5.5 V – 10 V)

4.1.2 Key Connections

The following test procedure is recommended primarily for powering up and shutting down the evaluation module. Never leave a powered EVM unattended for any length of time. Also, the unit should never be handled while power is applied to it.

WARNING

There are high voltages present on the EVM. Some components reach temperatures above 50°C. Precautions must be taken when handling the board.

4.1.2.1 Connect a Supply to J3 Connector

There is the bias supply EXTVCC (between 5.5 V and 10 V) for the LMG5200 driver. This driver supply is regulated to 5 V by the series LDO U2 (LP3869). This regulation ensures that the bias supply for the LMG5200 is accurate and is not exceeded beyond the gate voltage specifications. This user's guide refers to this supply as the driver bias supply.

4.1.2.2 PWM Input

Provide the PWM input using a function generator that is capable of providing the desired switching frequency and duty cycle. This function generator output should be connected to the J5 connector as shown in the Figure 4. The left-most pin in this view is the positive input of the PWM supply and the remaining three pins are connected to GND in the default assembly for the board.

Alternatively, two separate PWM inputs may be applied to control HI and LI independently. To apply this type of control, R11 must be removed, R13 must be populated with a 0-Ω resistor, and R12 should be replaced with a 10-kΩ resistor. On a board with these modifications, the HI signal should be applied at pin 4 of J5, and the LI signal at pin 2 of J5. Note that with this control scheme, the EVM will no longer generate a dead time separating HI and LI transitions. Therefore, careful consideration must be applied to the control signals in this mode of operation in order to prevent a shoot-through condition.

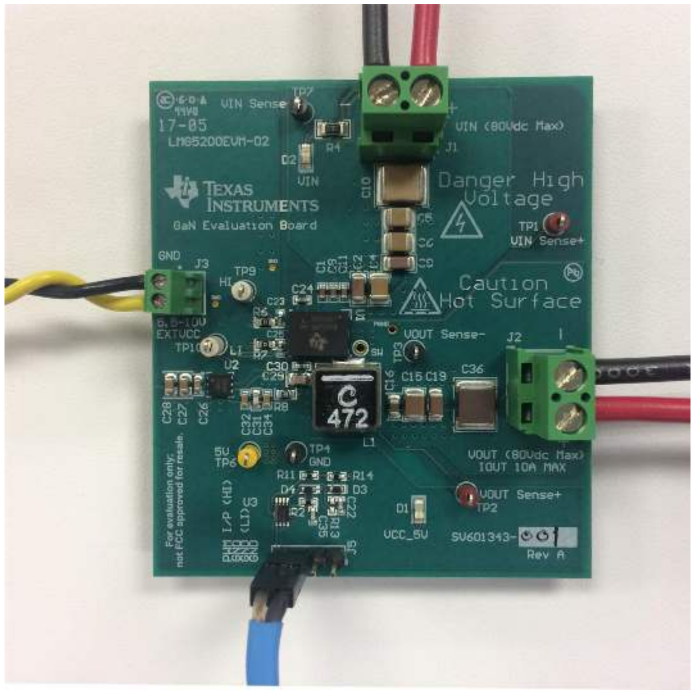

Figure 4. PWM Connection on J5

4.1.2.3 J1 Connector

Connect the input voltage to the J1 connector ensure that the positive and negative supply is connected appropriately - the positive and negative terminals are marked on the board. The sense connection for the input supply is through the TP1 and TP7 test points, respectively. This is useful when doing efficiency calculations as this will ensure that the resistive losses to the board are taken into account and the losses calculated are related to the board and the LMG5200 half bridge.

The output load is connected to the J2 connector. The positive and negative sense signals are TP2 and TP3, respectively.

4.1.3 Power-Up Procedure

4.1.3.1 Step 1: Driver Bias Supply

Power up the driver bias supply (5.5 V to 10 V) first. The D1 diode lights up after the driver bias supply comes up. After this step, observe the PWM signals on test points TP9 and TP10. Ensure that the PWM signal for the high and low side are of the desired frequency (100 kHz to 5 MHz depending on the input voltage and load). Also observe the default dead time between the high-to-low and low-to-high PWM transitions.

4.1.3.2 Step 2: Input Supply

Power up the input supply (10 V to 80 V). The D2 diode lights up after the input supply is powered up.

Observe the output voltage on the sense signals (TP2, TP3). Adjust the PWM duty cycle such that the output is of the desired voltage. Load the output with an appropriate electronic load.

NOTE: The PWM duty cycle must be adjusted to compensate for the losses when the supply is loaded

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4.1.3.3 Step 3

To observe the SW node connect a probe with a small pigtail to the via next to the SW pin, as shown in Figure 5. This ensures that the measurement loop is small and hence accurately reflects the behavior of the SW node. If a large loop is used, due to the high dv/dt on the SW node and the parasitic impedance (inductance) of the loop, a large amount of ringing will be observed on the SW node measurements. This ringing is not representative of the device performance, but is rather a measurement artifact. The probe connection should be made prior to the board being powered up and one should ensure that appropriate safety precautions are taken.

Connect the scope probe to measure the SW node as shown in Figure 5. Notice the small pigtail used to minimize the ground loop.

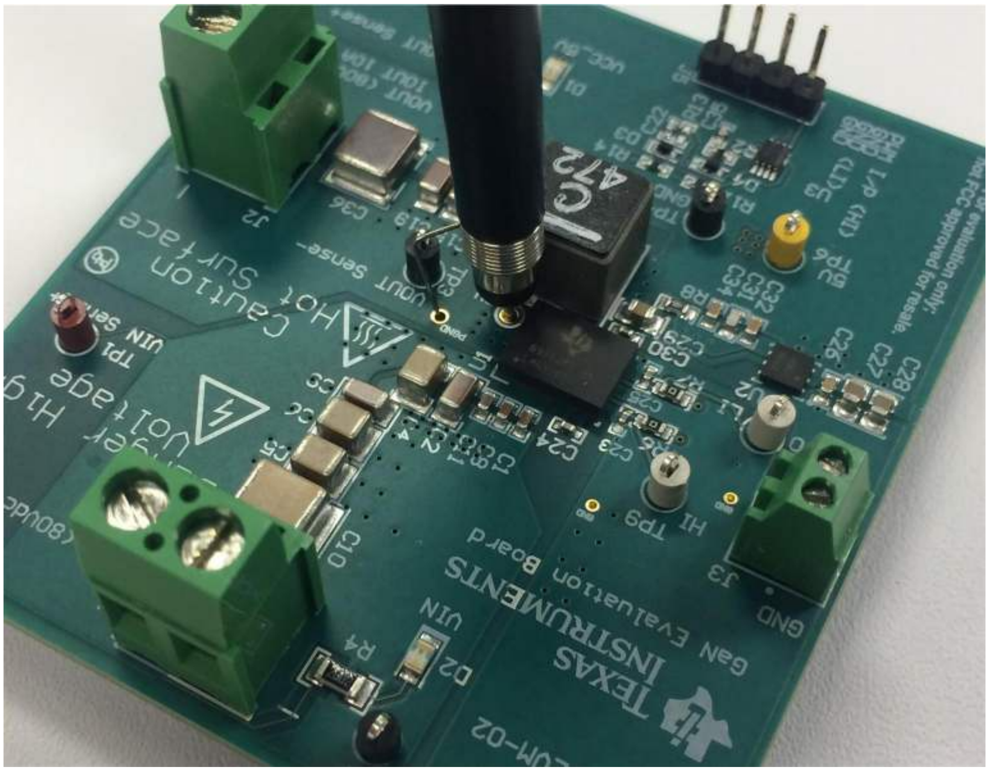

Figure 5. Measuring the SW Node

4.1.3.4 Setting Dead-Time

Dead times are set by the RC delays between the inverted and noninverted PWM input connected to jumper J3. The dead time typically does not require to be changed, however to evaluate impact of dead time on efficiency, you can vary the RC delay, its easy to change resistors R14 and R2 to get the appropriate dead time. Ensure that the dead time is not reduced so much that it causes a shoot-through condition.

4.1.4 Power-Down Procedure

To power down the board the power up procedures should be followed in reverse. Hence the load should be turned off first. Next the input supply should be turned off. Followed by the PWM signal and finally the driver bias supply.

4.2 Results

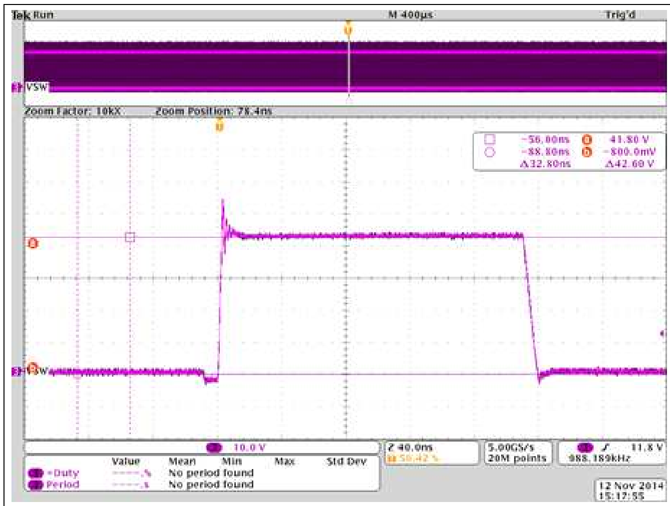

Figure 6. SW Node Behavior Showing the Dead Time and the Overshoot in the SW Node

Figure 7. Zoom in of the SW Node Showing the Dead Time of 7.7 ns (Converter Loaded With 2 A)

NOTE: Visit the E2E forum Gallium Nitride Solutions for more information regarding LMG5200 or LMG5200 hard-switched EVM.

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5 List of Materials

Table 2. LMG5200EVM-02 List of Materials(1)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
PCB1	1		Printed-Circuit Board		SV601343	Any
C1, C8, C11	3	0.1uF	CAP, CERM, 0.1uF, 100V, +/-10%, X7R, 0603	0603	GRM188R72A104KA35D	MuRata
C2, C9, C14	3	1uF	CAP, CERM, 1uF, 100V, +/-20%, X7R, 1206	1206	C3216X7R2A105M160AA	TDK
C3, C10	2	10uF	CAP, CERM, 10 µF, 100 V, +/- 20%, X7R, 2220	2220	22201C106MAT2A	AVX
C4, C5, C6, C7, C12, C13	6	2.2uF	CAP, CERM, 2.2 µF, 100 V, +/- 10%, X7R, 1210	1210	GRM32ER72A225KA35L	MuRata
C15, C21	2	4.7uF	CAP, CERM, 4.7 µF, 100 V, +/- 10%, X7S, 1210	1210	C3225X7S2A475K200AE	TDK
C16	1	1uF	CAP, CERM, 1 µF, 100 V, +/- 10%, X7S, 0805	0805	C2012X7S2A105K125AB	TDK
C17, C18, C19, C20	4	3.3uF	CAP, CERM, 3.3 µF, 100 V, +/- 20%, X7S, 1206_190	1206_190	C3216X7S2A335M160AB	TDK
C22, C35	2	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0402	0402	CC0402JRNPO9BN101	Yageo America
C23, C25	2	10pF	CAP, CERM, 10pF, 50V, +/-5%, C0G/NP0, 0402	0402	GRM1555C1H100JA01D	MuRata
C24	1	0.1uF	CAP, CERM, 0.1 µF, 10 V, +/- 10%, X5R, 0402	0402	C1005X5R1A104K050BA	TDK
C26, C33	2	0.1uF	CAP, CERM, 0.1 µF, 16 V, +/- 5%, X7R, 0603	0603	0603YC104JAT2A	AVX
C27	1	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 0805	0805	C2012X5R1E106K125AB	TDK
C28, C29	2	2.2uF	CAP, CERM, 2.2uF, 16V, +/-10%, X7R, 0805	0805	C0805C225K4RACTU	Kemet
C30	1	1uF	CAP, CERM, 1uF, 25V, +/-10%, X5R, 0402	0402	C1005X5R1E105K050BC	TDK
C31	1	100pF	CAP, CERM, 100pF, 25V, +/-10%, X7R, 0603	0603	06033C101KAT2A	AVX
C32, C34	2	2.2uF	CAP, CERM, 2.2uF, 10V, +/-10%, X7R, 0603	0603	GRM188R71A225KE15D	MuRata
C36, C37	2	15uF	CAP, CERM, 15 µF, 100 V, +/- 20%, X7S, 2220	2220	C5750X7S2A156M250KB	TDK
D1, D2	2	Green	LED, Green, SMD	LED_0805	LTST-C170KGKT	Lite-On
D3, D4	2	40V	Diode, Schottky, 40V, 0.03A, SOD-523	SOD-523	SDM03U40-7	Diodes Inc.
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2	2		Terminal Block, 2x1, 5.08mm, TH	10.16x15.2x9mm	282841-2	TE Connectivity
J3	1		Terminal Block, 2x1, 2.54mm, TH	Terminal Block, 2x1, 2.54mm, TH	282834-2	TE Connectivity
J5	1		Header, 100mil, 4x1, Tin, TH	Header, 4x1, 100mil, TH	5-146278-4	TE Connectivity
L1	1	4.7uH	Inductor, Shielded, Composite, 4.7 µH, 10.5 A, 0.00889 ohm, SMD	8.1 x 8 x 8.6mm	XAL8080-472ME	Coilcraft

(1) Unless otherwise noted, all parts may be substituted with equivalents.

Table 2. LMG5200EVM-02 List of Materials[1] (continued)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R1	1	1.0k	RES, 1.0k ohm, 5%, 0.1W, 0603	0603	CRCW06031K00JNEA	Vishay-Dale
R2, R14	2	47	RES, 47 ohm, 5%, 0.063W, 0402	0402	CRCW040247R0JNED	Vishay-Dale
R3	1	10.0k	RES, 10.0k ohm, 1%, 0.063W, 0402	0402	CRCW040210K0FKED	Vishay-Dale
R4	1	20k	RES, 20k ohm, 5%, 0.25W, 1206	1206	CRCW120620K0JNEA	Vishay-Dale
R6, R7, R10	3	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R8	1	0.05	RES, 0.05 ohm, 1%, 0.1W, 0603	0603	ERJ-L03KF50MV	Panasonic
R11, R12	2	0	RES, 0 ohm, 5%, 0.063W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale
TP1, TP2	2	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP3, TP4, TP7	3	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP6	1		Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
TP9, TP10	2		Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
U1	1		80V, 10A GaN Half-Bridge Power Stage, MOF0009A (QFM-9)	MOF0009A	LMG5200MOFR	Texas Instruments[2]
U2	1		1A Low Dropout CMOS Linear Regulators Stable with Ceramic Output Capacitors, 6-pin LLP, Pb-Free	SDE06A	LP38690SD-5.0/NOPB	Texas Instruments[2]
U3	1		Triple Schmitt-Trigger Inverter, DCU0008A	DCU0008A	SN74LVC3G14DCUR	Texas Instruments[2]
U4	1		Dual Schmitt-Trigger Inverter, YZP0006ADBD (DSBGA-6)	YZP0006ADBD	SN74LVC2G14YZPR	Texas Instruments[2]
R13	0	0	RES, 0 ohm, 5%, 0.063W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale

(2) No alternate component manufacturer.

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