

# NCV7684

## 12 Channels 60 mA LED Linear Current Driver I<sup>2</sup>C Controllable for Automotive Applications

The NCV7684 consists of twelve linear programmable constant current sources. The part is designed for use in the regulation and control of LED for automotive applications. The NCV7684 allows 128 different current levels adjustable with pulse width modulation (PWM) programmable via I<sup>2</sup>C serial interface. The device can be used with micro-controller applications using the I<sup>2</sup>C bus or in stand-alone applications where a choice could be done in between 2 different configuration settings. The IC also provides 3.3 V voltage reference to the application for loads up to 1 mA.

LED brightness level is easily programmed using an external resistor. Each channel has an internal circuitry to detect open-load conditions with an optional auto-recovery mode. If one driver is in open-load condition, all other channels could be turned off according to the programmable bit setting.

The device is available in small body size SSOP24-EP package.

### Features

- 12 programmable Current Sources Up to 60 mA
- Common PWM Gain Control via I<sup>2</sup>C
- On-chip 125, 250, or 500 Hz PWM
- Open LED String Diagnostic
- Low Dropout Operation for Pre-Regulator Applications
- Single Resistor for Current Set Point
- Voltage Reference 3.3 V / 1 mA
- 8 bits I<sup>2</sup>C Interface with CRC8 Error Detection
- OTP Bank for Stand-Alone Operation (2 Configurations)
- Detection and Protection Against Open Load and Under-Voltage
- Over Temperature Detection and Protection
- Low Emission with Spread Spectrum Oscillator
- AEC Q100 Qualified
- SSOP24-EP Packaging
- This is a Pb-Free Device

### Applications

- Dashboard Applications
- Rear Combination Lamps (RCL)
- Daytime Running Lights (DRL)
- Fog Lights
- Center High Mounted Stop Lamps (CHMSL) Arrays
- Turn Signal and other Externally Modulated Applications



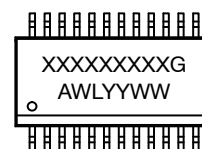
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SSOP24 NB EP  
CASE 940AP

### MARKING DIAGRAM



XXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping†
NCV7684DQR2G	SSOP24-EP (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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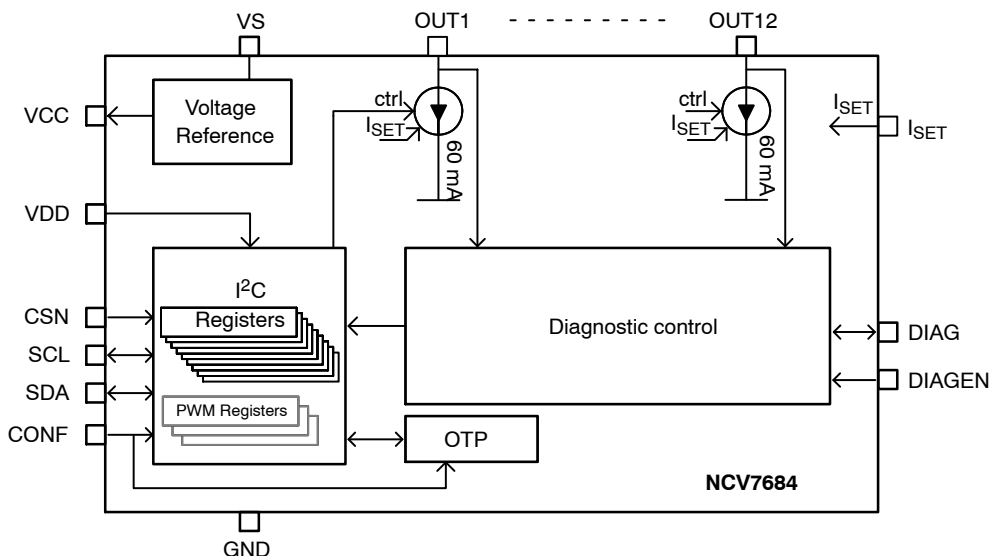


Figure 1. Block Diagram

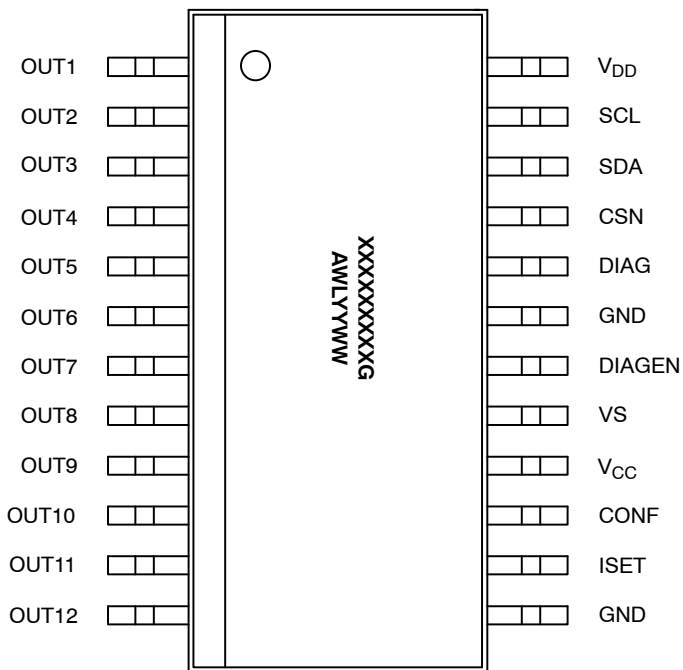


Figure 2. Pinout Diagram

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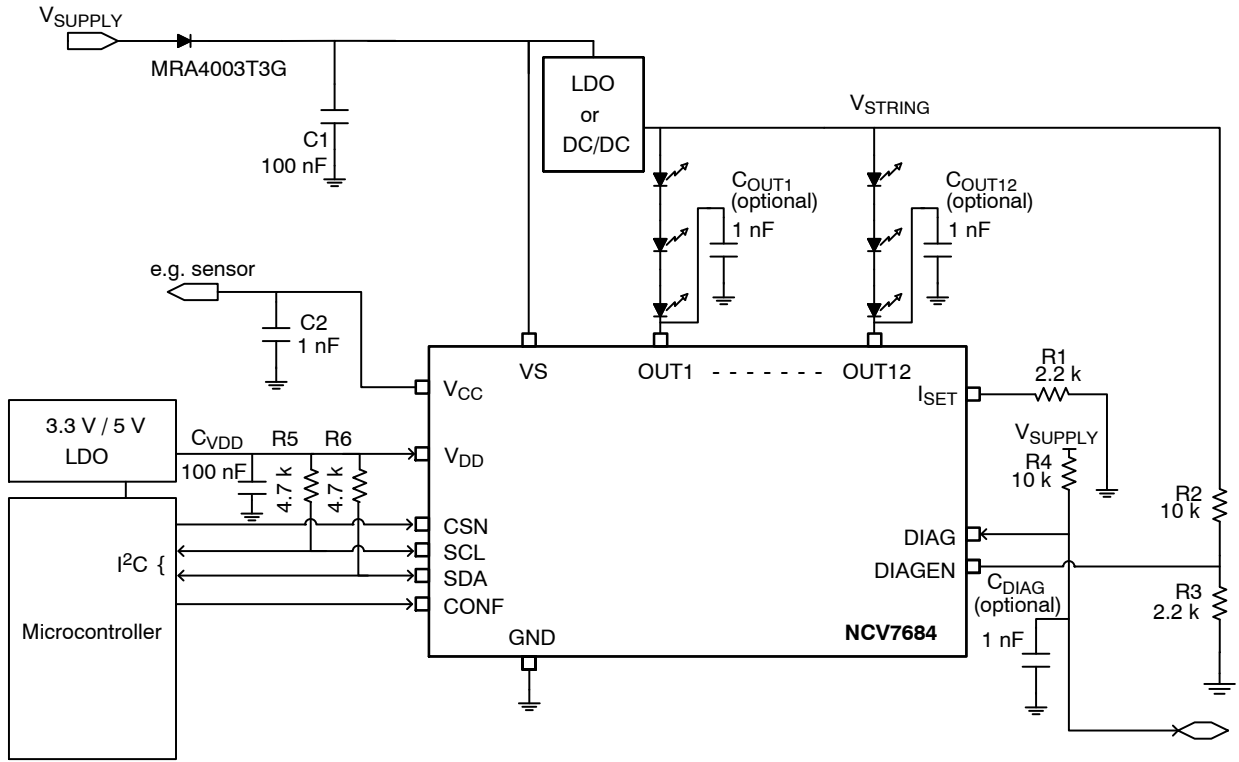


Figure 3. Application Diagram with Micro-controller (I<sup>2</sup>C Mode)

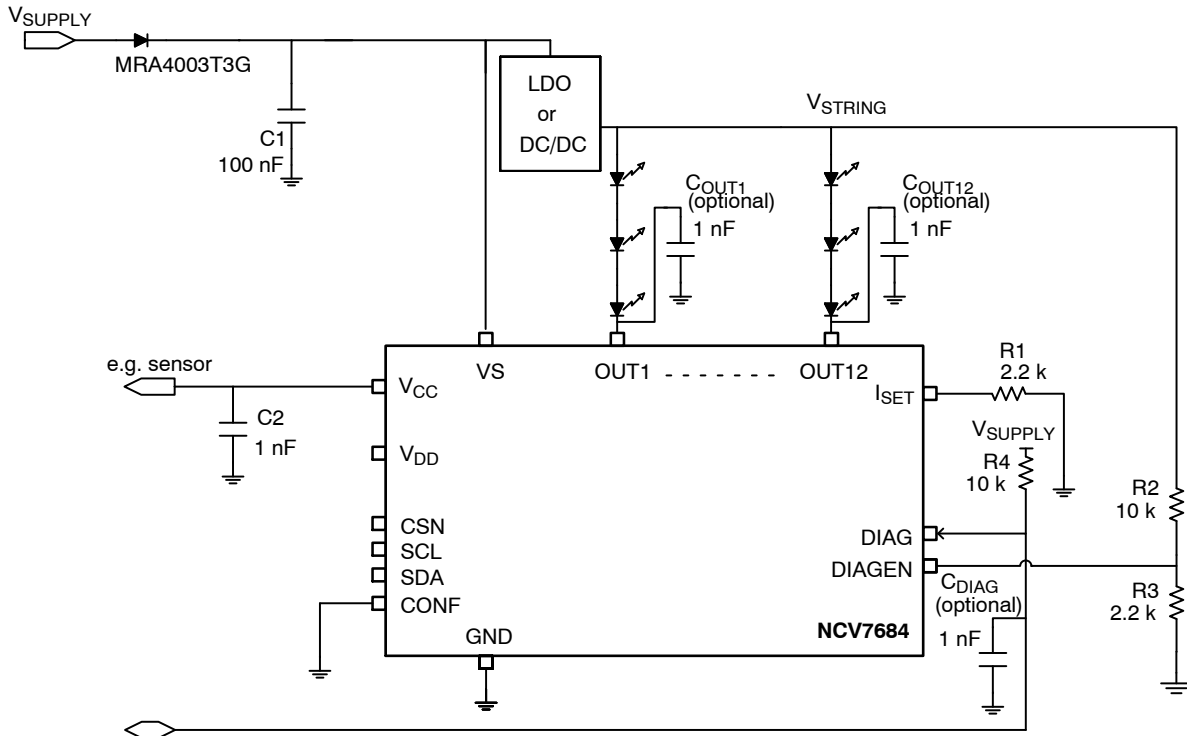


Figure 4. Application Diagram without Micro-controller (Stand Alone Mode)

Pin Function Description

Table 1. PIN FUNCTION DESCRIPTION

Pin #	Label	Description
1	OUT1	Channel 1 Current Output to LED
2	OUT2	Channel 2 Current Output to LED
3	OUT3	Channel 3 Current Output to LED
4	OUT4	Channel 4 Current Output to LED
5	OUT5	Channel 5 Current Output to LED
6	OUT6	Channel 6 Current Output to LED
7	OUT7	Channel 7 Current Output to LED
8	OUT8	Channel 8 Current Output to LED
9	OUT9	Channel 9 Current Output to LED
10	OUT10	Channel 10 Current Output to LED
11	OUT11	Channel 11 Current Output to LED
12	OUT12	Channel 12 Current Output to LED
13	GND	Ground
14	ISET	Current Setting
15	CONF	Stand Alone Mode Selection Bank
16	V <sub>CC</sub>	3.3 V Voltage Reference Output (Needs External Decoupling Capacitor)
17	VS	Supply Voltage Input
18	DIAGEN	Diagnostic Voltage Sensing Node for V <sub>STRING</sub> Via Resistor Divider
19	GND	Ground
20	DIAG	Open-drain diagnostic input/output. Reporting Open Circuit and thermal shutdown. Normal Operation = HIGH
21	CSN	End of Line Chip Select
22	SDA	I <sup>2</sup> C Serial Data
23	SCL	I <sup>2</sup> C Serial Clock
24	V <sub>DD</sub>	Digital Supply Voltage Input
epad	epad	True Ground Do NOT Connect to PCB Traces other than GND

Maximum Ratings

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V <sub>MAX_VS</sub>	Power supply voltage: Continuous supply voltage Transient Voltage (t < 500 ms, "load dump")	-0.3	28	V
		-0.3	40	V
V <sub>MAX_INx</sub>	Input pin voltage (DIAGEN, DIAG, CONF, CSN)	-0.3	40	V
V <sub>MAX_OUTx</sub>	Continuous Output Pin voltage Transient Voltage (t < 500 ms, "load dump")	-0.3	28	V
		-0.3	40	V
V <sub>MAX_VCC</sub>	Stabilized output voltage (V <sub>CC</sub> )	-0.3	3.6	V
V <sub>MAX_VDD</sub>	Digital input supply voltage (V <sub>DD</sub> )	-0.3	5.5	V
V <sub>MAX_IO</sub>	DC voltage at pins (V <sub>DD</sub> , SCL, SDA)	-0.3	5.5	V
V <sub>MAX_ISET</sub>	DC voltage at pin ISET	-0.3	3.6	V
I <sub>MAX_GND</sub>	Maximum Ground Current	-	750	mA
T <sub>JMAX</sub>	Junction Temperature, T <sub>J</sub>	-40	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.

ESD Protection and Packaging

Table 3. EDS PROTECTION (Note 1)

Parameter	Value	Unit
ESD Voltage, HBM (Human Body Model); (100 $\mu$ F, 1500 $\Omega$ ) All Pins Output Pins OUTx to GND	$\pm 2$ $\pm 4$	kV
ESD According to CDM (Charge Device Model) All Pins Corner Pins	$\pm 500$ $\pm 750$	V
ESD According to MM (Machine Model) All Pins	$\pm 150$	V
Moisture Sensitivity (SSOP24-EP)	MSL3	
Package Thermal Resistance Junction to Ambient (SSOP24-EP)	37	$^{\circ}$ C/W

1. This device series incorporates ESD protection and is tested by the following methods:  
 ESD HBM tested per AEC-Q100-002 (EIA/JESD22-A114)  
 ESD CDM tested per EIA/JES D22/C101, Field Induced Charge Model  
 MM according to AEC-Q100

Table 4. ELECTRICAL CHARACTERISTICS

(5 V < VS < 18 V, 3.15 V < V<sub>DD</sub> < 5.5 V, R1 = 1.82 k $\Omega$ , -40 $^{\circ}$ C  $\leq$  T<sub>J</sub>  $\leq$  150 $^{\circ}$ C, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
<b>GENERAL</b>						
Supply Voltage	VS_EXT	Functional extended range (limited temperature)	5	-	28	V
	VS_OP	Parametric operation	5	-	18	V
Supply Under-Voltage	VSUV	VS rising	3.8	4.1	4.4	V
Supply Under-Voltage Hysteresis	VSUV <sub>HYS</sub>	-	-	200	-	mV
Supply Current (Vs)	I <sub>S</sub> (error mode)	All OUTx OFF except channel in open load, VS = 12 V V <sub>DD</sub> = 0 V				
		I <sub>OUT_VCC</sub> = 0 mA	-	1.2	1.5	mA
		I <sub>OUT_VCC</sub> = 1 mA	-	2.2	2.5	mA
	I <sub>S</sub> (active)	Active Mode, V <sub>CC</sub> unloaded, VS = 16 V, R1 = 2 k $\Omega$	-	7	10	mA
Digital Supply Current	I <sub>DD</sub>	I <sup>2</sup> C mode, V <sub>DD</sub> = 5 V, VS = 16 V		1.5	2.0	mA
V <sub>DD</sub> Under Voltage Detection	V <sub>DDUV_R</sub>	V <sub>DD</sub> rising			2.9	V
	V <sub>DDUV_F</sub>	V <sub>DD</sub> falling	2			V

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**Table 4. ELECTRICAL CHARACTERISTICS** (continued)

(5 V < VS < 18 V, 3.15 V < VDD < 5.5 V, R1 = 1.82 kΩ, -40°C ≤ TJ ≤ 150°C, unless otherwise specified)

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
<b>CURRENT SOURCE OUTPUTS</b>						
Output Current	I <sub>OUTHOT</sub>	OUTx = 1 V, TJ = 150°C	50	55	60	mA
	I <sub>OUTCOLD</sub>	OUTx = 0.5 V, TJ = -40°C	50	55	60	mA
Current Matching from Channel to Channel	I <sub>MATCHCOLD</sub>	TJ = -40°C (Note 1)	-7	0	7	%
	I <sub>MATCH</sub>	TJ = 25°C (Note 1)	-6	0	6	%
	I <sub>MATCHHOT</sub>	TJ = 150°C (Note 1)	-5	0	5	%
Current Slew Rate	ISR <sub>x</sub>	10% to 90%	-	30	-	mA/μs
Open Circuit Detection Threshold	OLDT	I <sub>OUTx</sub> > 20 mA	30	50	70	% of output current
Open Load Recovery in Auto-recovery Mode	OLR	-	5	10	15	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Matching formulas:

$$\left[ \frac{2I_{OUTx(min)}}{I_{OUTx(min)} + I_{OUTx(max)}} - 1 \right] \times 100 \text{ and } \left[ \frac{2I_{OUTx(max)}}{I_{OUTx(min)} + I_{OUTx(max)}} - 1 \right] \times 100 \quad (\text{eq. 1})$$

**Table 5. ELECTRICAL CHARACTERISTICS**

(5 V < VS < 18 V, 3.15 V < VDD < 5.5 V, R1 = 1.82 kΩ, -40°C ≤ TJ ≤ 150°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>VOLTAGE REFERENCE</b>						
V <sub>VCC</sub>	Output Voltage Tolerance	I <sub>VCC</sub> ≤ 1 mA	3.20	3.30	3.45	V
I <sub>OUT_VCC</sub>	Output Current	-	-	-	-1	mA
C <sub>LOAD_VCC</sub>	Load Capacitor	ESR < 200 mΩ	0.9	1.0	2.5	nF
<b>INPUTS: CSN, CONF</b>						
V <sub>INL</sub>	Input Low Level	-	0.7	1.0	-	V
V <sub>INH</sub>	Input High Level	-	-	1.25	1.66	V
V <sub>IN_HYST</sub>	Input Hysteresis	-	100	250	400	mV
R <sub>IN_PD</sub>	Input Pull-down Resistor	0 V < V <sub>IN</sub> < 0.8 V	120	200	280	kΩ
<b>INPUTS: SCL, SDA</b>						
V <sub>INL</sub>	Input Low Level	-	-	-	0.3 × V <sub>DD</sub>	V
V <sub>INH</sub>	Input High Level	-	0.7 × V <sub>DD</sub>	-	-	V
V <sub>IN_HYST</sub>	Input Hysteresis	-	0.05 × V <sub>DD</sub>	-	-	V
I <sub>OUT_SDA</sub>	Output Current	V (SDA) = 0.4 V	3	-	-	mA
<b>DIAGEN PIN</b>						
V <sub>DIAGENTH</sub>	VS Diagnostic Enable Threshold	-	1.9	2.0	2.1	V
R <sub>DIAGEN_PD</sub>	Input Pull-down Resistor	0 V < V <sub>DIAG</sub> < 0.9 V	120	200	280	kΩ
<b>DIAG PIN</b>						
V <sub>OUTL</sub>	Output Low Level	Diagnostic Activated, I <sub>DIAG</sub> = 1 mA	-	0.2	0.4	V
DiagRes	Diagnostic Reset Voltage	-	1.65	1.80	1.95	V
tp <sub>DIAG</sub>	Filter Time to Set the DIAG Fail Pin in Failure Mode	I <sub>DIAG</sub> = 1 mA	-	10	20	μs
DIAG <sub>leak</sub>	DIAG Output Leakage	V <sub>DIAG</sub> = 5 V	-	-	10	μA

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**Table 5. ELECTRICAL CHARACTERISTICS** (continued)

( $5\text{ V} < V_S < 18\text{ V}$ ,  $3.15\text{ V} < V_{DD} < 5.5\text{ V}$ ,  $R_1 = 1.82\text{ k}\Omega$ ,  $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>ISET INPUT PIN</b>						
VISET	Global Current Setting	–	0.94	1.00	1.06	V
K	IOOUT ISET Factor	–	–	100	–	–
tsetupISET	Setup-up Time to 90% of the ISET Regulated Value	$V_S > 5\text{ V}$	–	–	50	$\mu\text{s}$
<b>INTERNAL PWM CONTROL UNIT (OUT1 – OUT12)</b>						
PWM1	PWM1 Frequency, I <sup>2</sup> C Mode	Configuration Via I <sup>2</sup> C	220	250	280	Hz
PWM2	PWM2 Frequency, I <sup>2</sup> C Mode	Configuration Via I <sup>2</sup> C	110	125	140	Hz
PWM3	PWM3 Frequency, I <sup>2</sup> C Mode	Configuration Via I <sup>2</sup> C	440	500	560	Hz

**Table 6. THERMAL WARNING AND THERMAL SHUTDOWN PROTECTION**

Characteristic	Symbol	Min	Typ	Max	Unit
T <sub>JWAR_ON</sub>	Thermal Warning Threshold (Junction Temperature)	–	TSD – 30	–	°C
TSD	Thermal Shutdown Threshold (Junction Temperature) T <sub>J</sub> Increasing	160	–	180	°C
T <sub>JSD_HYS</sub>	Thermal Shutdown Hysteresis	10	–	15	°C

**General**

The NCV7684 is a twelve channel LED driver. Each output can drive currents up to 60 mA/channel and are programmable via an external resistor. The target applications for the device are in automotive rear lighting systems and dashboard applications. The device can be used with micro-controller applications using the I<sup>2</sup>C bus or in stand-alone applications. In both cases it is mandatory to supply the LED channels by an external ballast transistor, or by an LDO or a DC/DC. In order to have very low electromagnetic emission, this device has an embedded spread spectrum oscillator.

Example:

R1 = 2 kΩ  
 using eq. 2 → I<sub>SET</sub> = 500 μA  
 and using eq. 3 → I<sub>OUTx</sub> = 50 mA

To avoid potential disturbances when all drivers are activated at the same time, a typical activation delay of 400 ns between groups of 2 consecutive outputs is implemented (see Figure 5).

**Output Current Programming (I<sub>SET</sub>/OUTx)**

The maximum current can be defined with the Iset input pin. The equations below can be used to calculate this maximum output current:

$$I_{set} = 1 \text{ V} / R1 \quad (\text{eq. 2})$$

$$I_{OUTx} = K \times I_{set} \quad (\text{eq. 3})$$

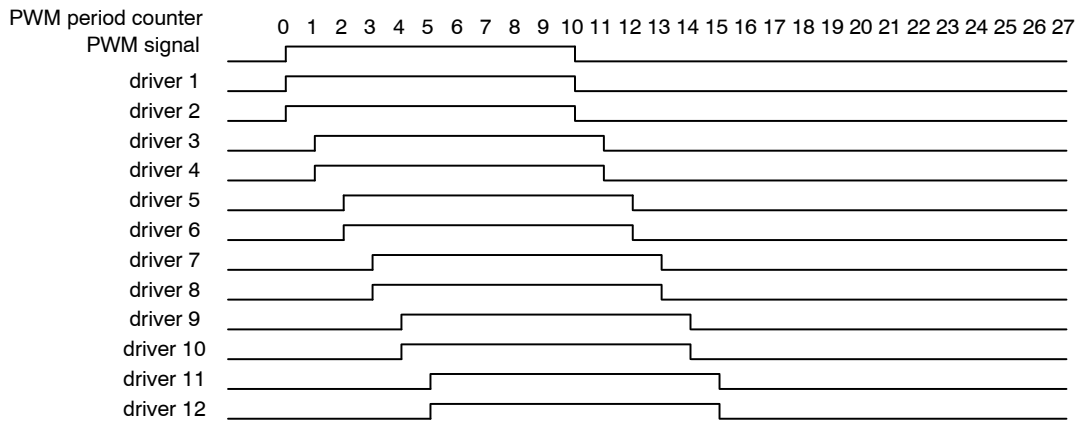


Figure 5.

**Power Supply and Voltage Reference (VS, V<sub>CC</sub>, V<sub>DD</sub>)**

VS is the analog power supply input of the device. VS supply is monitored with respect to the crossing of VSUV level (typ. 4.1 V). When VS rises above VSUV, the device starts the power-up state. When VS is above the VS\_OP minimum level (typ. 5 V), the device can work properly.

V<sub>CC</sub> is a voltage reference providing 3.3 V derived from the VS main supply. It is able to deliver up to 1 mA and is primarily intended to supply 3.3 V loads.

V<sub>DD</sub> is the digital power supply input of the device.

**Ground Connections (GND: Pin 13 and Pin 19)**

The device ground connection is split to two pins called GND. Both pins have to be connected on the application PCB.

**Chip Select (CSN)**

The device can be programmable using the I<sup>2</sup>C bus in End Of Line cases. When the CSN pin has a voltage above 1.66 V, the device will be set in zapping control mode via the I<sup>2</sup>C

bus. When CSN will be connected to ground or below 0.7 V, the device will be in a mode where zapping is not possible. Zapping is only possible with VS above 13 V.

**Configuration (CONF)**

When the CONF input voltage will be below 0.7 V the configuration 1 will be selected (One Time Programmable OTP 1 register called SAM\_CONF\_1) and when the CONF input voltage will be above 1.66 V the configuration 2 will be selected (OTP 2 register called SAM\_CONF\_2). There is ability to change the configuration in error mode (either with CONF in SAM or through I<sup>2</sup>C in I2C mode).

**I<sup>2</sup>C Bus (SCL, SDA)**

The I<sup>2</sup>C bus consists of two wires, Serial Data (SDA) and Serial Clock (SCL), carrying information between the devices connected on the bus. Each device connected to the bus is recognized by a unique address and operates as either a transmitter or receiver, depending on the function of the device. The NCV7684 can both receive and transmit data



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with CRC8 error detection algorithm. The NCV7684 is a slave device.

SDA is a bi-directional line connected to a positive supply voltage via an external pull-up resistor. When the bus is free both lines are HIGH. The output stages of the devices connected to the bus must have an open drain to perform the wired-AND function. Data on the I<sup>2</sup>C bus can be transferred up to 400 kb/s.

### Diagnostic Enabling (DIAGEN)

The device is capable to detect for each independent channel an open load condition. Versus the number of LEDs and the V<sub>STRING</sub> voltage supply, a wrong open load condition can be detected if the fault detection is activated when there is not enough voltage across the LEDs. This threshold can be programmable thanks to an external divider connected to the DIAGEN pin. When the divided voltage is below a typical value of 2 V, the LED diagnostic is disabled. When the divided voltage is above the typical value of 2 V, the LED diagnostic is enabled.

### Diagnostic Feedback (DIAG)

The DIAG is an open drain output pin who can alert a microcontroller as soon as one of the outputs is in error mode (DIAG Low = open load or thermal shut-down or Iset shorted). Forcing the DIAG pin below 1.8 V will force a fault condition if the DIAGEN input pin is above a typical value of 2 V. If the DIAGEN input pin is below the typical value of 2 V then forcing the DIAG input pin will not have any effect.

### Parallel Outputs (OUTx)

The maximum rating per output is 60 mA. In order to increase system level LED string current, parallel combinations of any number of outputs is allowed. Combining all 12 outputs will allow for a maximum system level string current design of 720 mA.

**DIGITAL PART AND I<sup>2</sup>C REGISTERS**

The I<sup>2</sup>C bus consists of two wires, serial data (SDA) and serial clock (SCL), carrying information between the devices connected on the bus. Each device connected to the bus is recognized by a unique address. The NCV7684 can both receive and transmit data with CRC8 error detection

algorithm. The NCV7684 is a slave device only. Generation of the signals on the I<sup>2</sup>C bus is always the responsibility of the master device.

They are multiple kinds of message structure possible versus ID code received.

**Table 7. IDENTIFIER ADDRESSING (ID) MESSAGE**

Name	ID	Access type	Name of Register Addressed
ID_I2C_CONF	00	W	I2C_CONF
ID_PWM	01	W	PWM_GAIN, PWM_GAIN_EN
ID_WRITEALL	02	W	I2C_CONF, PWM_GAIN, PWM_GAIN_EN
ID_PWM_CONF	03	W	PWM_CONF
ID_STATUS	08	R	I2C_STATUS
ID_FAULT	09	R	FAULT_STATUS
ID_READALL	0A	R	I2C_CH_STATUS, I2C_STATUS, FAULT_STATUS
ID_SET_OTP	20	W	SAM_CONF_1, SAM_CONF_2, ADD_SAM_SET
ID_LOCK_OTP	21	W	SAM_CONF_1, SAM_CONF_2, ADD_SAM_SET
ID_READ_OTP	28	R	ID_VERS_1, ID_VERS_2, SAM_CONF_1, SAM_CONF_2, ADD_SAM_SET

There are 3 kinds of registers, Hard Coding, OTP and volatile registers.

Hard Coding Registers:

- ID\_VERS\_1
- ID\_VERS\_2

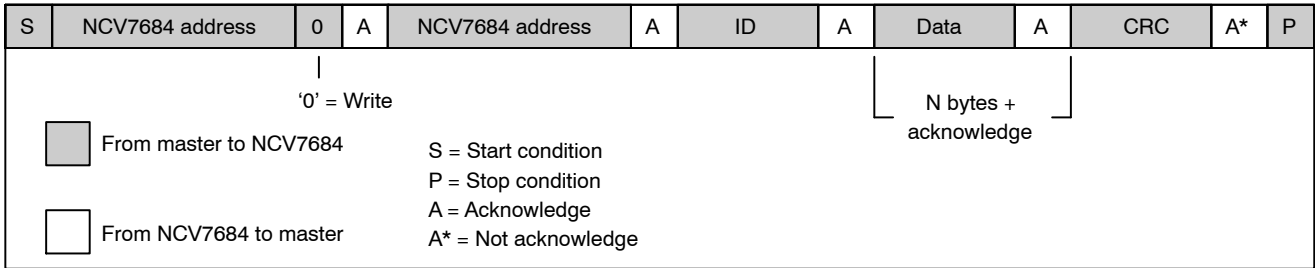
OTP Registers:

- ADD\_SAM\_SET
- SAM\_CONF\_1
- SAM\_CONF\_2

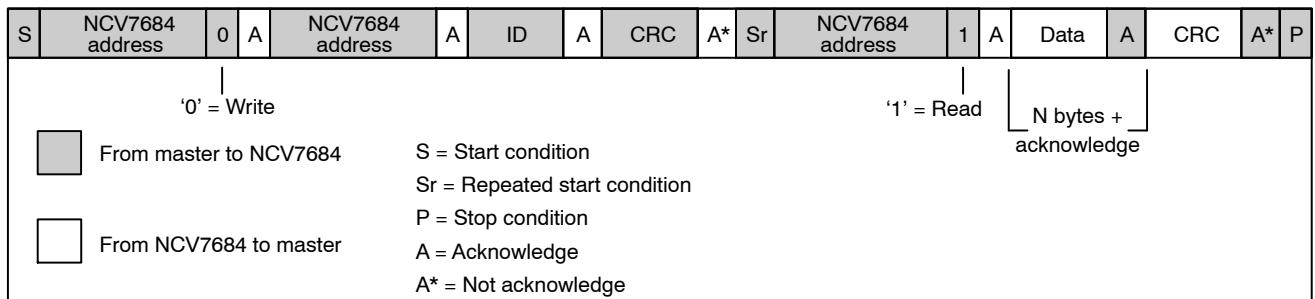
Volatile Registers:

- I2C\_CONF
- I2C\_STATUS
- I2C\_CH\_STATUS
- FAULT\_STATUS
- PWM\_GAIN
- PWM\_GAIN\_EN
- PWM\_CONF

**Format of the I2C frames**



**Figure 6. Format of I<sup>2</sup>C Write Access Frames**



**Figure 7. Format of I<sup>2</sup>C Read Access Frames**

*Remark:* CRC byte is not transmitted when CRC protection is turned off (ERREN = 0)

S	NCV7684 Address	0	NCV7684 Address	ID_I2C_CONF	I2C_CONF[15:8]	I2C_CONF[7:0]	CRC	P							
S	NCV7684 Address	0	NCV7684 Address	ID_PWM	PWM_GAIN	PWM_GAIN_EN[15:8]	PWM_GAIN_EN[7:0]	CRC							
S	NCV7684 Address	0	NCV7684 Address	ID_WRITEALL	I2C_CONF[15:8]	I2C_CONF[7:0]	PWM_GAIN	PWM_GAIN_EN[15:8]	PWM_GAIN_EN[7:0]	CRC	P				
S	NCV7684 Address	0	NCV7684 Address	ID_PWM_CONF	PWM_CONF	CRC	P								
S	NCV7684 Address	0	NCV7684 Address	ID_STATUS	CRC	Sr	NCV7684 Address	1	I2C_STATUS	CRC	P				
S	NCV7684 Address	0	NCV7684 Address	ID_FAULT	CRC	Sr	NCV7684 Address	1	FAULT_STATUS[15:8]	FAULT_STATUS[7:0]	CRC	P			
S	NCV7684 Address	0	NCV7684 Address	ID_READALL	CRC	Sr	NCV7684 Address	1	I2C_CH_STATUS[15:8]	I2C_CH_STATUS[7:0]	I2C_STATUS	FAULT_STATUS[15:8]	FAULT_STATUS[7:0]	CRC	P

Figure 8. Format of I<sup>2</sup>C Frames

- From master to NCV7684
  - From NCV7684 to master
- Acknowledges are omitted  
 S = Start condition  
 Sr = Repeated start condition  
 P = Stop condition

S	NCV7684 Address	0	NCV7684 Address	ID_SET_OTP	SAM_CONF_1[15:8]	SAM_CONF_1[7:0]	SAM_CONF_2[15:8]	SAM_CONF_2[7:0]	ADD_SAM_SET	CRC	P						
S	NCV7684 Address	0	NCV7684 Address	ID_LOCK_OTP	SAM_CONF_1[15:8]	SAM_CONF_1[7:0]	SAM_CONF_2[15:8]	SAM_CONF_2[7:0]	ADD_SAM_SET	CRC	P						
S	NCV7684 Address	0	NCV7684 Address	ID_READ_OTP	CRC	Sr	NCV7684 Address	1	ID_VERS_1	ID_VERS_2	SAM_CONF_1[15:8]	SAM_CONF_1[7:0]	SAM_CONF_2[15:8]	SAM_CONF_2[7:0]	ADD_SAM_SET	CRC	P

Figure 9. Format of I<sup>2</sup>C OTP Frames

- From master to NCV7684
  - From NCV7684 to master
- Acknowledges are omitted  
 S = Start condition  
 Sr = Repeated start condition  
 P = Stop condition

Note: Not to scale.

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There is a safety mechanism implemented by repeating the address. Since the I<sup>2</sup>C address is 7 bits long, first bit of the second address byte starts with a “0” in the repeated byte (see tables below).

**Table 8.**

1 <sup>st</sup> Byte							
7	6	5	4	3	2	1	0
I <sup>2</sup> C Device Address							R/W Bit
2 <sup>nd</sup> Byte							
7	6	5	4	3	2	1	0
I <sup>2</sup> C Device Address							0

### HARD CODING REGISTERS

**Table 9. HARD CODING REGISTERS**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
<b>ID_VERS_1</b>								
Bit name	ID1[7:0]							
Access type	R	R	R	R	R	R	R	R
Reset value	0	1	0	0	0	0	1	1
<b>ID_VERS_2</b>								
Bit name	ID2[7:0]							
Access type	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	1	0

1. ID1[7:0] = 43h (ON Semi Device Identifier)  
ID2[7:0] = 02h (The Actual Version)

OTP REGISTERS

Table 10. ADD\_SAM\_SET

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	AUTOR	DETONLY	ERREN	ADD[4:0]				
Access type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	1	0	0	0	0	0	0

ADD[4:0] are the programmable BUS address registers (in I2C mode ADD[6:5] = 11).

**AUTOR:** When AUTOR = 1 (and DIAGEN is high), open load diagnosis is performed. When a fault is detected, the DIAG pin is set and LED driver imposes a low current on the faulty branch alone, switching off the others. When fault is recovered, LED driver returns to normal operation after resetting the DIAG pin. If the DIAG pin is triggered externally, LED driver outputs are switched off and the low power mode is entered.

**DETONLY:** When DETONLY = 1, open load diagnostic is performed. When a fault is detected, the DIAG pin is set without taking any action on the current regulation. When fault is recovered, DIAG is reset. If the DIAG pin is triggered externally, no action is taken.

When AUTOR = DETONLY = 0, no diagnostic performed  
 When AUTOR = DETONLY = 1, no change (same as previously setting).

**ERREN:** When ERREN = 1, CRC error detection algorithm is activated for I<sup>2</sup>C communication.

Table 11. SAM\_CONF

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

SAM\_CONF\_1

Bit name	-	-	-	-	SAM1conf[11:0]											
Access type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

SAM\_CONF\_2

Bit name	-	-	-	-	SAM2conf[11:0]											
Access type	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset value	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

- SAM1conf[x] = 0 means channel is OFF and SAM1conf[x] = 1 means channel is ON  
 SAM2conf[x] = 0 means channel is OFF and SAM2conf[x] = 1 means channel is ON

VOLATILE REGISTERS

Table 12. I2C\_CONF

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	I2CFLAG	I2CautoR	I2CdOnly	PWMEN	I2Cconf[11:0]											
Access type	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**I2CFLAG:** the I2CFLAG should be reset whenever standalone mode is entered. When I2CFLAG = 1 and when V<sub>DD</sub> is high, the I2C mode is activated, in all other conditions the device is in Stand Alone Mode.

**I2CautoR:** When I2CautoR = 1 (and DIAGEN is high), open load diagnosis is performed. When a fault is detected, the DIAG pin is set and LED driver imposes a low current on the faulty branch alone, switching off the others. When fault is recovered, LED driver returns to normal operation after resetting the DIAG pin. If the DIAG pin is triggered externally, LED driver outputs are switched off and the low power mode is entered.

**I2CdOnly:** When I2CdOnly = 1, open load diagnostic is performed. When a fault is detected, the DIAG pin is set

without taking any action on the current regulation. When fault is recovered, DIAG is reset. If the DIAG pin is triggered externally, no action is taken.

When I2CautoR = I2CdOnly = 0, no diagnostic performed.

When I2CautoR = I2CdOnly = 1, no change (same as previously setting).

**PWMEN:** When PWMEN = 1, PWM is activated, when PWMEN = 0 the content of the complete register PWM\_GAIN\_EN is not reset and PWM is disabled.

I2Cconf[x] = 0 means channel is OFF and I2Cconf[x] = 1 means channel is ON.

Table 13. I2C STATUS

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	SC_Iset	I2Cerr	UV	diagRange	TW	TSD	DIAGERR	OL
Access type	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0

**SC\_Iset:** SC\_Iset = 1 means there is short-circuit on the external resistor on Iset pin and drivers are switched OFF and DIAG pin is set. SC\_Iset = 0 no short-circuit.

**I2Cerr:** I2Cerr = 1 means an error has been detected during the I2C communication, I2Cerr = 0 means no error during I2C communication has been detected.

**UV:** the device is in under voltage condition (VS is below VSUV threshold, all channels OFF).

**diagRange:** when diagRange = 1 the divided voltage is above the typical value of 2 V (LED diagnostic is enabled), diagRange = 0 means the divided voltage is below the typical value of 2 V (LED diagnostic is disabled).

**TW:** when TW=1 the device is in the thermal warning range (typ. 140°C), this flag is just a warning no action is foreseen on the output drivers. TW = 0 means the device is below the thermal warning range.

**TSD:** when TSD = 1 the device is in the Thermal shutdown range, TSD = 0 means the device is below the thermal shutdown range.

**DIAGERR:** DIAGERR = 1 means an error is detected by DIAG pin forced externally.

**OL:** OL = 1 means at least one channel is in Open Load condition, OL = 0 no Open Load.

Table 14.

SC_ISET	Set when a short-circuit on the external resistor on Iset pin, latched if permanent after 10 μs. Reset in case of short-circuit disappear permanently for at least 10 μs
I2CERR	Set if an error has been detected during the I2C communication. Reset on register reading
UV	Set when device is in under voltage condition (VS is low, all channels OFF)
diagRange	Set when divided voltage is above the V <sub>DIAGEN</sub> TH threshold. Reset when the divided voltage is below the V <sub>DIAGEN</sub> TH threshold
TW	Set when junction temperature is above the T <sub>JWAR_ON</sub> threshold. Reset on register reading and if temperature is below the (T <sub>JWAR_ON</sub> - T <sub>JSD_HYS</sub> ) threshold
TSD	Set when junction temperature is above the TSD threshold. Reset on register reading and if temperature is below the TSD - T <sub>JSD_HYS</sub> threshold

**Table 14.** (continued)

DIAGERR	Set by DIAG pin forced low externally, latched if permanent after 10 μs. Reset in case DIAG pin is not forced permanently for at least 10 μs
OL	Set in Open Load condition and DIAGEN is high, latched if permanent after 10 μs. Reset if Open Load disappear permanently for at least 10 μs. Fault information is maintained on falling DIAGEN threshold exceeded

**Table 15. I2C\_CH\_STATUS**

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	I2CFLAG	I2CautoR	I2CdOnly	PWMEN	I2C_CH_STATUS[11:0]											
Access type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*I2CFLAG*: same as I2C\_CONF register.

*I2CautoR*: same as I2C\_CONF register.

*I2CdOnly*: same as I2C\_CONF register.

*PWMEN*: same as I2C\_CONF register.

*I2C\_CH\_STATUS[11:0]*: same as I2C\_CONF[11:0] bits in I2C mode or same as SAM\_CONF\_1[11:0], SAM\_CONF\_2[11:0] bits in Standalone mode.

*Remark*: When NCV7684 is configured in I2C mode and output channel OUTx is configured to operate in PWM mode, I2C\_CH\_STATUS[x] shall contain value ‘1’.

**Table 16. FAULT\_STATUS**

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	-	-	-	-	FAULT[11:0]											
Access type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*FAULT[11:0]*: when FAULT[x] = 1 the OUTx channel is in fault mode (Open Load latched when the duration is longer than 10 μs), when FAULT[x] = 0 the OUTx channel

is working properly. The register is reset on each read operation.

**Table 17. PWM\_GAIN**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit Name	PWMF1	PWMGAIN[6:0]						
Access type	W	W	W	W	W	W	W	W
Reset Value	0	0	0	0	0	0	0	0

*PWMGAIN[6:0]*: logarithmic (or linear) dimming via embedded PWM generator (128 steps). Following formula applies when logarithmic dimming is selected:  
 $Duty\_Cycle\_Percent = 100 \times \alpha^{(N-i)}$  where  $\alpha = 0.9471$ ,  
 $N = 127$  and  $i = PWMGAIN[6:0]$  rounded with an accuracy of 400 ns.

*PWMF1*: when PWMF1 = 1, PWM dimming is done at a typical frequency of 250 Hz, when PWMF1 = 0 means PWM dimming is done at a typical frequency of 125 Hz (when PWMF2 = 0).

**Table 18. PWM\_GAIN\_EN**

Bit	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	-	-	-	-	PWMGAINen[11:0]											
Access type	-	-	-	-	W	W	W	W	W	W	W	W	W	W	W	W
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

*PWMGAINen[11 :0]* : when  $PWMGAINen[x] = 1$ , PWM dimming is enabled for OUTx channel, when  $PWMGAINen[x] = 0$  means PWM dimming is disabled for OUTx channel.

**Table 19. PWM\_CONF**

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Bit name	-	-	-	-	-	-	PWMLIN	PWMF2
Access type	W	W	W	W	W	W	W	W
Reset value	0	0	0	0	0	0	0	0

*PWMLIN* bit shall select between logarithmic ( $PWMLIN = 0$ ) and linear ( $PWMLIN = 1$ ) translation of *PWMGAIN* bits to duty cycle of internal PWM signal.

*PWMF2*: when  $PWMF2 = 1$ , PWM dimming is done at a typical frequency of 500 Hz, when  $PWMF2 = 0$ , *PWMF1* setting applies.





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