Click here to ask about the production status of specific part numbers.

MAX32650–MAX32652

Ultra-Low-Power Arm Cortex-M4 Processor with FPU-Based Microcontroller (MCU) with 3MB Flash and 1MB SRAM

General Description

DARWIN is a new breed of low-power microcontrollers built to thrive in the rapidly evolving Internet of Things (IoT). They are smart, with the biggest memories in their class and a massively scalable memory architecture. They run forever, thanks to wearable-grade power technology. They are also tough enough to withstand the most advanced cyberattacks. DARWIN microcontrollers are designed to run any application you can imagine—in places where you wouldn't dream of sending other microcontrollers.

Generation UP microcontrollers are designed to handle the increasingly complex applications demanded by today's advanced battery-powered devices and wireless sensors. The MAX32650–MAX32652 are ultra-low-power memory-scalable microcontrollers designed specifically for high-performance, battery-powered applications. They are based on an Arm® Cortex®-M4 with FPU CPU with 3MB flash and 1MB SRAM. Memory scalability is supported with multiple memory-expansion interfaces, including a HyperBus™/Xccela™ DDR interface and two SPI execute in place (SPIx) interfaces. A secure digital interface supports external high-speed memory cards, including SD, SDIO, MMC, SDHC, and microSD™.

Power-management features provide five low-power modes for clock, peripheral, and voltage control. Individual SRAM banks of 32KB, 96KB, or 1024KB (full retention) can be retained with reduced power consumption. A SmartDMA performs complex background processing while the CPU is off to dramatically reduce overall power consumption.

The MAX32651 is a secure version with a trust protection unit (TPU) which provides a modular arithmetic accelerator (MAA) for fast ECDSA, an AES engine, TRNG, SHA-256 hash, and secure bootloader. A memory decryption integrity unit (MDIU) provides on-the-fly data decryption (plain or executable) stored in external flash.

The MAX32652 is packaged in a high-density, 0.35mm pitch, 140-bump WLP targeted for tiny form factor products that require high I/O counts.

Applications

- Sports Watches, Fitness Monitors
- Wearable Medical Patches, Portable Medical Devices
- Industrial Sensors, IoT

Benefits and Features

- Ultra-Efficient Microcontroller for Battery-Powered Applications
  - 120MHz Arm Cortex-M4 Processor with FPU
  - SmartDMA Provides Background Memory Transfers with Programmable Data Processing
  - 120MHz High-Speed and 50MHz Low-Power Oscillators
  - 7.3728MHz Low-Power Oscillators
  - 32.768kHz and RTC Clock (Requires External Crystal)
  - 8kHz, Always-On, Ultra-Low-Power Oscillator
  - 3MB Internal Flash, 1MB Internal SRAM
  - 104µW/MHz Executing from Cache at 1.1V
  - Five Low-Power Modes: Active, Sleep, Background, Deep Sleep, and Backup
  - 1.8V and 3.3V I/O with No Level Translators
- Scalable Cached External Memory Interfaces:
  - 120MB/s HyperBus/Xccela DDR Interface
  - SPIXF/SPIXR for External Flash/RAM Expansion
  - 240Mbps SDHC/eMMC/SDIO/microSD Interface
- Optimal Peripheral Mix Provides Platform Scalability
  - 16-Channel DMA
  - Three SPI Master (60MHz)/Slave (48MHz)
  - One QuadSPI Master (60MHz)/Slave (48MHz)
  - Up to Three 4Mbaud UARTs with Flow Control
  - Two 1MHz I^2C Master/Slave
  - I^2S Slave
  - Four-Channel, 7.8ksps, 10-Bit Delta-Sigma ADC
  - USB 2.0 Hi-Speed Device Interface with PHY
  - 16 Pulse Train Generators
  - Six 32-Bit Timers with 8mA High Drive
  - 1-Wire® Master
- Trust Protection Unit (TPU) for IP/Data Security
  - Modular Arithmetic Accelerator (MAA), True Random Number Generator (TRNG)
  - Secure Nonvolatile Key Storage, SHA-256, AES-128/192/256
  - Memory Decryption Integrity Unit, Secure Boot ROM

***Ordering Information* appears at end of data sheet.**

19-100220; Rev 7; 10/20

maxim integrated™

Simplified Block Diagram

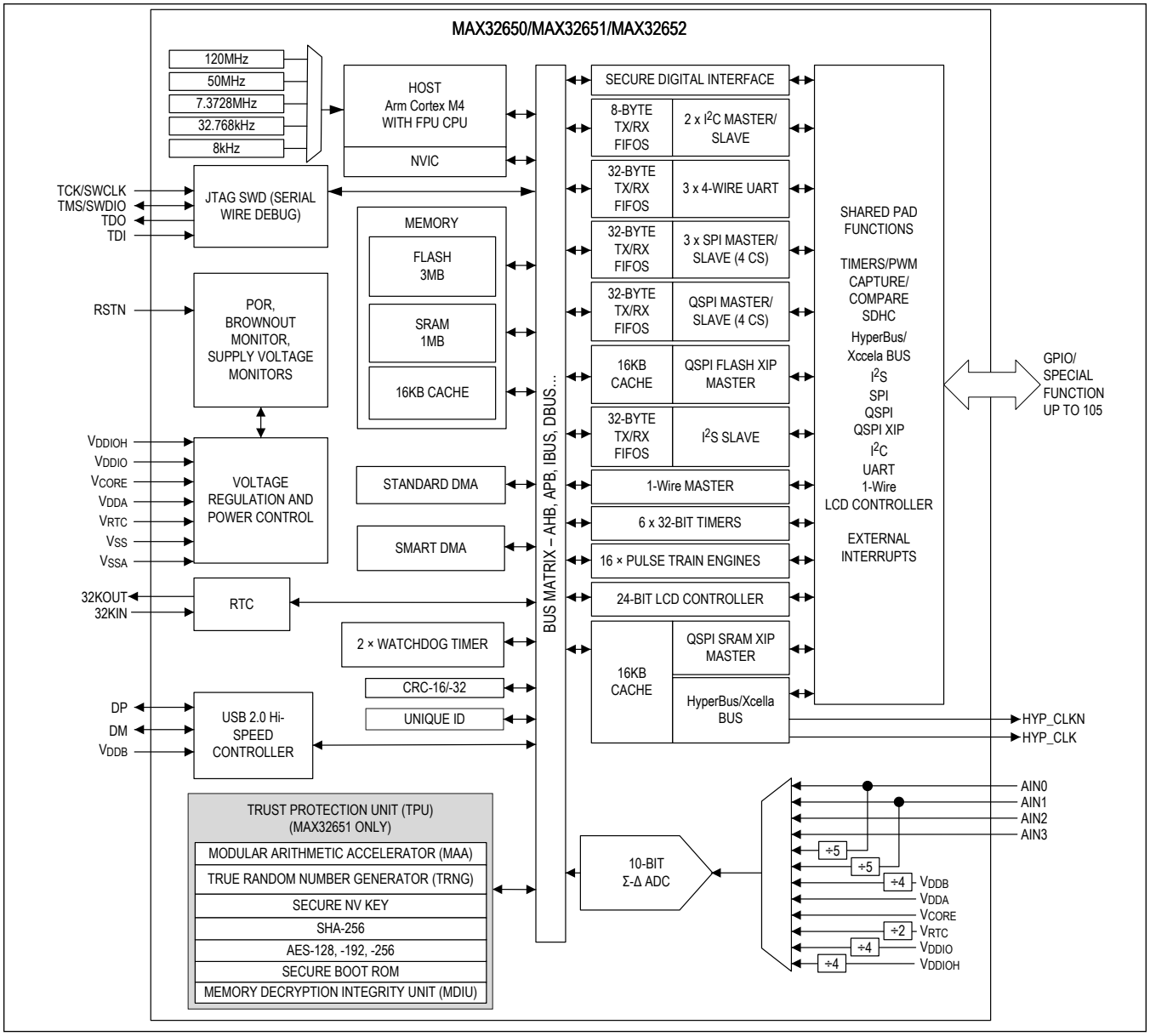


TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

LIST OF FIGURES

LIST OF TABLES

Absolute Maximum Ratings

(All voltages with respect to V_{SS}, unless otherwise noted.) .....
V_{CORE} ..... -0.3V to 1.21V
V_{DDA} ..... -0.3V to 1.98V
V_{DDIO} ..... -0.3V to 1.98V
V_{DDIOH} ..... -0.3V to 3.6V
V_{RTC} ..... -0.3V to 1.98V
RSTN, GPIO (V_{DDIO}) ..... -0.3V to V_{DDIO} + 0.5V
GPIO (V_{DDIOH}) ..... -0.3V to V_{DDIOH} + 0.5V
32KIN, 32KOUT ..... -0.3V to V_{RTC} + 0.2V
AIN[1:0] ..... -0.3V to 5.5V
AIN[3:2] ..... -0.3V to V_{DDA} + 0.2V
V_{DDB} ..... -0.3V to 3.6V
DM, DP ..... -0.3V to 3.6V
HYP_CLK, HYP_CLKN, P1.[21:18], P1.[16:11], P3.0 ..... -0.3V to V_{DDIO} + 0.3V, not to exceed 1.98V
V_{DDIO} pins (sink) 100mA
V_{DDIOH} pins (sink) 100mA
V_{SSA} 100mA
V_{SS} 100mA
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin ..... -25mA
Continuous Package Power Dissipation TQFP (multilayer board)
T_A = +70°C (derate 45.5mW/°C above +70°C) 2857.10mW
Operating Temperature Range ..... -40°C to +105°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

140 WLP

Package Code	W1404A4+1
Outline Number	21-100219
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	35.13°C/W
Junction to Case (θ_{JC})	N/A

96 WLP

Package Code	W964A4+1
Outline Number	21-100240
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	33.61°C/W
Junction to Case (θ_{JC})	N/A

144 TQFP

Package Code	C144+1
Outline Number	21-0087
Land Pattern Number	90-0144
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	28°C/W
Junction to Case (θ_{JC})	8°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER (Refer to the MAX32650 User Guide for sequencing requirements)						
Supply Voltage, Core	V_{CORE}	f_{SYS_CLK} = 120MHz	0.99	1.1	1.21	V
Supply Voltage, Analog	V_{DDA}		1.71	1.8	1.89	V
Supply Voltage, RTC	V_{RTC}		1.71	1.8	1.89	V
Supply Voltage, GPIO	V_{DDIO}		1.71	1.8	1.89	V
Supply Voltage, GPIO (High)	V_{DDIOH}		1.71	1.8	3.6	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{CORE}		0.835		V
		Monitors V_{DDA}		1.67		
		Monitors V_{RTC}		1.67		
		Monitors V_{DDIO}		1.67		
Power Fail Reset Voltage	V_{RST}	Monitors V_{DDB}		2.95		V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DDIOH}		1.67		V
Power-On Reset Voltage	V_{POR}	Monitors V_{CORE}		0.594		V
		Monitors V_{DDA}		1.52		
		Monitors V_{RTC}		1.17		
RAM Data Retention Voltage	V_{DRV}			0.81		V
V_{CORE} Dynamic Current, Active Mode	I_{CORE_DACT}	Total current into V_{CORE} pins, f_{SYS_CLK} = 120MHz, V_{CORE} = 1.1V, CPU in Active mode, executing from cache; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA		95		µA/MHz

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CORE} Fixed Current, Active Mode	I_{CORE_FACT}	120MHz oscillator enabled, total current into V_{CORE} pins, CPU in Active mode 0MHz execution; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	V_{CORE} = 1.0V		1200		µA
			V_{CORE} = 1.1V		1500		
		7.3728MHz oscillator enabled, total current into V_{CORE} pins, CPU in Active mode 0MHz execution; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA	V_{CORE} = 1.0V		555		
			V_{CORE} = 1.1V		790		
V_{DDA} Fixed Current, Active Mode	I_{DDA_FACT}	120MHz oscillator enabled, total current into V_{DDA} pins, CPU in Active mode 0MHz execution; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA, V_{CORE} and V_{DDA} voltage monitors enabled			348		µA
		7.3728MHz oscillator enabled, total current into V_{DDA} pins, CPU in Active mode 0MHz execution; inputs tied to V_{SS}, V_{DDIO}, or V_{DDIOH}; outputs source/sink 0mA, V_{CORE} and V_{DDA} voltage monitors enabled			39		
V_{CORE} Dynamic Current, Sleep Mode	I_{CORE_DSLP}	Total current into V_{CORE} pins, CPU in Sleep mode, standard DMA with two channels active			114		µA/MHz
V_{CORE} Fixed Current, Sleep Mode	I_{CORE_FSLP}	f_{SYS_CLK} = 120MHz, total current into V_{CORE} pins, CPU in Sleep mode, standard DMA with two channels active			1020		µA
		f_{SYS_CLK} = 7.3728MHz, total current into V_{CORE} pins, CPU in Sleep mode, standard DMA with two channels active			356		
V_{DDA} Fixed Current, Sleep Mode	I_{DDA_FSLP}	f_{SYS_CLK} = 120MHz, total current into V_{DDA} pins, CPU in Sleep mode, standard DMA with two channels active			348		µA
		f_{SYS_CLK} = 7.3728MHz, total current into V_{DDA} pins, CPU in Sleep mode, standard DMA with two channels active			49		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CORE} Dynamic Current, Background Mode	I_{CORE_DBKG}	f_{SYS_CLK} = 7.3728MHz, total current into V_{CORE} pins, CPU in Deep-Sleep mode, SmartDMA active			66		µA/MHz
V_{CORE} Fixed Current, Background Mode	I_{CORE_FBKG}	7.3728MHz oscillator enabled, total current into V_{CORE} pins, CPU in Deep-Sleep mode, SmartDMA active	V_{CORE} = 1.0V		224		µA
			V_{CORE} = 1.1V		330		
V_{CORE} Fixed Current, Deep-Sleep Mode	I_{CORE_FDSL}	Standby state with full data retention			70		µA
V_{DDA} Fixed Current, Deep-Sleep Mode	I_{DDA_FDSL}	Standby state with full data retention, V_{CORE} and V_{DDA} voltage monitors enabled			132		nA
V_{RTC} Fixed Current, Deep-Sleep Mode	I_{DDRTC_FDSL}	Standby state with full data retention, V_{RTC} = 1.8V, RTC enabled			540		nA
V_{CORE} Fixed Current, Backup Mode	I_{CORE_FBKU}	No SRAM retention (0KB)			30		µA
V_{DDA} Fixed Current, Backup Mode	I_{DDA_FBKU}	V_{DDA} voltage monitor enabled			132		nA
V_{RTC} Fixed Current, Backup Mode	I_{DDRTC_FBKU}	RTC enabled, retention regulator off			540		nA
		RTC enabled, 32KB SRAM retained, retention regulator on			720		
		RTC disabled, retention regulator off			156		
Sleep Mode Resume Time	t_{SLP_ON}				575		ns
Deep-Sleep Mode Resume Time	t_{DSL_ON}	Wake to f_{LPCLK}			9		µs
		Wake to f_{HSCLK}			18		
Backup Mode Resume Time	t_{BKU_ON}				5		ms
USB							
USB Supply Voltage	V_{DDB}			3.0	3.3	3.6	V
D+, D- Pin Capacitance	C_{IN_USB}	Pin to V_{SS}			8		pF
Driver Output Resistance	R_{DRV}	Steady-state drive			45 ± 10%		Ω
USB / FULL SPEED							
Single-Ended Input High Voltage (DP, DM)	V_{IH_USB}			2.0			V
Single-Ended Input Low Voltage (DP, DM)	V_{IL_USB}					0.6	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage (DP, DM)	V_{OH_USB}	R_L = 1.5kΩ from DP and DM to V_{SS}, I_{OH} = -4mA	V_{DDB} - 0.4		V_{DDB}	V
Output Low Voltage (DP, DM)	V_{OL_USB}	R_L = 1.5kΩ from DP to V_{DDB}, I_{OL} = 4mA	V_{SS}		0.4	V
Differential Input Sensitivity	V_{DI}	|DP to DM|	0.2			V
Common-Mode Voltage Range	V_{CM}	Includes V_{DI} range	0.8		2.5	V
Transition Time (Rise/ Fall) D+, D- (Note 11)	t_{RF}	C_L = 50pF	4		20	ns
Pullup Resistor on Upstream Ports	R_{PU}		1.05	1.5	1.95	kΩ
USB / HI-SPEED						
Hi-Speed Data Signaling Common-Mode Voltage Range	V_{HSCM}		-50		+500	mV
Hi-Speed Squelch Detection Threshold	V_{HSSQ}	Squelch detected		100		mV
		No squelch detected		200		
Hi-Speed Idle Level Output Voltage	V_{HSOI}		-10		+10	mV
Hi-Speed Low Level Output Voltage	V_{HSOL}		-10		+10	mV
Hi-Speed High Level Output Voltage	V_{HSOH}			400 ± 40		mV
Chirp-J Output Voltage (Differential)	V_{CHIRPJ}			900 ± 200		mV
Chirp-K Output Voltage (Differential)	V_{CHIRPK}			-700 ± 200		mV
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		0.256		120,000	kHz
System Clock Period	t_{SYS_CLK}			1/ f_{SYS_CLK}		ns
High-Speed Oscillator Frequency	f_{HSCLK}	Measured at +25°C, 120MHz		120 ± 1		MHz
Low-Power Oscillator Frequency	f_{LPCLK}			50		MHz
7MHz Oscillator Frequency	f_{7MCLK}			7.3728		MHz

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Nanoring Oscillator Frequency	f_{NANO}			8		kHz
RTC Input Frequency	f_{32KIN}	32kHz watch crystal, C_L = 6pF, ESR < 70kΩ		32.768		kHz
RTC Operating Current	I_{RTC_ACTSLP}	Sleep or Active mode		0.39		µA
RTC Power Up Time	$t_{RTC\_ ON}$			250		ms
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO	V_{IL_VDDIO}	V_{DDIO} selected as I/O supply			0.3 × V_{DDIO}	V
Input Low Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{IL_VDDIOH}	V_{DDIOH} selected as I/O supply			0.3 × V_{DDIOH}	V
Input Low Voltage for RSTN	V_{IL_RSTN}				0.3 x V_{DDIO}	V
Input High Voltage for All GPIO	V_{IH_VDDIO}	V_{DDIO} selected as I/O supply	0.75 × V_{DDIO}			V
Input High Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{IH_VDDIOH}	V_{DDIOH} selected as I/O supply	0.75 × V_{DDIOH}			V
Input High Voltage for RSTN	V_{IH_RSTN}		0.75 x V_{DDIO}			V
Output Low Voltage for All GPIO	V_{OL_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Output Low Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{OL_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 00, I_{OL} = 1mA		0.2	0.4	V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 01, I_{OL} = 2mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 10, I_{OL} = 4mA		0.2	0.4	
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 11, I_{OL} = 8mA		0.2	0.4	
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				48	mA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage for All GPIO	V_{OH_VDDIO}	V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = -1mA	V_{DDIO} - 0.4			V
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 01, I_{OL} = -2mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 10, I_{OL} = -4mA	V_{DDIO} - 0.4			
		V_{DDIO} selected as I/O supply, V_{DDIO} = 1.71V, DS[1:0] = 00, I_{OL} = -8mA	V_{DDIO} - 0.4			
Output High Voltage for All GPIO except P1.[21:18], P1.[16:11], P3.0	V_{OH_VDDIOH}	V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 00, I_{OL} = -1mA	V_{DDIOH} - 0.4			V
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 01, I_{OL} = -2mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 10, I_{OL} = -8mA	V_{DDIOH} - 0.4			
		V_{DDIOH} selected as I/O supply, V_{DDIOH} = 1.71V, DS[1:0] = 11, I_{OL} = -8mA	V_{DDIOH} - 0.4			
Combined I_{OH}, All GPIO	I_{OH_TOTAL}				-48	mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input Leakage Current Low	I_{IL}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 0V, internal pullup disabled	-1000		+1000	nA
Input Leakage Current High	I_{IH}	V_{DDIO} = 1.89V, V_{DDIOH} = 3.6V, V_{DDIOH} selected as I/O supply, V_{IN} = 3.6V, internal pulldown disabled	-1000		+1000	nA
	I_{OFF}	V_{DDIO} = 0V, V_{DDIOH} = 0V, V_{DDIO} selected as I/O supply, V_{IN} < 1.89V	-1		+1	µA
	I_{IH3V}	V_{DDIO} = V_{DDIOH} = 1.71V, V_{DDIO} selected as I/O supply, V_{IN} = 3.6V	-2		+2	
Input Pullup Resistor TMS, TCK, TDI	R_{PU_T}			25		kΩ
Input Pullup Resistor RSTN	R_{PU_R}			25		kΩ
Input Pullup/Pulldown Resistor for All GPIO	R_{PU1}	Normal resistance		25		kΩ
	R_{PU2}	Highest resistance		1		MΩ
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		
Flash Programming Time per Word	t_{PROG}	32-bit programming mode, f_{FLC_CLK} = 1MHz		60		µs
Flash Endurance			10			kcycles

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested. General-purpose I/O are only tested at T_A = +105°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Retention	t_{RET}	T_A = +85°C	10			years
ADC (DELTA-SIGMA)						
Resolution				10		bits
ADC Clock Rate	f_{ACLK}		0.1		8	MHz
ADC Clock Period	t_{ACLK}			$1/f_{ACLK}$		µs
Input Voltage Range	V_{AIN}	AIN[3:0], ADC_CHSEL = 0-3, ADC_REFSEL = 1	V_{SSA} + 0.05		$V_{BG}/2$	V
		AIN[3:0], ADC_CHSEL = 0-3, ADC_REFSEL = 0	V_{SSA} + 0.05		V_{BG}	
		AIN[1:0], ADC_CHSEL = 4-5, ADC_REFSEL = 0	V_{SSA} + 0.05		5.5	
Input Impedance	R_{AIN}	AIN[3:0], ADC_CHSEL = 0-3, ADC active		250		kΩ
		AIN[1:0], ADC_CHSEL = 4-5, ADC active		40		
Analog Input Capacitance	C_{AIN}	Fixed capacitance to V_{SSA}		1		pF
		Dynamically switched capacitance		250		fF
Integral Nonlinearity	INL		-2		+2	LSb
Differential Nonlinearity	DNL		-1		+2	LSb
Offset Error	V_{OS}			±1		LSb
Gain Error	GE			±2		LSb
ADC Active Current	I_{ADC}	ADC active, reference buffer enabled, input buffer disabled		210		µA
ADC Setup Time	t_{ADC_SU}	Any power-up of: ADC clock or ADC bias to CpuAdcStart			10	µs
ADC Output Latency	tADC			1025		t_{ACLK}
ADC Sample Rate	f_{ADC}				7.8	ksps
ADC Input Leakage	I_{ADC_LEAK}	AIN0 or AIN1, ADC inactive or channel not selected		0.01		nA
		AIN2 or AIN3, ADC inactive or channel not selected		0.01		
AIN0/AIN1 Resistor Divider Error		ADC_CHSEL = 4 or 5, not including ADC offset/gain error		±2		LSb
Full-Scale Voltage	V_{FS}	ADC code = 0x3FF		1.2		V
Bandgap Temperature Coefficient	V_{TEMPCO}	From +25°C to +105°C		15		ppm

Electrical Characteristics—SPI

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	$f_{MCK(MAX)} = f_{SYS\_CLK}/2$			60	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				48	MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs

Electrical Characteristics—I^2C

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs

Electrical Characteristics—I²C (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST MODE PLUS						
Output Fall Time	t_{OF}	From $V_{IH(MIN)}$ to $V_{IL(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

Electrical Characteristics—I²S Slave

(Timing specifications are guaranteed by design and not production tested., T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLK}	96kHz LRCLK frequency			3.072	MHz
BCLK High Time	t_{WBCLKH}			0.5		$1/f_{BCLK}$
BCLK Low Time				0.5		$1/f_{BCLK}$
LRCLK Setup Time	t_{LRCLK_BLCK}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDO}			12		ns

Electrical Characteristics—I²S Slave (continued)

(Timing specifications are guaranteed by design and not production tested., T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for SD (Input)	t_{SU_SDI}			6		ns
Hold Time SD (Input)	t_{HD_SDI}			3		ns

Electrical Characteristics—SD/SDIO/SDHC/MMC

(T_A = -40°C to +105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Frequency in Data Transfer Mode	f_{SDHC_CLK}		0		$f_{HSCLK}/2$	MHz
Clock Period	t_{CLK}			$1/f_{SDHC\_CLK}$		ns
Clock Low Time	t_{WCL}			7		ns
Clock High Time	t_{WCH}			7		ns
Input Setup Time	t_{ISU}			5		ns
Input Hold Time	t_{IHLD}			1		ns
Output Valid Time	t_{OVLD}			5		ns
Output Hold Time	t_{OHLD}			6		ns

Electrical Characteristics—HyperBus

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HYP_CLK, HYP_CLKN Frequency	f_{HYP_CLK}				60	MHz
HYP_CLK, HYP_CLKN Period	t_{HYP_CLK}		$1/f_{HYP\_CLK}$			ns
HYP_CLK, HYP_CLKN High Time	t_{WHCKH}			7		ns
HYP_CLK, HYP_CLKN Low Time	t_{WHCKL}			7		ns
CS Setup to RWDS	t_{CSSU}			6		ns
RWDS Setup to CK	t_{RWDS_CK}			10		ns
Dx Output Setup	t_{OSU}			5		ns
Dx Output Hold	t_{OH}			3		ns
CS Hold After CK Falling Edge	t_{CSH}			5		ns
CS High Between Transactions	t_{CHSI}			15		ns
Dx Input Setup to RWDS	t_{ISU}			4		ns

Electrical Characteristics—HyperBus (continued)

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dx Input Hold	t_{IHD}			2		ns

Electrical Characteristics—1-Wire Master

(Timing specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Write 0 Low Time	t_{W0L}	Standard		60		µs
		Overdrive		8		
Write 1 Low Time	t_{W1L}	Standard		6		µs
		Standard, Long Line mode		8		
		Overdrive		1		
Presence Detect Sample	t_{MSP}	Standard		70		µs
		Standard, Long Line mode		85		
		Overdrive		9		
Read Data Value	t_{MSR}	Standard		15		µs
		Standard, Long Line mode		24		
		Overdrive		3		
Recovery Time	t_{REC0}	Standard		10		µs
		Standard, Long Line mode		20		
		Overdrive		4		
Reset Time High	t_{RSTH}	Standard		480		µs
		Overdrive		58		
Reset Time Low	t_{RSTL}	Standard		600		µs
		Overdrive		70		
Time Slot	t_{SLOT}	Standard		70		µs
		Overdrive		12		

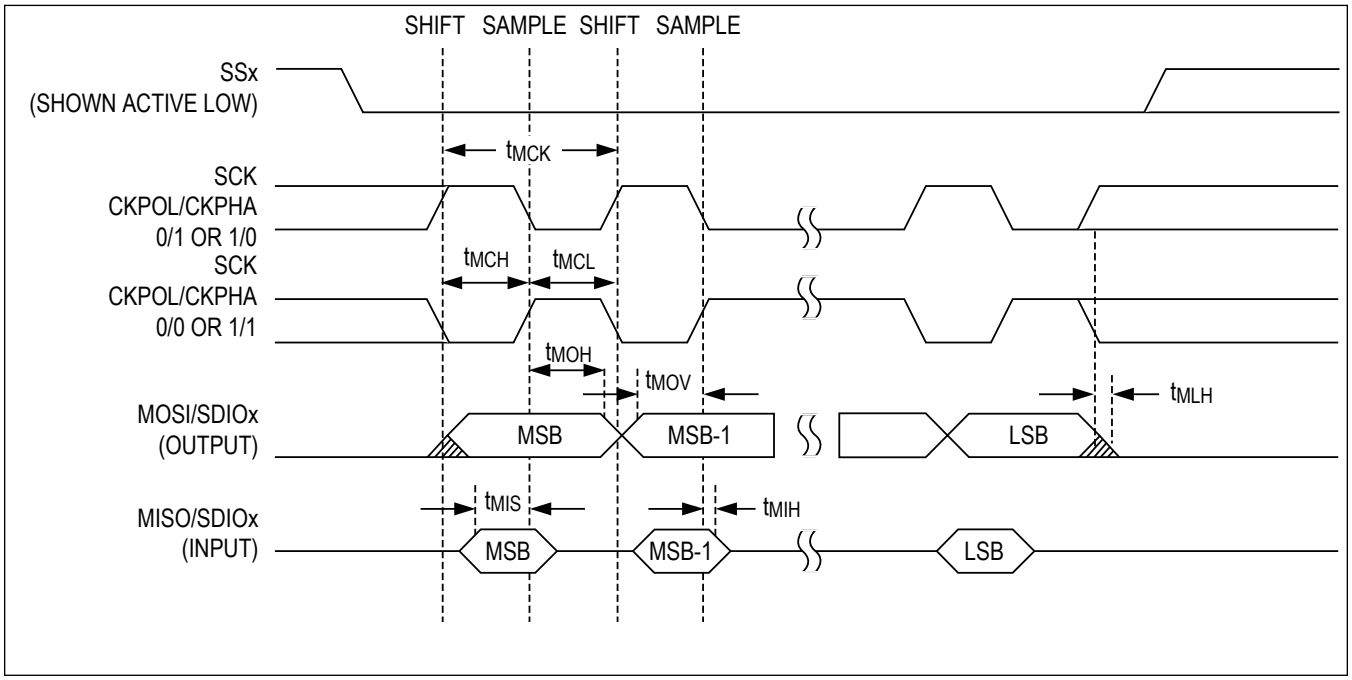


Figure 1. SPI Master Mode Timing Diagram

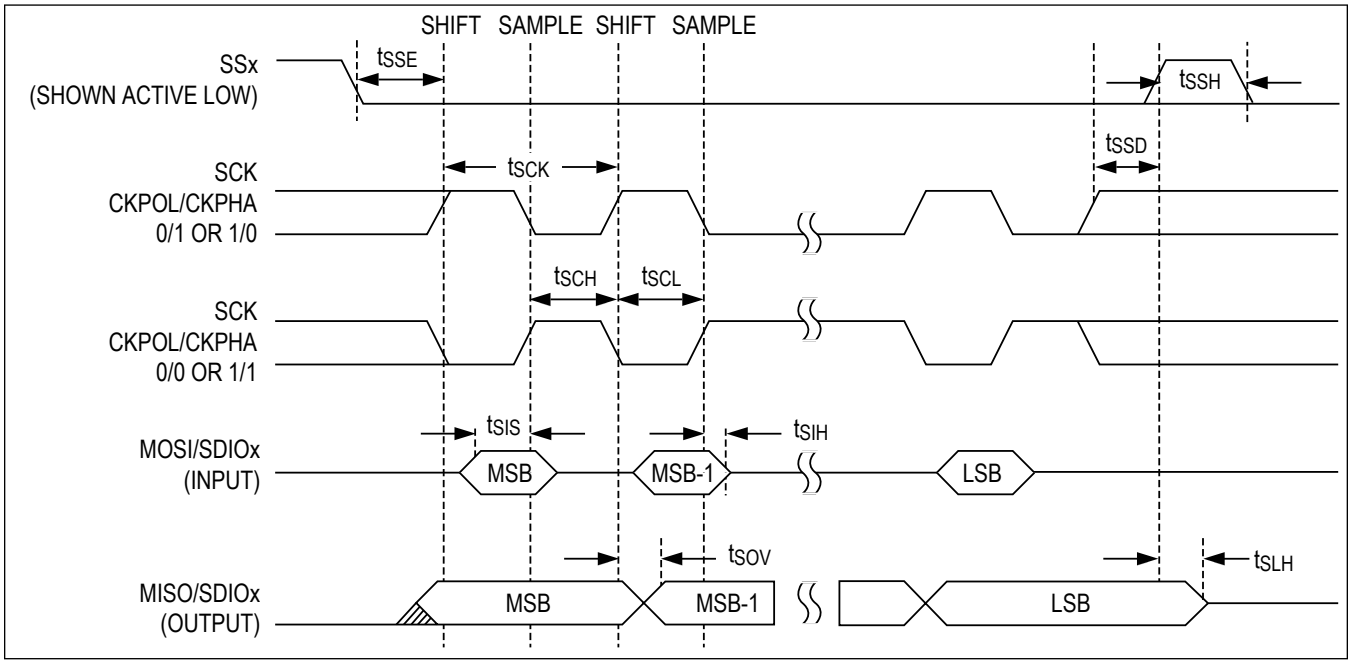


Figure 2. SPI Slave Mode Timing Diagram

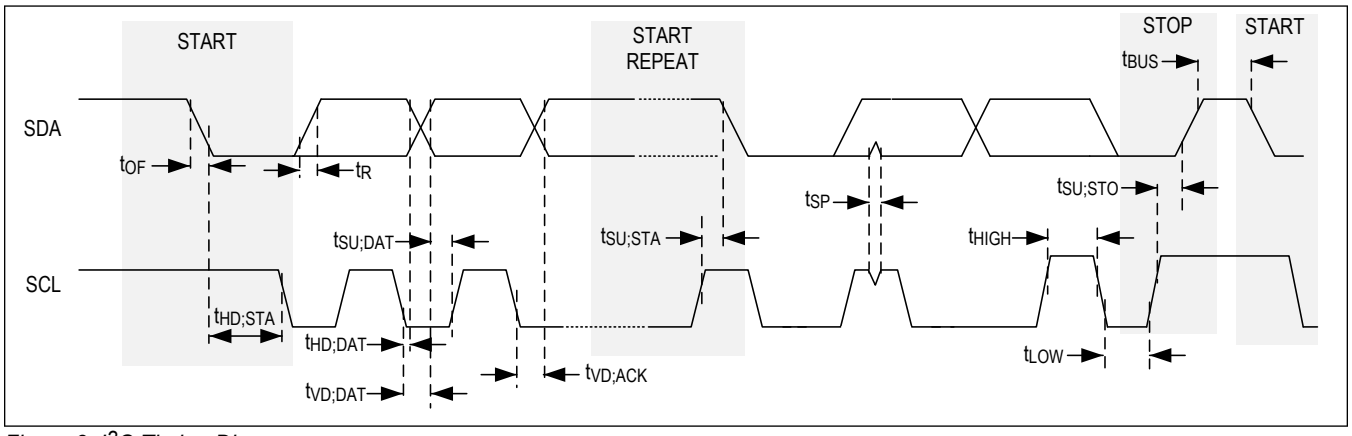


Figure 3. I²C Timing Diagram

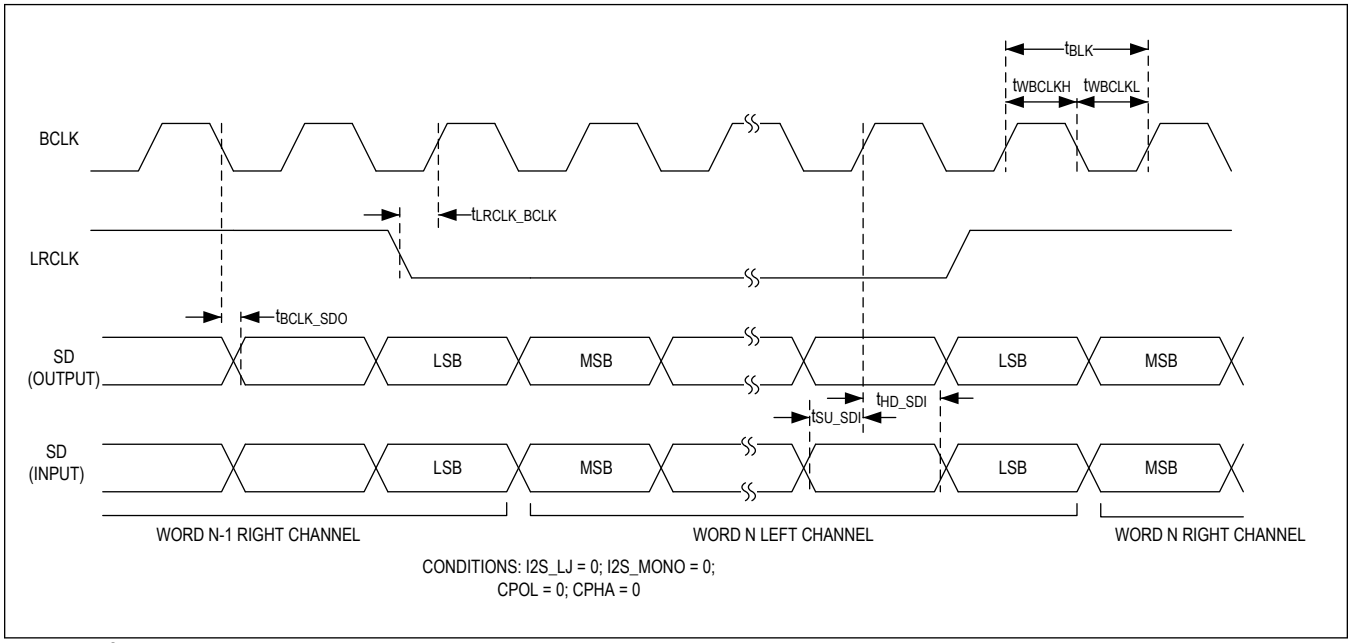


Figure 4. I²S Timing Diagram

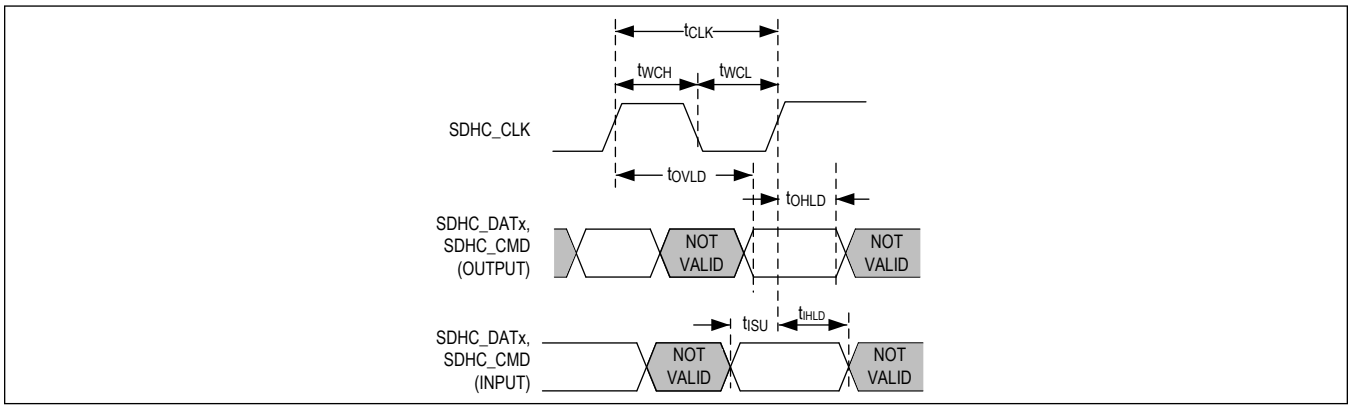


Figure 5. SD/SDIO/SDHC/MMC Timing Diagram

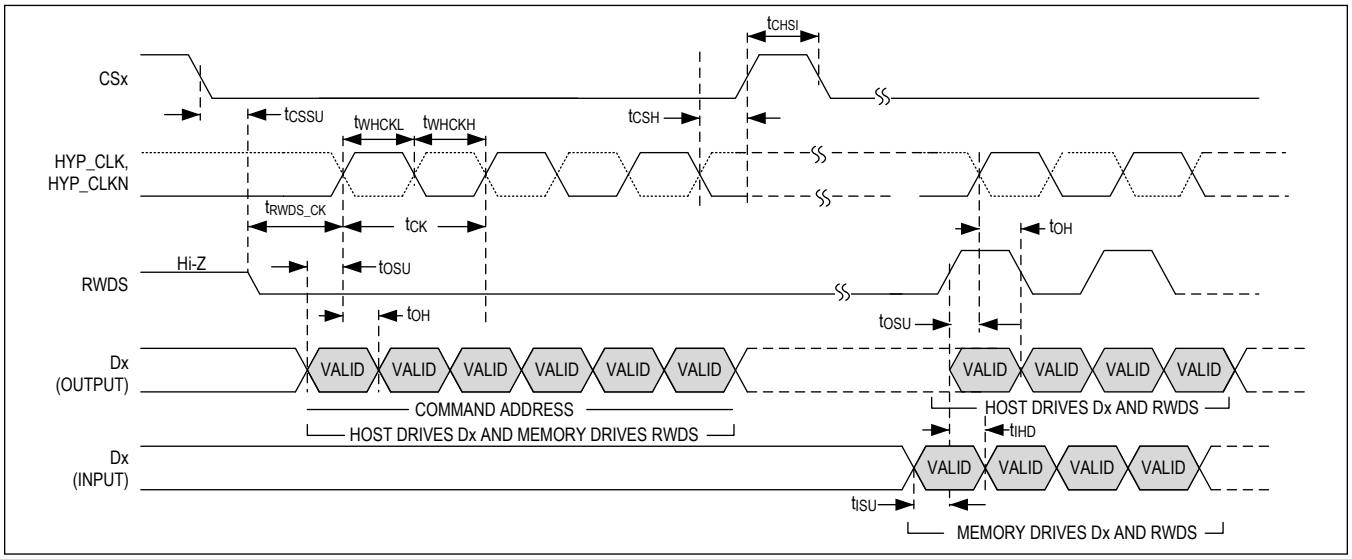


Figure 6. HyperBus/Xccela Bus Timing Diagram

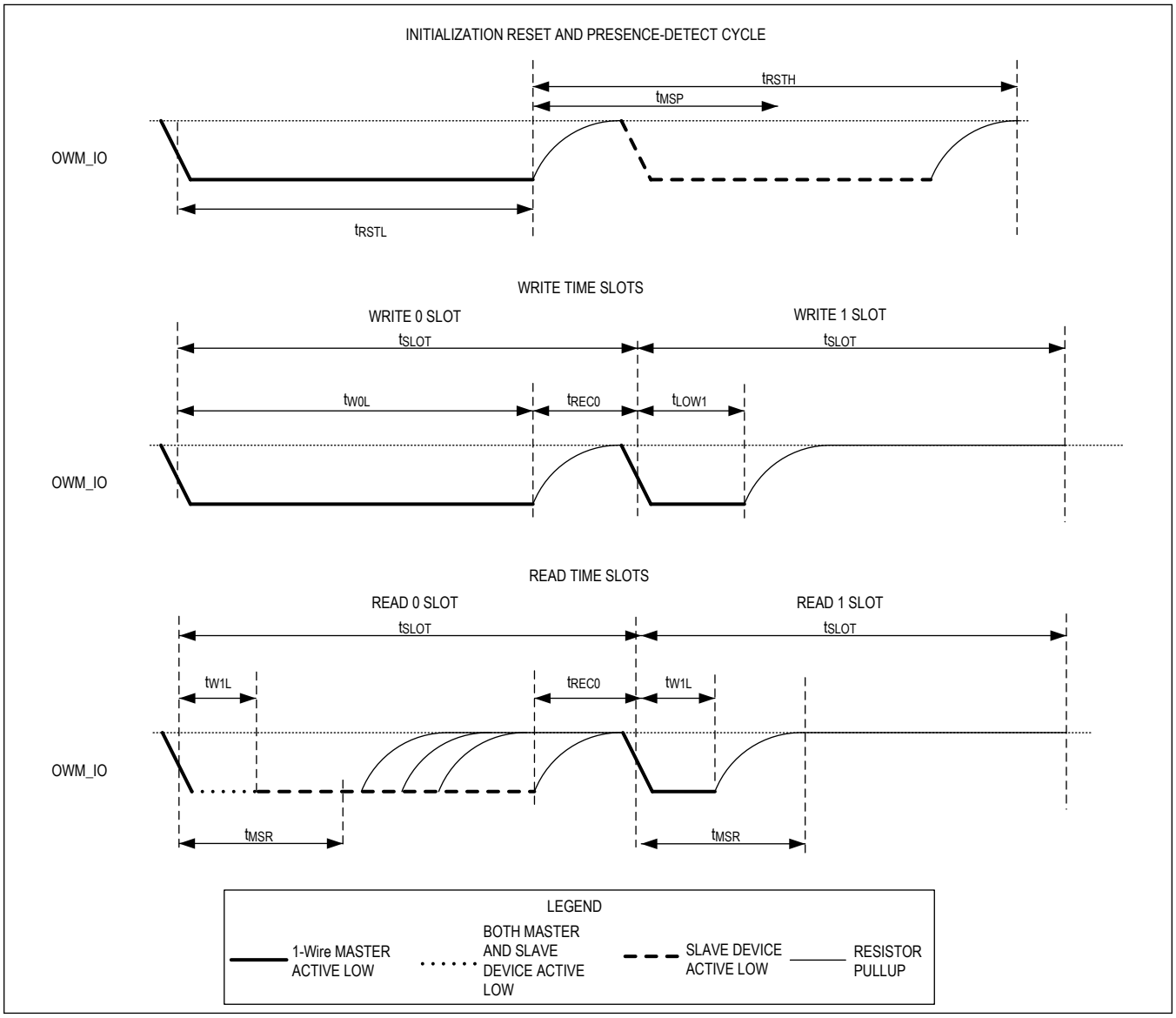
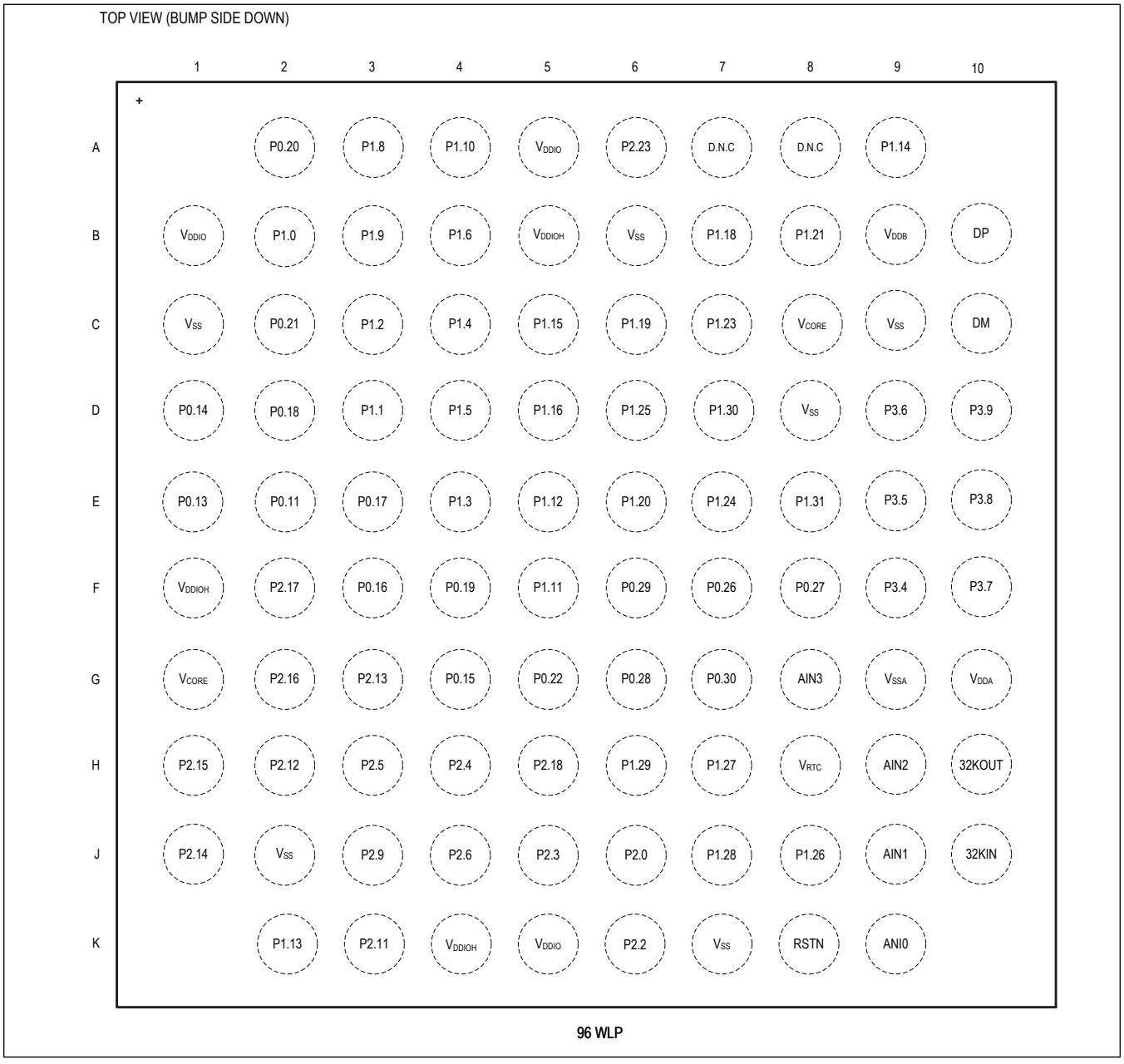


Figure 7. 1-Wire Master Data Timing Diagram

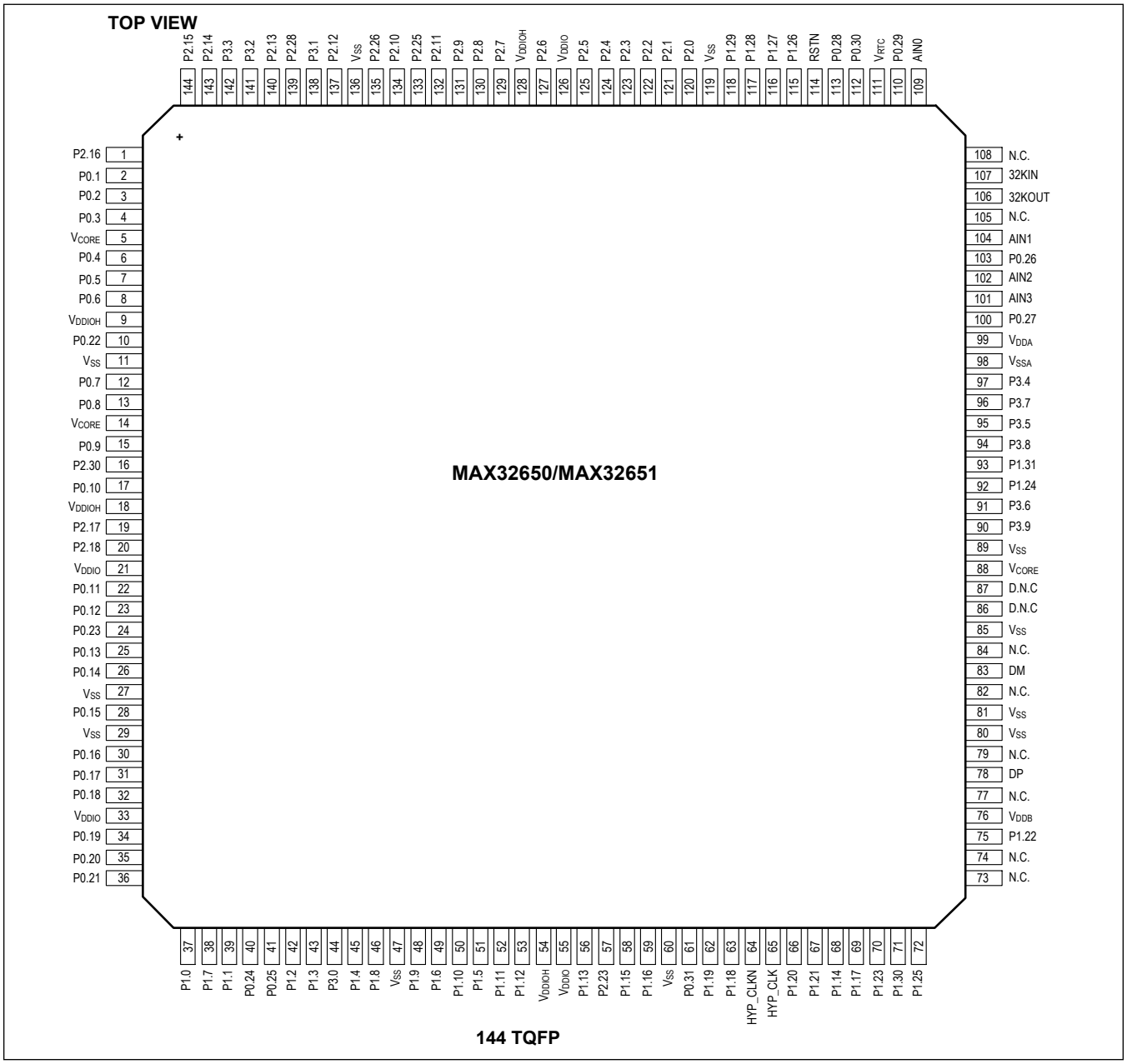
Pin Configurations

140 WLP

96 WLP


TOP VIEW (BUMP SIDE DOWN)
1 2 3 4 5 6 7 8 9 10
A P0.20 P1.8 P1.10 VDDIO P2.23 D.N.C D.N.C P1.14
B VDDIO P1.0 P1.9 P1.6 VDDIOH VSS P1.18 P1.21 VDDB DP
C VSS P0.21 P1.2 P1.4 P1.15 P1.19 P1.23 VCORE VSS DM
D P0.14 P0.18 P1.1 P1.5 P1.16 P1.25 P1.30 VSS P3.6 P3.9
E P0.13 P0.11 P0.17 P1.3 P1.12 P1.20 P1.24 P1.31 P3.5 P3.8
F VDDIOH P2.17 P0.16 P0.19 P1.11 P0.29 P0.26 P0.27 P3.4 P3.7
G VCORE P2.16 P2.13 P0.15 P0.22 P0.28 P0.30 AIN3 VSSA VDDA
H P2.15 P2.12 P2.5 P2.4 P2.18 P1.29 P1.27 VRTC AIN2 32KOUT
J P2.14 VSS P2.9 P2.6 P2.3 P2.0 P1.28 P1.26 AIN1 32KIN
K P1.13 P2.11 VDDIOH VDDIO P2.2 VSS RSTN ANI0
96 WLP

144 TQFP



Pin Description

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
POWER				
H1, H4, D12	G1, C8	5, 14, 88	V_{CORE}	Core Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
H11	G10	99	V_{DDA}	1.8V Analog Supply Voltage. This pin must be bypassed to V_{SSA} with 1.0µF and 0.01µF capacitors as close as possible to the package.
B11	B9	76	V_{DDB}	USB Transceiver Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
A7	A5	21	V_{DDIO}	GPIO Supply Voltage. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
E4, F1	B1, K5	33, 55		GPIO Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF and a 0.01µF capacitor as close as possible to the package.
M7	—	126		GPIO Supply Voltage. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
A6	B5	9	V_{DDIOH}	GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
G1	F1	18		GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. This pin must be bypassed to V_{SS}.
G4, M6	K4	54, 128		GPIO Supply Voltage, High. $V_{DDIOH} \geq V_{DDIO}$. This pin must be bypassed to V_{SS} with 1.0µF and 0.01µF capacitors as close as possible to the package.
M11	H8	111	V_{RTC}	RTC Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package.
A4, A8, C11, D1, D11, F4, J1, M4, M9	B6, C1, C9, D8, K7, J2	11, 27, 29, 47, 60, 80, 81, 85, 89, 119, 136	V_{SS}	Digital Ground
H12	G9	98	V_{SSA}	Analog Ground
RESET				
L10	K8	114	RSTN	External System Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin has an internal pullup to the V_{DDIO} supply.
CLOCK				
L12	J10	107	32KIN	32kHz Crystal Oscillator Input. Connect a 32kHz crystal between 32KIN and 32KOUT for RTC operation. Refer to the *MAX32650–MAX32652 User Guide* for determination of the required external stability capacitors. Optionally, an external clock source can be driven on 32KIN if the 32KOUT pin is left unconnected.
K12	H10	106	32KOUT	32kHz Crystal Oscillator Output. Refer to the *MAX32650–MAX32652 User Guide* for determination of the required external stability capacitors.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
GPIO AND ALTERNATE FUNCTIONS				
F5	—	—	P0.0	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
L2	—	2	P0.1	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K3	—	3	P0.2	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
L1	—	4	P0.3	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J3	—	6	P0.4	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K2	—	7	P0.5	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K1	—	8	P0.6	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
H3	—	12	P0.7	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
H2	—	13	P0.8	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G3	—	15	P0.9	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G2	—	17	P0.10	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
F2	E2	22	P0.11	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
F3	—	23	P0.12	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E2	E1	25	P0.13	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E3	D1	26	P0.14	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
D2	G4	28	P0.15	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C1	F3	30	P0.16	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C2	E3	31	P0.17	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
D3	D2	32	P0.18	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B1	F4	34	P0.19	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C3	A2	35	P0.20	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B2	C2	36	P0.21	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J2	G5	10	P0.22	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E1	—	24	P0.23	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
A2	—	40	P0.24	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B3	—	41	P0.25	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J10	F7	103	P0.26	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
H10	F8	100	P0.27	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K10	G6	113	P0.28	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G10	F6	110	P0.29	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
F10	G7	112	P0.30	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
F8	—	61	P0.31	General-Purpose I/O, Port 0. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
D4	B2	37	P1.0	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C4	D3	39	P1.1	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
D5	C3	42	P1.2	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C5	E4	43	P1.3	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B4	C4	45	P1.4	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
A5	D4	51	P1.5	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B5	B4	49	P1.6	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E5	—	38	P1.7	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E6	A3	46	P1.8	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
D6	B3	48	P1.9	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C6	A4	50	P1.10	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B6	F5	52	P1.11	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C7	E5	53	P1.12	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
B7	K2	56	P1.13	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
A11	A9	68	P1.14	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C8	C5	58	P1.15	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B8	D5	59	P1.16	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E9	—	69	P1.17	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B9	B7	63	P1.18	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C9	C6	62	P1.19	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
C10	E6	66	P1.20	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
B10	B8	67	P1.21	General-Purpose I/O, Port 1. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
—	—	75	P1.22	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
F9	C7	70	P1.23	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
H9	E7	92	P1.24	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G9	D6	72	P1.25	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
M10	J8	115	P1.26	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J9	H7	116	P1.27	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K9	J7	117	P1.28	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
L9	H6	118	P1.29	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
D10	D7	71	P1.30	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E10	E8	93	P1.31	General-Purpose I/O, Port 1. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G8	J6	120	P2.0	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
H8	—	121	P2.1	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
M8	K6	122	P2.2	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
L8	J5	123	P2.3	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K8	H4	124	P2.4	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J8	H3	125	P2.5	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
L7	J4	127	P2.6	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K7	—	129	P2.7	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J7	—	130	P2.8	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
L6	J3	131	P2.9	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
L5	—	134	P2.10	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
M5	K3	132	P2.11	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
L4	H2	137	P2.12	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J5	G3	140	P2.13	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K4	J1	143	P2.14	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
H5	H1	144	P2.15	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J4	G2	1	P2.16	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G7	F2	19	P2.17	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
F7	H5	20	P2.18	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details. This device pin has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.
D7	—	—	P2.19	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E7	—	—	P2.20	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E8	—	—	P2.21	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
D9	—	—	P2.22	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
D8	A6	57	P2.23	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
H7	—	—	P2.24	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K6	—	133	P2.25	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
J6	—	135	P2.26	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
H6	—	—	P2.27	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
K5	—	139	P2.28	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details. This device pin has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.
G5	—	—	P2.29	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G6	—	16	P2.30	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
F6	—	—	P2.31	General-Purpose I/O, Port 2. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
A3	—	44	P3.0	General-Purpose I/O, Port 3. Most port pins have multiple special functions. This pin is connected to V_{DDIO} only. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
M3	—	138	P3.1	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
L3	—	141	P3.2	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
M2	—	142	P3.3	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G11	F9	97	P3.4	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
F11	E9	95	P3.5	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.

Pin Description (continued)

PIN			NAME	FUNCTION
140 WLP	96 WLP	144 TQFP		
E11	D9	91	P3.6	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
G12	F10	96	P3.7	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
F12	E10	94	P3.8	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
E12	D10	90	P3.9	General-Purpose I/O, Port 3. Most port pins have multiple special functions. See Table 4, Table 5 and Table 6 GPIO and Alternate Function Matrix tables for details.
ANALOG INPUT PINS				
L11	K9	109	AIN0	ADC Input 0. 5V-tolerant input.
K11	J9	104	AIN1	ADC Input 1. 5V-tolerant input.
J11	H9	102	AIN2	ADC Input 2
J12	G8	101	AIN3	ADC Input 3
HyperBus CLOCKS				
A10	—	65	HYP_CLK	HyperBus Positive Clock
A9	—	64	HYP_CLKN	HyperBus Negative Clock
USB				
C12	C10	83	DM	USB DM Signal. This bidirectional pin carries the negative differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
B12	B10	78	DP	USB DP Signal. This bidirectional pin carries the positive differential data or single-ended data. This pin is weakly pulled high internally when the USB is disabled.
NO CONNECT				
—	A7, A8	86, 87	D.N.C.	Do Not Connect. Internally connected. Do not make any electrical connection to this pin, including power supply grounds.
—	—	73, 74, 77, 79, 82, 84, 105, 108	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX32650–MAX32652 are low-power, mixed-signal microcontrollers based on the Arm Cortex-M4 with FPU CPU, operating at a maximum frequency of 120MHz. The devices feature five powerful and flexible power modes. A SmartDMA performs complex background processing on data being transferred, from simple arithmetic to multiply/accumulate, while the CPU is off. This function dramatically reduces overall power consumption compared to conventional solutions. This allows, for example, an external display to be refreshed while most of the chip is powered off. Built-in dynamic clock gating and firmware-controlled power gating allows the user to optimize power for the specific application.

Application code executes from an onboard 3MB program flash memory, with 1MB SRAM available for general application use. A 16KB cache improves execution throughput. Additionally, a SPI execute in place (XIP) external memory interface allows application code and data (up to 128MB) to be accessed from an external SPI flash and/or SRAM memory device.

A 10-bit delta-sigma ADC is provided with a multiplexer front end for four external input channels (two of which are 5V tolerant) and six internal power supply monitoring channels. Dedicated divided supply input channels allow direct monitoring of internal power supply voltages by the ADC. Built-in limit monitors allow converted input samples to be compared against user-configurable high and low limits, with an option to trigger an interrupt and wake the CPU from a low-power mode if attention is required.

A wide variety of communications and interface peripherals are provided, including a Hi-Speed USB 2.0 device interface, three master/slave SPI interfaces, one QuadSPI master/slave interface, three UART interfaces with flow control support, two master/slave I^2C interfaces, I^2S bidirectional slave interface. A Cypress Spansion HyperBus interface and a Xccela bus interface provides support for HyperFlash, HyperRAM, and Xccela PSRAM operating up to 120MB/s throughput with access up to 512MB. A SD/SDIO/MMC interface running up to 60MB/s supporting media file storage. A 24-bit TFT LCD controller provides color and monochrome display support.

The MAX32651 is a secure version of the MAX32650. It provides a trust protection unit (TPU) with encryption and advanced security features. These features include a modular arithmetic accelerator (MAA) for fast ECDSA and RSA-4096 computation. A hardware AES engine uses 128/192/256-bit keys. A memory decryption integrity unit (MDIU) provides on-the-fly code or data decryption stored in external flash. A hardware TRNG and a hardware SHA-256 HASH function are also provided. A secure bootloader authenticates applications before they are allowed to execute and update firmware with confidentiality.

The MAX32652 is a high-density, 0.35mm pitch, 140-bump WLP targeted for tiny form factor products that require high I/O counts.

Arm Cortex-M4 with FPU

The Arm Cortex-M4 with FPU combines high-efficiency signal processing functionality with flexible low-power operating modes. The features of this implementation of the familiar Arm Cortex-M4 architecture include:

- Floating point unit (FPU)
- Memory protection unit
- Multilayer, 32-bit AHB matrix
- Full debug support level
  - Debug access port (DAP)
  - Breakpoints
  - Flash patch
  - Halting debug
  - Development and debug interface
- NVIC support
  - Programmable IRQ generation for each interrupt source
  - Unique vectors for each interrupt channel
  - 8 programmable priority levels support nesting and preemption
  - External GPIO interrupts grouped by GPIO port

- DSP supports single instruction multiple data (SIMD) path DSP extensions, providing:
  - 4 parallel 8-bit add/sub
  - 2 parallel 16-bit add/sub
  - 2 parallel MACs
  - 32- or 64-bit accumulate
  - Signed, unsigned, data with or without saturation

Memory

Internal Flash Memory

3MB of internal flash memory provides nonvolatile storage of program and data memory.

Flash can be expanded through the SPIXF flash serial interface backed by 16KB of cache. The SPIXF flash interface can address an additional 128MB.

Internal SRAM

The internal 1MB SRAM provides low-power retention of application information in all power modes except shutdown. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data retention feature is optional and configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

SRAM can be expanded through the SPIXR SRAM serial interface backed by 16KB of cache. The SPIXR SRAM interface can address an additional 512MB.

Secure Digital Interface

The secure digital interface (SDI) provides high-speed, high-density data storage capability for media files and large long-term data logs. This interface supports eMMC, SD, SDHC, and SDXC memory devices at transfer rates up to 60MB/s. The 7-pin interface (4 data, 1 clock, 1 command, 1 write-protect) supports the following specifications:

• SD Host Controller Standard Specification Version 3.00

• SDIO Card Specification Version 3.0

• SD Memory Card Specification Version 3.01

• SD Memory Card Security Specification Version 1.01

• MMC Specification Version 4.51

Spansion HyperBus/Xccela Bus

The Spansion HyperBus/Xccela bus interface provides access to external Cypress Spansion HyperBus and Xccela bus memory products both SRAM and/or flash. This interface provides a means of high-speed execution from external SRAM or flash allowing system expansion when internal memory resources are insufficient. Up to 512MB SRAM or 512MB flash at a speed of up to 60MHz or 120MB/s is supported. It is a high-speed low-pin count interface that is memory-mapped into the CPU memory space making access to this external memory as easy as accessing on-chip RAM. Data is transferred over a high-speed, 8-bit bus. Slave memory devices are selected with two chip selects. HyperBus transfers are clocked using a differential clock while Xccela bus transfers use a single-ended clock. This interface supports 1.8V operation only.

Features of the HyperBus/Xccela bus interface include:

- Master/slave system
- 120MB/s maximum data transfer rate
- Double data rate (DDR): two data transfers per clock cycle
- Transparent bus operation to the processor
- 16KB write-through cache
- Two chip selects for two memory ports

  - Each port supports memories up to 512MB
- Addresses two external memories, one at a time
- Interfaces to HyperFlash, HyperRAM, and Xccela PSRAM
- Zero wait state burst mode operation
- Low-power half sleep mode
  - Puts the external memory device into low-power mode while retaining memory contents
- Configurable timing parameters

Clocking Scheme

The high-frequency oscillator operates at a maximum frequency of 120MHz.

Optionally, four other oscillators can be selected depending upon power needs:

- 50MHz low-power oscillator
- 8kHz nanoring oscillator
- 32.768kHz oscillator (external crystal required)
- 7.3728MHz oscillator

This clock is the primary clock source for the digital logic and peripherals. Select the 7.3728MHz internal oscillator to optimize active power consumption. Using the 7.3727MHz oscillator allows UART communications to meet a ±2% baud rate tolerance.

Wake-up is possible from either the 7.3728MHz internal oscillator or the high-frequency oscillator. The device exits power-on reset using the the 50MHz oscillator.

An external 32.768kHz timebase is required when using the RTC.

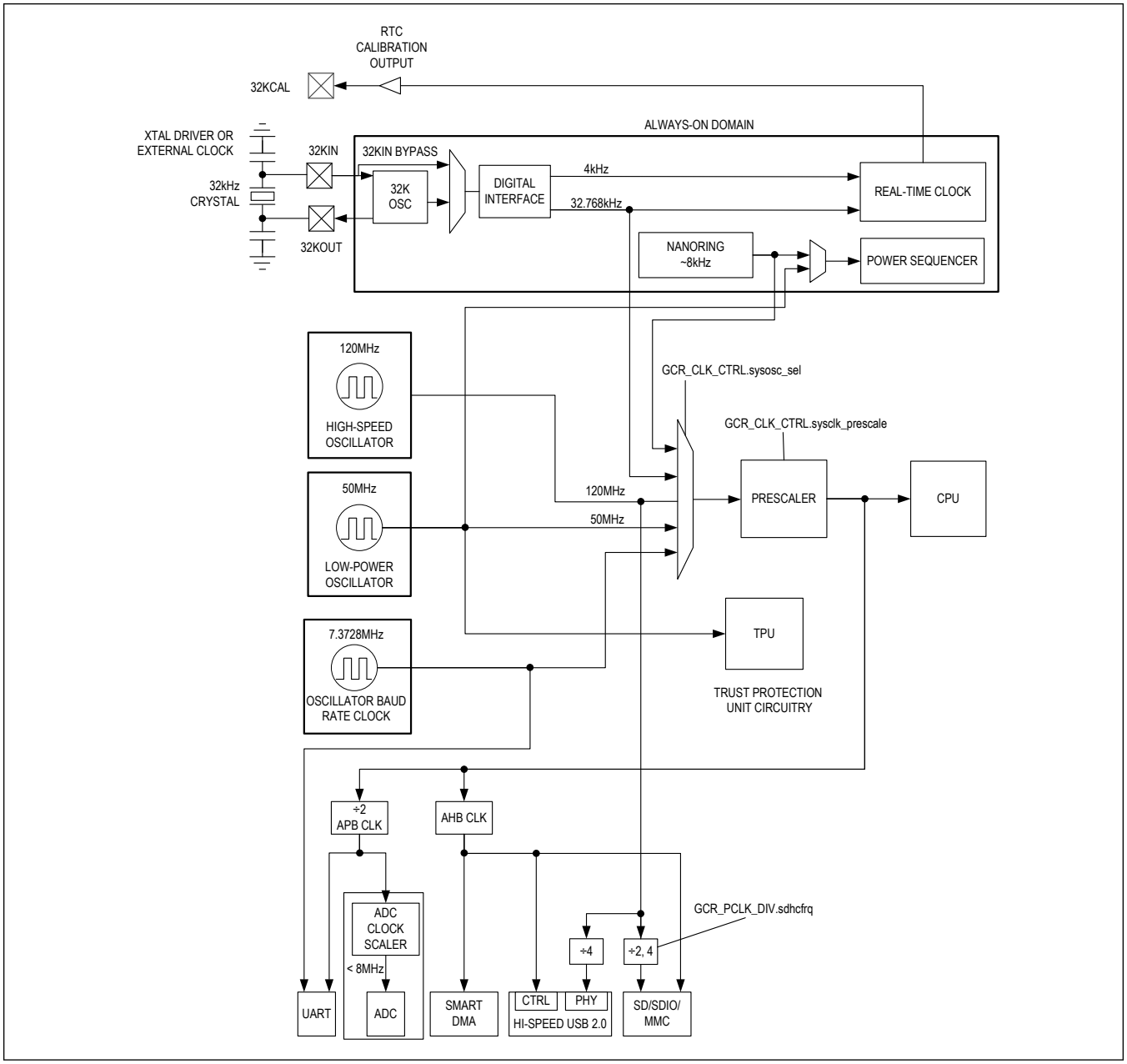


Figure 8. Clocking Scheme Diagram

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more special function signals associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Though this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the electrical characteristics tables.

In GPIO mode, pins are logically divided into ports of 32 pins. Each pin of a port has an interrupt function that can be

independently enabled, and configured as a level- or edge-sensitive interrupt. All GPIOs of a given port share the same interrupt vector. Some packages do not have all of the GPIOs available.

When configured as GPIO, the following features are provided. The features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32650–MAX32652 provides up to 105 GPIO (140 WLP), 97 GPIO (144 TQFP), and 67 GPIO (96 WLP).

GPIOs, which have any HyperBus alternate functionality (P1.[21:18], P1.[16:11], P3.0), can only be used with the V_{DDIO} supply, whether used as a GPIO or any alternate function.

Standard DMA Controller

The Standard DMA (direct memory access) controller provides a means to off-load the CPU for memory/peripheral data transfer leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources.

The following transfer modes are supported:

- 16 channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

SmartDMA Controller

The SmartDMA controller provides low-power memory/peripheral access control that can run data collection tasks and perform complex background processing on data being transferred, from simple arithmetic to multiply/accumulate, while the CPU is off, significantly reducing power consumption (Background mode). The SmartDMA controller allows peripherals on the AHB to access main system memory (SRAM) independent of the CPU. It is configured through the APB and can configure itself through the AHB-to-APB bridge. The SmartDMA engine runs code from system SRAM. If desired, custom SmartDMA algorithms supporting data post-processing can be developed by the user.

Key features:

- Dedicated 32-bit controller with general-purpose timer
- APB read access to the SmartDMA registers
- Configurable start IP address
- Selects 32 interrupts from peripherals from a total of 80 available interrupts to initiate DMA operations
- Global enable (SDMA_EN) keeps SmartDMA in reset except APB interface
- Synchronous interrupt output to CPU

Analog-to-Digital Converter

The 10-bit delta-sigma ADC provides an integrated reference generator and a single-ended input multiplexer. The multiplexer selects an input channel from either the external analog input signals (AIN0, AIN1, AIN2, and AIN3) or the internal power supply inputs. AIN0 and AIN1 are 5V tolerant, making them suitable for monitoring batteries. An internal 1.22V bandgap or the V_{DDA} analog supply can be chosen as the ADC reference.

An optional feature allows samples captured by the ADC to be automatically compared against user-programmable high and low limits. Up to four channel limit pairs can be configured in this way. The comparison allows the ADC to trigger an interrupt (and potentially wake the CPU from a low-power sleep mode) when a captured sample goes outside the

preprogrammed limit range. Since this comparison is performed directly by the sample limit monitors, it can be performed even while the main CPU is suspended in a low-power mode.

The ADC measures:

- AIN[3:2] (up to 3.3V)
- AIN[1:0] (up to 5.5V)
- V_{CORE}
- V_{DD18}
- V_{DDB}
- V_{RTC}
- V_{DDIO}
- V_{DDIOH}

Power Management

Power Management Unit

The power management unit (PMU) provides high-performance operation while minimizing power consumption. It exercises intelligent, precise control of power distribution to the CPU and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple clock domains
- Fast wake-up of powered-down peripherals when activity detected

Active Mode

In this mode, the CPU is executing application code and all digital and analog peripherals are available on demand. Dynamic clocking disables peripherals not in use, providing the optimal mix of high performance and low power consumption.

Sleep Mode

This mode allows for low power consumption, but a faster wake-up because the clocks can optionally be enabled. The CPU is asleep, peripherals are on, and the standard and SmartDMA blocks are available for optional use. The GPIO or any active peripheral interrupt can be configured to interrupt and cause transition to the Active mode.

Background Mode

This mode is suitable for running the SmartDMA engine to collect and move data from enabled peripherals. The CPU is in its Deep-sleep mode. Memory retention is configurable. The SmartDMA engine can access the SPI, UARTS, I^2C, 1-Wire, timers, pulse train engines, and the secure digital interface as well as SRAM. The transition from Background to Active mode is faster than the transition from Backup mode because system initialization is not required. There are four sources from which Background mode can be exited to return to Active mode: RTC interrupt, GPIO interrupt, USB interrupt, or RSTN assertion.

Deep-Sleep Mode

This mode corresponds to the Arm Cortex-M4 with FPU Deep-Sleep mode. In this mode, the register settings and all volatile memory is preserved. The GPIO pins retain their state in this mode. The transition from Deep-Sleep to Active mode is faster than the transition from Backup mode because system initialization is not required.

The high-speed oscillator that generates the 120MHz system clock can be shut down to provide additional power savings over Sleep or Background modes.

There are four sources from which Background mode can be exited to return to Active mode: RTC interrupt, GPIO interrupt, USB interrupt, or RSTN assertion.

Backup Mode

This mode places the CPU in a static, low-power state that supports a fast wake-up to Active mode feature. In Backup mode, all of the SRAM can be retained with restrictions depending upon which supply is used to support this mode. Data retention in this mode can be maintained using only the V_{CORE} or V_{RTC} supplies. Optionally, the V_{CORE} voltage input can be turned off at its source and an internal retention regulator can be enabled to power the state so that the V_{RTC} voltage input is all that is required for mode operation including the RTC.

If the V_{RTC} supply is used, then either 32KB or 96KB of SRAM can be retained and all GPIO can be retained. If the V_{CORE} supply is subsequently turned on then the power mode will wake to the Active state.

If the V_{CORE} supply is used, then either 32KB, 96KB, or 1024KB of SRAM can be retained and all GPIO can be retained.

There are four sources from which Background mode can be exited to return to Active mode: RTC interrupt, GPIO interrupt, USB interrupt, or RSTN assertion.

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 subsecond alarm can be programmed between 244µs and 1s. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low-power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

The RTC calibration feature provides the ability for user-software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the 32KCAL alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

CRC Module

A cyclic redundancy check (CRC) hardware module provides fast calculations and data integrity checks by application software. The CRC module supports the following polynomials:

- CRC-16-CCITT
- CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$)

Programmable Timers

32-Bit Timer/Counter/PWM (TMR)

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating or capture
- Timer output pin
- Timer interrupt

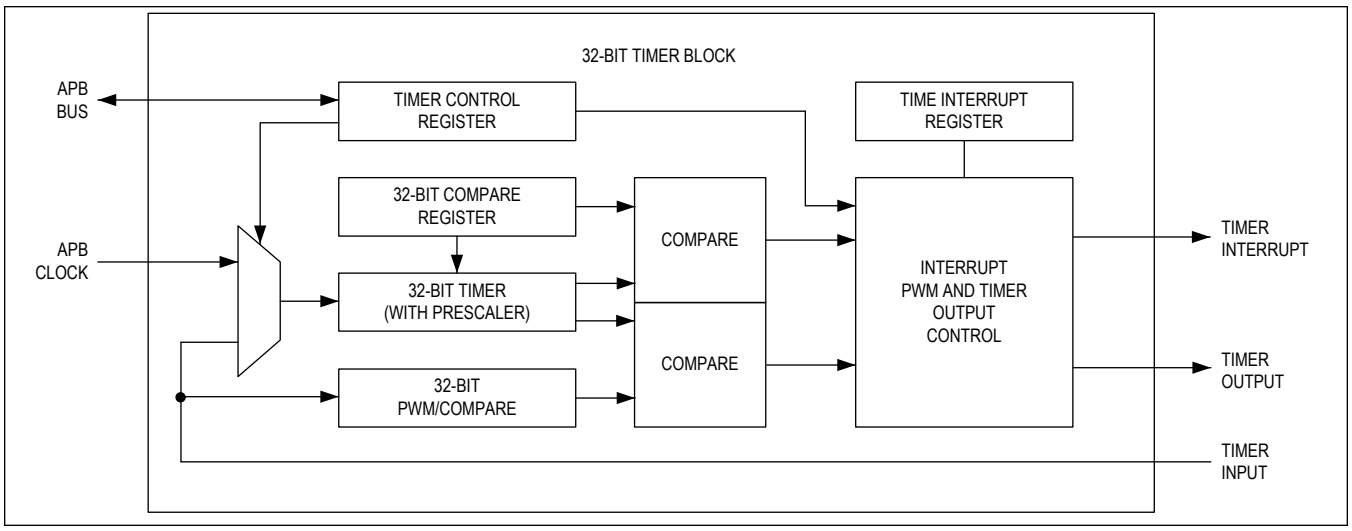


Figure 9. 32-Bit Timer

The MAX32650–MAX32652 provides six instances of the general-purpose 32-bit timer (TMR0–TMR5).

Pulse Train Engine (PT)

Multiple, independent pulse train generators can provide either a square wave or a repeating pattern from 2 to 32 bits in length. Any single pulse train generator or any desired group of pulse train generators can be synchronized at the bit level allowing for multibit patterns. Each pulse train generator is independently configurable.

The pulse train generators provide the following features:

- Independently enabled
- Safe enable and disable for pulse trains without bit banding
- Multiple pin configurations allow for flexible layout
- Pulse trains can be started/synchronized independently or as a group
- Frequency of each enabled pulse train generator is also set separately, based on a divide down (divide by 2, divide by 4, divide by 8, and so on) of the input pulse train module clock
- Multiple repetition options
  - Single shot (nonrepeating pattern of 2 to 32 bits)
  - Pattern repeats user-configurable number of times or indefinitely
  - Termination of one pulse train loop count can restart one or more other pulse trains

The pulse train engine feature is an alternate function associated with a GPIO pin. In most cases, enabling the pulse train engine function supersedes the GPIO function.

The MAX32650–MAX32652 provide up to 16 instances of the pulse train engine peripheral (PT[15:0]).

Serial Peripherals

Serial Peripheral Interface

The serial peripheral interface (SPI) is a highly configurable, flexible, and efficient synchronous interface between multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals, and one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and provide the following features:

- SPI modes 0, 1, 2, 3 for single-bit communication

- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Dual and quad data modes supported
- Multiple slave select lines on some instances
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and deassertion timing with respect to leading/trailing SCK edge

The MAX32650–MAX32652 provide four instances of the SPI peripheral (SPI0, SPI1 and SPI2, SPI3) in accordance with the specifications shown in Table 1:

Table 1. SPI Configuration Options

INSTANCE	DATA	SLAVE SELECT LINES			MAXIMUM FREQUENCY (MASTER MODE) (MHz)	MAXIMUM FREQUENCY (SLAVE MODE) (MHz)
		144 TQFP	140 WLP	96 WLP		
SPI0	3-wire, 4-wire	1	1	0	60	48
SPI1	3-wire, 4-wire	4	4	4	60	48
SPI2	3-wire, 4-wire	4	4	3	60	48
SPI3	3-wire, 4-wire, dual, or quad data support	4	4	4	60	48

I²S Interface

The I²S interface is a bidirectional, three-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I²S Bus Specification, June 5, 1996. It provides the following features:

- Slave mode operation
- Normal and left-justified data alignment
- 16-bit audio transfer
- Wake-up on FIFO status (full/empty/threshold)
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The MAX32650–MAX32652 provide one instance of the I²S peripheral that is multiplexed with the SPI2 peripheral.

USB Controller

The integrated USB device controller is compliant with the Hi-Speed (480Mbps) USB 2.0 specification. The integrated USB physical interface (PHY) reduces board space and system cost. An integrated voltage regulator enables smart switching between the main supply and V_{DDB} when connected to a USB host controller.

- Supports DMA for the endpoint buffers. A total of 12 endpoint buffers are supported with configurable selection of IN or OUT in addition to endpoint 0.
- Isochronous, bulk, interrupt, and control transfers
- Automatic packet splitting and combining
- FIFOs up to 4096 bytes deep
- Double packet buffering
- USB 2.0 test mode support

I²C Interface

The I²C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many or many-to-many communications medium. Two I²C master/slave interface to a

wide variety of I2C-compatible peripherals. These engines support standard mode, fast mode, and fast mode plus I2C speeds. It provides the following features:

- Master or slave mode operation
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive Receive mode
- Tx FIFO Preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1000kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX32650–MAX32652 provide two instances of the I2C peripheral (I2C0 and I2C1).

UART

The universal asynchronous receiver-transmitter (UART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry standard request to send (RTS) and clear to send (CTS) flow control signaling. Each UART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 32-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, RX FIFO overrun and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- Baud rate generation with ±2% optionally utilizing the 7.3727MHz oscillator baud rate clock
- Maximum baud rate 4000kB
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32650–MAX32652 provide three instances of the UART peripheral (UART0, UART1, and UART2) according to the specifications in Table 2:

Table 2. UART Configuration Options

INSTANCE	FLOW CONTROL			MAXIMUM BAUD RATE (kb)
	144 TQFP	140 WLP	96 WLP	
UART0	Yes	Yes	No	4000
UART1	Yes	Yes	Yes	4000
UART2	Yes	Yes	No	4000

Serial Peripheral Interface Execute in Place (SPIX) Master

There are two SPI execute-in-place master interfaces. One for SRAM (SPIXR) and one for flash (SPIXF) with dedicated slave selects. This feature allows the CPU to transparently execute instructions stored in an external SPI memory device.

Instructions fetched through the SPI master are cached just like instructions fetched from internal program memory. The SPI SRAM master provides write-back capability. These two SPI execute in place master interfaces can also be used to access large amounts of external static data that would otherwise reside in internal data memory.

1-Wire Master

Maxim's 1-Wire bus consists of a single line to provide both power and data communications and a ground return. The bus supports a serial, multidrop communication protocol between a master and one or more slave devices with the minimum amount of interconnection.

Maxim's 1-Wire bus consists of one signal that carries data and also supplies power to the slave devices, and a ground return. The bus master communicates serially with one or more slave devices through the bidirectional, multidrop 1-Wire bus. The single contact serial interface is ideal for communication networks requiring minimal interconnection.

The provided 1-Wire master supports the following features:

- Single contact for control and operation
- Unique factory identifier for any 1-Wire device
- Multiple device capability on a single line

The MAX32650–MAX32652 1-Wire master supports both the standard (15.6kbps) and overdrive (110kbps) speeds.

24-Bit Color TFT Controller

The 24-bit color TFT controller is controlled by the CPU through the APB and fed graphic data through the AHB. The controller supports the following display types:

- Active matrix TFT panels with up to 24-bit bus interface
- Single/dual-panel monochrome STN panels (4-bit and 8-bit bus interfaces)
- Single/dual-panel color STN panels, 8-bit bus interface
- TFT panels up to 24 bpp, direct 8:8:8 RG
- Color STN panels up to 16bpp, direct 5:5:5 with one bit not being used
- Mono STN panels up to 4bpp, pelletized, 16 gray scales selected from 16

The controller can be programmed to operate a wide range of panel resolutions (including but not limited to the following settings):

- 320 x 200, 320 x 240
- 640 x 200, 640 x 240, 640 x 480
- 800 x 600
- 1024 x 768
- 2048 x 2048
- 4096 x 4096

Debug and Development Interface (SWD/JTAG)

Special versions of the device are available with a serial wire debug or JTAG interface that is used only during application development and debugging. The interface is used for code loading, ICE debug activities, and control of boundary scan activities.

Trust Protection Unit (MAX32651 Only)

True Random Number Generator

Random numbers are a vital part of a secure application, providing random numbers that can be used for cryptographic seeds or strong encryption keys to ensure data privacy.

Software can use random numbers to trigger asynchronous events that result in nondeterministic behavior. This is helpful in thwarting replay attacks or key search approaches. An effective true random number generator (TRNG) must be continuously updated by a high-entropy source.

The provided TRNG is continuously driven by a physically-unpredictable entropy source. It generates a 128-bit true random number in 128 system clock cycles.

The TRNG can support the system-level validation of many security standards such as FIPS 140-2, PCI-PED, and Common Criteria. Contact Maxim for details of compliance with specific standards.

MAA

The provided high-speed, hardware-based modulo arithmetic accelerator (MAA) performs mathematical computations that support strong cryptographic algorithms. These include:

- 2048-bit DSA
- 4096-bit RSA
- Elliptic curve public key infrastructure

AES

The dedicated hardware-based AES engine supports the following algorithms:

- AES-128
- AES-192
- AES-256

The AES keys are automatically generated by the engine and stored in dedicated flash to protect against tampering. Key generation and storage is transparent to the user.

SHA-256

SHA-256 is a cryptographic hash function part of the SHA-2 family of algorithms. It authenticates user data and verifies its integrity. It is used for digital signatures.

The device provides a hardware SHA-256 engine for fast computation of 256-bit digests.

Memory Decryption Integrity Unit

The external SPI flash can optionally be encrypted for additional security. Data can be transparently encrypted when it is loaded and decrypted on-the-fly. Encryption keys are stored in the always-on domain and preserved as as long as V_{RTC} is present.

Secure Firmware Updates

Root of Trust

The root of trust starts with trusted software and the microcontroller's TPU. Communications between a host and the device must be secure and authenticated, and program integrity must be verified each time before execution to ensure the trustworthiness of device.

The device's root of trust is based on a Maxim Integrated master root verification key and a signed customer verification key (CVK). Customers submit their public CVK to Maxim Integrated, which is then signed and this public key sent back to the customer. This process is quick and required only once before the software is released for the first time and is not needed during the software development. A customer can then load their own key and download their signed binary executable code.

A life-cycle scheme allows devices to be permanently disabled to deactivate a deployed application. After the software development is complete, but before deployment, the JTAG debugger interface must be disabled in a separate step.

Secure Communications Protocol Bootloader (SCPBL)

Communication between a host system and the device uses a system of digitally signed packets. This guarantees the integrity and authenticity of all communication before executing configuration commands and the loading or verification of program memory. One or more serial interfaces are available for communication.

This also enables the assembly and programming of the customers final product by third-party assembly houses without

the required cost and complexity of ensuring that the assembly house implements and maintains a secure production facility. It also allows for in-field software upgrades to deployed products, thus eliminating the costly need to return a product to the manufacturer for any software changes.

The MAX32651 SCPBL selects the USB as the factory default interface using preprogrammed software. Performing a mass erase before executing the preprogrammed software or erasing the last page of flash memory will select UART0 as the interface. Once an SCPBL session is opened, the chosen interface must be explicitly assigned using a dedicated command SCPBL command. This allows the last page of flash memory to be erased, if needed, and used by the application software. The 96-bump WLP can only use the USB interface and must run the preprogrammed software to select USB as the factory interface.

Table 3. MAX32651 SCPBL Interface Options

INTERFACE	BOOTLOADER STIMULUS PIN	INTERFACE PINS REQUIRED FOR PROGRAMMING
UART (115200bps)	P2.28 (active high)	UART0 RX (P2.11) UART0 TX (P2.12)
USB (DEFAULT)	P2.18 (active high)	DP DM V_{DDB}
JTAG (Debugger)	N/A	TDI (P0.26) TDO (P0.27) TMS (P0.28) TCK (P0.29)

Figure 10 depicts a flowchart of the SCP activation. It shows the actions of the device and how the SCPBL interfaces are selected.

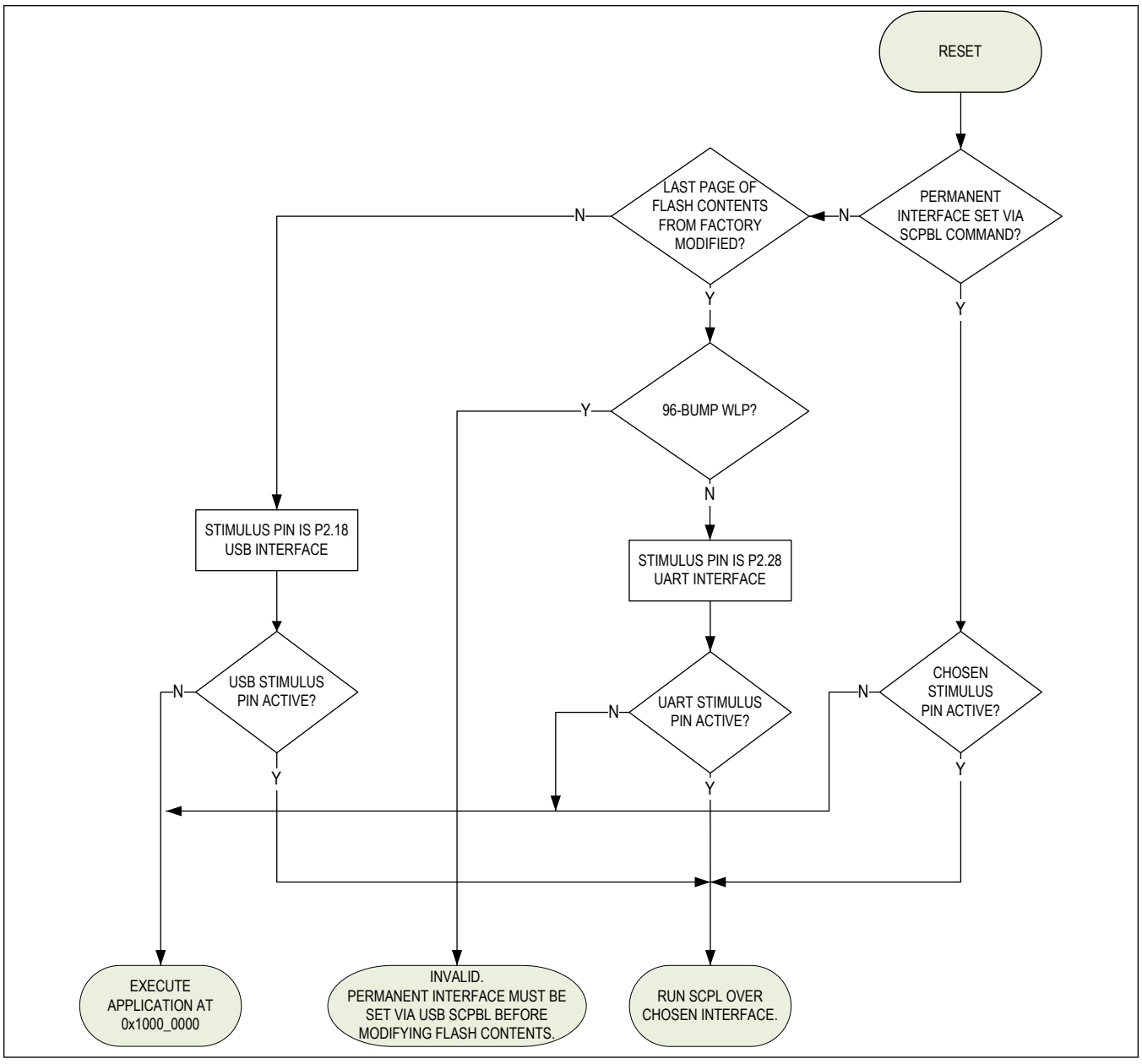


Figure 10. Secure Communications Protocol Interface Activation

Secure Boot

Following every reset, the device performs a secure boot to confirm the root of trust has not been compromised. The secure boot verifies the digital signature of the program memory to confirm it has not been modified or corrupted ensuring the trustworthiness of the application software. Failure to verify the digital signature will transition the device to safe mode, which prevents execution of the customer code. During the development phase, the bootloader can be reactivated and new, trusted program memory loaded. The device can be locked prior to deployment to prevent any changes to program memory.

Additional Documentation and Technical Support

Designers must have the following documents to use all the features of this device.

- This data sheet, which contains electrical/timing specifications, package information, and pin descriptions.
- The corresponding revision-specific errata sheet.
- The corresponding user guide, which contains detailed information and programming guidelines for core features and peripherals.

Applications Information

GPIO and Alternate Function Matrix, 140 WLP

Table 4. GPIO and Alternate Function Matrix, 140 WLP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.0	PT3	SPIXF_SDIO2**
P0.1	SPIXR_SDIO0**	—
P0.2	SPIXR_SDIO2**	—
P0.3	SPIXR_SCK**	—
P0.4	SPIXR_SDIO3**	—
P0.5	SPIXR_SDIO1**	—
P0.6	SPIXR_SS0**	—
P0.7	SPIXF_SS0**	—
P0.8	SPIXF_SCK**	—
P0.9	SPIXF_SDIO1**	—
P0.10	SPIXF_SDIO0**	—
P0.11	SPIXF_SDIO2**	—
P0.12	SPIXF_SDIO3**	—
P0.13	SPI3_SS1	CLCD_G0
P0.14	SPI3_SS2	CLCD_G1
P0.15	SPI3_SDIO3	CLCD_G2
P0.16	SPI3_SCK	CLCD_G3
P0.17	SPI3_SDIO2	CLCD_G4
P0.18	SPI3_SS3	CLCD_G5
P0.19	SPI3_SS0	CLCD_G6
P0.20	SPI3_SDIO1	CLCD_G7
P0.21	SPI3_SDIO0	—
P0.22	SPI0_SS0	CLCD_VDEN
P0.23	PT15	CLCD_CLK
P0.24	RXEV	CLCD_HSYNC
P0.25	TXEV	CLCD_B0
P0.26	TDI	TDI
P0.27	TDO	TDO
P0.28	TMS (SWDIO)††	TMS (SWDIO)††
P0.29	TCK (SWDCLK)††	TCK (SWDCLK)††
P0.30	—	CLCD_B0
P0.31	32KCAL	SDHC_CDN
P1.0	SDHC_CMD	SPIXF_SDIO3**
P1.1	SDHC_DAT2	SPIXF_SDIO1**
P1.2	SDHC_WP	SPIXF_SS0**
P1.3	SDHC_DAT3	CLCD_CLK

Table 4. GPIO and Alternate Function Matrix, 140 WLP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P1.4	SDHC_DAT0	SPIXF_SDIO0**
P1.5	SDHC_CLK	SPIXF_SCK**
P1.6	SDHC_DAT1	PT0
P1.7	UART2_CTS	PT1
P1.8	UART2_RTS	PT2
P1.9	UART2_RX	PT3
P1.10	UART2_TX	PT4
P1.11	HYP_CS0N	SPIXR_SDIO0**
P1.12	HYP_D0	SPIXR_SDIO1**
P1.13	HYP_D4	SPIXR_SS0**
P1.14	HYP_RWDS	PT5
P1.15	HYP_D1	SPIXR_SDIO2**
P1.16	HYP_D5	SPIXR_SCK**
P1.17	PT9	—
P1.18	HYP_D6	PT6
P1.19	HYP_D2	PT7
P1.20	HYP_D3	CLCD_HSYNC
P1.21	HYP_D7	PT8
P1.22*	—	—
P1.23	SPI1_SS0	CLCD_B1
P1.24	SPI1_SS2	CLCD_B2
P1.25	SPI1_SS1	CLCD_B3
P1.26	SPI1_SCK	CLCD_B4
P1.27	SPI1_SS3	CLCD_B5
P1.28	SPI1_MISO	CLCD_B6
P1.29	SPI1_MOSI	CLCD_B7
P1.30	OWM_PUPEN	CLCD_R0
P1.31	OWM_IO	CLCD_R1
P2.0	SPI2_SS2	PT9
P2.1	SPI2_SS1	PT10
P2.2	SPI2_SCK (I2S_BCLK)†	CLCD_LEND
P2.3	SPI2_MISO (I2S_SDI)†	CLCD_PWREN
P2.4	SPI2_MOSI (I2S_SDO)†	—
P2.5	SPI2_SS0 (I2S_LRCLK)†	PT11
P2.6	SPI2_SS3	CLCD_VSYNC
P2.7	I2C0_SDA	—
P2.8	I2C0_SCL	—
P2.9	UART0_CTS	PT12
P2.10	UART0_RTS	PT14
P2.11	UART0_RX	PT13

Table 4. GPIO and Alternate Function Matrix, 140 WLP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P2.12	UART0_TX	PT15
P2.13	UART1_CTS	CLCD_R2
P2.14	UART1_RX	CLCD_R3
P2.15	UART1_RTS	CLCD_R4
P2.16	UART1_TX	CLCD_R5
P2.17	I2C1_SDA	CLCD_R6
P2.18	I2C1_SCL. This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.	CLCD_R7. This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.
P2.19	PT4	—
P2.20	PT5	—
P2.21	PT7	—
P2.22	PT8	—
P2.23	PT6	SPIXR_SDIO3**
P2.24	PT10	—
P2.25	PT11	—
P2.26	PT12	—
P2.27	PT13	—
P2.28	PT14.This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.	This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.
P2.29	PT0	—
P2.30	PT1	—
P2.31	PT2	—
P3.0	PDOWN†††	HYP_CS1N
P3.1	SPI0_MISO	—
P3.2	SPI0_MOSI	—
P3.3	SPI0_SCK	—
P3.4	TMR0	—
P3.5	TMR2	—
P3.6	TMR4	—
P3.7	TMR1	—
P3.8	TMR3	—
P3.9	TMR5	—

**GPIO not pinned out.*

***This signal can be mapped to more than one GPIO, but there is only one instance of this peripheral.*

†I2S_BCLK, I2S_LRCLK, I2S_SDI, and I2S_SDO when enabled.

††Single-wire debug when enabled.

†††PDOWN is not operative during or immediately after reset since this function appears as an Alternate Function 1.

GPIO and Alternate Function Matrix, 96 WLP

Table 5. GPIO and Alternate Function Matrix, 96 WLP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.0*	—	—
P0.1*	—	—
P0.2*	—	—
P0.3*	—	—
P0.4*	—	—
P0.5*	—	—
P0.6*	—	—
P0.7*	—	—
P0.8*	—	—
P0.9*	—	—
P0.10*	—	—
P0.11	SPIXF_SDIO2**	P0.11
P0.12*	—	—
P0.13	SPI3_SS1	CLCD_G0
P0.14	SPI3_SS2	CLCD_G1
P0.15	SPI3_SDIO3	CLCD_G2
P0.16	SPI3_SCK	CLCD_G3
P0.17	SPI3_SDIO2	CLCD_G4
P0.18	SPI3_SS3	CLCD_G5
P0.19	SPI3_SS0	CLCD_G6
P0.20	SPI3_SDIO1	CLCD_G7
P0.21	SPI3_SDIO0	—
P0.22	—	CLCD_VDEN
P0.23*	—	—
P0.24*	—	—
P0.25*	—	—
P0.26	TDI	—
P0.27	TDO	—
P0.28	TMS (SWDIO)††	—
P0.29	TCK (SWDCLK)††	—
P0.30	—	CLCD_B0
P0.31*	—	—
P1.0	SDHC_CMD	SPIXF_SDIO3**
P1.1	SDHC_DAT2	SPIXF_SDIO1**
P1.2	SDHC_WP	SPIXF_SS0**
P1.3	SDHC_DAT3	CLCD_CLK
P1.4	SDHC_DAT0	SPIXF_SDIO0**
P1.5	SDHC_CLK	SPIXF_SCK**
P1.6	SDHC_DAT1	PT0

Table 5. GPIO and Alternate Function Matrix, 96 WLP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P1.7*	—	—
P1.8	UART2_RTS	PT2
P1.9	UART2_RX	PT3
P1.10	UART2_TX	PT4
P1.11	—	SPIXR_SDIO0**
P1.12	—	SPIXR_SDIO1**
P1.13	—	SPIXR_SS0**
P1.14	—	PT5
P1.15	—	SPIXR_SDIO2**
P1.16	—	SPIXR_SCK**
P1.17*	—	—
P1.18	—	PT6
P1.19	—	PT7
P1.20	—	CLCD_HSYNC
P1.21	—	PT8
P1.22*	—	—
P1.23	SPI1_SS0	CLCD_B1
P1.24	SPI1_SS2	CLCD_B2
P1.25	SPI1_SS1	CLCD_B3
P1.26	SPI1_SCK	CLCD_B4
P1.27	SPI1_SS3	CLCD_B5
P1.28	SPI1_MISO	CLCD_B6
P1.29	SPI1_MOSI	CLCD_B7
P1.30	OWM_PUPEN	CLCD_R0
P1.31	OWM_IO	CLCD_R1
P2.0	SPI2_SS2	PT9
P2.1*	—	—
P2.2	SPI2_SCK (I2S-BCLK)†	CLCD_LEND
P2.3	SPI2_MISO (I2S-SDI)†	CLCD_PWREN
P2.4	SPI2_MOSI (I2S-SDO)†	—
P2.5	SPI2_SS0 (I2S_LRCLK)†	PT11
P2.6	SPI2_SS3	CLCD_VSYNC
P2.7*	—	—
P2.8*	—	—
P2.9	UART0_CTS	PT12
P2.10*	—	—
P2.11	UART0_RX	PT13
P2.12	UART0_TX	PT15
P2.13	UART1_CTS	CLCD_R2
P2.14	UART1_RX	CLCD_R3

Table 5. GPIO and Alternate Function Matrix, 96 WLP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P2.15	UART1_RTS	CLCD_R4
P2.16	UART1_TX	CLCD_R5
P2.17	I2C1_SDA	CLCD_R6
P2.18	I2C1_SCL. This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.	CLCD_R7. This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.
P2.19*	—	—
P2.20*	—	—
P2.21*	—	—
P2.22*	—	—
P2.23	PT6	SPIXR_SDIO3**
P2.24*	—	—
P2.25*	—	—
P2.26*	—	—
P2.27*	—	—
P2.28*	—	—
P2.29*	—	—
P2.30*	—	—
P2.31*	—	—
P3.0*	—	—
P3.1*	—	—
P3.2*	—	—
P3.3*	—	—
P3.4	TMR0	—
P3.5	TMR2	—
P3.6	TMR4	—
P3.7	TMR1	—
P3.8	TMR3	—
P3.9	TMR5	—

**GPIO not pinned out.*

***This signal can be mapped to more than one GPIO, but there is only one instance of this peripheral.*

†*I2S_BCLK, I2S_LRCLK, I2S_SDI, I2S_SDO when enabled.*

††*Single-wire debug when enabled.*

GPIO and Alternate Function Matrix, 144 TQFP

Table 6. GPIO and Alternate Function Matrix, 144 TQFP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.0*	—	—
P0.1	SPIXR_SDIO0**	—
P0.2	SPIXR_SDIO2**	—

Table 6. GPIO and Alternate Function Matrix, 144 TQFP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P0.3	SPIXR_SCK**	—
P0.4	SPIXR_SDIO3**	—
P0.5	SPIXR_SDIO1**	—
P0.6	SPIXR_SS0**	—
P0.7	SPIXF_SS0**	—
P0.8	SPIXF_SCK**	—
P0.9	SPIXF_SDIO1**	—
P0.10	SPIXF_SDIO0**	—
P0.11	SPIXF_SDIO2**	—
P0.12	SPIXF_SDIO3**	—
P0.13	SPI3_SS1	CLCD_G0
P0.14	SPI3_SS2	CLCD_G1
P0.15	SPI3_SDIO3	CLCD_G2
P0.16	SPI3_SCK	CLCD_G3
P0.17	SPI3_SDIO2	CLCD_G4
P0.18	SPI3_SS3	CLCD_G5
P0.19	SPI3_SS0	CLCD_G6
P0.20	SPI3_SDIO1	CLCD_G7
P0.21	SPI3_SDIO0	—
P0.22	SPI0_SS0	CLCD_VDEN
P0.23	PT15	CLCD_CLK
P0.24	RXEV	CLCD_HSYNC
P0.25	TXEV	CLCD_B0
P0.26	TDI	—
P0.27	TDO	—
P0.28	TMS (SWDIO)†††	—
P0.29	TCK (SWDCLK)†††	—
P0.30	—	CLCD_B0
P0.31	32KCAL	SDHC_CDN
P1.0	SDHC_CMD	SPIXF_SDIO3**
P1.1	SDHC_DAT2	SPIXF_SDIO1**
P1.2	SDHC_WP	SPIXF_SS0**
P1.3	SDHC_DAT3	CLCD_CLK
P1.4	SDHC_DAT0	SPIXF_SDIO0**
P1.5	SDHC_CLK	SPIXF_SCK**
P1.6	SDHC_DAT1	PT0
P1.7	UART2_CTS	PT1
P1.8	UART2_RTS	PT2
P1.9	UART2_RX	PT3
P1.10	UART2_TX	PT4

Table 6. GPIO and Alternate Function Matrix, 144 TQFP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P1.11	HYP_CS0N	SPIXR_SDIO0**
P1.12	HYP_D0	SPIXR_SDIO1**
P1.13	HYP_D4	SPIXR_SS0**
P1.14	HYP_RWDS	PT5
P1.15	HYP_D1	SPIXR_SDIO2**
P1.16	HYP_D5	SPIXR_SCK**
P1.17	PT9	-
P1.18	HYP_D6	PT6
P1.19	HYP_D2	PT7
P1.20	HYP_D3	CLCD_HSYNC
P1.21	HYP_D7	PT8
P1.22	—	—
P1.23	SPI1_SS0	CLCD_B1
P1.24	SPI1_SS2	CLCD_B2
P1.25	SPI1_SS1	CLCD_B3
P1.26	SPI1_SCK	CLCD_B4
P1.27	SPI1_SS3	CLCD_B5
P1.28	SPI1_MISO	CLCD_B6
P1.29	SPI1_MOSI	CLCD_B7
P1.30	OWM_PUPEN	CLCD_R0
P1.31	OWM_IO	CLCD_R1
P2.0	SPI2_SS2	PT9
P2.1	SPI2_SS1	PT10
P2.2	SPI2_SCK (I2S-BCLK)†	CLCD_LEND
P2.3	SPI2_MISO (I2S-SDI)†	CLCD_PWREN
P2.4	SPI2_MOSI (I2S-SDO)†	—
P2.5	SPI2_SS0 (I2S_LRCLK)†	PT11
P2.6	SPI2_SS3	CLCD_VSYNC
P2.7	I2C0_SDA	—
P2.8	I2C0_SCL	—
P2.9	UART0_CTS	PT12
P2.10	UART0_RTS	PT14
P2.11	UART0_RX	PT13
P2.12	UART0_TX	PT15
P2.13	UART1_CTS	CLCD_R2
P2.14	UART1_RX	CLCD_R3
P2.15	UART1_RTS	CLCD_R4
P2.16	UART1_TX	CLCD_R5
P2.17	I2C1_SDA	CLCD_R6

Table 6. GPIO and Alternate Function Matrix, 144 TQFP (continued)

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2
P2.18	I2C1_SCL. This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.	CLCD_R7. This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.
P2.19*	—	—
P2.20*	—	—
P2.21*	—	—
P2.22*	—	—
P2.23	PT6	SPIXR_SDIO3**
P2.24*	—	—
P2.25	PT11	—
P2.26	PT12	—
P2.27*	—	—
P2.28	PT14. This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.	This device pin also has a special function associated with the Secure Communications Protocol Bootloader. See Table 3 for details.
P2.29*	—	—
P2.30	PT1	—
P2.31*	—	—
P3.0	PDOWN††	HYP_CS1N
P3.1	SPI0_MISO	—
P3.2	SPI0_MOSI	—
P3.3	SPI0_SCK	—
P3.4	TMR0	—
P3.5	TMR2	—
P3.6	TMR4	—
P3.7	TMR1	—
P3.8	TMR3	—
P3.9	TMR5	—

**GPIO not pinned out.*

***This signal can be mapped to more than one GPIO, but there is only one instance of this peripheral.*

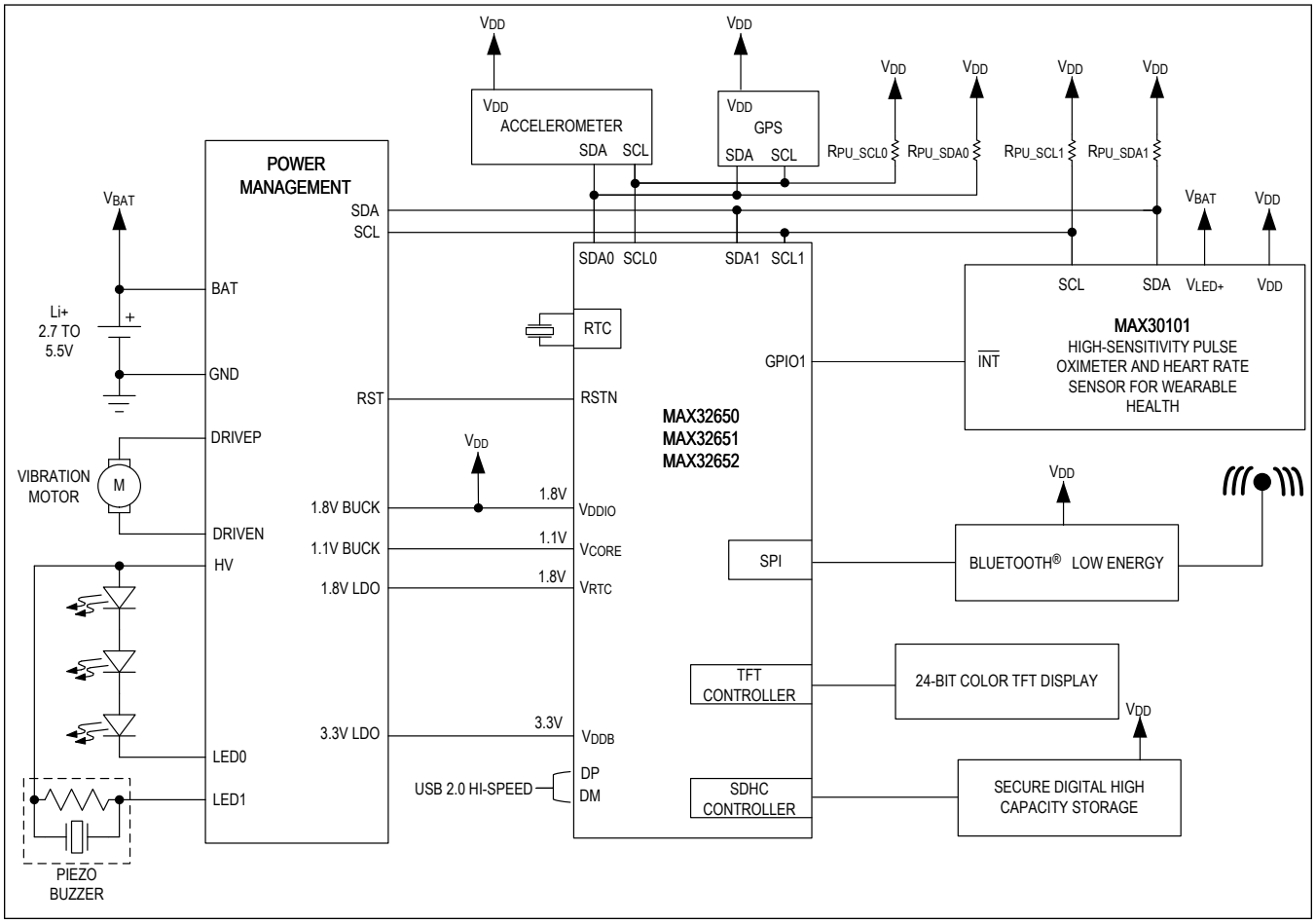
†I2S_BCLK, I2S_LRCLK, I2S_SDI, I2S_SDO when enabled.

††PDOWN does not operate during or immediately after reset since this function appears as an Alternate Function 1.

†††Single-wire debug when enabled.

Typical Application Circuits

Pulse Oximeter and Heart Rate Monitor with Bluetooth LE and GPS Location



Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The Blueooth word mark is a registered trademark owned by Bluetooth SIG, Inc. and any use of such marks by Maxim is under license.

HyperBus is a trademark of Cypress Semiconductor Corporation.

microSD is a trademark of SD-3C.

Xccela is a trademark of Micron Technology, Inc.

Ordering Information

PART	TRUST PROTECTION UNIT WITH SECURE BOOTLOADER	PIN-PACKAGE
MAX32650GWQ+	No	96 WLP (0.4mm pitch)
MAX32650GWQ+T	No	96 WLP (0.4mm pitch)
MAX32650GCE+	No	144 TQFP
MAX32651GWQ+	Yes	96 WLP (0.4mm pitch)
MAX32651GWQ+T	Yes	96 WLP (0.4mm pitch)
MAX32651GCE+	Yes	144 TQFP
MAX32651GWE+	Yes	140 WLP (0.35mm pitch)
MAX32651GWE+T	Yes	140 WLP (0.35mm pitch)
MAX32652GWE+	No	140 WLP (0.35mm pitch)
MAX32652GWE+T	No	140 WLP (0.35mm pitch)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/17	Initial release	—
1	3/18	Updated *General Description* and *Benefits and Features* sections	1
2	10/18	Updated title, *Absolute Maximum Ratings*, *Debug and Development Interface (SWD/JTAG)*, and *Ordering Information* sections	1, 2, 39, 46
3	12/18	Updated *Debug and Development Interface (SWD/JTAG)* section and *Ordering Information*	39, 46
4	8/19	Updated *General Description*, *Benefits and Features, Simplified Block Diagram, Absolute Maximum Ratings, Package Information, Electrical Characteristics*, Figure 1, Figure 2, *Pin Description, Secure Digital Interface, Spansion HyperBus/Xccela Bus, Clocking Scheme*, Figure 8, *Standard DMA Controller, Background Mode, Deep-Sleep Mode, Real-Time Clock, UART, 24-Bit Color TFT Controller, Additional Documentation* and *Technical Support*, Table 3, Table 4, Table 5, *Pulse Oximeter and Heart Rate Monitor with Bluetooth LE and GPS Location*, and *Ordering Information*	1, 2, 7–11, 13, 19, 25, 33, 35–41, 43, 44, 48, 49, 56
5	2/20	Updated *Ordering Information*	58
6	3/20	Updated *Ordering Information*	58
7	10/20	Added discussion of *Secure Firmware Updates*. Updated *Clocking Scheme Diagram*. Updated *32KIN* and *32KOUT Pin Descriptions*. Update *Detailed Description 32-Bit Timer/Counter/PWM (TMR).* Updated *Electrical Characteristics Table Parameter Flash Programming Time per Word* conditions	13, 27, 39, 42–43, 47

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.