CY62168DV30
MoBL®

16-Mbit (2048K x 8) Static RAM

Features

- **Very high speed: 55 ns and 70 ns**
- **Wide voltage range: 2.2V to 3.6V**
- **Ultra-low active power**
  - **Typical active current: 2 mA @ f = 1 MHz**
  - **Typical active current: 15 mA @ f = f_{MAX}**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered in a 48-ball FBGA**

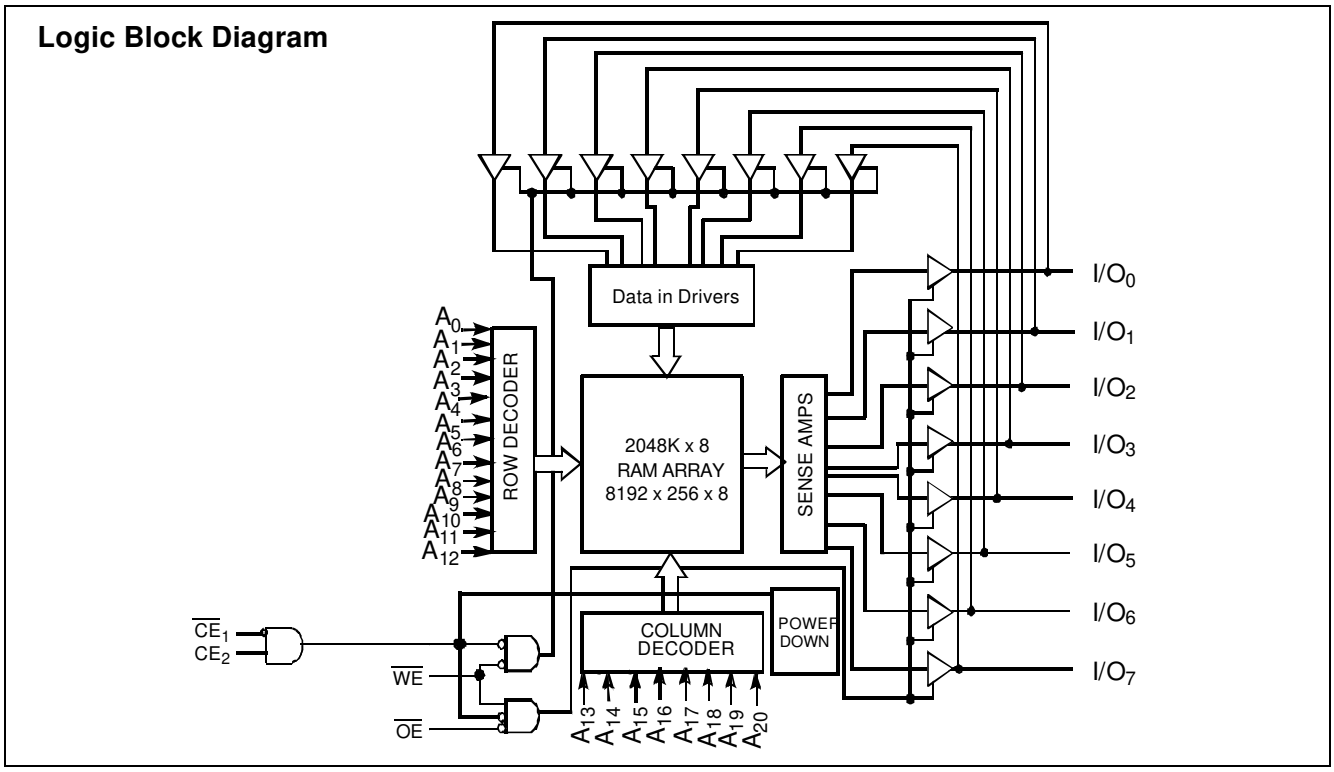
Functional Description[1]

The CY62168DV30 is a high-performance CMOS static RAM organized as 2048K words by eight bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. The device can be put into standby mode reducing power consumption by more than 99% when deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW. The input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when: deselected Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW, outputs are disabled ($\overline{OE}$ HIGH), or during a write operation (Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and Write Enable ($\overline{WE}$) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{20}).

Reading from the device is accomplished by taking Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins. The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}_1$ LOW and CE_2 HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the truth table at the back of this data sheet for a complete description of read and write modes.

Logic Block Diagram

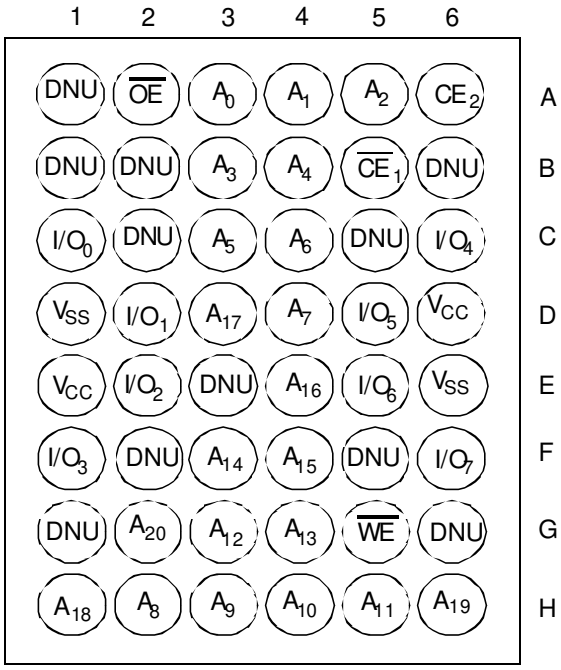


Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

Pin Configuration

FBGA
Top View



Note:
2. DNU pins are to be connected to V_{SS} or left open.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage to Ground Potential .–0.3V to V_{CCMAX} + 0.3V

DC Voltage Applied to Outputs in High-Z State[3, 4].....–0.3V to V_{CCMAX} + 0.3V

DC Input Voltage[3, 4].....–0.3V to V_{CCMAX} + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A)	V_{CC}[5]
Industrial	–40°C to +85°C	2.2V to 3.6V

Product Portfolio

Product	V_{CC} Range(V)			Speed (ns)	Power Dissipation					
					Operating, Icc (mA)				Standby, I_{SB2} (µA)	
					f = 1 MHz		f = f_{MAX}			
	Min.	Typ.[6]	Max.		Typ.[6]	Max.	Typ.[6]	Max.	Typ.[6]	Max.
CY62168DV30L	2.2	3.0	3.6	55	2	4	15	30	2.5	30
				70			12	25	2.5	30
CY62168DV30LL	2.2	3.0	3.6	55	2	4	15	30	2.5	22
				70			12	25	2.5	22

DC Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions			CY62168DV30-55			CY62168DV30-70			Unit
					Min.	Typ.[6]	Max.	Min.	Typ.[6]	Max.	
V_{OH}	Output HIGH Voltage	2.2 ≤ V_{CC} ≤ 2.7	I_{OH} = –0.1 mA		2.0			2.0			V
		2.7 ≤ V_{CC} ≤ 3.6	I_{OH} = –1.0 mA		2.4			2.4			
V_{OL}	Output LOW Voltage	2.2 ≤ V_{CC} ≤ 2.7	I_{OL} = 0.1 mA				0.4			0.4	V
		2.7 ≤ V_{CC} ≤ 3.6	I_{OH} = 2.1 mA				0.4			0.4	
V_{IH}	Input HIGH Voltage	2.2 ≤ V_{CC} ≤ 2.7			1.8		V_{CC} + 0.3	1.8		V_{CC} + 0.3	V
		2.7 ≤ V_{CC} ≤ 3.6			2.2		V_{CC} + 0.3	2.2		V_{CC} + 0.3	
V_{IL}	Input LOW Voltage	2.2 ≤ V_{CC} ≤ 2.7			–0.3		0.6	–0.3		0.6	V
		2.7 ≤ V_{CC} ≤ 3.6			–0.3		0.8	–0.3		0.8	
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}			–1		+1	–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output disabled			–1		+1	–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	Vcc = 3.6V, I_{OUT} = 0mA, CMOS level			15	30		12	25	mA
		f = 1 MHz				2	4		2	4	
I_{SB1}	Automatic CE Power-down Current – CMOS Inputs	CE_1 ≥ V_{CC} – 0.2V, CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V, V_{IN} ≤ 0.2V, f = f_{MAX} (Address and Data Only), f= 0 (OE, WE,)		L		2.5	30		2.5	30	µA
				LL		2.5	22		2.5	22	
I_{SB2}	Automatic CE Power-down Current – CMOS Inputs	CE_1 ≥ V_{CC} – 0.2V, CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC}=3.6V		L		2.5	30		2.5	30	µA
				LL		2.5	22		2.5	22	

Notes:

3. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to V_{cc}(min) and 100 µs wait time after V_{cc} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25°C.

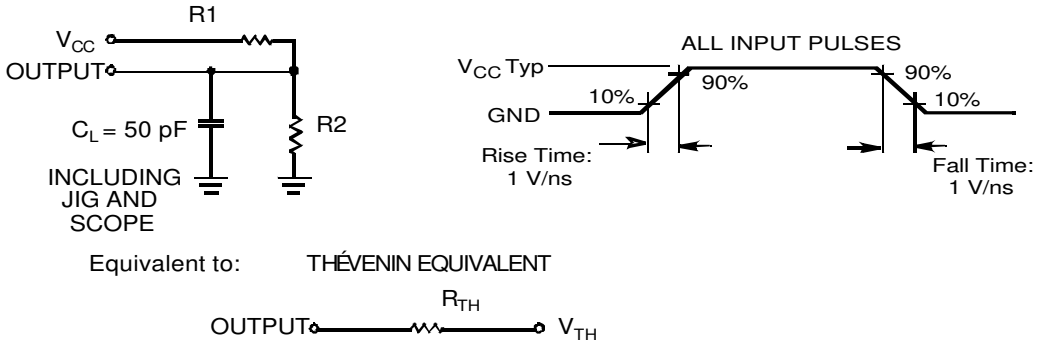
Capacitance[7]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	TA = 25°C, f = 1 MHz $V_{CC} = V_{CC(typ)}$	8	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)[7]	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	55	C/W
θ_{JC}	Thermal Resistance (Junction to Case)[7]		16	C/W

AC Test Loads and Waveforms



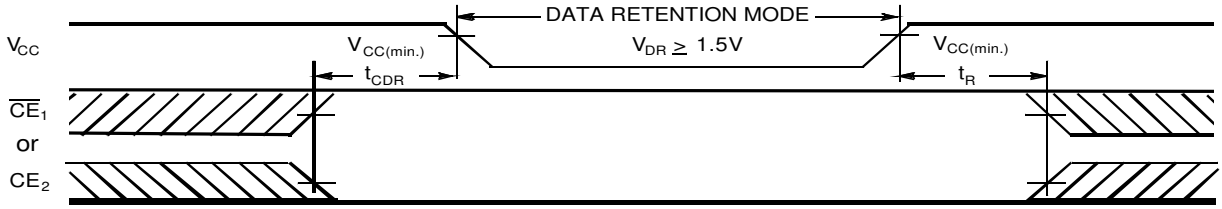
Parameters	2.5V (2.2–2.7V)	3.0V (2.7–3.6V)	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.2	1.75	V

Data Retention Characteristics

Parameter	Description	Conditions		Min.	Typ.[5]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5		3.6	V
I_{CCDR}	Data Retention Current	V_{CC}=1.5V, $CE_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L			15	µA
			LL			10	
t_{CDR}[7]	Chip Deselect to Data Retention Time			0			ns
t_R[8]	Operation Recovery Time			t_{RC}			ns

Notes:
7. Tested initially and after any design or proces changes that may affect these parameters.
8. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)}$ > 100 µs or stable at $V_{CC(min.)}$ > 100 µs.

Data Retention Waveform



Switching Characteristics (Over the Operating Range)[9]

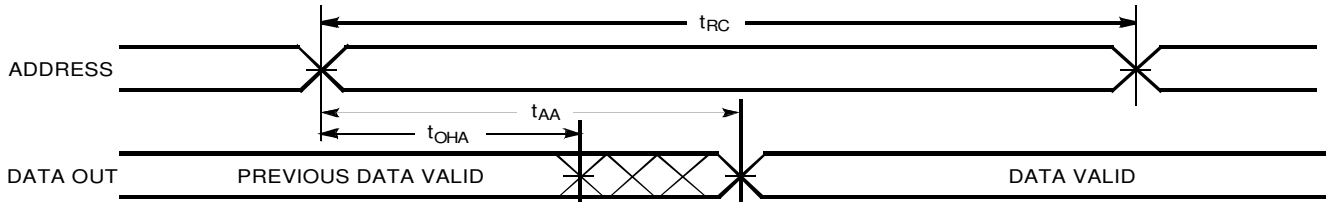
Parameter	Description	CY62168DV30-55		CY62168DV30-70		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	CE_1 LOW or CE_2 HIGH to Data Valid		55		70	ns
t_{DOE}	OE LOW to Data Valid		25		35	ns
t_{LZOE}	OE LOW to Low Z[10]	5		5		ns
t_{HZOE}	OE HIGH to High Z[10, 11]		20		25	ns
t_{LZCE}	CE_1 LOW or CE_2 HIGH to Low Z[10]	10		10		ns
t_{HZCE}	CE_1 HIGH or CE_2 LOW to High Z[10, 11]		20		25	ns
t_{PU}	CE_1 LOW or CE_2 HIGH to Power-up	0		0		ns
t_{PD}	CE_1 HIGH or CE_2 LOW to Power-down		55		70	ns
Write Cycle[12]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	CE_1 LOW or CE_2 HIGH to Write End	40		60		ns
t_{AW}	Address Set-up to Write End	40		60		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	WE Pulse Width	40		45		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	WE LOW to High Z[10, 11]		20		25	ns
t_{LZWE}	WE HIGH to Low Z[10]	10		10		ns

Notes:

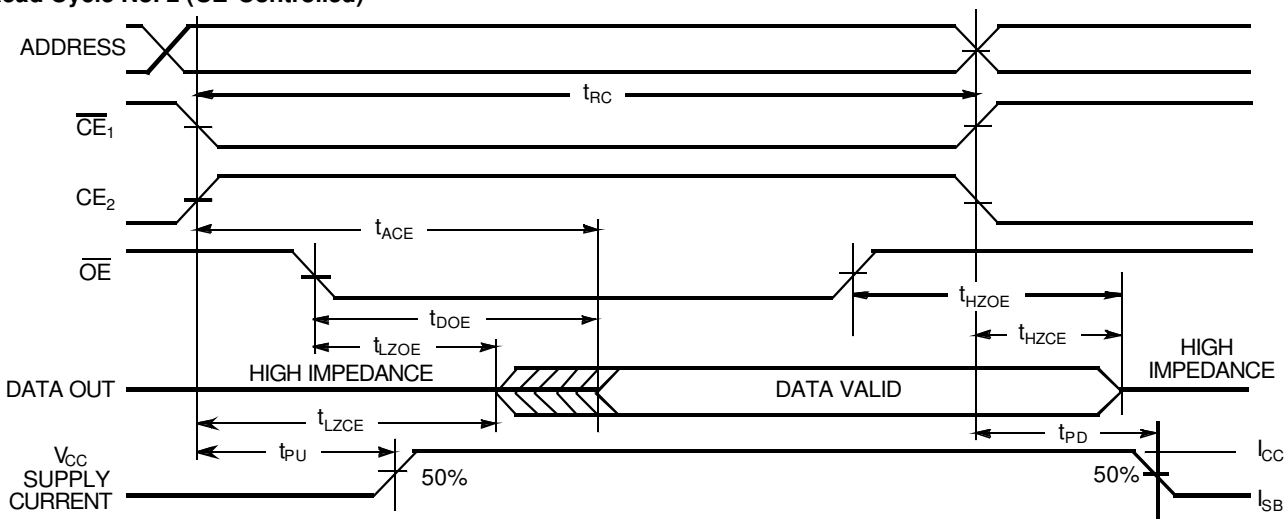
9. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ.)/2}$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t.
11. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

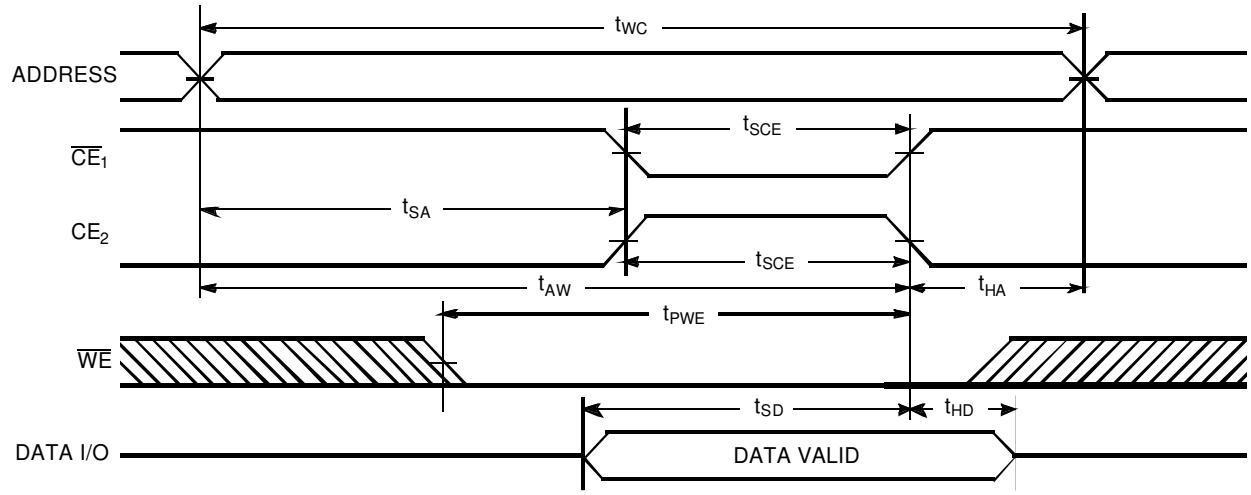
Read Cycle No. 1 (Address Transition Controlled)[13, 14]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]



Write Cycle No. 1 ($\overline{WE}$ Controlled)[12, 16, 17]

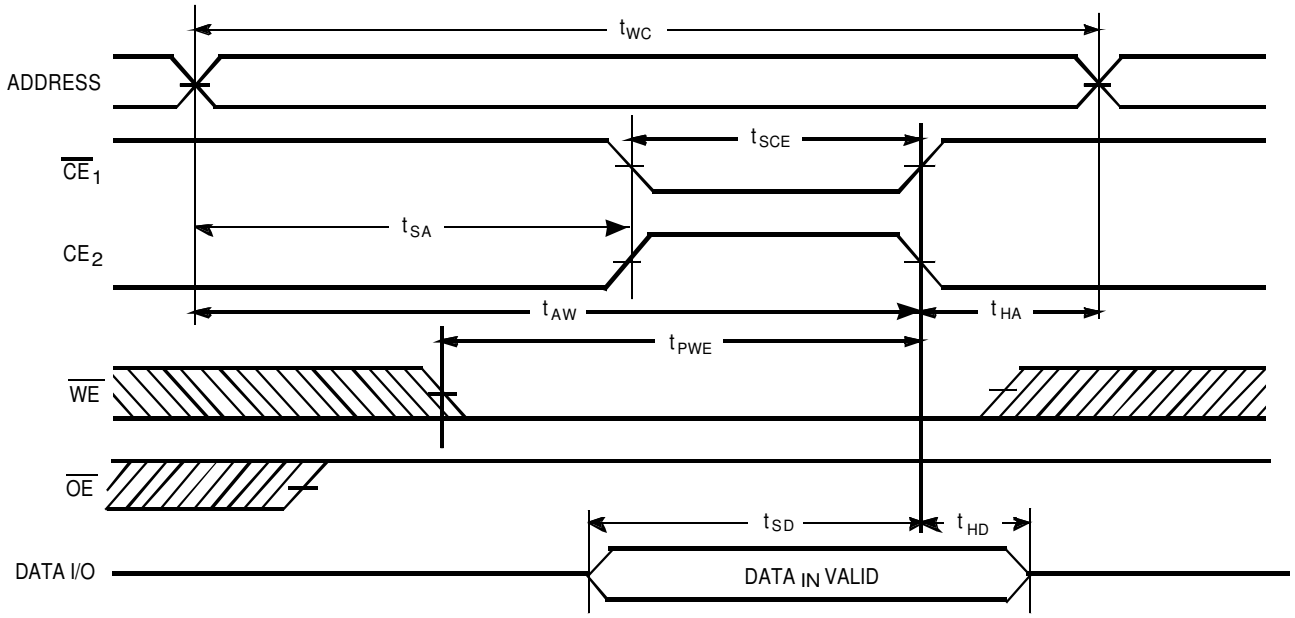


Notes:

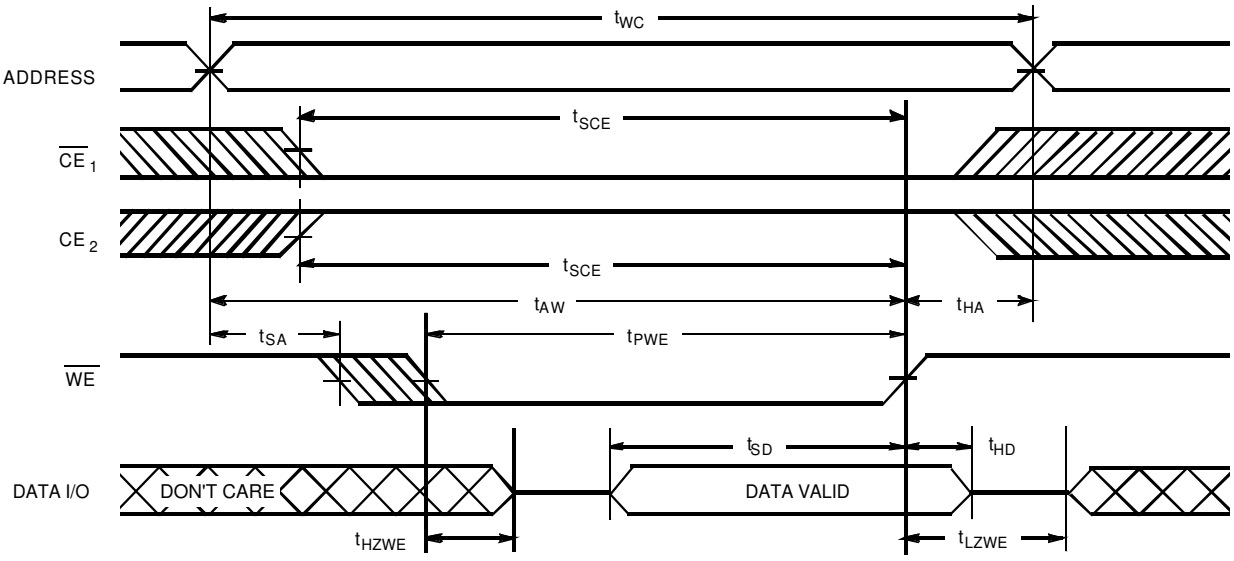
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, CE_2 = V_{IH}.
14. $\overline{WE}$ is HIGH for Read cycle.
15. Address valid prior to or coincident with $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.
16. Data I/O is high-impedance if $\overline{OE}$ = V_{IH}.
17. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
18. During the DON'T CARE period in the DATA I/O waveform, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}_1$ or CE_2 Controlled) [12, 16, 17]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[17, 18]



Truth Table

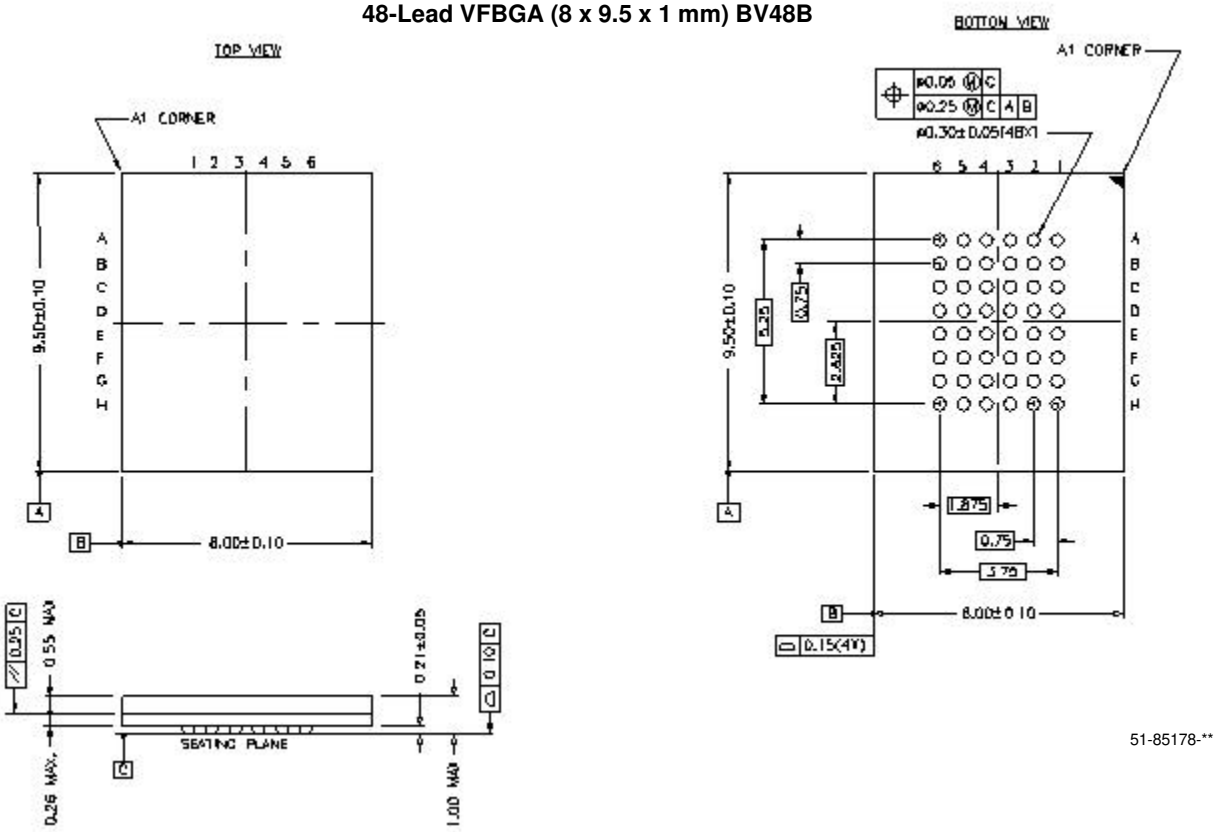
$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs / Outputs	Mode	Power
H	X	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data Out ($I/O_0 – I/O_7$)	Read	Active (I_{CC})
L	H	H	H	High Z	Output Disabled	Active (Icc)
L	H	L	X	Data In ($I/O_0 – I/O_7$)	Write	Active (Icc)

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62168DV30L-55**I	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	Industrial
	CY62168DV30LL-55**I	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	
70	CY62168DV30L-70**I	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	Industrial
	CY62168DV30LL-70**I	BV48B	48-ball Fine Pitch BGA (8.0 x 9.5 x 1.0 mm)	

Package Diagram

48-Lead VFBGA (8 x 9.5 x 1 mm) BV48B



Document History Page

Document Title: CY62168DV30 MoBL® 16-Mbit (2048K x 8) Static RAM Document Number: 38-05329				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	118409	09/30/02	GUG	New Data Sheet
*A	123693	02/05/03	DPM	Changed Advance Information to Preliminary Added package diagram
*B	126556	04/24/03	DPM	Minor change: Change sunset owner from DPM to HRT
*C	132869	01/15/04	XRJ	Change for Preliminary to Final