Low Distortion Digital-to-Analog Converter for Seismic Monitoring

Check for Samples: DAC1280

FEATURES

- **Outstanding Performance:**
  - **THD: –125dB**
  - **SNR: 120dB (413Hz BW, Gain = 1/1)**
  - **Gain Error: 0.1%**
- **Pin Operation: No Registers to Program**
- **Gain: 1/1 to 1/64**
- **SYNC Input for Phase Control**
- **Power-Down Mode**
- **Low Power: 18mW**
- **Analog Supply: +5V or ±2.5V**
- **Digital Supply: 1.8V to 3.3V**
- **Small 16-Pin TSSOP Package**
- **Temperature Range: –40°C to +85°C**

APPLICATIONS

- **Energy Exploration Equipment**
- **Seismic Monitoring Systems**

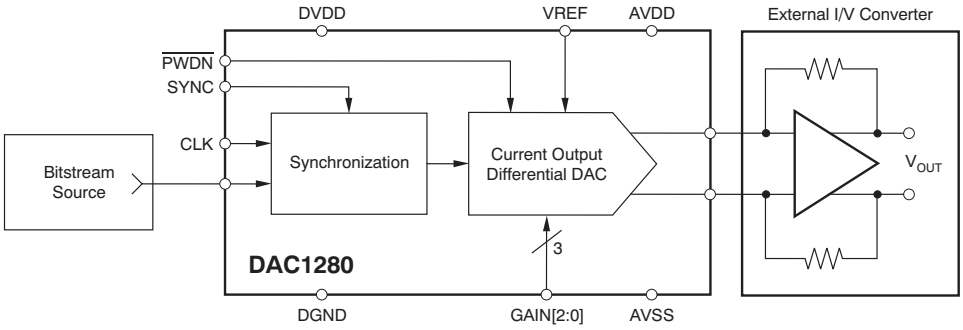
DESCRIPTION

The DAC1280 is a very low distortion digital-to-analog converter (DAC) suited for performance testing of seismic equipment. The DAC1280 provides a high-accuracy output signal from a bitstream input. The device achieves very high linearity in a small package while dissipating only 18mW. Together with the high-performance ADS1281 and ADS1282 analog-to-digital converters (ADCs), these devices create a test and measurement system that meets the exacting demands of energy exploration and seismic monitoring equipment.

The DAC1280 is designed to match the system components (power supply, clock and reference voltage) of the companion ADCs, the ADS1281 and ADS1282. The input to the DAC1280 is a 1s density modulated bitstream. The DAC1280 output is a differential current intended for use with an active I/V converter. The I/V converter provides a voltage output suitable for performance testing of sensors and ADCs.

Three gain control pins set the output range in 6dB steps from 0dB to –36db (±2.5V to ±0.039V differential). The attenuation ranges match the gains of the ADS1282 for testing at all gains. The DAC uses a reference voltage and bias resistor to set the full-scale output. The resistor can be adjusted to fine-trim the DAC full-scale.

The SYNC pin aligns the input data sampling to the CLK phase. A power-down pin shuts down the device when not in use. The DAC1280 is available in a small, 16-pin TSSOP package and is fully specified for operation over –40°C to +85°C temperature range with a maximum operating temperature of +125°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	DAC1280		
	MIN	MAX	UNIT
AVDD to AVSS	–0.3	+5.5	V
AVSS to DGND	–2.8	+0.3	V
DVDD to DGND	–0.3	+3.6	V
Input current, momentary	–100	+100	mA
Input current, continuous	–10	+10	mA
Analog input or output voltage to DGND	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage to DGND	–0.3	DVDD + 0.3	V
Maximum junction temperature		+150	°C
Operating temperature range	–40	+125	°C
Storage temperature range	–60	+150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

THERMAL INFORMATION

THERMAL METRIC(1)		DAC1280 TSSOP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	111.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	33.3	
θ_{JB}	Junction-to-board thermal resistance(4)	52.4	
ψ_{JT}	Junction-to-top characterization parameter(5)	2.0	
ψ_{JB}	Junction-to-board characterization parameter(6)	51.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

Minimum/maximum specifications at –40°C to +85°C, typical specifications at +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = 3.3V, CLK = 4.096MHz, V_{REF} = 5V, and R_{REF} = 30kΩ, unless otherwise noted. Refer to circuit configuration shown in Figure 35.

PARAMETER			TEST CONDITIONS	DAC1280 MIN	DAC1280 TYP	DAC1280 MAX	UNIT
ANALOG OUTPUTS							
Full-scale output current	I_{FS} = (IOUTP – IOUTN)(1)		Gain = 1/1 to 1/64		±1250 • Gain		μA
Output common-mode voltage(2)				– 0.15	0	+ 0.15	V
DC PERFORMANCE(3)							
Gain error			Gain = 1/1		±0.02	±0.25	%
Gain match			Relative to Gain = 1/1		±0.1	±0.5	%
Gain drift(4)					4		ppm/°C
Offset			Gain = 1/1 to 1/64		±50	±800	ppm of FS
Offset drift(4)					0.2		ppm of FS/°C
DC noise(5)			Gain = 1/1		1.2		μV_{RMS}
			Gain = 1/2		1.4		μV_{RMS}
			Gain = 1/4		1.8		μV_{RMS}
			Gain = 1/8		2.9		μV_{RMS}
			Gain = 1/16		5.5		μV_{RMS}
			Gain = 1/32		10		μV_{RMS}
			Gain = 1/64		19		μV_{RMS}
AC PERFORMANCE							
Total harmonic distortion(6)	THD		Gain = 1/1		–125	–118	dB
			Gain = 1/2, 1/4, 1/8		–125		dB
			Gain = 1/16		–124		dB
			Gain = 1/32		–118		dB
			Gain = 1/64		–113		dB
Signal-to-noise ratio(7)	SNR		Gain = 1/1	116	120		dB
			Gain = 1/2		119		dB
			Gain = 1/4		117		dB
			Gain = 1/8		114		dB
			Gain = 1/16		109		dB
			Gain = 1/32		105		dB
			Gain = 1/64		99		dB
Power-supply rejection	PSR	AVDD, AVSS	60Hz ac, gain = 1/8		85		dB
		DVDD	60Hz ac		115		dB
–3dB bandwidth					8.2		kHz
REFERENCE VOLTAGE INPUT (VREF)							
Reference voltage	V_{REF} = VREF – AVSS			2.4	5	AVDD + 0.25	V
Input impedance			Operating		220		kΩ
			Power-down		10		MΩ

(1) TDATA modulated 75% and 25% yielding positive full-scale output and negative full-scale output, respectively. Full-scale positive and negative output current is given by:

$$I_{FS} = IOUTP - IOUTN = \pm 7.5 \bullet \frac{V_{REF}}{R_{REF}} \bullet Gain; \quad V_{REF} = 5V, R_{REF} = 30k\Omega \text{ nominal}$$

Gain can be trimmed by adjusting V_{REF}/R_{REF} ratio over the range of 40% to 105% of nominal.

(2) Output common-mode voltage is regulated by the external I/V converter. The specified output common-mode voltage range is: (AVDD + AVSS)/2 ±0.15V.

(3) Excludes the tolerances of external components.

(4) Drift is calculated over the specified temperature range using the box calculation method.

(5) DC noise measured by ADS1282 with complementing gain over 413Hz bandwidth with DAC output = 0V.

(6) THD = Total harmonic distortion; measured by ADS1282 with complementing gain including first nine harmonics, DAC output = –0.5dBFS, 31.25Hz.

(7) SNR = Signal-to-noise ratio; measured by ADS1282 with complementing gain over 413Hz bandwidth, DAC output = –0.5dBFS, 31.25Hz.

ELECTRICAL CHARACTERISTICS (continued)

Minimum/maximum specifications at –40°C to +85°C, typical specifications at +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = 3.3V, CLK = 4.096MHz, V_{REF} = 5V, and R_{REF} = 30kΩ, unless otherwise noted. Refer to circuit configuration shown in Figure 35.

PARAMETER	TEST CONDITIONS	DAC1280			UNIT
		MIN	TYP	MAX	
REFERENCE RESISTOR (RREF)					
Reference resistor		28	30	60	kΩ
DIGITAL INPUTS (DVDD = 1.65V to 3.6V)					
V_{IH}		0.8 × DVDD		DVDD	V
V_{IL}		DGND		0.2 × DVDD	V
Input hysteresis			0.5		V
Input leakage	0 < V_{IN} < DVDD	–10		10	µA
CLOCK INPUT (f_{CLK})					
Frequency		1		4.096	MHz
TDATA INPUT					
Frequency			f_{CLK}/16		MHz
1s density modulation		25		75	%
POWER SUPPLY					
AVSS		–2.6		0	V
AVDD		AVSS + 4.75		AVSS + 5.25	V
DVDD		1.65		3.6	V
AVDD, AVSS current(8)	Gain = 1/1		3.6	3.7	| mA |
	Power-down		1	10	| µA |
DVDD current	Operating		60	150	µA
	Power-down(9)		1	10	µA
Power dissipation	Gain = 1/1		18		mW
	Power-down		8		µW
TEMPERATURE RANGE					
Specified temperature range		–40		+85	°C
Operating temperature range		–40		+125	°C
Storage temperature range		–40		+150	°C

(8) Typical analog supply current depends on gain, V_{REF}, and R_{REF}:

$$I_{AVDD}, |I_{AVSS}| = 0.94 \bullet \frac{V_{REF}}{R_{REF}} (1 + 22 \bullet \text{Gain})$$

(9) CLK and TDATA stopped. Digital inputs maintained at V_{IH} or V_{IL} levels.

TIMING CHARACTERISTICS

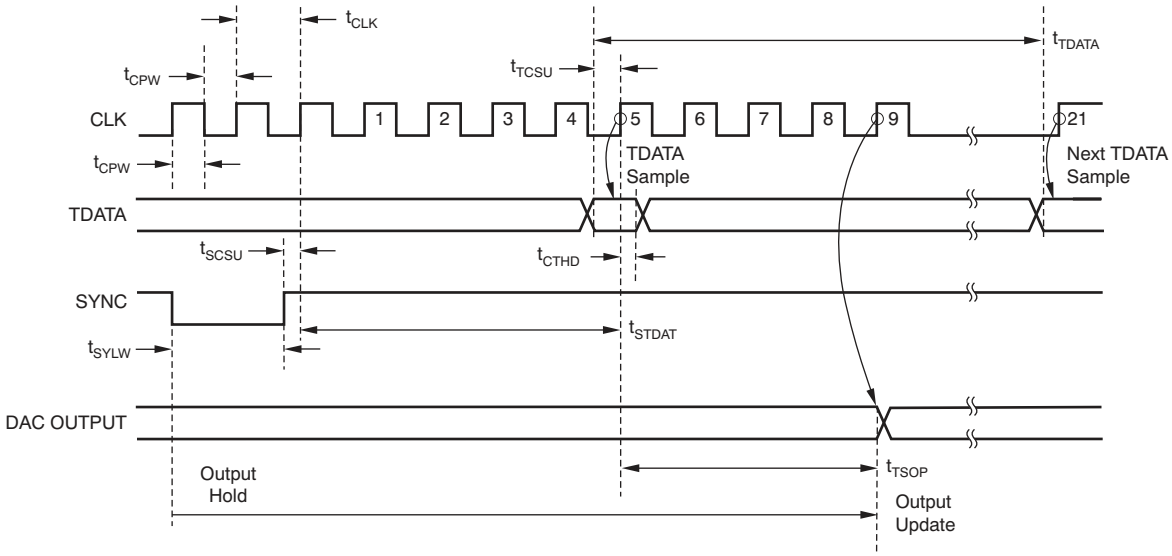


Figure 1.

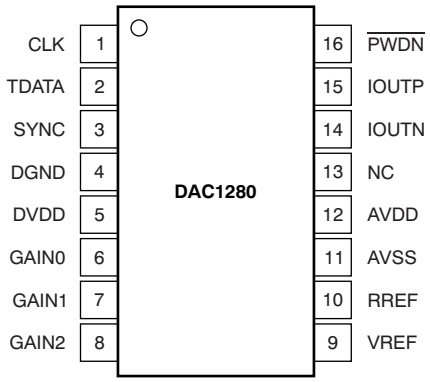
TIMING REQUIREMENTS

At T_A = –40°C to +85°C and DVDD = 1.65V to 3.6V.

PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLK period ($1/f_{CLK}$)	240		1000	ns
t_{CPW}	CLK high or low pulse width	100			ns
t_{SCSU}	SYNC rising edge to CLK rising edge setup time	30			ns
t_{TCSU}	TDATA to CLK rising edge setup time	30			ns
t_{CTHD}	CLK rising edge to TDATA hold time	10			ns
t_{SYLW}	SYNC low pulse width	2			t_{CLK}
t_{STDAT}	Rising CLK after SYNC high to TDATA sample time		5		t_{CLK}
t_{TSOP}	TDATA sample to output update		4		t_{CLK}
t_{TDATA}	TDATA period		16		t_{CLK}

DEVICE INFORMATION

PW PACKAGE
TSSOP-16
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
CLK	1	Digital Input	4.096MHz master clock
TDATA	2	Digital Input	Bitstream digital data
SYNC	3	Digital Input	Synchronize control
DGND	4	Digital Ground	Digital ground
DVDD	5	Digital Supply	Digital power supply
GAIN0	6	Digital Input	Gain select 0
GAIN1	7	Digital Input	Gain select 1
GAIN2	8	Digital Input	Gain select 2
VREF	9	Analog Input	Voltage reference input
RREF	10	Analog	Full-scale range resistor
AVSS	11	Analog Supply	Negative analog power supply, V_{REF} common, R_{REF} common
AVDD	12	Analog Supply	Positive analog power supply
NC	13	—	No connection; do not connect externally.
IOUTN	14	Analog Output	Negative signal output current
IOUTP	15	Analog Output	Positive signal output current
$\overline{\text{PWDN}}$	16	Digital Input	Power-down control; active low

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +2.5V, AVSS = +2.5V, DVDD = +3.3V, CLK = 4.096MHz, V_{REF} = +5V, and R_{REF} = 30kΩ, unless otherwise noted. Data acquired using circuit configuration shown in Figure 35. THD and SNR measured by ADS1282 (1ms sampling and complement gain setting).

OUTPUT SPECTRUM

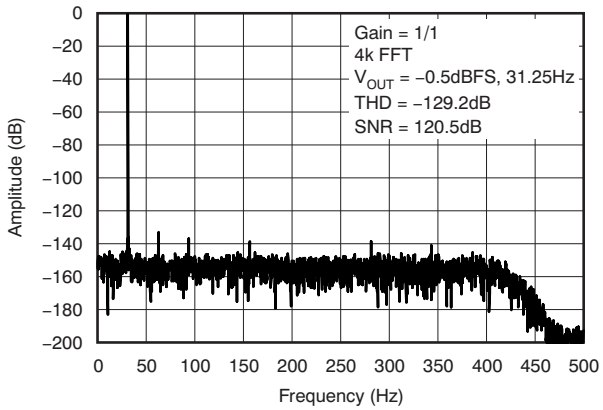


Figure 2.

OUTPUT SPECTRUM

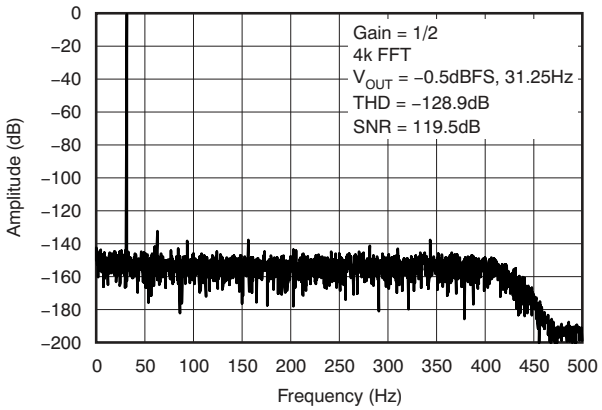


Figure 3.

OUTPUT SPECTRUM

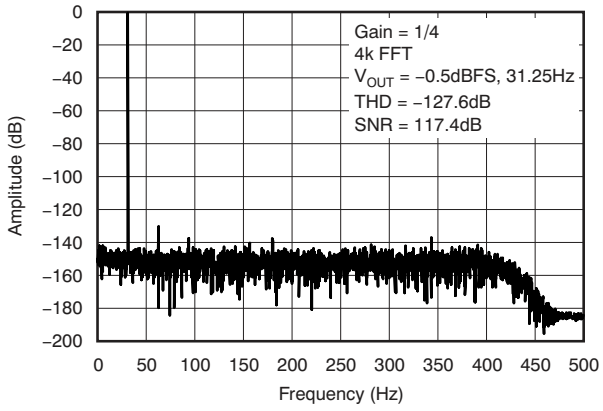


Figure 4.

OUTPUT SPECTRUM

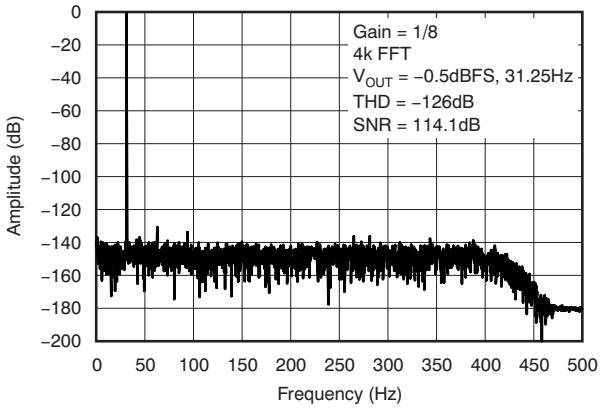


Figure 5.

OUTPUT SPECTRUM

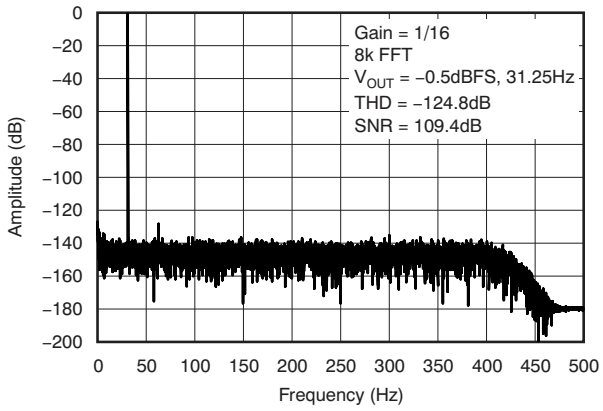


Figure 6.

OUTPUT SPECTRUM

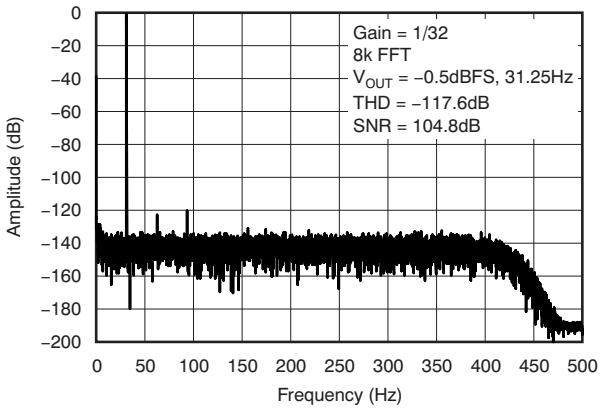


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = +2.5V, DVDD = +3.3V, CLK = 4.096MHz, V_{REF} = +5V, and R_{REF} = 30kΩ, unless otherwise noted. Data acquired using circuit configuration shown in Figure 35. THD and SNR measured by ADS1282 (1ms sampling and complement gain setting).

OUTPUT SPECTRUM

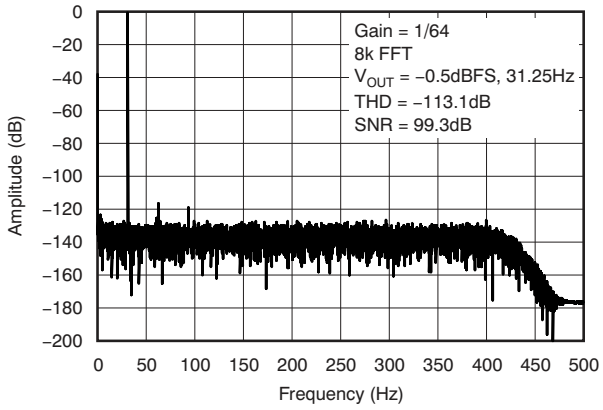


Figure 8.

GAIN MATCH HISTOGRAM

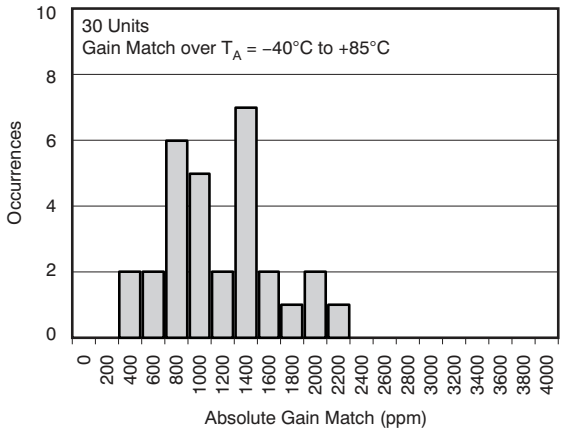


Figure 9.

GAIN ERROR vs TEMPERATURE

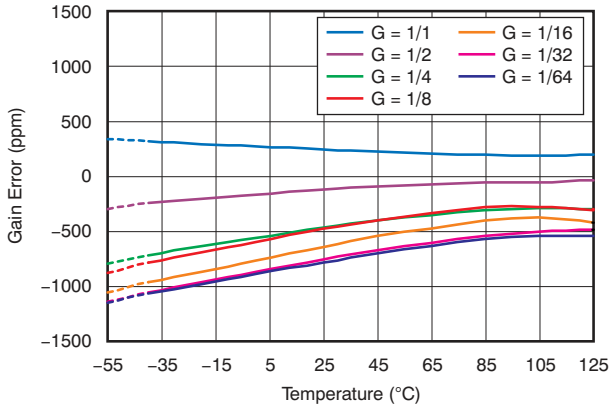


Figure 10.

GAIN ERROR HISTOGRAM

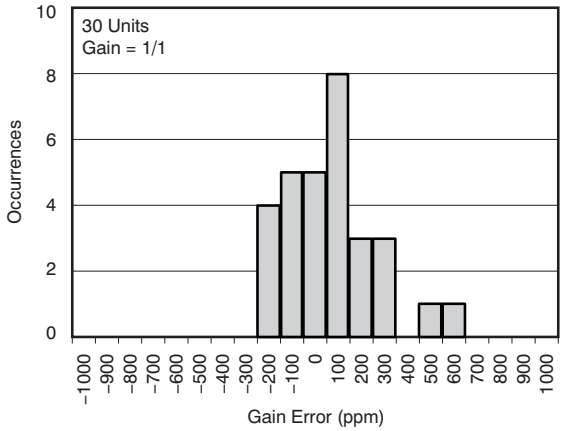


Figure 11.

OFFSET vs TEMPERATURE

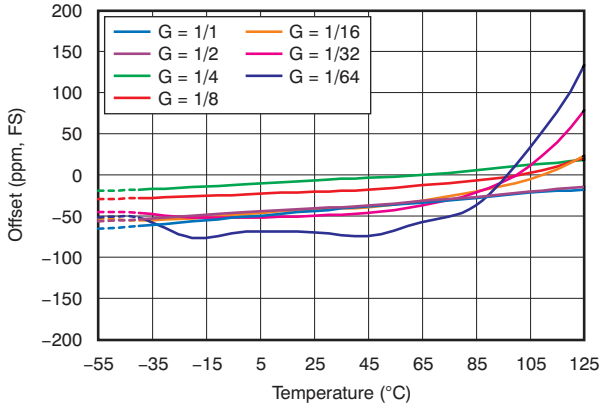


Figure 12.

OFFSET HISTOGRAM

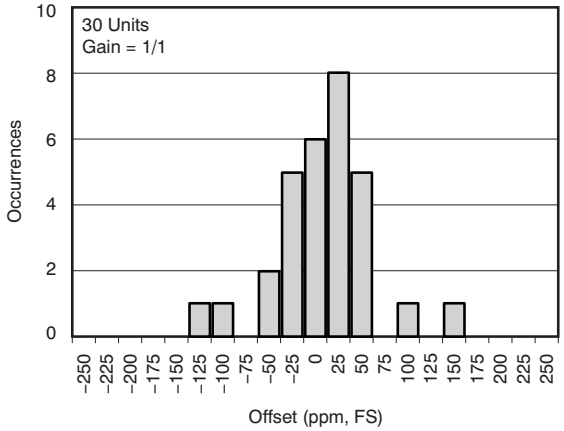


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = +2.5V, DVDD = +3.3V, CLK = 4.096MHz, V_{REF} = +5V, and R_{REF} = 30kΩ, unless otherwise noted. Data acquired using circuit configuration shown in Figure 35. THD and SNR measured by ADS1282 (1ms sampling and complement gain setting).

THD vs TEMPERATURE

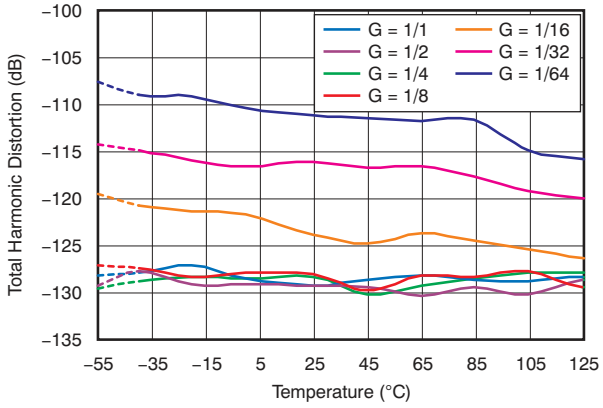


Figure 14.

SNR vs TEMPERATURE

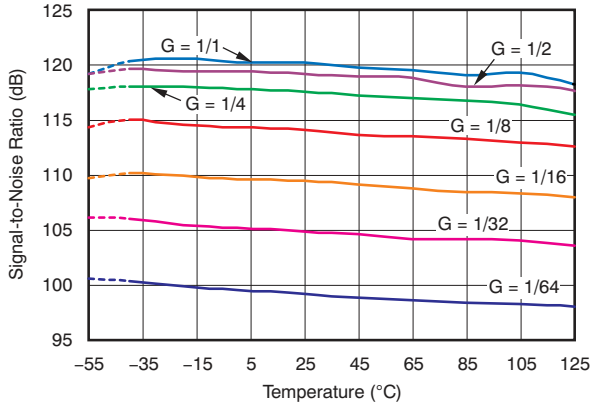


Figure 15.

THD vs OUTPUT FREQUENCY

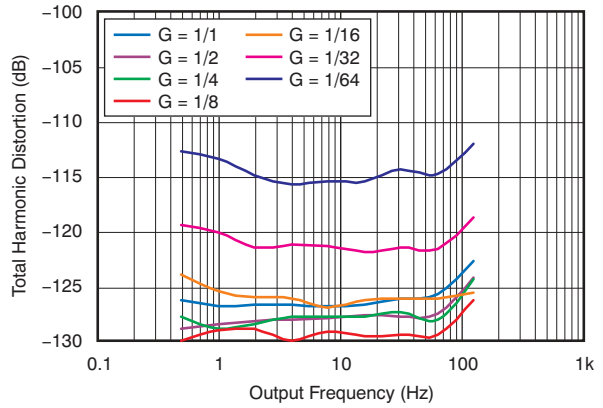


Figure 16.

SNR vs OUTPUT FREQUENCY

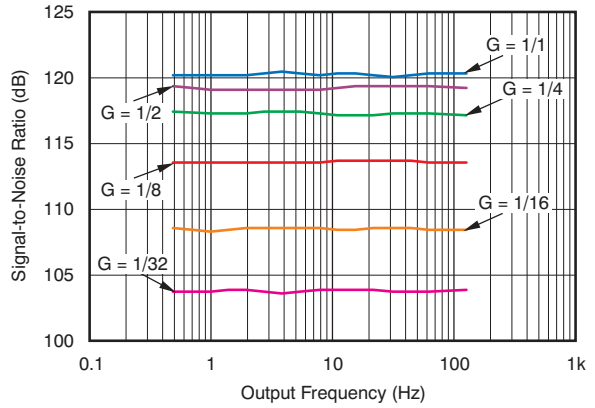
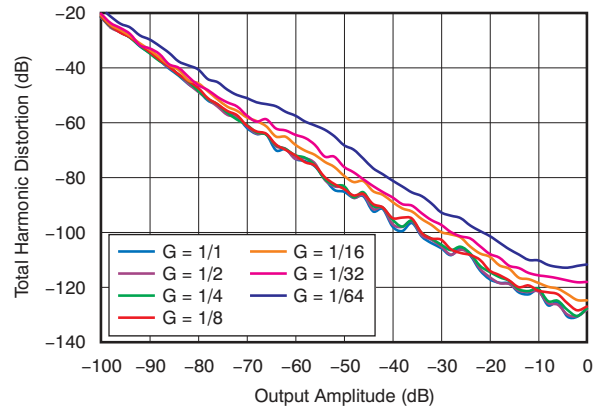


Figure 17.

THD vs OUTPUT AMPLITUDE(1)



(1) THD measurement noise limited for amplitudes less than –10dB.

Figure 18.

SNR vs OUTPUT AMPLITUDE

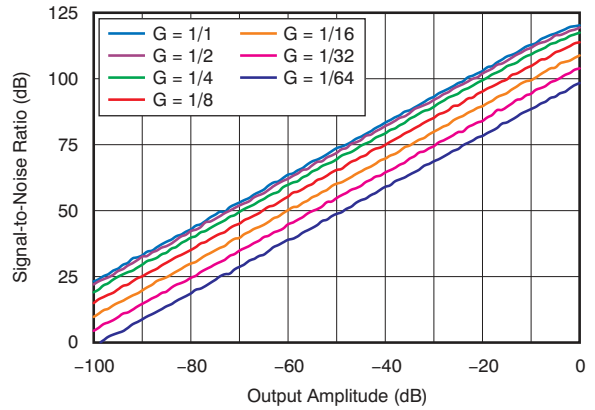


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = +2.5V, DVDD = +3.3V, CLK = 4.096MHz, V_{REF} = +5V, and R_{REF} = 30kΩ, unless otherwise noted. Data acquired using circuit configuration shown in Figure 35. THD and SNR measured by ADS1282 (1ms sampling and complement gain setting).

THD vs CLK

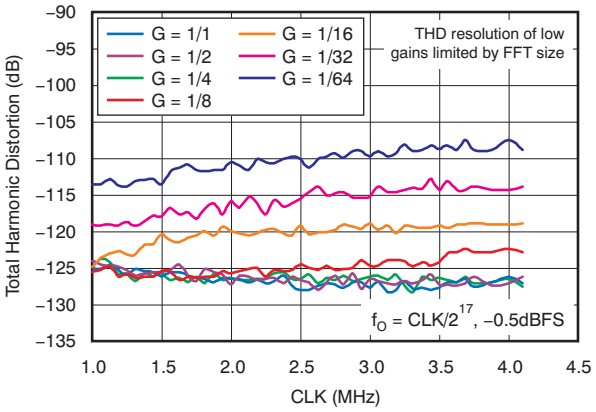


Figure 20.

SNR vs CLK

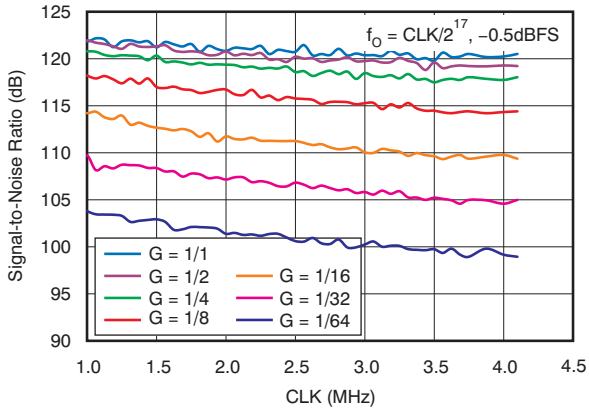


Figure 21.

THD vs V_{REF}

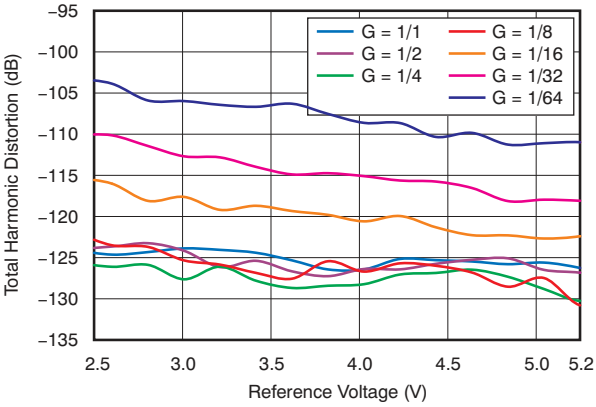


Figure 22.

SNR vs V_{REF}

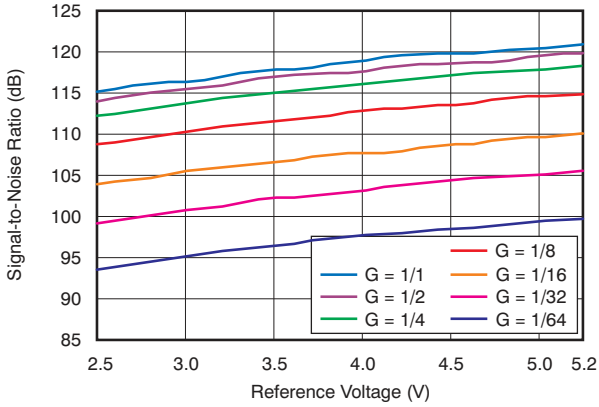


Figure 23.

THD HISTOGRAM

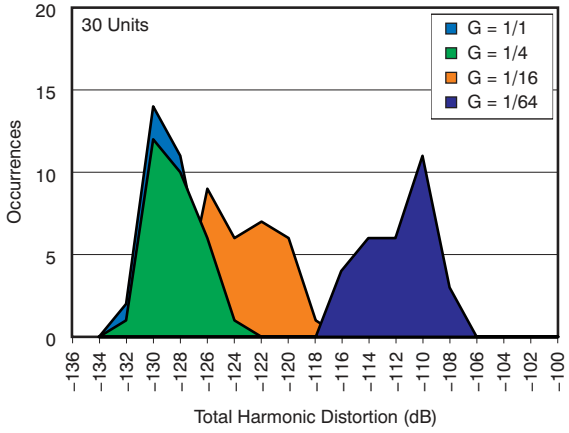


Figure 24.

ANALOG POWER-SUPPLY CURRENT vs TEMPERATURE

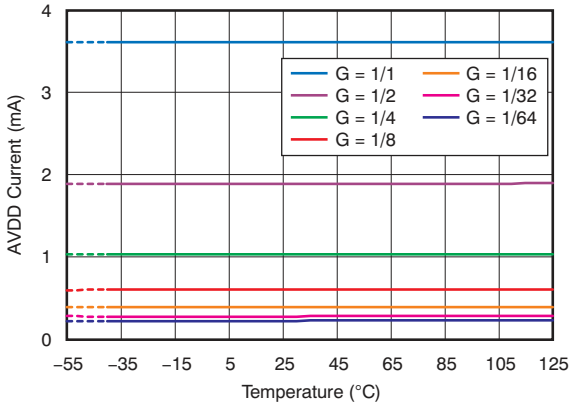


Figure 25.

DAC1280 OVERVIEW

The DAC1280 is a high-accuracy digital-to-analog converter (DAC) that provides outstanding THD performance together with low noise. The DAC1280 is suitable for the demanding requirements of energy exploration and precision instrumentation where a low-distortion test signal is needed.

Figure 26 shows the DAC1280 block diagram. The DAC provides a signal output proportional to a 1s density input. The DAC design is a multi-tap, current-steering filter that provides a differential current output. An external current-to-voltage (I-V) converter is required to provide a voltage output. V_{REF} and R_{REF} program the full-scale current, and GAIN[2:0] pins set the output range.

V_{REF} and R_{REF} establish an internal current that is mirrored to a multi-tap, current-steering filter stage through a reference current control block. The output of the control block is set by the GAIN[2:0] inputs, which fix the weighted tap currents in one of seven ranges. The magnitude of the tap currents results in the maximum differential output current ranges of 1250μA to the lowest range of 19.5μA.

The current-steering stage switches the tap current to either output, IOUTP or IOUTN, as a result of the sampling of TDATA. A higher 1s density directs more current toward IOUTP and less to IOUTN. Conversely, a higher density of 0s directs more current to IOUTN than to IOUTP. Steering of the output current yields an average output proportional to the 1s density input.

An integrated power-on-reset (POR) function resets the current taps, resulting in a zero differential output signal at power-up. The active low $\overline{PWDN}$ input powers down the device to a low-power (μW) state. The SYNC input synchronizes the DAC1280 TDATA sampling.

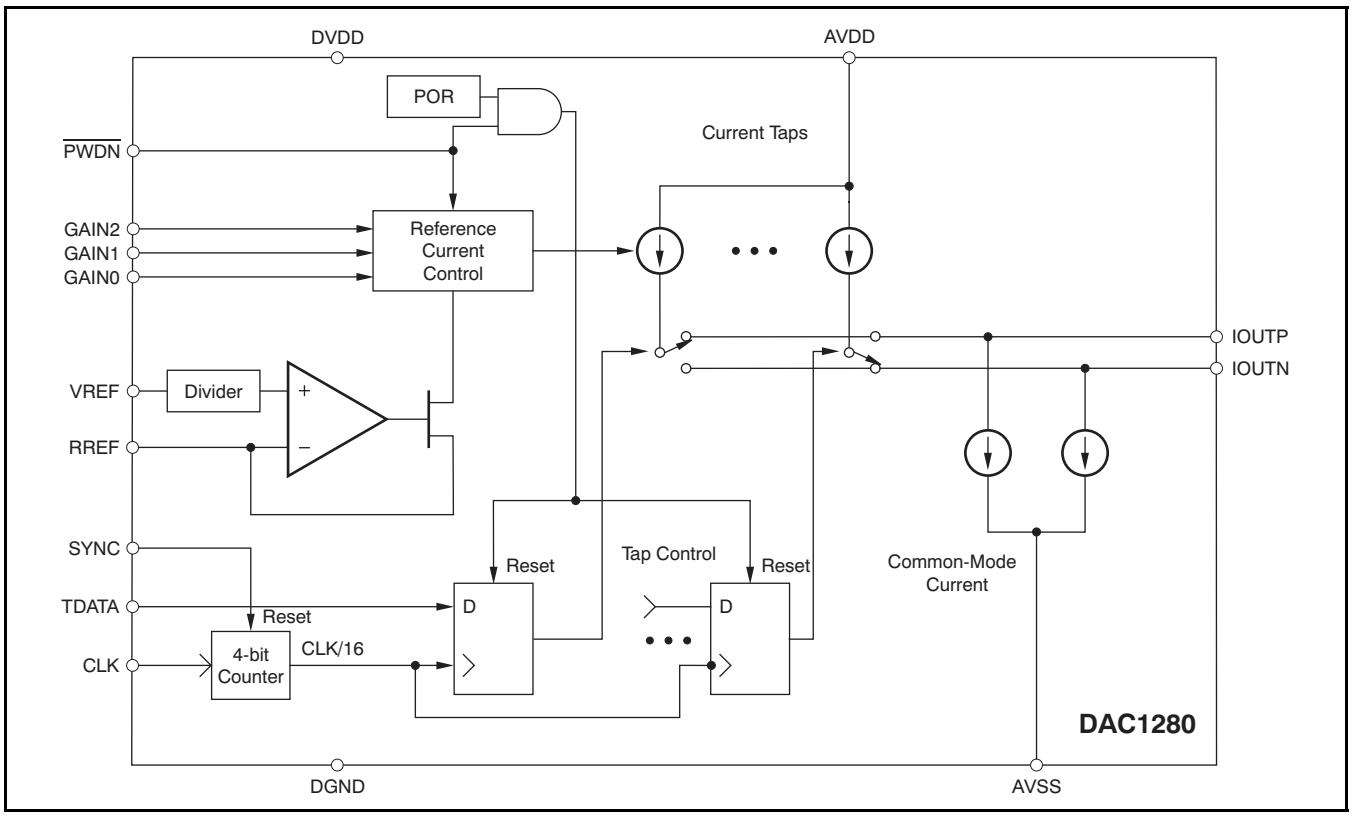
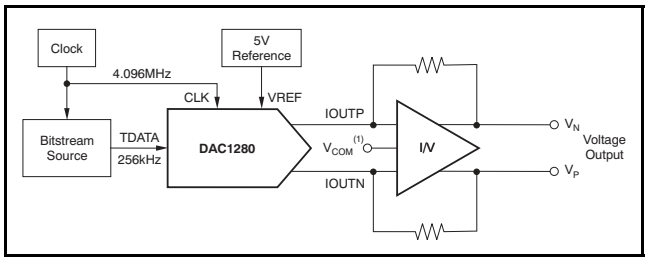


Figure 26. DAC1280 Block Diagram

DAC1280 Basics

The basic requirements of DAC1280 operation are a clock, a bitstream input, an external current-to-voltage converter, and a reference voltage. The bitstream originates either from an FPGA-based digital modulator or playback from a ROM device holding a stored bitstream file. The external reference voltage is +5V and should be precision (low drift and low noise). The current-to-voltage converter is an active circuit. The amplifiers used for the current-to-voltage converter should have good dynamic characteristics (low THD) with low noise. Figure 27 illustrates the system block diagram.



(1) V_{COM} = midsupply voltage.

Figure 27. DAC1280 System Block Diagram

Output Voltage

As shown in the system block diagram, the external I/V circuit converts the current output of the DAC to a voltage output. The voltage output of the I/V circuit is differential, as shown in Figure 28. The common-mode output voltage (V_{COM}) at the I/V circuit is normally set to the midsupply point of the DAC. The differential output voltage is ±2.5V/gain.

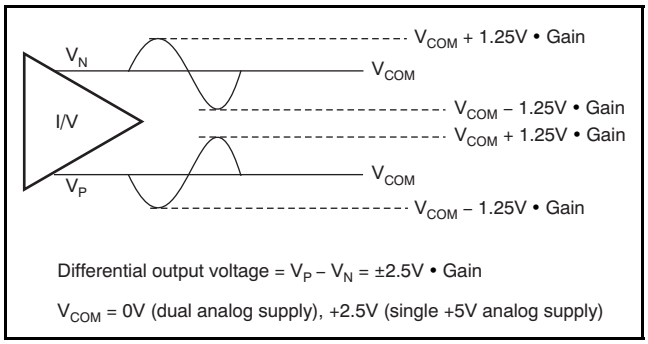


Figure 28. I/V Converter Output Voltage

Output Scaling

The full-scale output of the DAC1280 is set by the reference voltage and an external reference resistor. The GAIN[2:0] control pins select one of seven output ranges. In operation, the reference voltage and reference resistor are usually fixed, and the DAC output range is selected by the gain pins.

The DAC1280 differential output current is determined by Equation 1:

$$\text{Differential Output Current} = 7.5 \bullet \frac{V_{REF}}{R_{REF}} \bullet \text{Gain} \bullet \frac{(\text{TDATA} - 50\%)}{25\%} \quad (1)$$

Where:

- V_{REF} = 5V (nominal)
- R_{REF} = 30kΩ (nominal)
- Gain = 1/1 to 1/64
- TDATA = TDATA 1s density, ranging 25% to 75%

The DAC full-scale output can be fine-trimmed, if desired, by changing the $\frac{V_{REF}}{R_{REF}}$ ratio from the nominal values of V_{REF} = 5V and R_{REF} = 30kΩ. See the Electrical Characteristics for the adjustment range.

The external current-to-voltage converter scales the DAC output current into an output voltage. Table 1 shows the DAC1280 gain (differential output current to bitstream density) and the resulting output voltage of the external current-to-voltage converter.

Table 1. DAC1280 Ideal Output Scaling(1)

TDATA 1s DENSITY (%)	IOUTP – IOUTN (μA)	$V_P - V_N$ (V)
25	–1250 ● Gain	–2.5 ● Gain
37.5	–625 ● Gain	–1.25 ● Gain
50	0	0
62.5	+625 ● Gain	+1.25 ● Gain
75	+1250 ● Gain	+2.5 ● Gain

(1) V_{REF} = 5V, R_{REF} = 30kΩ, external current-to-voltage converter resistors = 2kΩ. Output current and voltage are differential. Excludes the effects of DAC1280 offset, gain and linearity errors, errors in reference voltage, errors as a result of external resistors, and errors from the external current-to-voltage conversion. Refer to Figure 27.

VREF Reference Voltage Input

The DAC1280 requires an external reference for operation. The reference voltage of the DAC1280 is defined as the voltage difference between VREF and AVSS (that is, V_{REF} = VREF – AVSS). The DAC1280 output directly scales with V_{REF}; consequently, noise or drift on the reference appear at the DAC1280 output. A low-drift and low-noise precision reference is recommended for best performance.

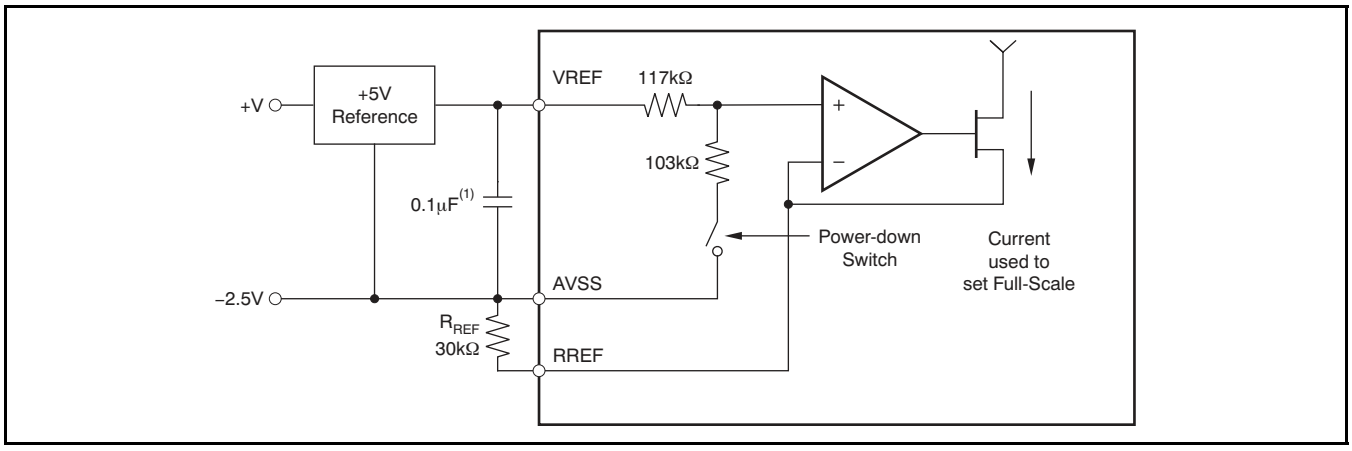
For best layout, connect the ground pin of the external reference directly to the AVSS terminal to minimize possible crosstalk. A recommended 0.1μF ceramic capacitor connected directly across VREF and AVSS reduces noise susceptibility.

Figure 29 shows the reference input voltage and reference resistor connection to the DAC1280. The DAC1280 loads VREF with 220kΩ. The 220kΩ resistor disconnects in power-down mode.

RREF Reference Resistor

A 30kΩ resistor, connected from VREF to AVSS, is required for operation. This resistor, in combination with VREF, is used to set the DAC full-scale output. The resistor can be used to fine-trim the DAC gain by changing the value from the nominal 30kΩ. See the *Output Scaling* section for more information.

The external resistor accuracy and temperature drift directly affect the DAC1280 output accuracy. A low-drift, precision resistor is recommended for best performance. Connect the resistor directly to the RREF and AVSS pins using short and direct traces. Keep RREF stray capacitance to a minimum. Refer to Figure 29 for the reference input connection.



(1) Recommended noise capacitor.

Figure 29. Reference Input Connection

Pin Descriptions

GAIN[2:0] Pins

The DAC1280 output range can be set in 6dB steps, controlled by three digital inputs. The ranges match the gains of the ADS1282 for testing at all gains. Table 2 shows the output range versus gain settings for the DAC1280.

NOTE: It is recommended that the DAC and ADC use complementary gains when testing. ADC instability may result because of the combination of the noise-shaped DAC input and if the ratio of ADC/DAC gain is greater than 2.

IOUTP, IOUTN

IOUTP and IOUTN are the differential current outputs. The outputs are intended to be used in conjunction with an external current-to-voltage converter, as shown in the circuit of Figure 35. Note that the current-to-voltage converter also sets the DAC1280 DAC output common-mode voltage. See specifications for the allowable common-mode output voltage.

CLK

CLK is the master clock input to the DAC1280 (nominally 4.096MHz). As with any high-performance ADC or DAC, a high-quality, low-jitter clock source is essential. A crystal oscillator clock source is recommended. Make sure to avoid excess ringing on the clock input: keeping the printed circuit board (PCB) trace short, and using source termination resistors (20Ω to 50Ω) placed close to the source end, often helps.

TDATA

TDATA is the digital signal input and determines the output frequency and amplitude. TDATA is encoded as a 1s density bitstream where the DAC1280 output is proportional to the 1s density. When the 1s density input is 75% (that is, on average, three out of four TDATA bits are '1'), the differential output current is at a positive maximum value; when the 1s density input is at 25% (on average, three out of four TDATA bits are '0'), the differential output current is at a negative maximum value. When the 1s density is 50% (on average, an equal number of '1's and '0's), the differential output current is 0. See Table 1.

TDATA is sampled by the DAC1280 at CLK/16 rate (nominally 256kHz with 4.096MHz master clock), and therefore, the sampling of TDATA can have 16 CLK cycles of uncertainty. SYNC can be used to eliminate the uncertainty by synchronizing TDATA sampling. Synchronizing TDATA sampling yields a consistent test signal phase response.

SYNC

SYNC is an input used to synchronize the CLK cycle at which the DAC1280 samples TDATA. When SYNC is low, the internal CLK is disabled (ignoring TDATA input), and the DAC output is held constant. When SYNC is taken high, the DAC resumes sampling TDATA on the sixth rising CLK edge after SYNC is high. TDATA is then sampled on periodic 16 CLK intervals. Four CLK cycles propagate from the TDATA sample to the physical update of the DAC output. If SYNC is not used, tie SYNC high. Refer to Figure 1 for an illustration of the SYNC timing sequence.

$\overline{\text{PWDN}}$

$\overline{\text{PWDN}}$ is an input used to power down the DAC1280. To power down the device, take the $\overline{\text{PWDN}}$ pin low. In power-down mode, the device bias is disabled and the outputs are Hi-Z. Note that the digital inputs must remain defined in power-down mode either as logic low or logic high; do not float the inputs. Disable the CLK and TDATA inputs to minimize power-supply leakage. To exit power-down mode, take $\overline{\text{PWDN}}$ high. The DAC1280 output is reset to zero when the $\overline{\text{PWDN}}$ pin goes high.

Table 2. Differential Current Output vs Gain Setting(1)

GAIN[2:0] PINS	GAIN	GAIN (dB)	IOUTP – IOUTN (μA)	$V_P - V_N$ (V)
000	1/1	0	±1250	±2.5
001	1/2	–6	±625	±1.25
010	1/4	–12	±312	±0.625
011	1/8	–18	±156	±0.312
100	1/16	–24	±78.1	±0.156
101	1/32	–30	±39.1	±0.0781
110	1/64	–36	±19.5	±0.0391

(1) TDATA 1s density 25%/75%, V_{REF} = 5V, R_{REF} = 30kΩ, external current-to-voltage converter resistors = 2kΩ. Output current and voltage are differential. Excludes the effects of DAC1280 offset, gain and linearity errors, errors in reference voltage, errors caused by external resistors, and errors as a result of external current-to-voltage conversion. See Figure 27.

Power Supplies

The DAC1280 has two power supplies, analog and digital. The analog supply is 5V and can be configured for bipolar operation (with AVDD = 2.5V and AVSS = –2.5V), or configured for unipolar operation (with AVDD = 5V and AVSS grounded). The common-mode voltage of the external I/V converter is normally set to the DAC1280 midsupply.

Because AVSS is shared with the reference low terminal, and the analog supply pins draw signal-dependent current, the external reference ground terminal should connect to AVSS using a *star* connection close to the DAC. This approach helps to minimize power-supply coupling to the reference input.

DVDD is the digital supply and operates over the range of 1.65V to 3.6V. Bypass the DVDD as well as the analog supplies with a capacitor (minimum 1μF).

The power supplies can be sequenced in any order. At power-on, the latter occurrence of DVDD exceeding 1V, or (AVDD – AVSS) exceeding 3V, causes an internal power-on reset (POR) to occur. A POR resets the output to zero. After reset, the first sampling of TDATA by the DAC1280 occurs on the sixth CLK rising edge, as Figure 30 shows.

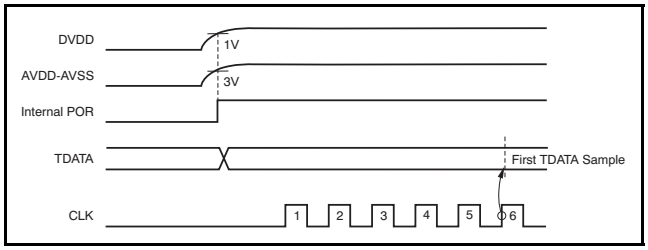


Figure 30. Power-On Sequence

Power Consumption

The total power consumption is the power consumed by the DAC1280 plus that of the external current-to-voltage converter. The power consumption of the DAC1280, in turn, depends on the gain setting. Table 3 summarizes the DAC1280 power consumption.

Table 3. DAC1280 Power Consumption

GAIN	DAC1280 POWER (mW)
1/1	18
1/2	9.6
1/4	5.3
1/8	3.1
1/16	2.1
1/32	1.5
1/64	1.2

Offset and Gain Error

The DAC1280 features low offset error (±50ppmFS, typical) and low gain error (±0.02%, gain = 1/1, typical). Gain match is specified as the maximum error of gain = 1/1 relative to gains 1/2 to 1/64 of a single device. Typical gain match error is ±0.1%.

Offset and gain drift are also very low for the DAC1280. Drift is calculated using the box calculation method:

$$\text{Drift calculation: } \frac{\text{Max} - \text{Min}}{\text{Temp Range}} \quad (\text{ppm}/^{\circ}\text{C}) \tag{2}$$

Where Max and Min are respectively the maximum and minimum offset or gain errors (in ppm) recorded over the specified temperature range of –40°C to +85°C.

Noise Performance (SNR)

The DAC1280 achieves excellent signal-to-noise ratio (SNR) performance. The SNR figures were obtained using the circuit of Figure 35. SNR is measured by the ADS1282 over a bandwidth of 0 to 413Hz (with 1ms sampling). The ADC and DAC have complementing gains for each measurement.

SNR is measured with a signal output of –0.5dBFS and 31.25Hz, then taking the Fast Fourier Transformation (FFT) of the ADC data, and calculating the noise power over the specified bandwidth. The dc, fundamental, and harmonic bins are removed for the SNR calculations. Measured this way, SNR is the combination of the individual noise sources including ADC noise, DAC1280 noise, voltage and current noise of the external op amp, and thermal noise of the I/V resistors.

If desired, SNR can be improved by decreasing the 2kΩ I/V feedback resistors and then applying correspondingly higher DAC1280 gains. Decreasing the resistor values results in a decrease of the maximum output amplitude as shown in Figure 31, SNR versus output amplitude for I/V resistor values of 2kΩ, 1kΩ, and 500Ω. If decreasing the I/V feedback resistor, increase the I/V capacitor proportionally to maintain the same low-pass corner frequency.

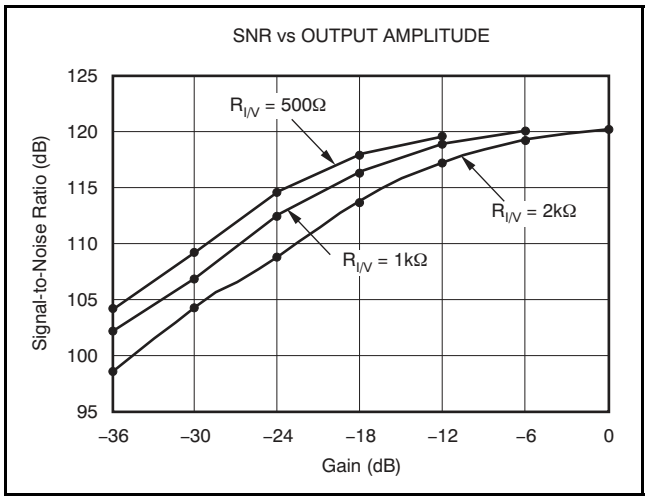


Figure 31. SNR vs Output Amplitude

DC Noise

DC noise is measured by the ADS1282 with the circuit configuration of Figure 35. The measurement bandwidth is 413Hz and the ADC is set to a complementing gain. The measurement is taken with a 50% 1s density input that results in a 0V differential signal output. DC noise is the standard deviation (RMS, referred to output).

Total Harmonic Distortion (THD)

The DAC1280 achieves excellent THD performance. THD was characterized using the circuit shown in Figure 35 and the ADS1282 with complementary ADC gain settings for each DAC gain. Note that a low-distortion op amp for current-to-voltage conversion (such as the OPA211) is essential in order to achieve rated performance.

Settling Time

The settling time of the DAC1280 resulting from a step input change consists of the DAC1280 settling time and the I/V filter settling time. Other filter components used in the DAC signal path may also add to the settling time.

When a step input is applied to TDATA, the DAC output begins to change. The DAC completely settles in 78μs (CLK = 4.096MHz). As the DAC output is settling, the I/V filter network is also settling. The suggested I/V RC components (R = 2kΩ, C = 1nF) result in an I/V time constant of approximately 2μs. Figure 32 shows the composite step response of the circuit in Figure 35.

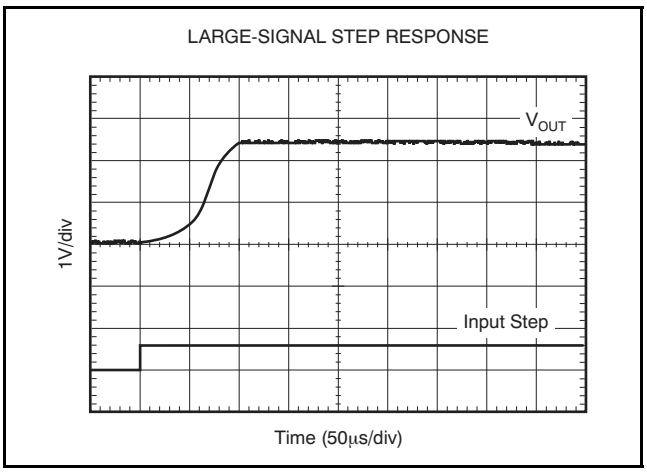


Figure 32. DAC1280 Large-Signal Step Response (Noise Removed for Clarity)

Frequency Response

The DAC1280 low-pass filters the bitstream input, resulting in a sinc2 frequency response profile with the first notch (zero) located at $f_{CLK}/160$ (25.6kHz with CLK = 4.096MHz). However, the aspect of noise shaping of the digital modulator may result in rising noise versus frequency. This rising noise may limit the usable bandwidth to less than the DAC inherent bandwidth. Figure 33 illustrates the DAC1280 frequency response.

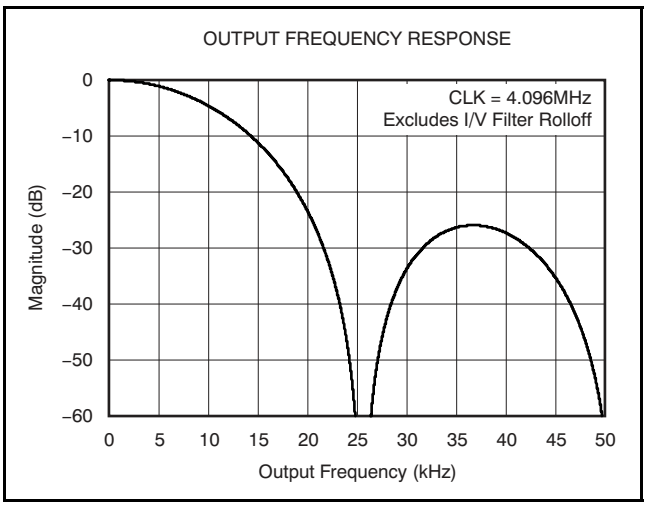


Figure 33. Output Frequency Response

Seismic System

Figure 34 illustrates an example of a three-channel seismic measurement system that consists of the DAC1280 and three ADS1282s.

The DAC1280 drives the ADS1282s and the geophone sensors for testing. The DAC signal can be routed through the ADS1282 input mux to the geophone or routed through an external switch network. The DAC input signal is sourced from a bitstream pattern stored in the device flash memory (as shown here), or supplied directly from a bitstream modulator implemented in an FPGA.

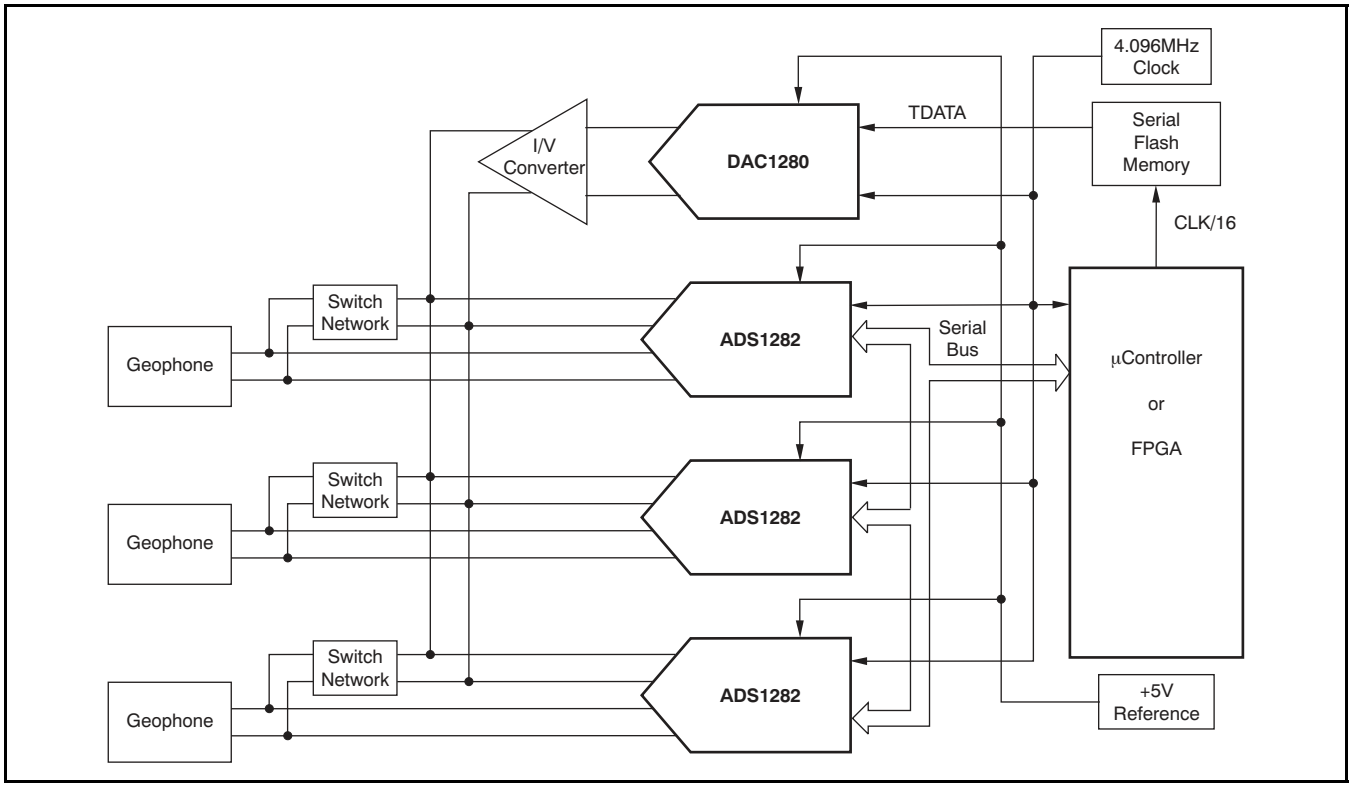


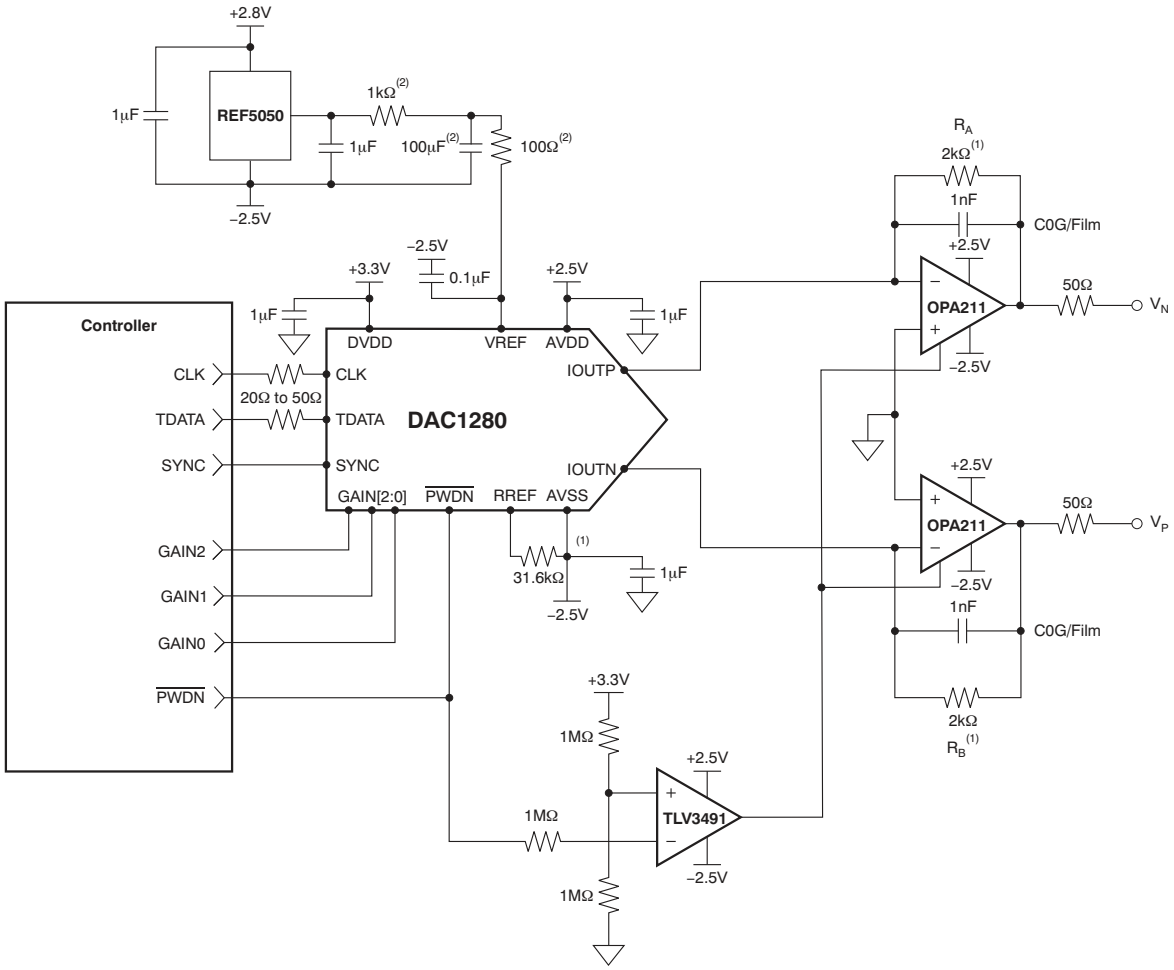
Figure 34. Three-Channel Seismic System Block Diagram

Basic Connection

Figure 35 shows a basic connection of the DAC1280, with an external op amp current-to-voltage converter. Bipolar analog supplies are shown (±2.5V). Single-supply operation (+5V) is also possible by grounding AVSS; for single-supply operation, bias the current-to-voltage converter noninverting terminals to midsupply.

A low-noise, low-drift, precision reference is recommended for operation with the DAC1280, such as the REF5050. The REF5045 or REF02 are also suitable, depending on the end system SNR requirements. The REF5045 operates from a minimum 5V power supply; the REF5050 operates from a minimum 5.3V power supply; and the REF02 operates from a minimum 8.5V power supply. The optional reference RC filter reduces broadband reference noise. Using the filter network, loading of the VREF input results in –0.5% gain error. The reference bias resistor is a 31.6kΩ precision resistor. Increasing the resistor value (from 30kΩ nominal) reduces the DAC full-scale output by –0.5db, to avoid clipping of the ADC. The filter series resistance and the VREF input impedance interaction results in a gain error of –0.5%

Two OPA211s and R_A, R_B implement the current-to-voltage converter. R_A and R_B scale the DAC current output to a voltage output. 1nF capacitors filter the DAC sampling noise, and 50Ω resistors isolate the op amp from capacitive loads. Place the current-to-voltage converter circuit components close to the DAC1280 using a symmetrical layout. A comparator, such as the TLV3491, translates the PWDN logic level signal to the OPA211 level requirements.



(1) Precision resistors.

(2) Optional reference noise filter.

Figure 35. Basic Connection

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC1280IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DAC1280	Samples
DAC1280IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DAC1280	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

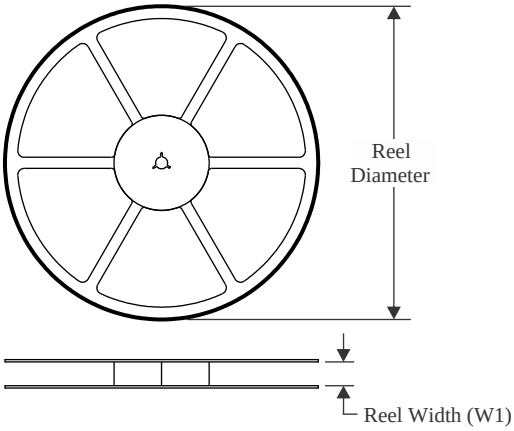
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

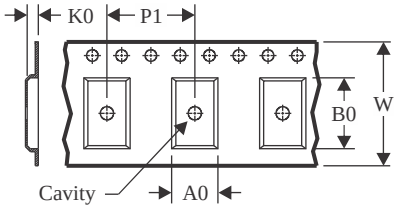
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

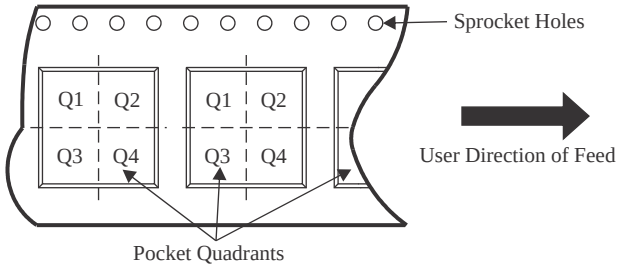


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

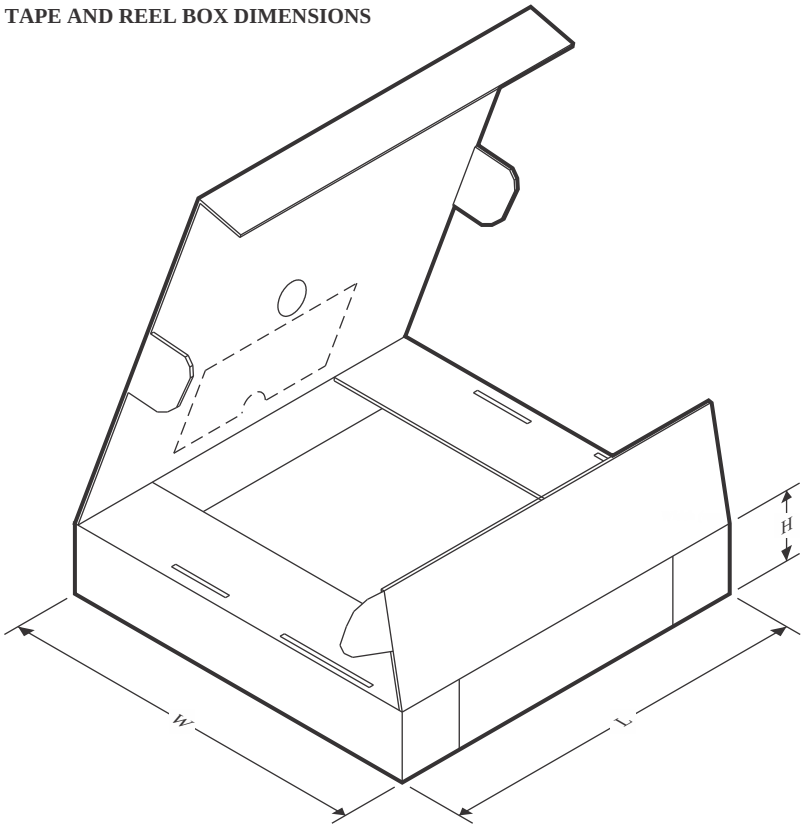
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC1280IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

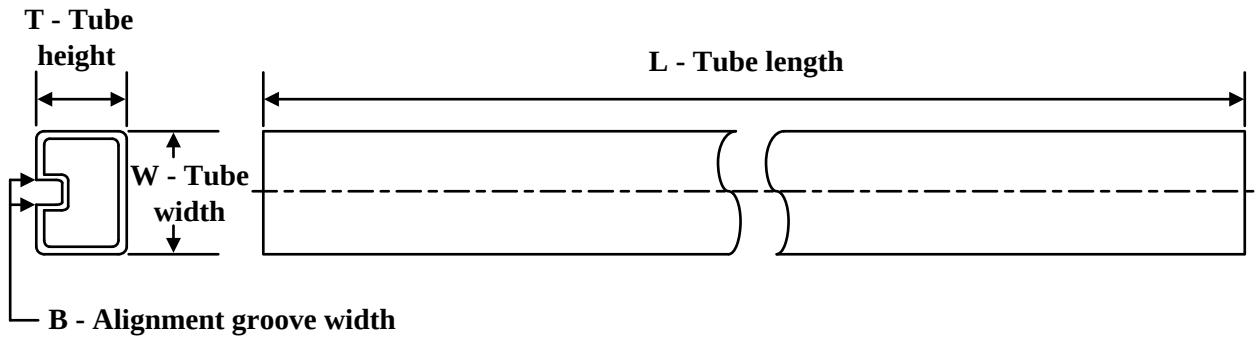
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC1280IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE

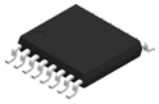


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC1280IPW	PW	TSSOP	16	90	530	10.2	3600	3.5

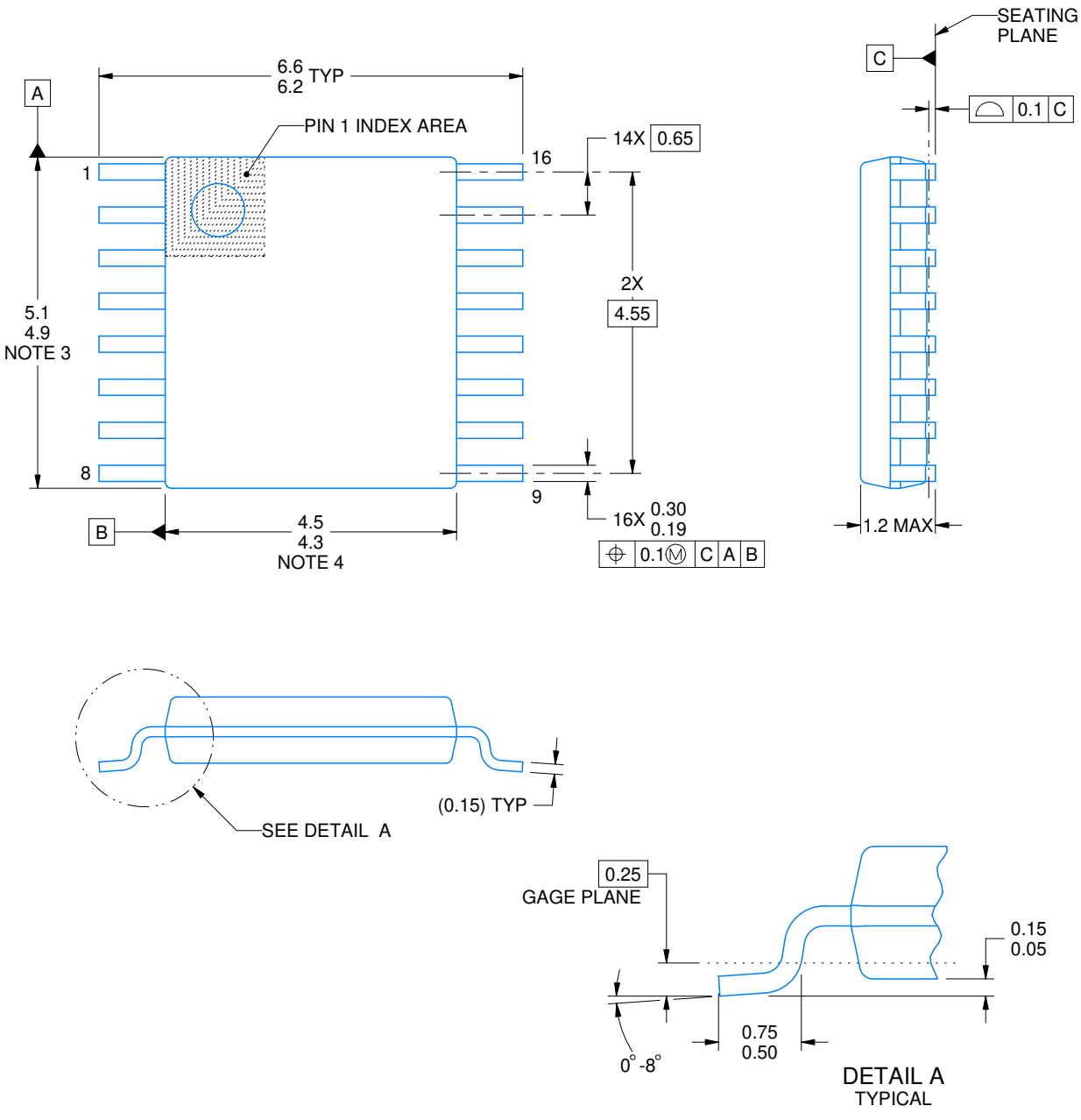
PACKAGE OUTLINE

PW0016A



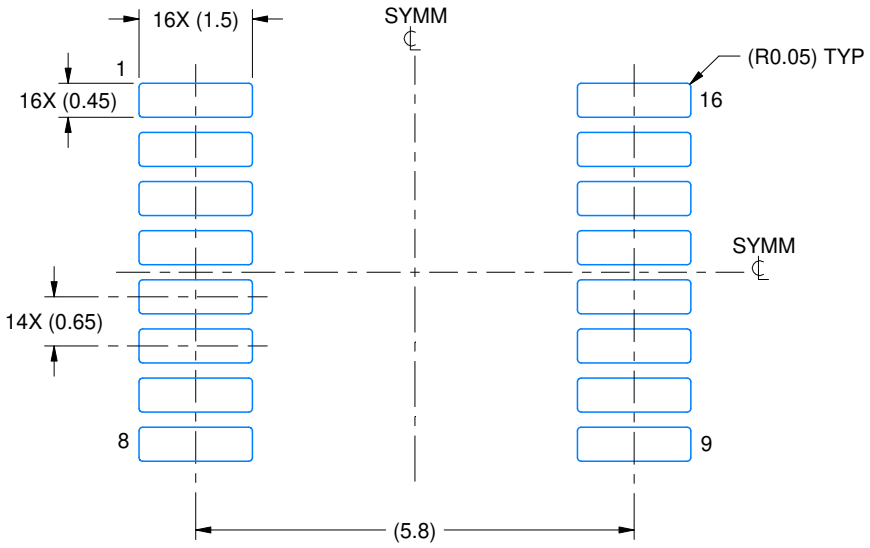
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

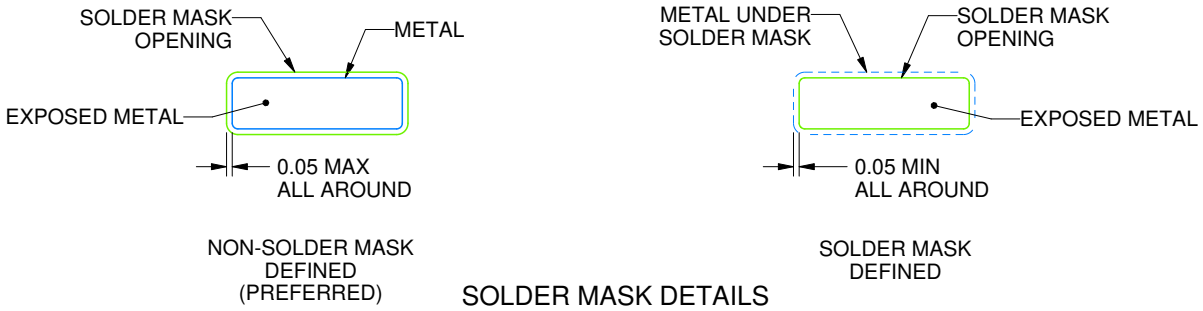


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

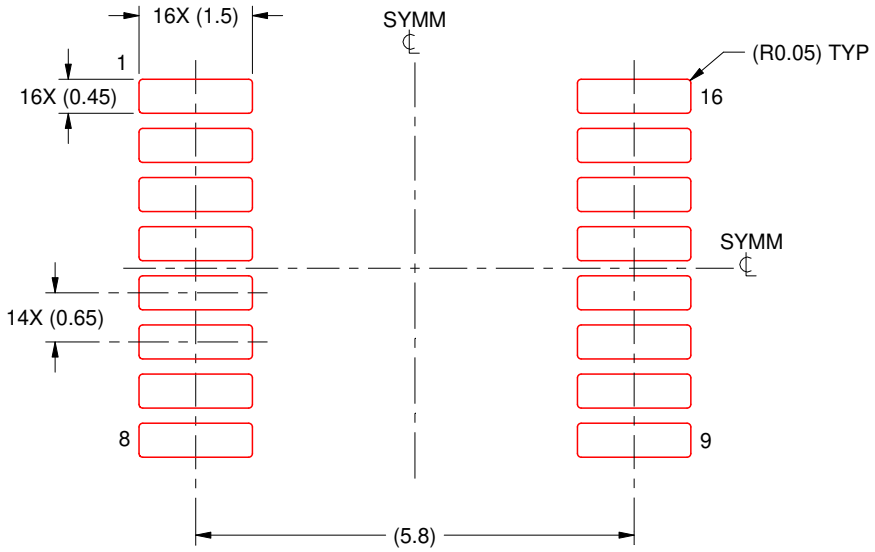


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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