20 V, 6 A Synchronous Step-Down Regulator with Low-Side Driver

Data Sheet

ADP2381

FEATURES

- Input voltage: 4.5 V to 20 V
- Integrated 44 mΩ high-side MOSFET
- 0.6 V ± 1% reference voltage over temperature
- Continuous output current: 6 A
- Programmable switching frequency: 250 kHz to 1.4 MHz
- Synchronizes to external clock: 250 kHz to 1.4 MHz
- 180° out-of-phase synchronization
- Programmable UVLO
- Power-good output
- External compensation
- Internal soft start with external adjustable option
- Startup into a precharged output
- Supported by ADIsimPower design tool

APPLICATIONS

- Communication infrastructure
- Networking and servers
- Industrial and instrumentation
- Healthcare and medical
- Intermediate power rail conversion
- DC-to-dc point of load application

TYPICAL APPLICATIONS CIRCUIT

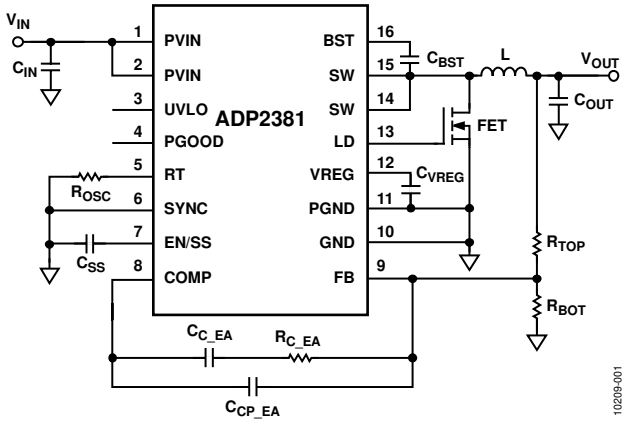

Figure 1.

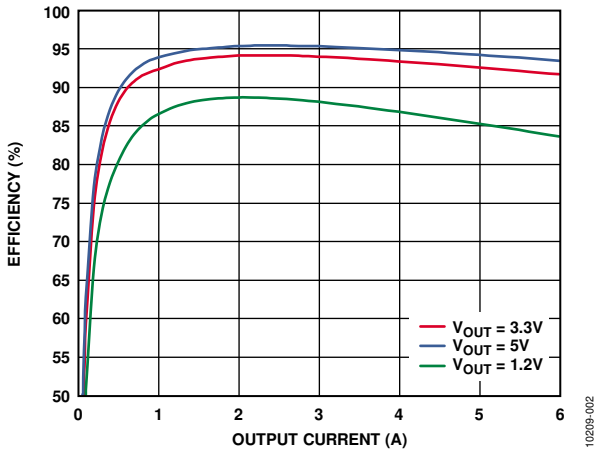

Figure 2. ADP2381 Efficiency vs. Output Current, V_{IN} = 12 V, f_{SW} = 250 kHz

GENERAL DESCRIPTION

The ADP2381 is a current mode control, synchronous, step-down, dc-to-dc regulator. It integrates a 44 mΩ power MOSFET and a low-side driver to provide a high efficiency solution. The ADP2381 runs from an input voltage of 4.5 V to 20 V and can deliver 6 A of output current. The output voltage can be adjusted to 0.6 V to 90% of the input voltage. The switching frequency of the ADP2381 can be programmed from 250 kHz to 1.4 MHz or fixed at 290 kHz or 550 kHz. The synchronization function allows the switching frequency to be synchronized to an external clock to minimize system noise.

External compensation and an adjustable soft start provide design flexibility. The power-good output provides simple and reliable power sequencing. Additional features include programmable undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP), and thermal shutdown (TSD).

The ADP2381 operates over the −40°C to +125°C junction temperature range and is available in a 16-lead TSSOP_EP package.

Rev. 0

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TABLE OF CONTENTS

REVISION HISTORY

3/12—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = 12 V, T_J = −40°C to +125°C for min/max specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
PVIN						
PVIN Voltage Range	V_{PVIN}		4.5		20	V
Quiescent Current	I_Q	No switching	2	2.8	3.5	mA
Shutdown Current	I_{SHDN}	EN/SS = GND	80	130	170	µA
PVIN Undervoltage Lockout Threshold		PVIN rising		4.3	4.5	V
		PVIN falling	3.7	3.9		V
FB						
FB Regulation Voltage	V_{FB}	0°C < T_J < 85°C	0.594	0.6	0.606	V
		−40°C < T_J < +125°C	0.591	0.6	0.609	V
FB Bias Current	I_{FB}			0.01	0.1	µA
ERROR AMPLIFIER (EA)						
Transconductance	g_m		360	500	620	µS
EA Source Current	I_{SOURCE}		40	60	80	µA
EA Sink Current	I_{SINK}		40	60	80	µA
INTERNAL REGULATOR (VREG)						
VREG Voltage	V_{VREG}	V_{PVIN} = 12 V, I_{VREG} = 50 mA	7.6	8	8.4	V
Dropout Voltage		V_{PVIN} = 12 V, I_{VREG} = 50 mA		350		mV
Regulator Current Limit			65	100	135	mA
SW						
High-Side On Resistance[1]		$V_{BST} - V_{SW}$ = 5 V		44	70	mΩ
High-Side Peak Current Limit			7.7	9.6	11.5	A
Negative Current-Limit Threshold Voltage[2]				20		mV
SW Minimum On Time	t_{MIN_ON}			120	170	ns
SW Minimum Off Time	t_{MIN_OFF}			200	300	ns
LOW-SIDE DRIVER (LD)						
Rising Time[2]	t_R	C_{DL} = 2.2 nF; see Figure 17		20		ns
Falling Time[2]	t_F	C_{DL} = 2.2 nF; see Figure 20		10		ns
Sourcing Resistor				4	6	Ω
Sinking Resistor				2	3.5	Ω
BST						
Bootstrap Voltage	V_{BOOT}		4.5	5	5.7	V
OSCILLATOR (RT PIN)						
Switching Frequency	f_{SW}	RT pin connected to GND	210	290	360	kHz
		RT pin open	400	550	690	kHz
		R_{OSC} = 100 kΩ	425	500	570	kHz
Switching Frequency Range	f_{SW}		250		1400	kHz
SYNC						
Synchronization Range			250		1400	kHz
SYNC Minimum Pulse Width			100			ns
SYNC Minimum Off Time			100			ns
SYNC Input High Voltage			1.3			V
SYNC Input Low Voltage					0.4	V
EN/SS						
Enable Threshold					0.5	V
Internal Soft Start				1500		Clock cycles
SS Pin Pull-Up Current	I_{SS_UP}		2.6	3.3	4	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER GOOD (PGOOD)						
PGOOD Range		FB rising threshold		95		%
		FB falling threshold		90		%
PGOOD Deglitch Time		PGOOD from low to high		1024		Clock cycles
		PGOOD from high to low		16		Clock cycles
PGOOD Leakage Current		V_{PGOOD} = 5 V		0.01	0.1	µA
PGOOD Output Low Voltage		I_{PGOOD} = 1 mA		125	200	mV
UVLO						
Rising Threshold				1.2	1.28	V
Falling Threshold			1.02	1.1		V
THERMAL						
Thermal Shutdown Threshold				150		°C
Thermal Shutdown Hysteresis				25		°C

[1] Pin-to-pin measurement.
[2] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
PVIN, PGOOD	−0.3 V to +22 V
SW	−1 V to +22 V
BST	V_{SW} + 6 V
UVLO, FB, EN/SS, COMP, SYNC, RT	−0.3 V to +6 V
VREG, LD	−0.3 V to +12 V
PGND to GND	−0.3 V to +0.3 V
Operating Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

THERMAL INFORMATION

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
16-lead TSSOP_EP	39.48	°C/W

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in circuit board (4-layer, JEDEC standard board) for surface-mount packages.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

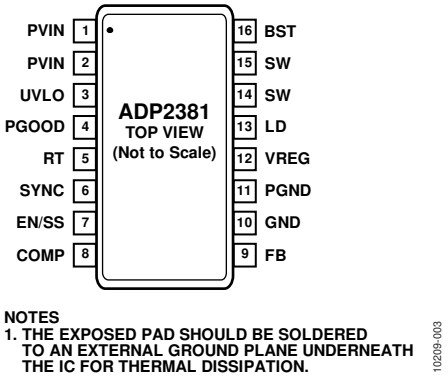

Figure 3. Pin Configuration (Top View)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2	PVIN	Power Input. Connect to the input power source and connect a bypass capacitor between this pin and PGND.
3	UVLO	Undervoltage Lockout Pin. An external resistor divider can be used to set the turn-on threshold.
4	PGOOD	Power-Good Output (Open Drain). A pull-up resistor of 10 kΩ to 100 kΩ is recommended.
5	RT	Frequency Setting. Connect a resistor between RT and GND to program the switching frequency between 250 kHz and 1.4 MHz. If the RT pin is connected to GND, the switching frequency is set to 290 kHz. If the RT pin is open, the switching frequency is set to 550 kHz.
6	SYNC	Synchronization Input. Connect this pin to an external clock to synchronize the switching frequency between 250 kHz and 1.4 MHz (see the Oscillator section and the Synchronization section for details).
7	EN/SS	Enable Pin (EN). When this pin voltage falls below 0.5 V, the regulator is disabled. Soft Start (SS). This pin can also be used to set the soft start time. Connect a capacitor from SS to GND to program the slow soft start time. If this pin is open, the regulator is enabled and uses the internal soft start.
8	COMP	Error Amplifier Output. Connect an RC network from COMP to FB.
9	FB	Feedback Voltage Sense Input. Connect to a resistor divider from V_{OUT}.
10	GND	Analog Ground. Connect to the ground plane.
11	PGND	Power Ground. Connect to the source of the synchronous N-channel MOSFET.
12	VREG	Internal 8 V Regulator Output. Place a 1 µF ceramic capacitor between this pin and GND.
13	LD	Low-Side Gate Driver Output. Connect this pin to the gate of the synchronous N-MOSFET.
14, 15	SW	Switch Node Output. Connect this pin to the output inductor.
16	BST	Supply Rail for the High-Side Gate Drive. Place a 0.1 µF ceramic capacitor between SW and BST.
17	EPAD	The exposed pad should be soldered to an external ground plane underneath the IC for thermal dissipation.

TYPICAL PERFORMANCE CHARACTERISTICS

Operating conditions: T_A = 25°C, V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 2.2 µH, C_{OUT} = 2 × 100 µF, f_{SW} = 500 kHz, unless otherwise noted.

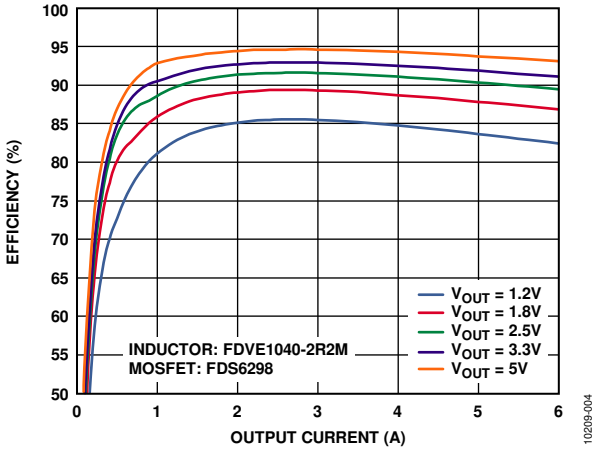

Figure 4. Efficiency at V_{IN} = 12 V, f_{SW} = 500 kHz

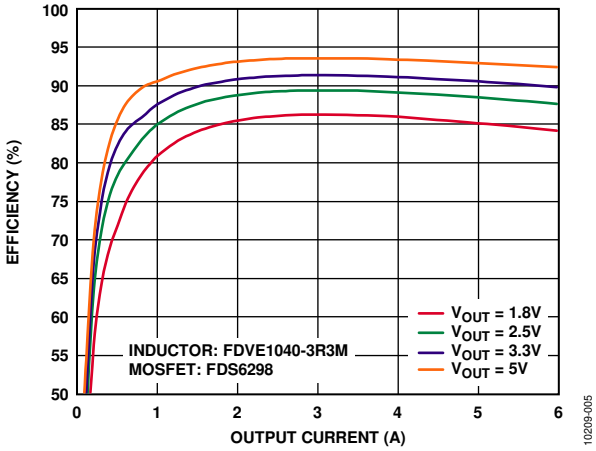

Figure 5. Efficiency at V_{IN} = 18 V, f_{SW} = 500 kHz

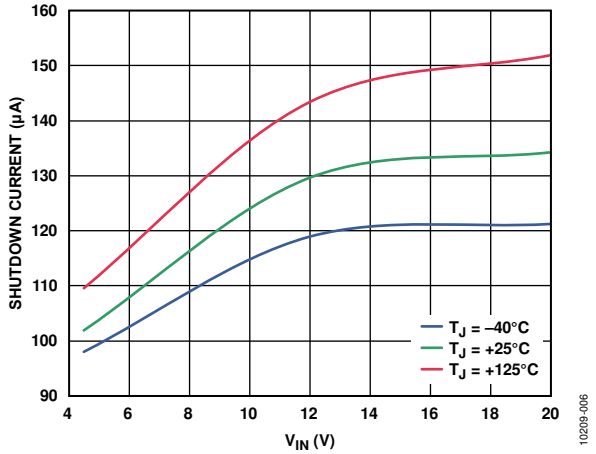

Figure 6. Shutdown Current vs. V_{IN}

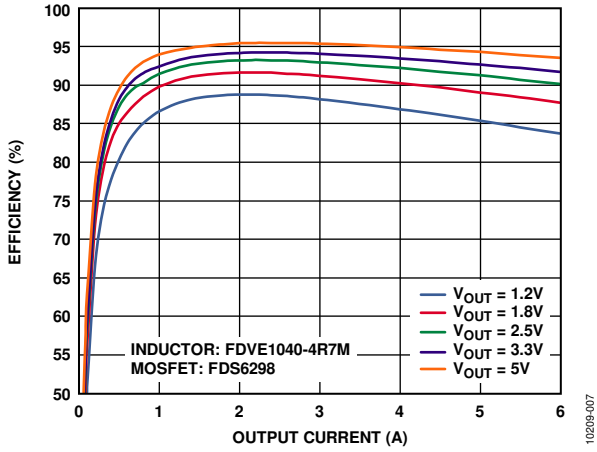

Figure 7. Efficiency at V_{IN} = 12 V, f_{SW} = 250 kHz

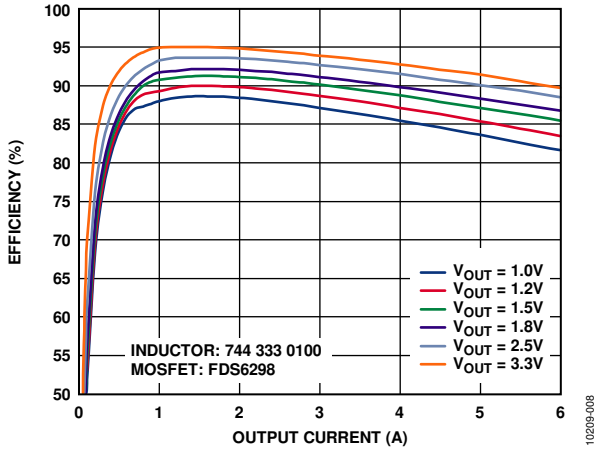

Figure 8. Efficiency at V_{IN} = 5 V, f_{SW} = 500 kHz

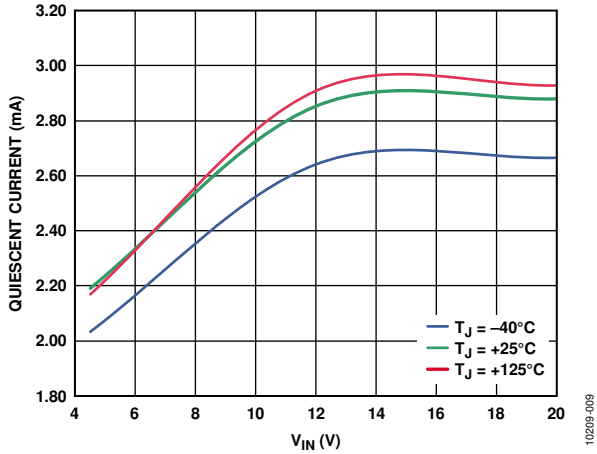

Figure 9. Quiescent Current vs. V_{IN}

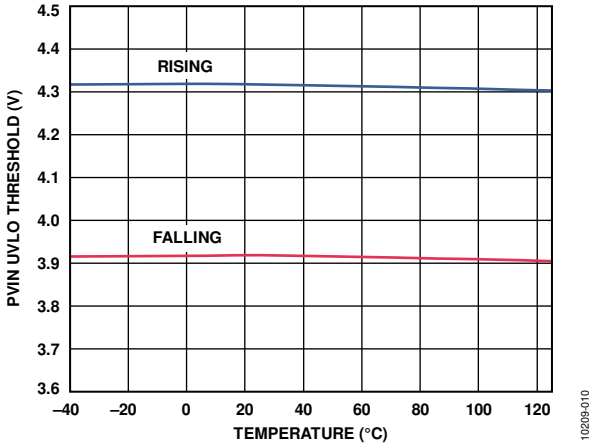

Figure 10. PVIN UVLO Threshold vs. Temperature

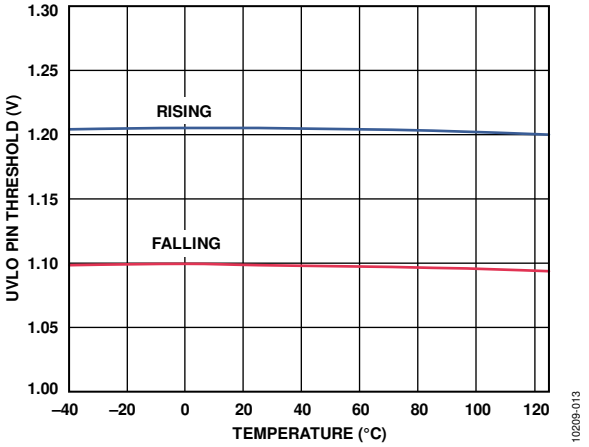

Figure 13. UVLO Pin Threshold vs. Temperature

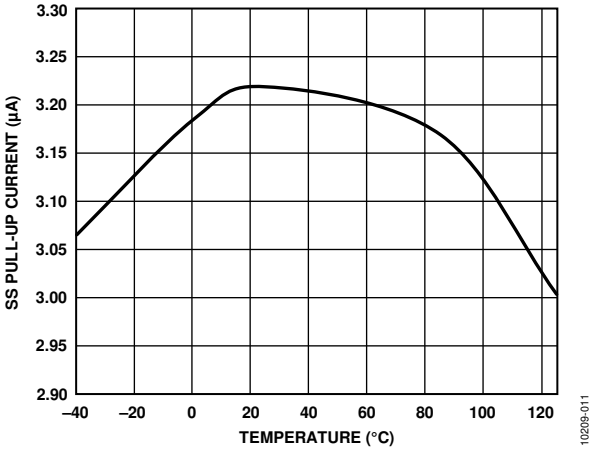

Figure 11. SS Pin Pull-Up Current vs. Temperature

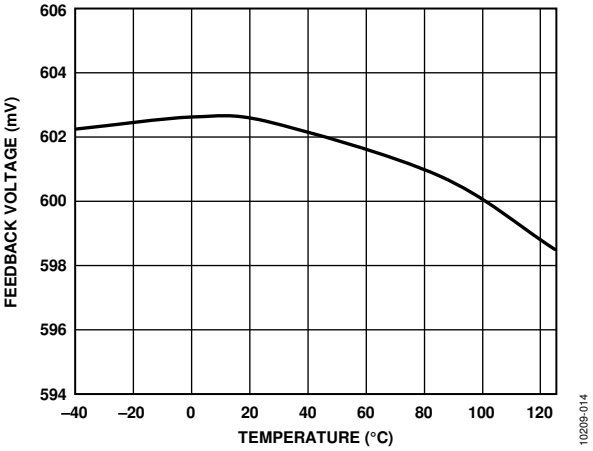

Figure 14. FB Voltage vs. Temperature

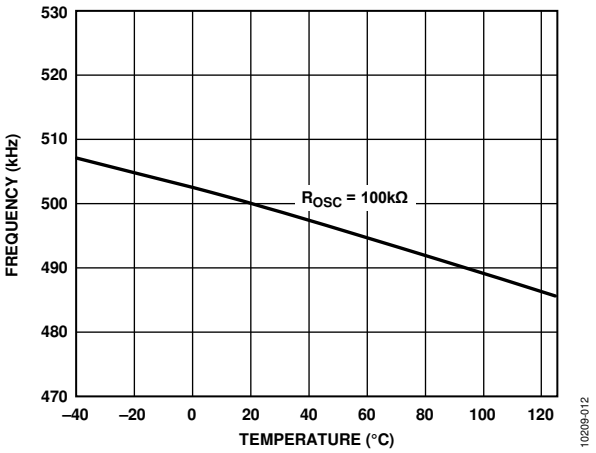

Figure 12. Frequency vs. Temperature

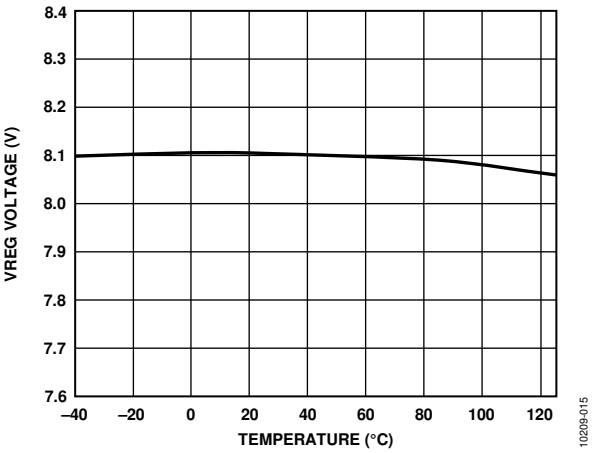

Figure 15. VREG Voltage vs. Temperature

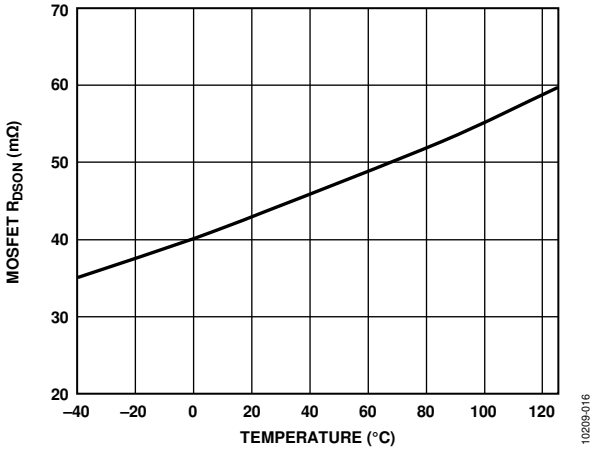

Figure 16. MOSFET R_{DSON} vs. Temperature

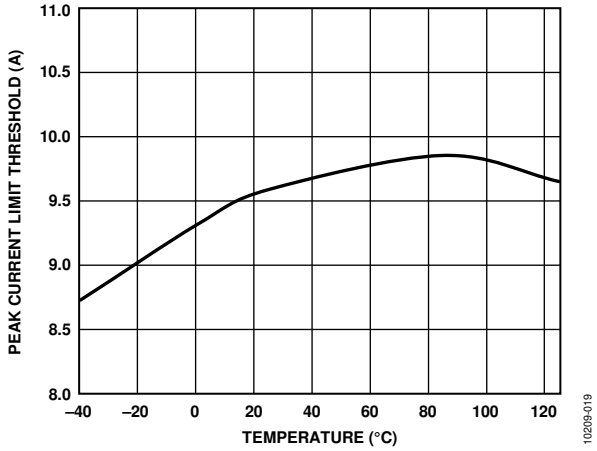

Figure 19. Current-Limit Threshold vs. Temperature

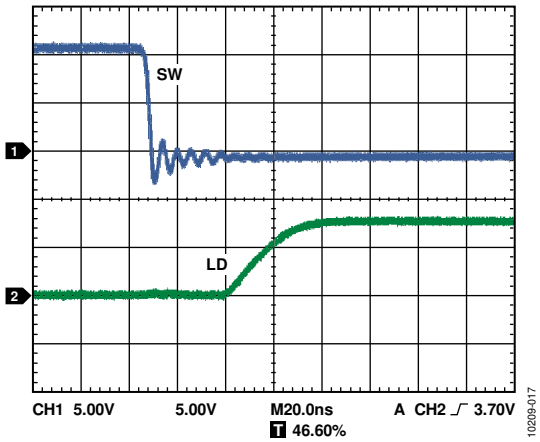

Figure 17. Low-Side Driver Rising Edge Waveform, C_{DL} = 2.2 nF

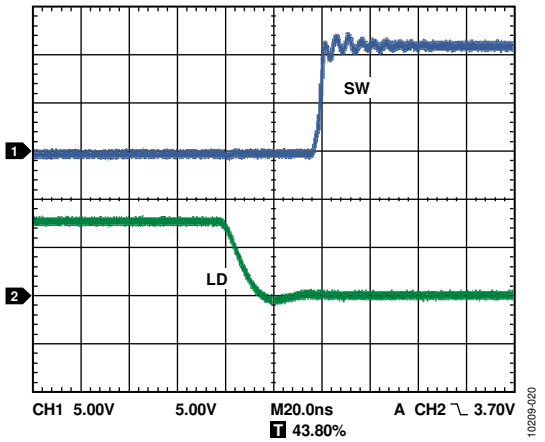

Figure 20. Low-Side Driver Falling Edge Waveform, C_{DL} = 2.2 nF

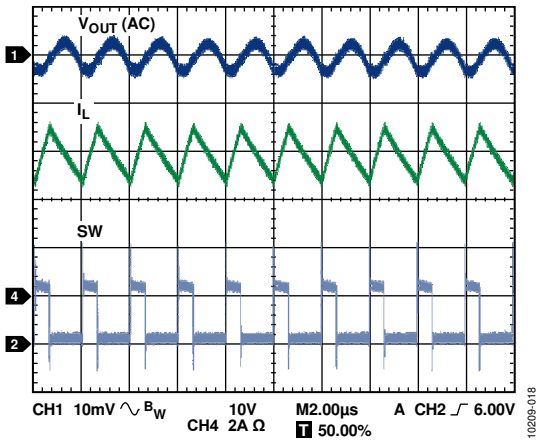

Figure 18. Working Mode Waveform

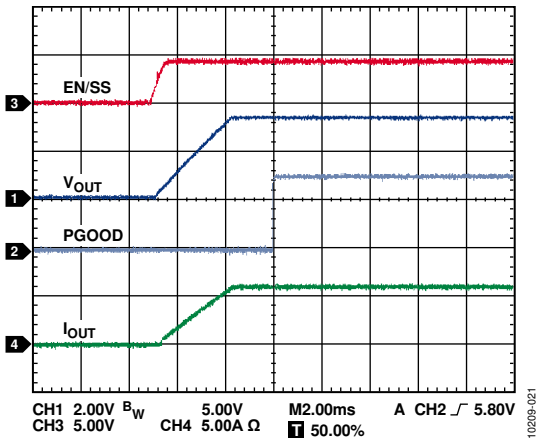

Figure 21. Soft Start with Full Load

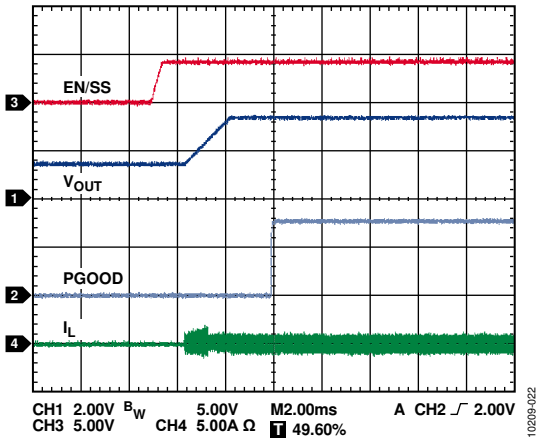

Figure 22. Precharged Output

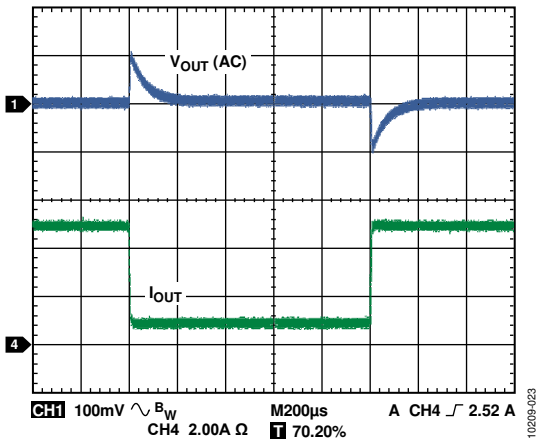

Figure 23. Load Transient Response, 1 A to 5 A

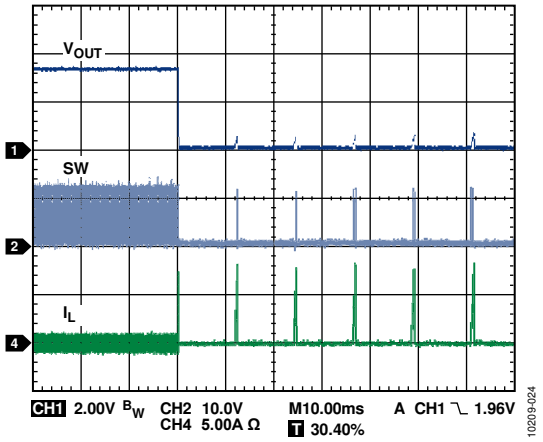

Figure 24. Output Short Entry

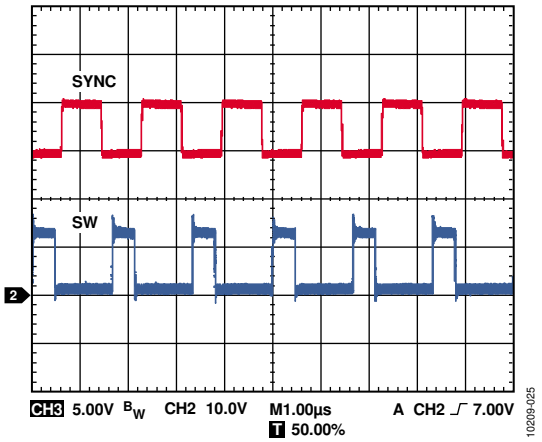

Figure 25. External Synchronization

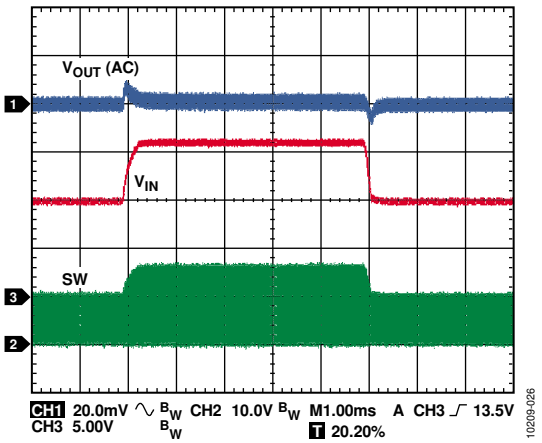

Figure 26. Line Transient Response, V_{IN} from 10 V to 16 V, I_{OUT} = 6 A

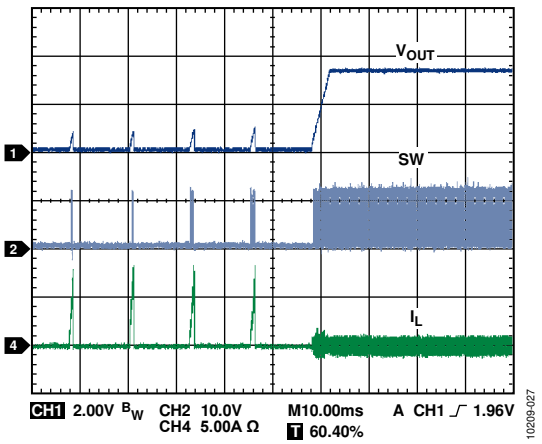

Figure 27. Output Short Recovery

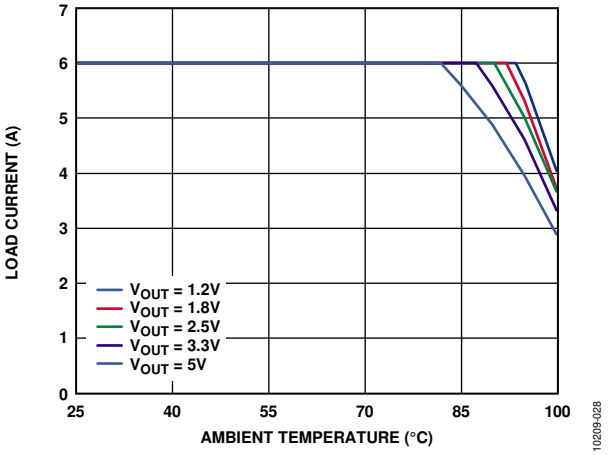

Figure 28. Load Current vs. Ambient Temperature, V_{IN} = 12 V, f_{SW} = 500 kHz

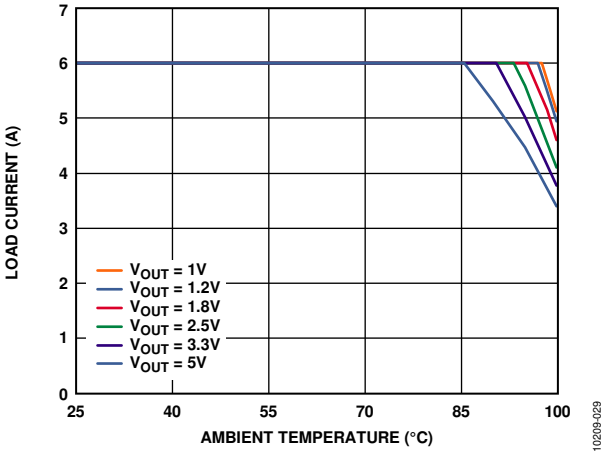

Figure 29. Load Current vs. Ambient Temperature, V_{IN} = 12 V, f_{SW} = 250 kHz

FUNCTIONAL BLOCK DIAGRAM

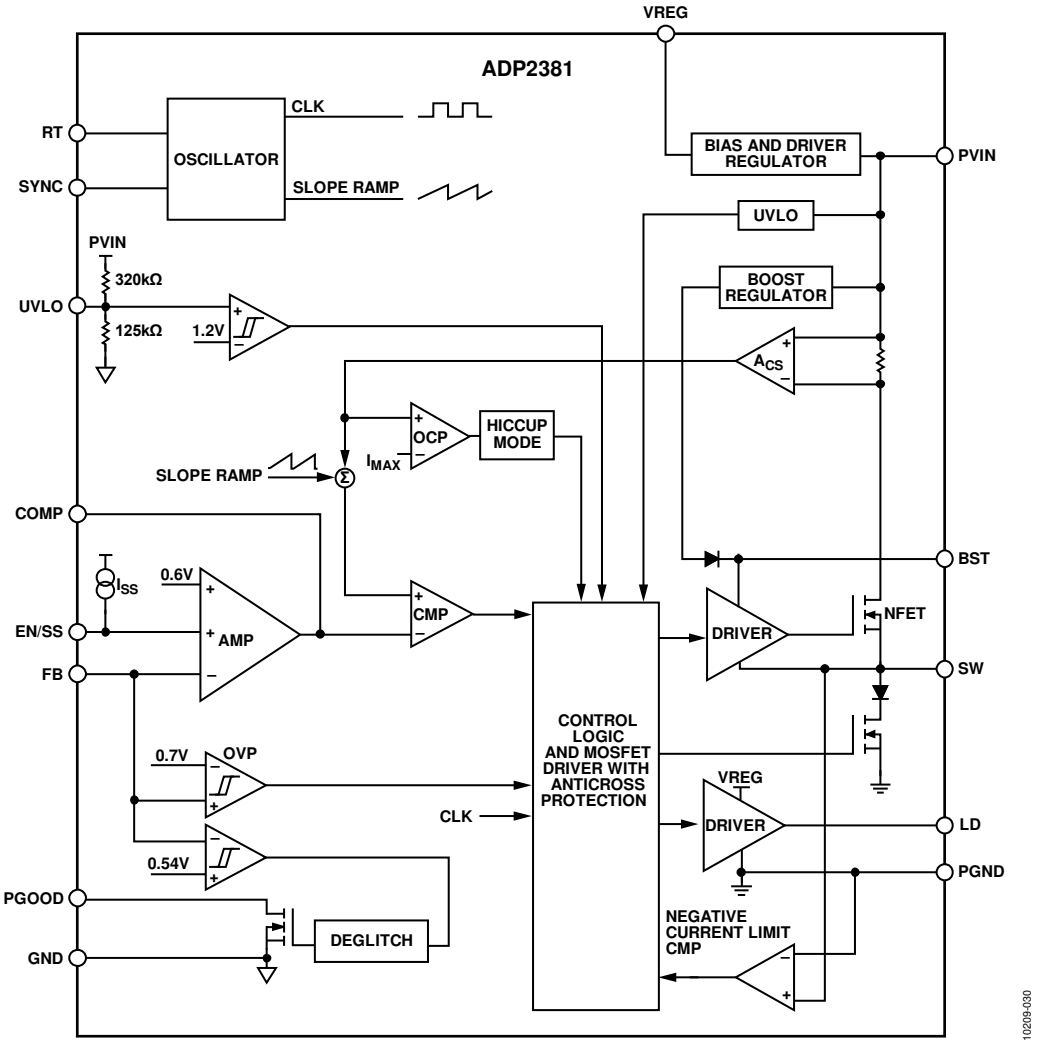

Figure 30. Functional Block Diagram

THEORY OF OPERATION

The ADP2381 is a synchronous, step-down, dc-to-dc regulator. It uses current-mode architecture with an integrated high-side power switch and a low-side driver. It targets high performance applications that require high efficiency and design flexibility.

The ADP2381 can operate with an input voltage from 4.5 V to 20 V and regulate the output voltage down to 0.6 V. Additional features for design flexibility include programmable switching frequency, soft start, external compensation, and power-good pin.

CONTROL SCHEME

The ADP2381 uses fixed frequency, peak current-mode PWM control architecture. At the start of each oscillator cycle, the high-side N-MOSFET is turned on, putting a positive voltage across the inductor. Current in the inductor increases until the current sense signal crosses the peak inductor current threshold that turns off the high-side N-MOSFET and turns on the low-side N-MOSFET. This puts a negative voltage across the inductor, causing the inductor current to decrease. The low-side N-MOSFET stays on for the rest of the cycle.

INTERNAL REGULATOR (VREG)

The internal regulator provides a stable supply for the internal circuits and provides bias voltage for the low-side gate driver. Placing a 1 µF ceramic capacitor between VREG and GND is recommended. The internal regulator also includes a current-limit circuit to protect the circuit if the maximum external load is added.

BOOTSTRAP CIRCUITRY

The ADP2381 has integrated the boot regulator to provide the gate drive voltage for the high-side N-MOSFET. It generates a 5 V bootstrap voltage between BST and SW by differential sensing.

It is recommended to place a 0.1 µF, X7R or X5R ceramic capacitor between the BST pin and the SW pin.

LOW-SIDE DRIVER

The LD pin provides the gate driver for the low-side N-channel MOSFET. Internal circuitry monitors the external MOSFET to ensure break-before-make switching to prevent cross conduction.

OSCILLATOR

The ADP2381 switching frequency is controlled by the RT pin. If the RT pin is connected to GND, the switching frequency is set to 290 kHz. If the RT pin is open, the switching frequency is set to 550 kHz. A resistor connected from RT to GND can program the switching frequency according to the following equation:

$$f_{SW}[\text{kHz}] = \frac{57{,}600}{R_{OSC}[\text{k}\Omega] + 15}$$

A 100 kΩ resistor sets the frequency to 500 kHz, and a 215 kΩ resistor sets the frequency to 250 kHz. Figure 31 shows the typical relationship between f_{SW} and R_{OSC}.

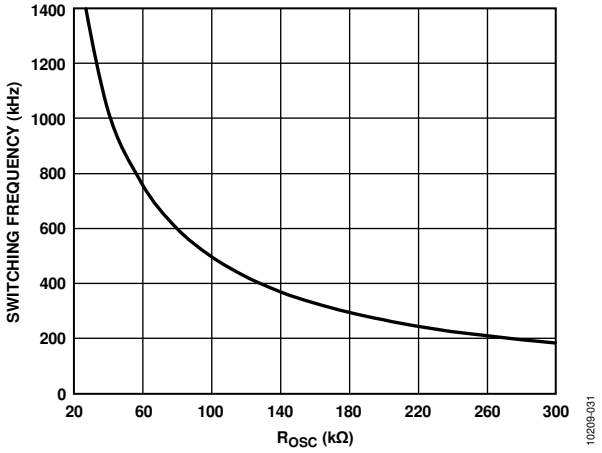

Figure 31. Switching Frequency vs. R_{OSC}

SYNCHRONIZATION

To synchronize the ADP2381, connect an external clock to the SYNC pin. The frequency of the external clock can be in the range of 250 kHz to 1.4 MHz. During synchronization, the switching rising edge runs 180° out of phase with the external clock rising edge.

When the ADP2381 is being synchronized, connect a resistor from the RT pin to GND to program the internal oscillator to run at 90% to 110% of the external synchronization clock.

ENABLE AND SOFT START

When the voltage of the EN/SS pin exceeds 0.5 V, the ADP2381 starts operation.

The ADP2381 has an internal digital soft start. The internal soft start time can be calculated by using the following equation:

$$t_{SS\_INT} = \frac{1500}{f_{SW}[\text{kHz}]}(\text{ms})$$

A slow soft start time can be programmed by the EN/SS pin. Place a capacitor between the EN/SS pin and GND. An internal current charges this capacitor to establish the soft start ramp. The soft start time can be calculated by using the following equation:

$$t_{SS\_EXT} = \frac{0.6\,\text{V} \times C_{SS}}{I_{SS\_UP}}$$

where:
C_{SS} is the soft start capacitance.
I_{SS_UP} is the soft start pull-up current (3.3 µA).

The internal error amplifier includes three positive inputs: the internal reference voltage, the internal digital soft start voltage, and the EN/SS voltage. The error amplifier regulates the FB voltage to the lowest of the three voltages.

If the output voltage is charged prior to turn-on, the ADP2381 prevents the low-side MOSFET from turning on, which discharges the output voltage until the soft start voltage exceeds the voltage on the FB pin.

When the regulator is disabled or a current fault happens, the soft start capacitor is discharged, and the internal digital soft start is reset to 0 V.

POWER GOOD

The power-good (PGOOD) pin is an active high, open-drain output that requires a pull-up resistor. A logic high indicates that the voltage at the FB pin (and, therefore, the output voltage) is above 95% of the reference voltage and there is a 1024 cycle waiting period before PGOOD is pulled high. A logic low indicates that the voltage at the FB pin is below 90% of the reference voltage and there is a 16-cycle waiting period before PGOOD is pulled low.

PEAK CURRENT LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2381 has a peak current-limit protection circuit to prevent current runaway. During soft start, the ADP2381 uses frequency foldback to prevent output current runaway. The switching frequency is reduced according to the voltage on the FB pin, which allows more time for the inductor to discharge. The correlation between the switching frequency and FB pin voltage is shown in Table 5.

Table 5. Switching Frequency and FB Pin Voltage

FB Pin Voltage	Switching Frequency
$V_{FB} \geq 0.4$ V	f_{SW}
$0.4 \text{ V} > V_{FB} \geq 0.2$ V	$f_{SW}/2$
$V_{FB} < 0.2$ V	$f_{SW}/4$

For heavy load protection, the ADP2381 uses hiccup mode for overcurrent protection. When the inductor peak current reaches the current-limit value, the high-side MOSFET turns off and the low-side driver turns on until the next cycle, while the overcurrent counter increments. If the overcurrent counter reaches 10, or the FB pin voltage falls to ≤0.4 V after the soft start, the regulator enters hiccup mode. The high-side MOSFET and low-side MOSFET are both turned off. The regulator remains in this mode for 4096 clock cycles and then attempts to restart. If the current limit fault is cleared, the regulator resumes normal operation. Otherwise, it reenters hiccup mode.

The ADP2381 also provides a sink current limit to prevent the low-side MOSFET from sinking a lot of current from the load. When the voltage across the low-side MOSFET exceeds the sink current-limit threshold, which is typically 20 mV, the low-side MOSFET turns off immediately for the rest of this cycle. Both high-side and low-side MOSFETs turn off until the next clock cycle.

In some cases, the input voltage (PVIN) ramp rate is too slow or the output capacitor is too large to support the setting regulation voltage during the soft start, causing the regulator to enter hiccup mode. To avoid such cases, use a resistor divider at the UVLO pin to program the UVLO input voltage, or use a longer soft start time.

OVERVOLTAGE PROTECTION (OVP)

The ADP2381 provides an overvoltage protection feature to protect the system against an output shorting to a higher voltage supply or a strong load transient occurring. If the feedback voltage increases to 0.7 V, the internal high-side MOSFET and low-side driver are turned off until the voltage at FB decreases to 0.63 V. At that time, the ADP2381 resumes normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)

The UVLO pin enable threshold is 1.2 V with 100 mV hysteresis.

The ADP2381 has an internal voltage divider consisting of two resistors from PVIN to GND, 320 kΩ for the high-side resistor and 125 kΩ for the low-side resistor. An external resistor divider from PVIN to GND can be used to override the internal resistor divider.

THERMAL SHUTDOWN

In the event that the ADP2381 junction temperatures rise above 150°C, the thermal shutdown circuit turns off the regulator. Extreme junction temperatures can be the result of high current operation, poor circuit board design, and/or high ambient temperature. A 25°C hysteresis is included so that when thermal shutdown occurs, the ADP2381 does not return to operation until the on-chip temperature drops below 125°C. Upon recovery, soft start is initiated prior to normal operation.

APPLICATIONS INFORMATION

INPUT CAPACITOR SELECTION

The input decoupling capacitor is used to attenuate high frequency noise on the input. This capacitor should be a ceramic capacitor in the range of 10 µF to 47 µF. It should be placed close to the PVIN pin. The loop composed by this input capacitor, high-side NFET, and low-side NFET must be kept as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The rms current rating of the input capacitor should be larger than the following equation:

$$I_{C_{IN}\_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

OUTPUT VOLTAGE SETTING

The output voltage of ADP2381 can be set by an external resistive divider using the following equation:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{TOP}}{R_{BOT}}\right)$$

To limit output voltage accuracy degradation due to FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that R_{BOT} is less than 30 kΩ.

Table 6 gives the recommended resistor divider values for various output voltage options.

Table 6. Resistor Divider for Different Output Voltages

V_{OUT} (V)	R_{TOP}, ±1% (kΩ)	R_{BOT}, ±1% (kΩ)
1.0	10	15
1.2	10	10
1.5	15	10
1.8	20	10
2.5	47.5	15
3.3	10	2.21
5.0	22	3

VOLTAGE CONVERSION LIMITATIONS

The minimum output voltage for a given input voltage and switching frequency is constrained by the minimum on time. The minimum on time of the ADP2381 is typically 120 ns. The minimum output voltage at a given input voltage and frequency can be calculated using the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON_HS} is the high-side MOSFET on resistance.
R_{DSON_LS} is the low-side MOSFET on resistance.
I_{OUT_MIN} is the minimum output current.
R_L is the series resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is constrained by the minimum off time and the maximum duty cycle. The minimum off time is typically 200 ns, and the maximum duty cycle of the ADP2381 is typically 90%.

The maximum output voltage limited by the minimum off time at a given input voltage and frequency can be calculated using the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
V_{OUT_MAX} is the maximum output voltage.
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

The maximum output voltage, limited by the maximum duty cycle at a given input voltage, can be calculated by using the following equation:

$$V_{OUT\_MAX} = D_{MAX} \times V_{IN} \quad (3)$$

where D_{MAX} is the maximum duty.

As Equation 1 to Equation 3 show, reducing the switching frequency alleviates the minimum on time and minimum off time limitation.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor leads to a faster transient response, but it degrades efficiency due to larger inductor ripple current, whereas using a large inductor value leads to smaller ripple current and better efficiency, but it results in a slower transient response.

As a guideline, the inductor ripple current, ΔI_L, is typically set to 1/3 of the maximum load current. The inductor can be calculated using the following equation:

$$L = \frac{(V_{IN} - V_{OUT})}{\Delta I_L \times f_{SW}} \times D$$

where:
V_{IN} is the input voltage.
V_{OUT} is the output voltage.
ΔI_L is the inductor current ripple.
f_{SW} is the switching frequency.
D is the duty cycle.

$$D = \frac{V_{OUT}}{V_{IN}}$$

The ADP2381 uses adaptive slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

For a duty cycle that is larger than 50%, the minimum inductor value is determined by the following equation:

$$\frac{V_{OUT} \times (1 - D)}{2 \times f_{SW}}$$

The inductor peak current is calculated using the following equation:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

The saturation current of the inductor must be larger than the peak inductor current. For the ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor should be higher than the current-limit threshold of the switch to prevent the inductor from becoming saturated.

The rms current of the inductor can be calculated by

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low EMI. Table 7 lists some recommended inductors.

Table 7. Recommended Inductors

Vendor	Part No.	Value (µH)	I_{SAT} (A)	I_{RMS} (A)	DCR (mΩ)
Toko	FDVE0630-R47M	0.47	15.6	14.1	3.7
	FDVE0630-R75M	0.75	10.9	10.7	6.2
	FDVE0630-1R0M	1.0	9.5	9.5	8.5
	FDVE1040-1R5M	1.5	13.7	14.6	4.6
	FDVE1040-2R2M	2.2	11.4	11.6	6.8
	FDVE1040-3R3M	3.3	9.8	9.0	10.1
	FDVE1040-4R7M	4.7	8.2	8.0	13.8
Vishay	IHLP3232DZ-R47M-11	0.47	14	25	2.38
	IHLP3232DZ-R68M-11	0.68	14.5	22.2	3.22
	IHLP3232DZ-1R0M-11	1.0	12	18.2	4.63
	IHLP4040DZ-1R5M-01	1.5	27.5	15	5.8
	IHLP4040DZ-2R2M-01	2.2	25.6	12	9
	IHLP4040DZ-3R3M-01	3.3	18.6	10	14.4
	IHLP4040DZ-4R7M-01	4.7	17	9.5	16.5
Wurth Elektronik	744 325 120	1.2	25	20	1.8
	744 325 180	1.8	18	16	3.5
	744 325 240	2.4	17	14	4.75
	744 325 330	3.3	15	12	5.9
	744 325 420	4.2	14	11	7.1

OUTPUT CAPACITOR SELECTION

The output capacitor selection affects both the output ripple voltage and the loop dynamics of the regulator.

During a load step transient on the output, for example, when the load is suddenly increased, the output capacitor supplies the load until the control loop has a chance to ramp up the inductor current, which causes the output to undershoot. The output capacitance required to satisfy the voltage droop requirement can be calculated using the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor typically of 2.
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another case occurs when a load is suddenly removed from the output. The energy stored in the inductor rushes into the capacitor, which causes the output to overshoot. The output capacitance required to meet the overshoot requirement can be calculated using the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}{}^2}$$

where:
K_{OV} is a factor typically of 2.
ΔV_{OUT_OV} is the allowable undershoot on the output voltage.

The output ripple is determined by the ESR and the capacitance. Use the following equation to select a capacitor that can meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where:
ΔV_{OUT_RIPPLE} is the allowable output ripple voltage.
R_{ESR} is the equivalent series resistance of the output capacitor.

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple performance.

The selected output capacitor voltage rating should be greater than the output voltage. The rms current rating of the output capacitor should be larger than the following equation:

$$I_{C_{OUT}\_RMS} = \frac{\Delta I_L}{\sqrt{12}}$$

LOW-SIDE POWER DEVICE SELECTION

The ADP2381 has an integrated low-side MOSFET driver that drives the low-side NFET. The selection of the low-side NFET affects the dc-to-dc regulator performance.

The selected MOSFET must meet the following requirements:

- Drain-source voltage (V_{DS}) must be higher than $1.2 \times V_{IN}$.
- Drain current (I_D) must be greater than $1.2 \times I_{LIMIT\_MAX}$, which is the selected maximum current-limit threshold.
- The ADP2381 low-side gate drive voltage is 8 V. Make sure that the selected MOSFET can fully turn on at 8 V. Total gate charge (Q_g at 8 V) must be less than 50 nC. Lower Q_g characteristics constitute higher efficiency.
- The low-side MOSFET carries the inductor current when the high-side MOSFET is turned off. For low duty cycle application, the low-side MOSFET carries the output current during most of the period. To achieve higher efficiency, it is important to select a low on-resistance MOSFET. The power conduction loss of the low-side MOSFET can be calculated by using the following equation:

  $$P_{FET\_LOW} = I_{OUT}{}^2 \times R_{DSON} \times (1 - D)$$

  where R_{DSON} is the on resistance of the low-side MOSFET.
- Make sure that the MOSFET can handle the thermal dissipation due to the power loss.

Some recommended MOSFETs are listed in Table 8.

Table 8. Recommended MOSFETs

Vendor	Part No.	V_{DS} (V)	I_D (A)	R_{DSON} (mΩ)	Q_g (nC)
Fairchild	FDS6298	30	13	12	10
Fairchild	FDS8880	30	10.7	12	12
Fairchild	FDM7578	25	14	8	8
Vishay	SiA430DJ	20	10.8	18.5	5.3
AOS	AON7402	30	39	15	7.1
AOS	AO4884L	40	10	16	13.6

PROGRAMMING INPUT VOLTAGE UVLO

The internal voltage divider from PVIN to GND sets the default start/stop values of the input voltage to achieve undervoltage lockout (UVLO) performance. The default rising/falling threshold of PVIN and UVLO are listed in Table 9. These default values can be replaced by using an external voltage divider to achieve a more accurate externally adjustable UVLO, as shown in Figure 32. Lower values of the external resistors are recommended to obtain a high accuracy UVLO threshold because the values of the internal 320 kΩ and 125 kΩ resistors may vary by as much as 20%.

Table 9. Default Rising/Falling Voltage Threshold

Pin	Rising Threshold (V)	Falling Threshold (V)
PVIN	4.28	3.92
UVLO	1.2	1.1

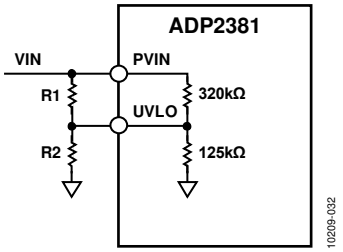

Figure 32. External Programmable UVLO

A 1 kΩ resistor for R2 is an appropriate choice. Use the following equation to obtain the value of R1 for a chosen input voltage rising threshold:

$$R1 = \frac{(V_{IN\_RISING} - 1.2\ \text{V}) \times R2}{1.2\ \text{V}}$$

where V_{IN_RISING} is the rising threshold of V_{IN}.

The falling threshold of VIN can be determined by the following equation:

$$V_{IN\_FALLING} = \frac{1.1\ \text{V} \times R1}{R2} + 1.1\ \text{V}$$

where $V_{IN\_FALLING}$ is the falling threshold of V_{IN}.

COMPENSATION DESIGN

The ADP2381 uses a peak current-mode control architecture for excellent load and line transient response. For peak current-mode control, the power stage can be simplified as a voltage controlled current source, supplying current to the output capacitor and load resistor. It consists of one domain pole and one zero contributed by the output capacitor ESR.

The control to output transfer function is given by the following equation:

$$G_{VD}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_Z}\right)}{1 + \frac{s}{2 \times \pi \times f_P}}$$

$$f_Z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_P = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where:
A_{VI} = 8.7 A/V.
R is the load resistance.
C_{OUT} is the output capacitance.
R_{ESR} is the equivalent series resistance of the output capacitor.

The external voltage loop is compensated by a transconductance amplifier with a simple external RC network placed either between COMP and GND or between COMP and FB, as shown in Figure 33 and Figure 34, respectively.

Compensation Network Between COMP and GND

Figure 33 shows the simplified peak current mode control small signal circuit with a compensation network placed between COMP and GND.

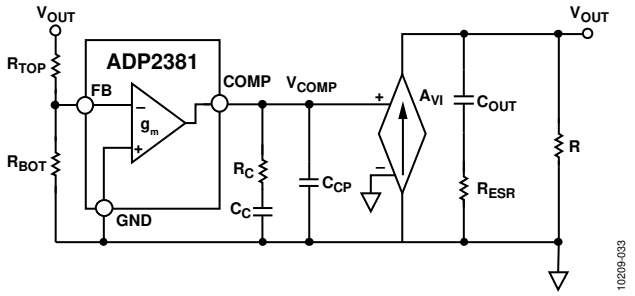

Figure 33. Small Signal Circuit with Compensation Network Between COMP and GND

The R_C and C_C compensation components contribute a zero, and the optional C_{CP} and R_C contribute an optional pole.

The closed-loop transfer function is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{VD}(s)$$

Use the following design guidelines to select the R_C, C_C, and C_{CP} compensation components:

- Determine the cross frequency, f_C. Generally, fc is between $f_{SW}/12$ and $f_{SW}/6$.
- R_C can be calculated by

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{V_{REF} \times g_m \times A_{VI}}$$

  where:
  V_{REF} = 0.6 V.
  g_m = 500 µS.
- Place the compensation zero at the domain pole, f_P. C_C can be determined by:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

- C_{CP} is optional, and it can be used to cancel the zero caused by the ESR of the output capacitors.

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

Compensation Network Between COMP and FB

The compensation RC network can also be placed between COMP and FB, as shown in Figure 34.

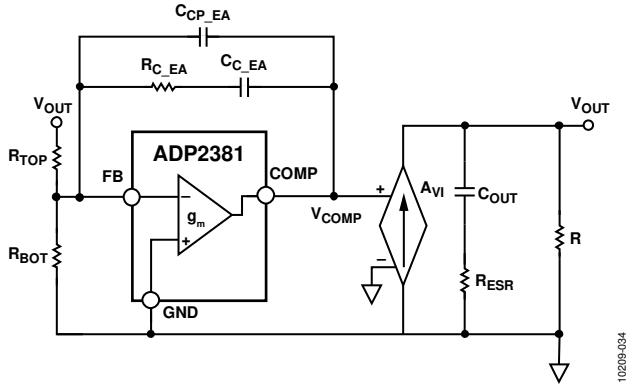

Figure 34. Small Signal Circuit with Compensation Network Between COMP and FB

When connecting the compensation network as shown in Figure 34, it should have the same pole and zero as in Figure 33 to maintain the same compensation performance.

Assuming that the compensation networks of Figure 33 and Figure 34 have the same pole and zero,

$$R_C C_C = R_{C\_EA} C_{C\_EA} - \frac{C_{CP\_EA} + C_{C\_EA}}{g_m}$$

$$r_0 R_C C_C C_{CP} = r_0 R_{C\_EA} C_{C\_EA} C_{CP\_EA} + R_{C\_EA} C_{C\_EA} C_{CP\_EA} (R_{TOP} // R_{BOT})(1 + g_m \times r_0)$$

$$r_0 (C_{CP} + C_C) + R_C C_C = r_0 (C_{CP\_EA} + C_{C\_EA}) + R_{C\_EA} C_{C\_EA} + (C_{CP\_EA} + C_{C\_EA})(R_{TOP} // R_{BOT})(1 + g_m \times r_0)$$

where:

r_0 is the equivalent output impedance of the trans-conductance amplifier, 40 MΩ.

$$R_{TOP} // R_{BOT} = \frac{R_{TOP} R_{BOT}}{R_{TOP} + R_{BOT}}$$

Solve the preceding equations to obtain:

$$C_{C\_EA} = B \times g_m - \frac{r_0 R_C C_C C_{CP}}{(B + R_C C_C)(r_0 + A)}$$

$$R_{C\_EA} = \frac{B + R_C C_C}{C_{C\_EA}}$$

$$C_{CP\_EA} = \frac{r_0 R_C C_C C_{CP}}{(B + R_C C_C)(r_0 + A)}$$

where:

$$A = (R_{TOP} // R_{BOT})(1 + g_m \times r_0)$$

$$B = \frac{r_0 (C_{CP} + C_C)}{1 + g_m (A + r_0)}$$

ADIsimPower DESIGN TOOL

The ADP2381 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs that are optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count, while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about the ADIsimPower design tools, visit www.analog.com/ADIsimPower. The tool set is available from this website, and users can request an unpopulated board.

DESIGN EXAMPLE

This section provides the procedures of selecting the external components based on the example specifications listed in Table 10. The schematic of this design example is shown in Figure 36.

Table 10. Step-Down DC-to-DC Regulator Requirements

Parameter	Specification
Input Voltage	V_{IN} = 12.0 V ± 10%
Output Voltage	V_{OUT} = 3.3 V
Output Current	I_{OUT} = 6 A
Output Voltage Ripple	ΔV_{OUT_RIPPLE} = 33 mV
Load Transient	±5%, 1 A to 5 A, 2 A/µs
Switching Frequency	f_{SW} = 500 kHz

OUTPUT VOLTAGE SETTING

Choose a 10 kΩ resistor as the top feedback resistor (R_{TOP}) and calculate the bottom feedback resistor (R_{BOT}) by using the following equation:

$$R_{BOT} = R_{TOP} \times \left(\frac{0.6}{V_{OUT} - 0.6} \right)$$

To set the output voltage to 3.3 V, the resistors values are R_{TOP} = 10 kΩ, R_{BOT} = 2.21 kΩ.

FREQUENCY SETTING

Connect a 100 kΩ resistor from RT pin to GND to set the switching frequency at 500 kHz.

INDUCTOR SELECTION

The peak-to-peak inductor ripple current, ΔI_L, is set to 30% of the maximum output current. Use the following equation to estimate the inductor value:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:
V_{IN} = 12 V.
V_{OUT} = 3.3 V.
$D = V_{OUT}/V_{IN}$ = 0.275.
ΔI_L = 1.8A.
f_{SW} = 500 kHz.

This results in L = 2.659 µH. Choose the standard inductor value of 2.2 µH.

The peak-to-peak inductor ripple current can be calculated by the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

This results in ΔI_L = 2.18 A.

The peak inductor current can be calculated using the following equation:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

This results in I_{PEAK} = 7.09 A.

The rms current flowing through the inductor can be calculated by the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

This results in I_{RMS} = 6.03 A.

According to the calculated rms and peak inductor current values, select an inductor with a minimum rms current rating of 6.03 A and a minimum saturation current rating of 7.09 A.

To protect the inductor from reaching its saturation limit, the inductor should be rated for at least 9.6 A saturation current for reliable operation.

Based on these requirements, select a 2.2 µH inductor, such as the FDVE1040-2R2M from Toko, which has 6.8 mΩ DCR and 11.4 A saturation current.

OUTPUT CAPACITOR SELECTION

The output capacitor is required to meet both the output voltage ripple requirement and the load transient response.

To meet the output voltage ripple requirement, use the following equation to calculate the ESR and capacitance of the output capacitor:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

This results in C_{OUT_RIPPLE} = 16.5 µF and R_{ESR} = 15.1 mΩ.

To meet the ±5% overshoot and undershoot transient requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}^2}$$

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
$K_{OV} = K_{UV}$ = 2, the coefficients for estimation purposes.
ΔI_{STEP} = 4 A, the load transient step.
$\Delta V_{OUT\_OV} = 5\% V_{OUT}$, the overshoot voltage.
$\Delta V_{OUT\_UV} = 5\% V_{OUT}$, the undershoot voltage.

This results in C_{OUT_OV} = 63.1 µF and C_{OUT_UV} = 24.5 µF.

According to the preceding calculation, the output capacitance must be larger than 63 µF, and the ESR of the output capacitor must be smaller than 15 mΩ. It is recommended that one 100 µF, X5R, 6.3 V ceramic capacitor and one 47 µF, X5R, 6.3 V ceramic capacitor be used, such as the GRM32ER60J107ME20 and GRM32ER60J476ME20 from Murata with an ESR = 2 mΩ.

LOW-SIDE MOSFET SELECTION

A low R_{DSON} N-channel MOSFET is selected as a high efficiency solution. The breakdown voltage of the MOSFET must be higher than $1.2 \times V_{IN}$, and the drain current must be larger than $1.2 \times I_{LIMIT}$.

It is recommended that a 30 V, N-channel MOSFET, such as the FDS6298 from Fairchild, be used. The R_{DSON} of the FDS6298 at a 4.5 V driver voltage is 9.4 mΩ, and the total gate charge at 5 V is 10 nC.

COMPENSATION COMPONENTS

For a better load transient and stability performance, set the cross frequency, f_C, at $f_{SW}/10$. In this case, f_C = 1/500 kHz = 50 kHz.

$$C_{C\_EA} = B \times g_m - \frac{r_0 R_C C_C C_{CP}}{(B + R_C C_C)(r_0 + A)}$$

$$R_{C\_EA} = \frac{B + R_C C_C}{C_{C\_EA}}$$

$$C_{CP\_EA} = \frac{r_0 R_C C_C C_{CP}}{(B + R_C C_C)(r_0 + A)}$$

where:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{V_{REF} \times g_m \times A_{VI}} = \frac{2 \times \pi \times 3.3V \times 94\mu F \times 50\,kHz}{0.6\,V \times 500\ \mu S \times 8.7\,A/V} = 37.3\,k\Omega$$

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C} = \frac{(3.3\,V/6\,A + 0.002\,\Omega) \times 94\,\mu F}{37.3\,k\Omega} = 1.39\,nF$$

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C} = \frac{0.002\,\Omega \times 94\,\mu F}{37.3\,k\Omega} = 5.04\,pF$$

$$A = \frac{R_{TOP} R_{BOT}}{R_{TOP} + R_{BOT}}\left(1 + g_m \times r_0\right) = \frac{10\,k\Omega \times 2.21\,k\Omega}{10\,k\Omega + 2.21\,k\Omega} \times \left(1 + 500\,\mu S \times 40\,M\Omega\right) = 3.62 \times 10^7$$

$$B = \frac{r_0(C_{CP} + C_C)}{1 + g_m(A + r_0)} = \frac{40\,M\Omega \times (5.04\,pF + 1.39\,nF)}{1 + 500\mu S \times (3.62 \times 10^7 + 40\,M\Omega)} = 1.46 \times 10^{-6}$$

This results in

R_{C_EA} = 73.3 kΩ.
C_{C_EA} = 727.6 pF.
C_{CP_EA} = 2.56 pF.

Choose the standard values for R_{C_EA} = 73.2 kΩ, C_{C_EA} = 820 pF, and C_{CP_EA} = 2.2 pF.

Figure 35 shows the bode plot at 6 A. The cross frequency is 32 kHz, and the phase margin is 61°.

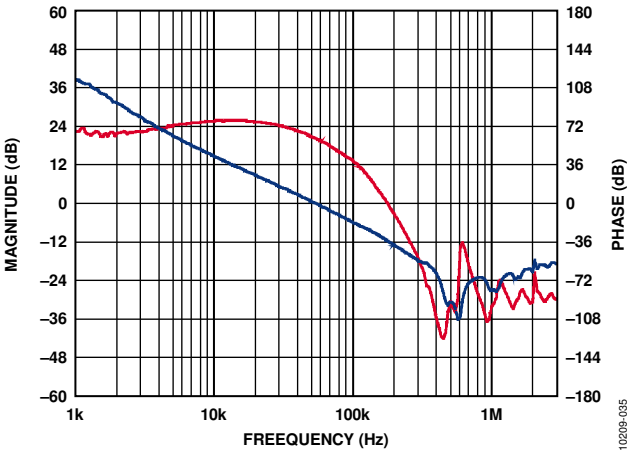

Figure 35. Bode Plot at 6 A

SOFT START TIME PROGRAM

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current. Set the soft start time to 4 ms.

$$C_{SS} = \frac{t_{SS\_EXT} \times I_{SS\_UP}}{0.6} = \frac{4\,ms \times 3.3\,\mu A}{0.6\,V} = 22\,nF$$

Choose a standard component value, C_{SS} = 22 nF.

INPUT CAPACITOR SELECTION

A minimum 10 µF ceramic capacitor is required to be placed near the PVIN pin. In this application, one 10 µF, X5R, 25 V ceramic capacitor is recommended.

SCHEMATIC OF DESIGN EXAMPLE

See Figure 36 for a schematic of the design example.

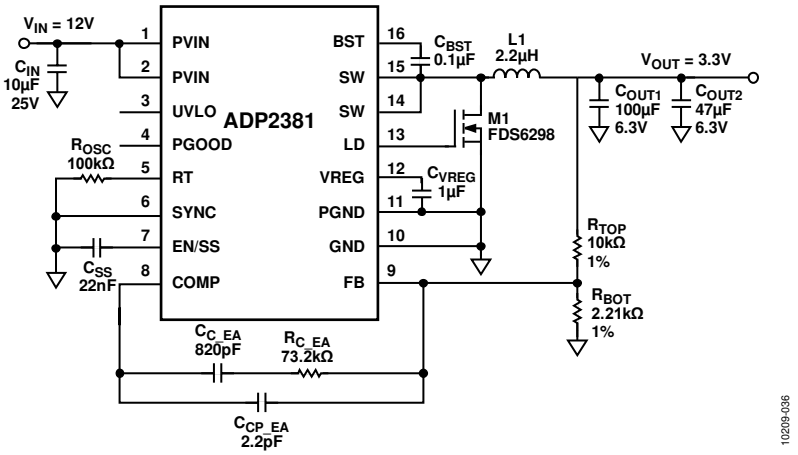

Figure 36. Schematic of Design Example

EXTERNAL COMPONENTS RECOMMENDATION

Table 11. Recommended External Components for Typical Applications with Compensation Network Between COMP and GND, 6 A Output Current

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)[1]	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_C (kΩ)	C_C (pF)	C_{CP} (pF)
250	12	1	2.2	680 + 470	10	15	68	2700	150
	12	1.2	2.2	680 + 2 × 100	10	10	56	2700	130
	12	1.5	3.3	680 + 2 × 100	15	10	71.5	2700	100
	12	1.8	3.3	680	20	10	71.5	2700	91
	12	2.5	4.7	470	47.5	15	69.8	2700	62
	12	3.3	4.7	3 × 100	10	2.21	36	2700	10
	12	5	6.8	2 × 100	22	3	36	2700	6.8
	5	1	1.5	680 + 2 × 100	10	15	47	2700	150
	5	1.2	2.2	680 + 2 × 100	10	10	56	2700	130
	5	1.5	2.2	680	15	10	59	2700	100
	5	1.8	2.2	470	20	10	47	2700	91
	5	2.5	3.3	3 × 100	47.5	15	28	2700	10
	5	3.3	2.2	3 × 100	10	2.21	36	2700	10
500	12	1.2	1	470	10	10	62	1500	68
	12	1.5	1.5	470	15	10	82	1500	56
	12	1.8	1.5	3 × 100	20	10	39	1500	10
	12	2.5	2.2	3 × 100	47.5	15	56	1500	6.8
	12	3.3	2.2	2 × 100	10	2.21	47	1500	4.7
	12	5	3.3	100	22	3	36	1500	3.3
	5	1	1	680	10	15	75	1500	82
	5	1.2	1	470	10	10	62	1500	68
	5	1.5	1	3 × 100	15	10	33	1500	10
	5	1.8	1	2 × 100	20	10	25.5	1500	8.2
	5	2.5	1.5	2 × 100	47.5	15	36	1500	6.8
	5	3.3	1	100 + 47	10	2.21	36	1500	4.7
1000	12	1.8	1	2 × 100	20	10	51	680	4.7
	12	2.5	1	100	47.5	15	36	680	3.3
	12	3.3	1.5	100	10	2.21	47	680	2.2
	12	5	1.5	100	22	3	73.2	680	1.8
	5	1	0.47	3 × 100	10	15	43	680	8.2
	5	1.2	0.47	2 × 100	10	10	34.8	680	6.8
	5	1.5	0.68	2 × 100	15	10	43	680	6.8
	5	1.8	0.68	100 + 47	20	10	39	680	4.7
	5	2.5	0.68	100	47.5	15	36	680	3.3
	5	3.3	0.68	100	10	2.21	47	680	2.2

[1] 680 µF: 4 V, Sanyo 4TPF680M; 470 µF: 6.3 V, Sanyo 6TPF470M; 100 µF: 6.3 V, X5R, Murata GRM32ER60J107ME20; 47 µF: 6.3 V, X5R, Murata GRM32ER60J476ME20.

Table 12. Recommended External Components for Typical Applications with Compensation Network between COMP and FB, 6 A Output Current

f_{SW} (kHz)	V_{IN} (V)	V_{OUT} (V)	L (µH)	C_{OUT} (µF)[1]	R_{TOP} (kΩ)	R_{BOT} (kΩ)	R_{C_EA} (kΩ)	C_{C_EA} (pF)	C_{CP_EA} (pF)
250	12	1	2.2	680 + 470	10	15	270	750	39
	12	1.2	2.2	680 + 2 × 100	10	10	200	820	39
	12	1.5	3.3	680 + 2 × 100	15	10	287	680	22
	12	1.8	3.3	680	20	10	316	680	22
	12	2.5	4.7	470	47.5	15	470	470	10
	12	3.3	4.7	3 × 100	10	2.21	71.5	1500	4.7
	12	5	6.8	2 × 100	22	3	86.6	1200	2.2
	5	1	1.5	680 + 2 × 100	10	15	191	750	39
	5	1.2	2.2	680 + 2 × 100	10	10	200	820	39
	5	1.5	2.2	680	15	10	240	680	22
	5	1.8	2.2	470	20	10	220	680	22
	5	2.5	3.3	3 × 100	47.5	15	187	390	2.2
	5	3.3	2.2	3 × 100	10	2.21	71.5	1500	4.7
500	12	1.2	1	470	10	10	220	390	22
	12	1.5	1.5	470	15	10	330	390	15
	12	1.8	1.5	3 × 100	20	10	169	330	2.2
	12	2.5	2.2	3 × 100	47.5	15	360	220	1
	12	3.3	2.2	2 × 100	10	2.21	93.1	680	2.2
	12	5	3.3	100	22	3	86.6	620	1.5
	5	1	1	680	10	15	330	390	22
	5	1.2	1	470	10	10	220	390	22
	5	1.5	1	3 × 100	15	10	130	330	2.2
	5	1.8	1	2 × 100	20	10	100	330	2.2
	5	2.5	1.5	2 × 100	47.5	15	220	220	1
	5	3.3	1	100 + 47	10	2.21	71.5	680	2.2
1000	12	1.8	1	2 × 100	20	10	232	160	1
	12	2.5	1	100	47.5	15	240	100	1
	12	3.3	1.5	100	10	2.21	93.1	390	1
	12	5	1.5	100	22	3	169	330	1
	5	1	0.47	3 × 100	10	15	178	180	2.2
	5	1.2	0.47	2 × 100	10	10	120	220	2.2
	5	1.5	0.68	2 × 100	15	10	178	180	1
	5	1.8	0.68	100 + 47	20	10	169	160	1
	5	2.5	0.68	100	47.5	15	240	100	1
	5	3.3	0.68	100	10	2.21	93.1	390	1

[1] 680 µF: 4V, Sanyo 4TPF680M; 470 µF: 6.3 V, Sanyo 6TPF470M; 100 µF: 6.3 V, X5R, Murata GRM32ER60J107ME20; 47 µF: 6.3 V, X5R, Murata GRM32ER60J476ME20.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good circuit board layout is essential for obtaining the best performance from the ADP2381. Poor printed circuit board (PCB) layout degrades the output regulation as well as the electromagnetic interface (EMI) and electromagnetic compatibility (EMC) performance. Figure 38 shows a PCB layout example. For optimum layout, use the following guidelines:

- Use separate analog ground and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to analog ground. In addition, connect the ground reference of power components, such as input and output capacitors and a low-side MOSFET, to power ground. Connect both ground planes to the exposed pad of the ADP2381.
- Place the input capacitor, inductor, low-side MOSFET, output capacitor as close to the IC as possible and use short traces.
- Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane. In addition, ensure that the high current path from the power ground plane through the external MOSFET, inductor, and output capacitor back to the power ground plane is as short as possible by tying the MOSFET source node to the PGND plane as close as possible to the input and output capacitors.
- Make the low-side driver path from the LD pin of the ADP2381 to the external MOSFET gate node and back to the PGND pin of the ADP2381 as short as possible, and use a wide trace for better noise immunity.
- Connect the exposed pad of the ADP2381 to a large copper plane to maximize its power dissipation capability for better thermal dissipation.
- Place the feedback resistor divider network as close as possible to the FB pin to prevent noise pickup. Try to minimize the length of the trace that connects the top of the feedback resistor divider to the output while keeping the trace away from the high current traces and the switching node to avoid noise pickup. To further reduce noise pickup, place an analog ground plane on either side of the FB trace and ensure that the trace is as short as possible to reduce parasitic capacitance pickup.

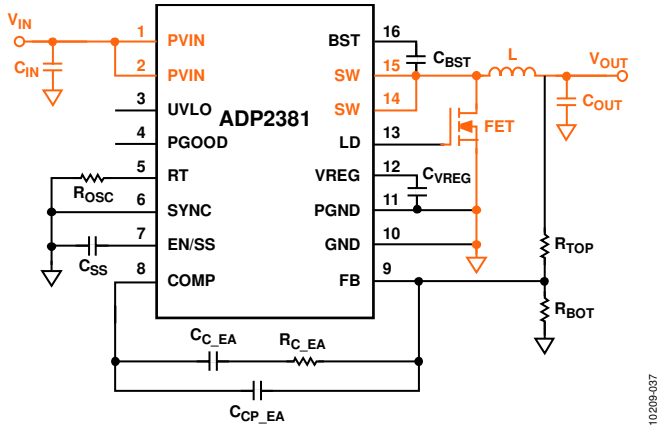

Figure 37. High Current Path in the PCB Circuit

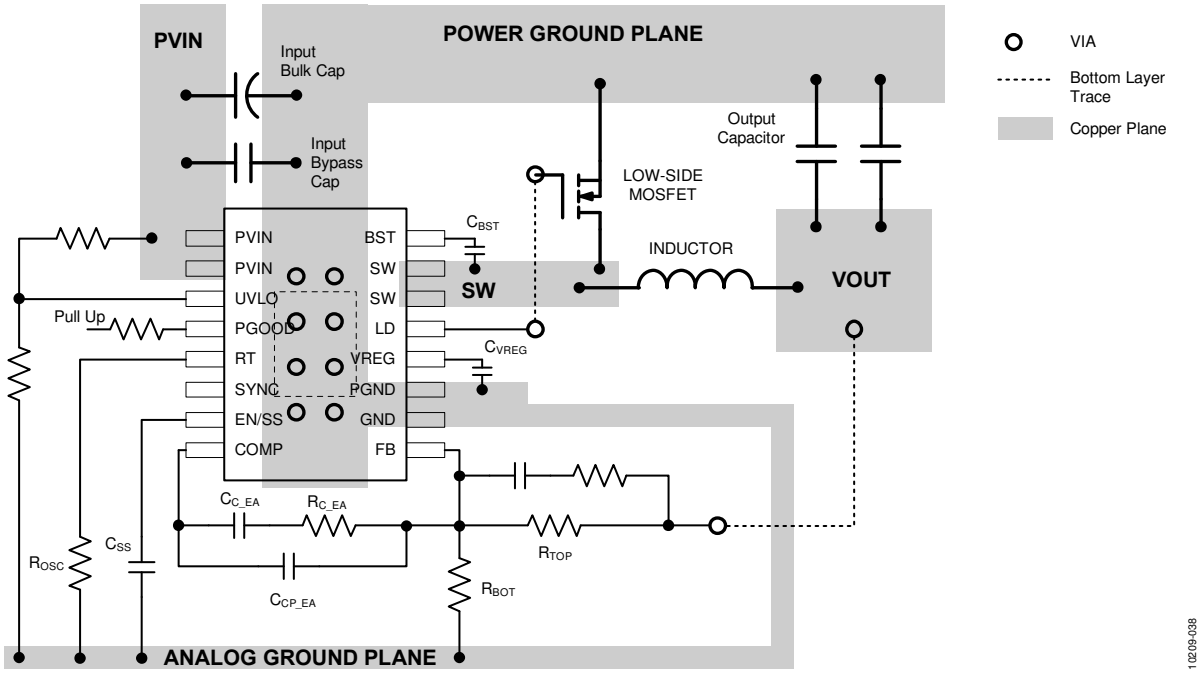

Figure 38. Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

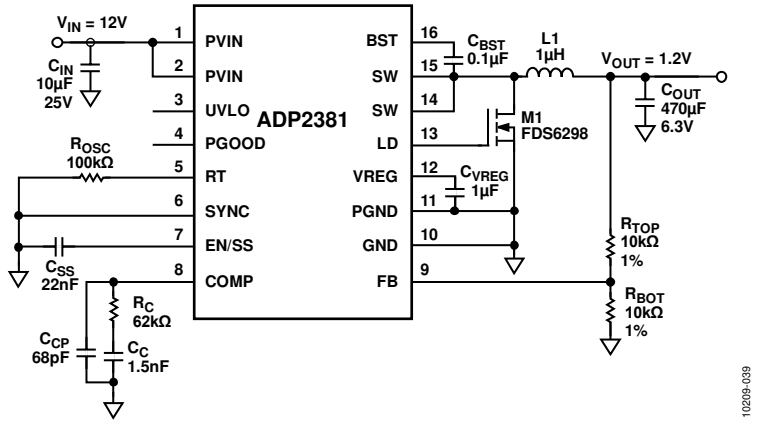

Figure 39. Compensation Network Between COMP and GND, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 6 A, f_{SW} = 500 kHz

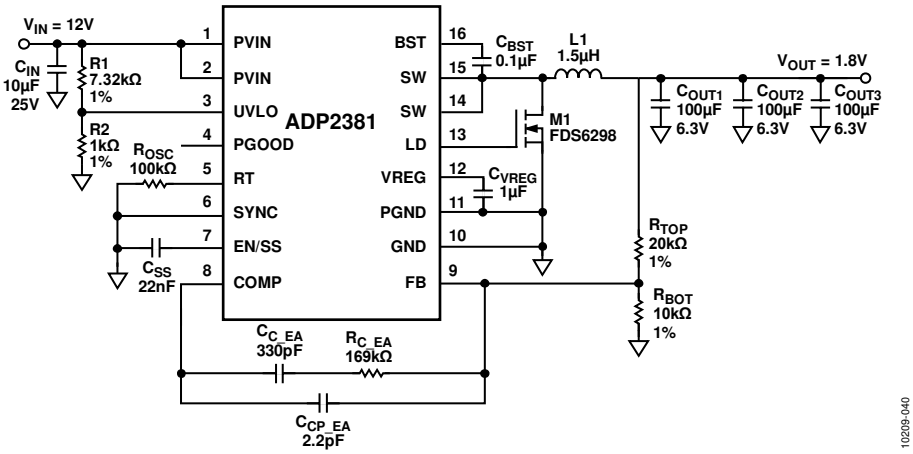

Figure 40. Programming Input Voltage UVLO Rising Threshold at 10 V, V_{IN} = 12 V, V_{OUT} = 1.8 V, I_{OUT} = 6 A, f_{SW} = 500 kHz

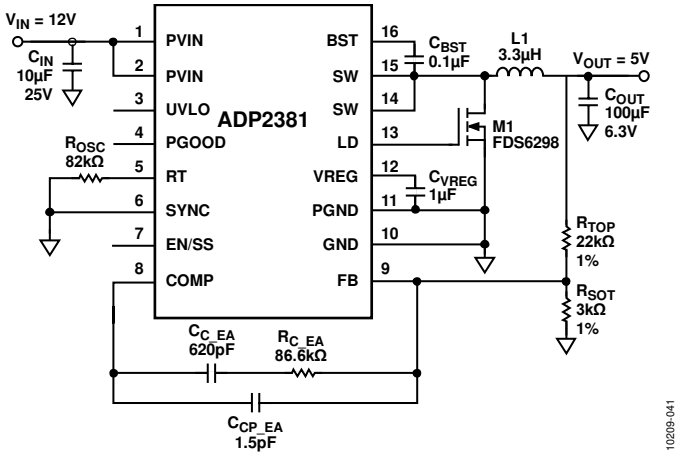

Figure 41. Using Internal Soft Start, Programming Switching Frequency at 600 kHz, V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 6 A, f_{SW} = 600 kHz

OUTLINE DIMENSIONS

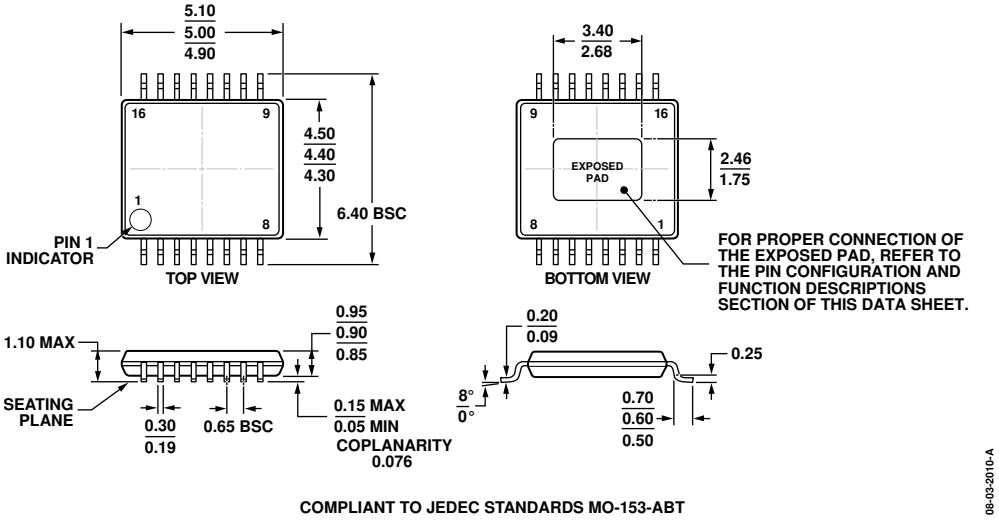

Figure 42. 16-Lead Thin Shrink Small Outline With Exposed Pad [TSSOP_EP]
(RE-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Packing
ADP2381AREZ-R7	−40°C to +125°C	16-Lead TSSOP_EP	RE-16-4	Reel
ADP2381AREZ	−40°C to +125°C	16-Lead TSSOP_EP	RE-16-4	Tube
ADP2381-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.