TPS386000-Q1 Quad Supply Voltage Supervisors With Programmable Delay and Watchdog Timer

1 Features

- Qualified for Automotive Applications
- AEC Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C4B
- Four Complete SVS Modules on one Silicon Platform
- Programmable Delay Time: 1.4 ms to 10 s
- Very Low Quiescent Current: 12 µA Typical
- Threshold Accuracy: 0.25% Typical
- SVS-1: Manual Reset ($\overline{MR}$) Input
- SVS-1, 2, 3: Adjustable Threshold Down to 0.4 V
- SVS-4:
  - Adjustable Threshold at Any Positive or Negative Voltage with VREF (1.2 V)
  - Window Comparator
- Watchdog Timer with Dedicated Output
- Well-Controlled $\overline{RESETn}$ Output During Power-Up
- Open-Drain $\overline{RESETn}$ and $\overline{WDO}$
- Package: 4-mm x 4-mm, 20-pin VQFN

2 Applications

- Automotive
- ADAS
  - Front Camera, Surround View, Long-Range Radar, and Short-Range Radar

3 Description

The TPS386000-Q1 family of voltage supervisors can monitor four power rails that are greater than 0.4 V and one power rail less than 0.4 V (including negative voltage) with a 0.25% (typical) threshold accuracy. Each of the four supervisory circuits (SVS-n) assert a $\overline{RESETn}$ or RESETn output signal when the SENSEm input voltage drops below the programmed threshold. With external resistors, the threshold of each SVS-n can be programmed (where n = 1, 2, 3, 4 and m = 1, 2, 3, 4L, 4H).

Each SVS-n has a programmable delay before releasing $\overline{RESETn}$ or RESETn. The delay time can be set from 1.4 ms to 10 s through the CTn pin connection. Only SVS-1 has an active-low manual reset ($\overline{MR}$) input; a logic-low input to $\overline{MR}$ asserts $\overline{RESET1}$ or RESET1.

SVS-4 monitors the threshold window using two comparators. The extra comparator can be configured as a fifth SVS to monitor negative voltage with voltage reference output VREF.

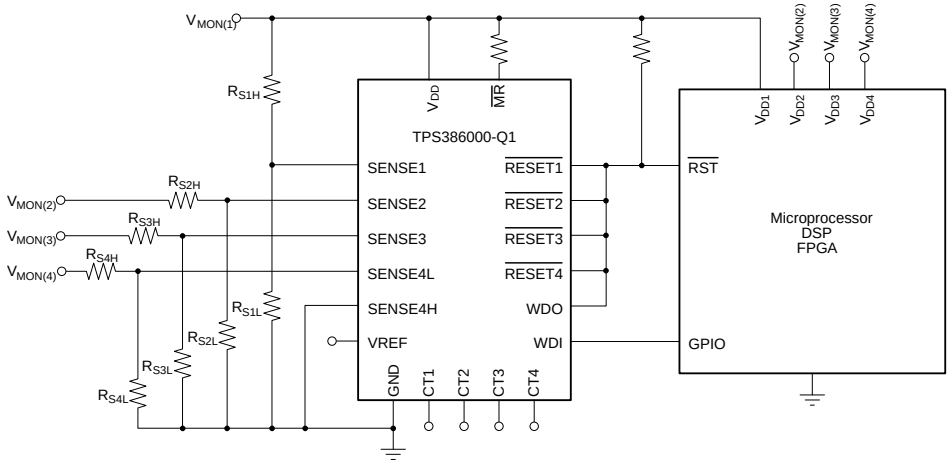
The TPS386000-Q1 device has a very low quiescent current of 12 µA (typical) and is available in a small, 4-mm x 4-mm, VQFN-20 package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS38600-Q1	VQFN (20)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

TPS386000-Q1 Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2013) to Revision B — **Page**

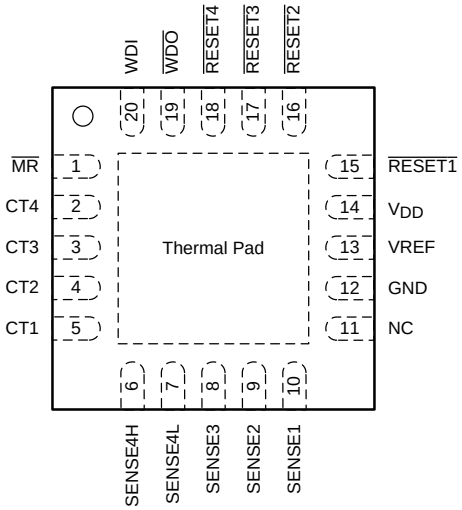
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed all references of V_{CC} (and I_{CC}) to V_{DD} (and I_{DD}) throughout the document ... 3
- Changed ITN to IT– and ITP to IT+ throughout ... 3
- Changed V_{HYSN} to $V_{HYS–}$ and V_{HYS+} to V_{HYS+} ... 5
- Moved timing and switching parameters (t_W, t_D, t_{WDT}) from the *Electrical Characteristics* table to the respective *Timing Requirements* and *Switching Characteristics* tables ... 6
- Deleted *Test Circuit* section ... 14
- Deleted references to push-pull reset and active-high outputs ... 17
- Changed Truth Tables to *Device Functional Modes* section ... 19

Changes from Original (September 2010) to Revision A — **Page**

- Added AEC Q100 text to features which includes ambient operating temperature range, HBM and CDM classification levels ... 1
- Deleted Latch-up performance text from *ABSOLUTE MAXIMUM RATINGS* table ... 4
- Added ESD ratings for HBM and CDM to *ABSOLUTE MAXIMUM RATINGS* table ... 4

5 Pin Configuration and Functions

RGP Package
20-Pin VQFN With Thermal Pad
Top View



NC = No internal connection

Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.			
CT1	5	—	Reset delay programming pin for SVS-1	Connecting this pin to V_{DD} through a 40-kΩ to 200-kΩ resistor, or leaving it open, selects a fixed delay time (see the *Electrical Characteristics*). Connecting a capacitor > 220 pF between this pin and GND selects the programmable delay time (see the *Reset Delay Time* section).
CT2	4	—	Reset delay programming pin for SVS-2	
CT3	3	—	Reset delay programming pin for SVS-3	
CT4	2	—	Reset delay programming pin for SVS-4	
GND	12	—	Ground	
$\overline{MR}$	1	I	Manual reset input for SVS-1. Logic low level of this pin asserts $\overline{RESET1}$ or RESET1.	
NC	11	—	Not connected. TI recommends to connect this pin to the GND pin (pin 12), which is next to this pin.	
$\overline{RESET1}$	15	O	Active low reset output of SVS-1	$\overline{RESETn}$ is an open-drain output pin. When $\overline{RESETn}$ is asserted, this pin remains in a low-impedance state. When $\overline{RESETn}$ is released, this pin goes to a high-impedance state after the delay time programmed by CTn.
$\overline{RESET2}$	16	O	Active low reset output of SVS-2	
$\overline{RESET3}$	17	O	Active low reset output of SVS-3	
$\overline{RESET4}$	18	O	Active low reset output of SVS-4	
SENSE1	10	I	Monitor voltage input to SVS-1	When the voltage at this terminal drops below the threshold voltage (V_{IT-}), $\overline{RESET1}$ is asserted.
SENSE2	9	I	Monitor voltage input to SVS-2	When the voltage at this terminal drops below the threshold voltage (V_{IT-}), $\overline{RESET2}$ is asserted.
SENSE3	8	I	Monitor voltage input to SVS-3	When the voltage at this terminal drops below the threshold voltage (V_{IT-}), $\overline{RESET3}$ is asserted.
SENSE4L	7	I	Falling monitor voltage input to SVS-4. When the voltage at this terminal drops below the threshold voltage (V_{IT-}), $\overline{RESET4}$ or RESET4 is asserted.	
SENSE4H	6	I	Rising monitor voltage input to SVS-4. When the voltage at this terminal exceeds the threshold voltage (V_{IT+}), $\overline{RESET4}$ or RESET4 is asserted. This pin can also be used to monitor the negative voltage rail in combination with VREF pin.	

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	14	I	Supply voltage. TI recommends connecting a 0.1-µF ceramic capacitor close to this pin.
VREF	13	O	Reference voltage output. By connecting a resistor network between this pin and the negative power rail, SENSE4H can monitor the negative power rail. This pin is intended to only source current into resistor(s). Do not connect only capacitors and do not connect resistor(s) to a higher voltage than this pin.
WDI	20	I	Watchdog timer (WDT) trigger input. Inputting either a positive or negative logic edge every 610 ms (typical) prevents WDT time out at the $\overline{WDO}$ or WDO pin. Timer starts from releasing event of $\overline{RESET1}$ or RESET1.
$\overline{WDO}$	19	O	Watchdog timer output. This is an open-drain output pin. When WDT times out, this pin goes to a low-impedance state to GND. If there is no WDT timeout, this pin stays in a high-impedance state.
(Thermal Pad)	(PAD)	—	This is the IC substrate. This pad must be connected only to GND or to the floating thermal pattern on the printed circuit board (PCB).

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	Input, V_{DD}	–0.3	7	V
	CT pin, V_{CT1}, V_{CT2}, V_{CT3}, V_{CT4}	–0.3	V_{DD} + 0.3	
	V_{RESET1}, V_{RESET2}, V_{RESET3}, V_{RESET4}, V_{MR}, V_{SENSE1}, V_{SENSE2}, V_{SENSE3}, $V_{SENSE4L}$, $V_{SENSE4H}$, V_{WDI}, V_{WDO}	–0.3	7	
Current	$\overline{RESETn}$, RESETn, $\overline{WDO}$, WDO, VREF pin current		5	mA
Power Dissipation	Continuous total	See *Thermal Information Table*.		
Temperature	Operating virtual junction, T_J (2)	–40	150	°C
	Operating ambient, T_A	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 5, 6, 10, 11, 15, 16)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		1.8		6.5	V
	Reset delay programming	CT1, CT2, CT3, CT4	0		V_{DD}	V
	Manual reset input	$\overline{MR}$	0		V_{DD}	V
	Watchdog timer trigger input WDI		0		V_{DD}	V
T_A	Operating free-air temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1]		TPS386000-Q1 RGP (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	21.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	42.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	21.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, 1.8 V < V_{DD} < 6.5 V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100 kΩ to V_{DD}, C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50 pF to GND, R_{WDO} = 100 kΩ to V_{DD}, C_{WDO} = 50 pF to GND, V_{MR} = 100 kΩ to V_{DD}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range			1.8		6.5	V
I_{DD}	Supply current (current into VDD pin)		V_{DD} = 3.3 V, $\overline{RESETn}$ or RESETn not asserted, WDI toggling[1], no output load, and VREF open		11	19	µA
			V_{DD} = 6.5 V, $\overline{RESETn}$ or RESETn not asserted, WDI toggling[1], no output load, and VREF open		13	22	
	Power-up reset voltage[2][3]		V_{OL} (max) = 0.2 V, I_{RESETn} = 15 µA			0.9	V
$V_{IT–}$	Negative-going input threshold voltage		SENSE1, SENSE2, SENSE3, SENSE4L	396	400	404	mV
V_{IT+}	Positive-going input threshold voltage		SENSE4H	396	400	404	mV
$V_{HYS–}$	Hysteresis (positive-going) on $V_{IT–}$		SENSE1, SENSE2, SENSE3, SENSE4L		3.5	10	mV
V_{HYS+}	Hysteresis (negative-going) on V_{IT+}		SENSE4H		3.5	10	mV
I_{SENSE}	Input current at SENSEm pin		V_{SENSEm} = 0.42 V	–25	±1	+25	nA
I_{CT}	CTn pin charging current	CT1	C_{CT1} > 220 pF, V_{CT1} = 0.5 V[4]	245	300	355	nA
		CT2, CT3, CT4	C_{CTn} > 220 pF, V_{CTn} = 0.5 V[4]	235	300	365	
$V_{TH(CTn)}$	CTn pin threshold		C_{CTn} > 220 pF	1.18	1.238	1.299	V
V_{IL}	$\overline{MR}$ and WDI logic low input			0		0.3 × V_{DD}	V

(1) Toggling WDI for a period less than t_{WDT} negatively affects I_{DD}.
(2) These specifications are beyond the recommended V_{DD} range, and only define $\overline{RESETn}$ or RESETn output performance during V_{DD} ramp up.
(3) The lowest supply voltage (V_{DD}) at which $\overline{RESETn}$ or RESETn becomes active; t_{RISE}(VDD) ≥ 15 µs/V.
(4) CTn (where *n* = 1, 2, 3, or 4) are constant current charging sources working from a range of 0 V to $V_{TH(CTn)}$, and the device is tested at V_{CTn} = 0.5 V. For I_{CT} performance between 0V and $V_{TH(CTn)}$, see Figure 26.

Electrical Characteristics (continued)

Over the operating temperature range of T_J = –40°C to +125°C, 1.8 V < V_{DD} < 6.5 V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100 kΩ to V_{DD}, C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50 pF to GND, R_{WDO} = 100 kΩ to V_{DD}, C_{WDO} = 50 pF to GND, V_{MR} = 100 kΩ to V_{DD}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	$\overline{MR}$ and WDI logic high input		0.7 × V_{DD}			V
V_{OL}	Low-level $\overline{RESETn}$ or RESETn output voltage	I_{OL} = 1 mA			0.4	V
		SENSEn = 0V, 1.3 V < V_{DD} < 1.8 V, I_{OL} = 0.4 mA(2)			0.3	
	Low-level WDO output voltage	I_{OL} = 1 mA			0.4	
I_{LKG}	$\overline{RESETn}$, RESETn, $\overline{WDO}$, and WDO leakage current	V_{RESETn} = 6.5 V, $\overline{RESETn}$, RESETn, $\overline{WDO}$, and WDO are logic high	–300		300	nA
V_{REF}	Reference voltage output	1 µA < I_{VREF} < 0.2 mA (source only, no sink)	1.18	1.20	1.22	V
C_{IN}	Input pin capacitance	CTn: 0 V to V_{DD}, other pins: 0 V to 6.5 V		5		pF

6.6 Timing Requirements

Over operating temperature range of T_J = –40°C to 125°C, 1.8 V < V_{DD} < 6.5 V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100 kΩ to V_{DD}, C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50 pF to GND, R_{WDO} = 100 kΩ to V_{DD}, C_{WDO} = 50 pF to GND, V_{MR} = 100 kΩ to V_{DD}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Nominal values are at T_J = 25°C.

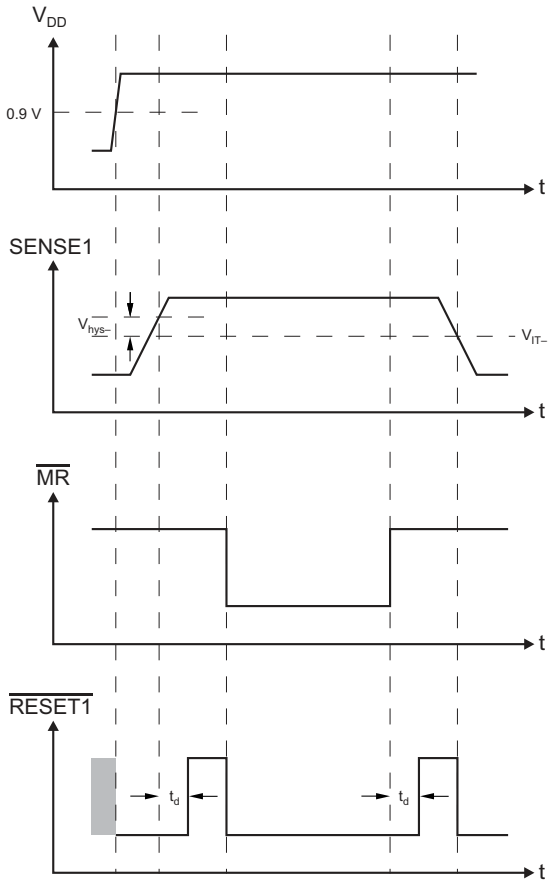
		MIN	NOM	MAX	UNIT
t_W	Input pulse width to SENSEm and $\overline{MR}$ pins	SENSEm: 1.05 V_{IT-} → 0.95 V_{IT-} or 0.95 V_{IT+} → 1.05 V_{IT+}		4		µs
		$\overline{MR}$: 0.7 V_{DD} → 0.3 V_{DD}		1		ns

6.7 Switching Characteristics

Over operating temperature range of T_J = –40°C to 125°C, 1.8 V < V_{DD} < 6.5 V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100 kΩ to V_{DD}, C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50 pF to GND, R_{WDO} = 100 kΩ to V_{DD}, C_{WDO} = 50 pF to GND, V_{MR} = 100 kΩ to V_{DD}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Typical values are at T_J = 25°C.

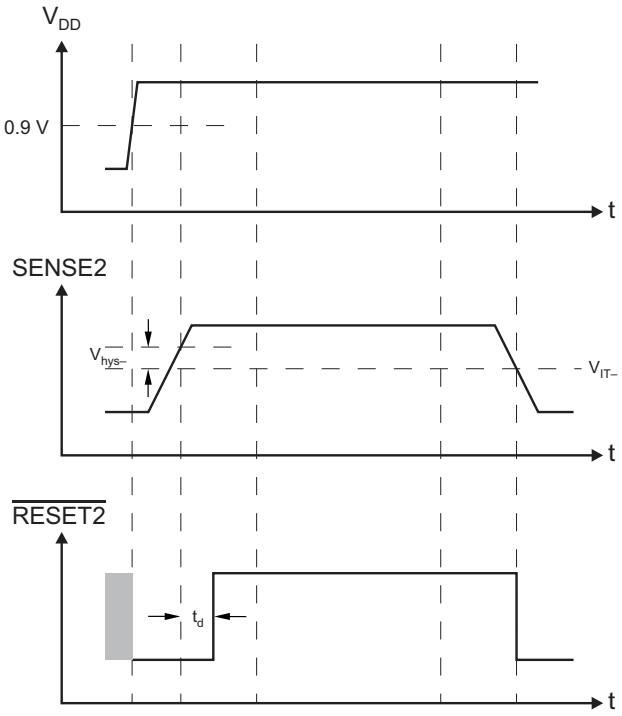
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	$\overline{RESETn}$ or RESETn delay time	CTn = Open	14	20	24	ms
		CTn = V_{DD}	225	300	375	
t_{WDT}	Watchdog timer time-out period(1)		450	600	750	ms

(1) Start from $\overline{RESET1}$ or RESET1 release or last WDI transition.



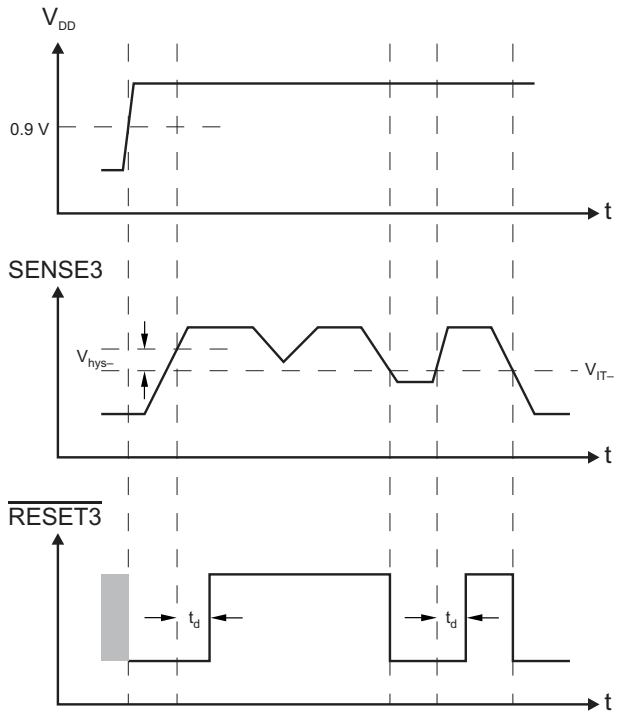
NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$.

Figure 1. SVS-1 Timing Diagram



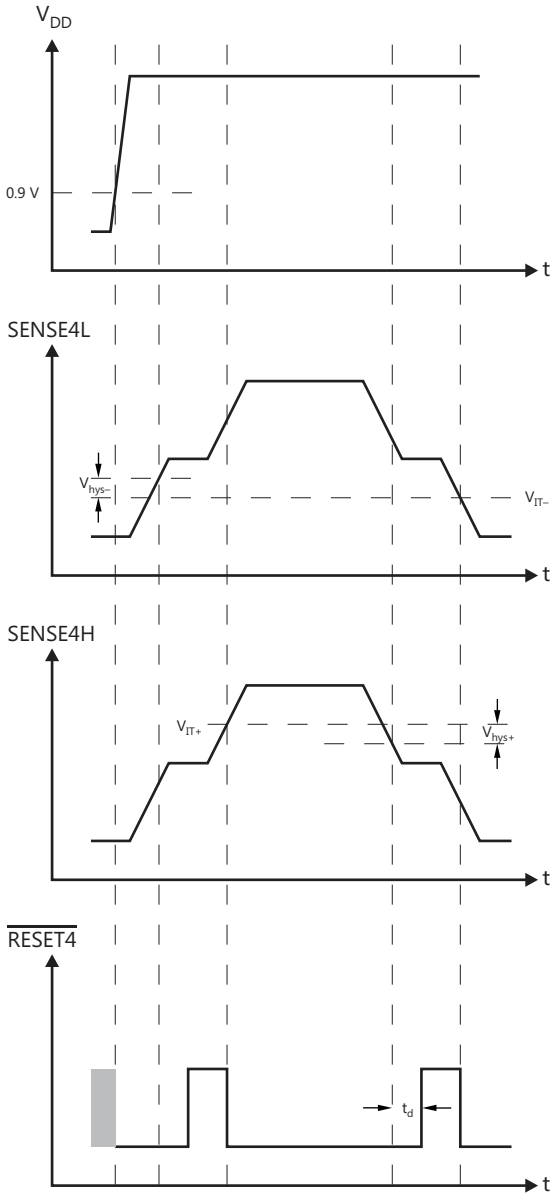
NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$.

Figure 2. SVS-2 Timing Diagram



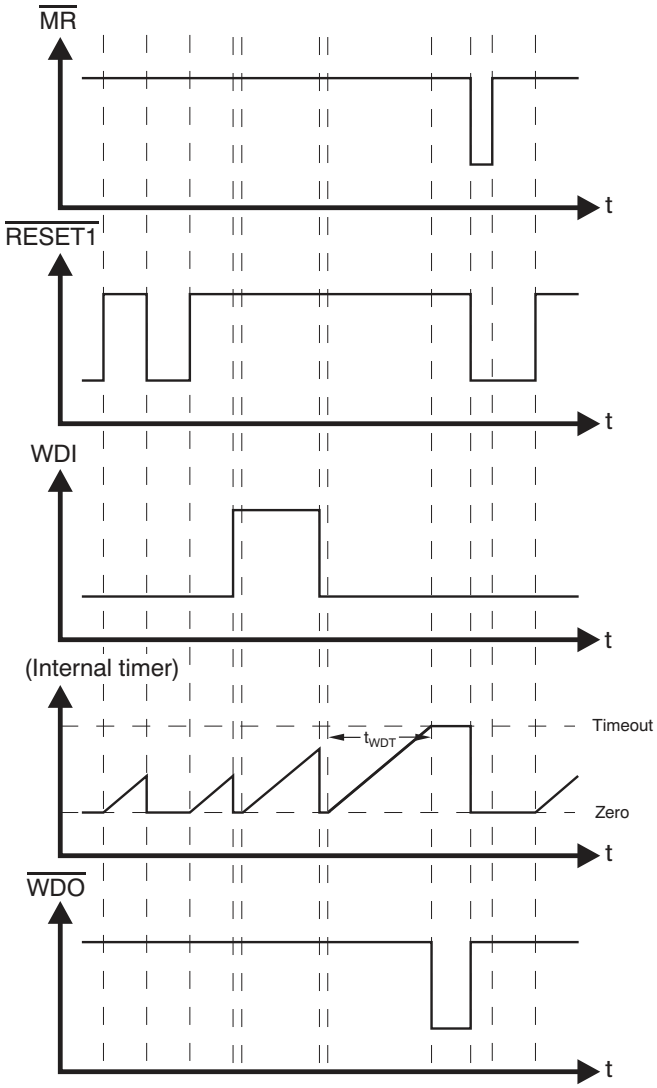
NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$.

Figure 3. SVS-3 Timing Diagram



NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$.

Figure 4. SVS-4 Timing Diagram

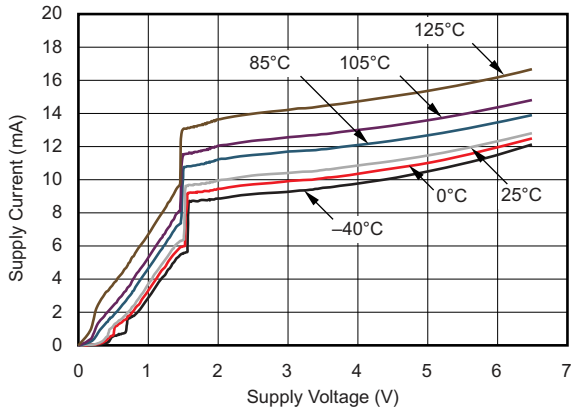


NOTE: The TPS386000-Q1 is shown here using $\overline{\text{RESETn}}$ and $\overline{\text{WDO}}$.

Figure 5. WDT Timing Diagram

6.8 Typical Characteristics

At T_A = +25°C, and V_{DD} = 3.3 V, unless otherwise noted.



UVLO released at approximately 1.5 V.

Figure 6. TPS386000-Q1 Supply Current vs Supply Voltage

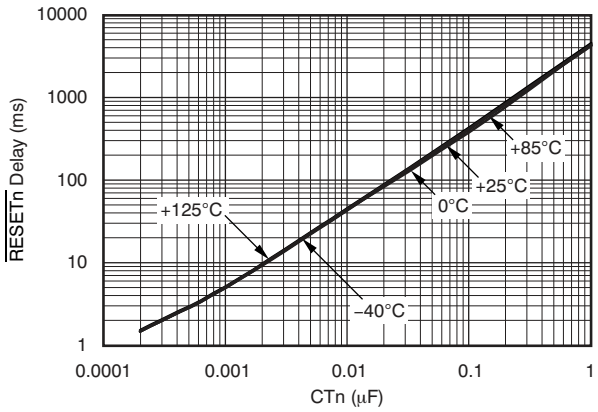


Figure 7. TPS386000-Q1 $\overline{\text{RESETn}}$ Timeout Period vs CTn

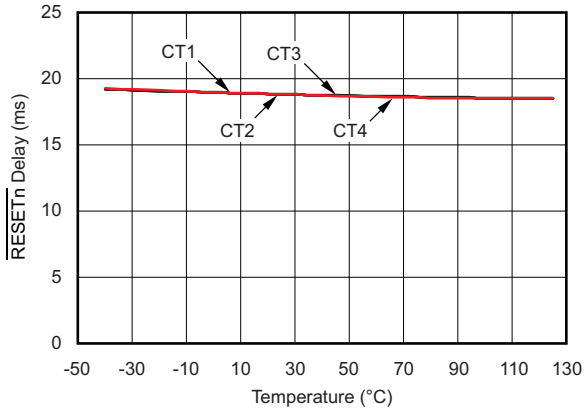


Figure 8. TPS386000-Q1 $\overline{\text{RESETn}}$ Timeout Period vs Temperature (CTn = Open)

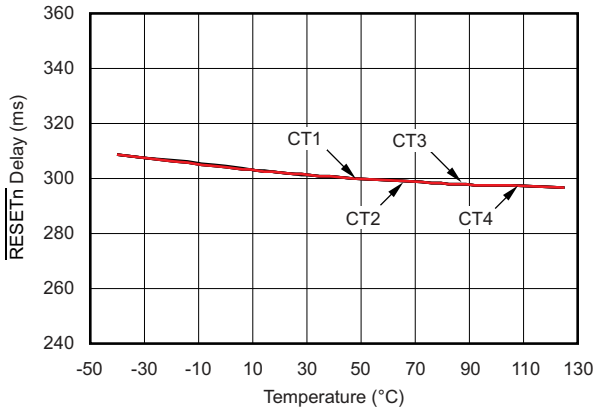
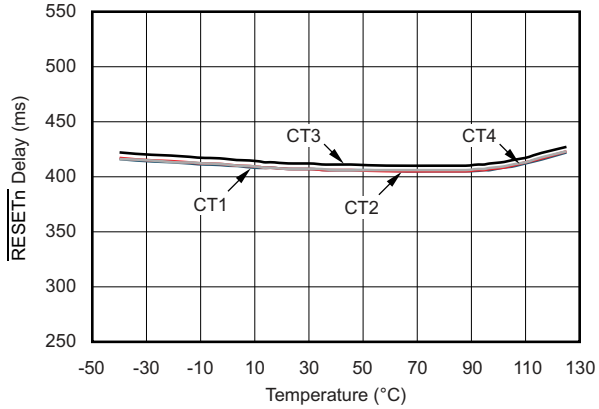


Figure 9. TPS386000-Q1 $\overline{\text{RESETn}}$ Timeout Period vs Temperature ($CTn = V_{DD}$)



These curves contain variance of capacitor values

Figure 10. TPS386000-Q1 $\overline{\text{RESETn}}$ Timeout Period vs Temperature (CTn = 0.1 µF)

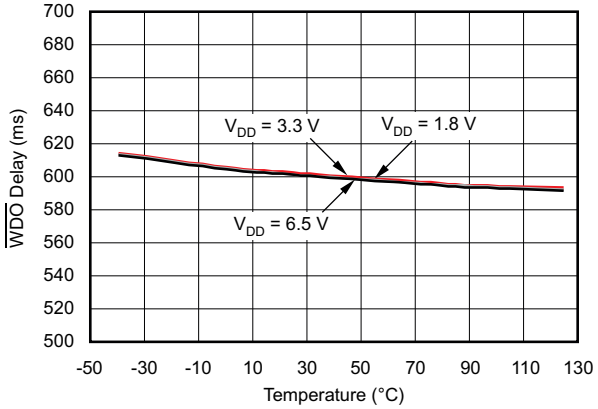
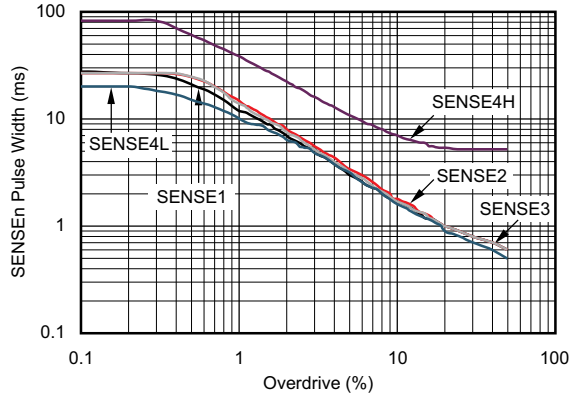


Figure 11. TPS386000-Q1 $\overline{\text{WDO}}$ Timeout Period vs Temperature

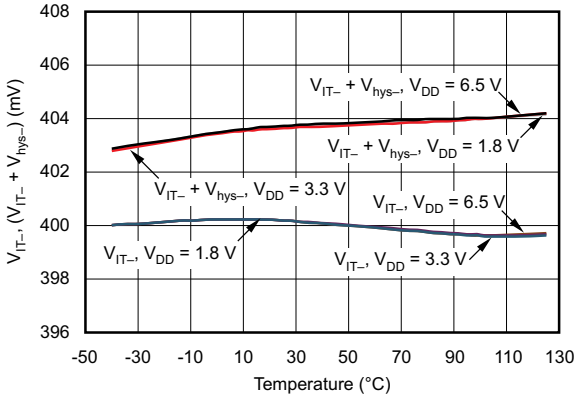
Typical Characteristics (continued)

At T_A = +25°C, and V_{DD} = 3.3 V, unless otherwise noted.



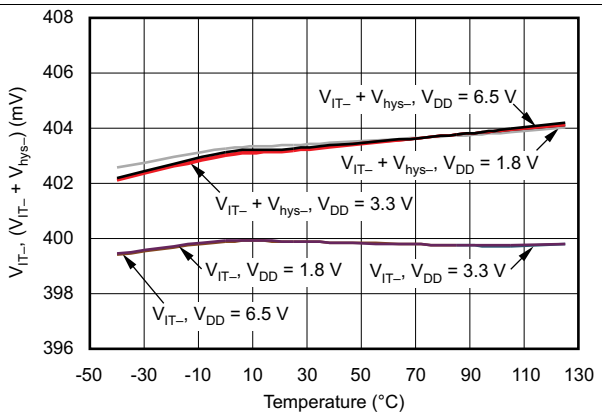
See Figure 5 for the measurement technique.

Figure 12. TPS386000-Q1 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage



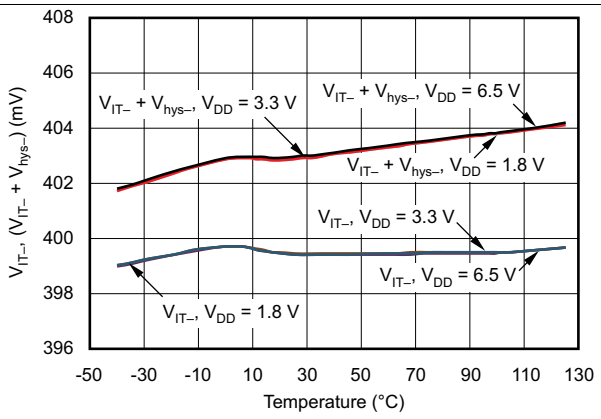
2 mV » 0.5%

Figure 13. TPS386000-Q1 SENSE1 Threshold Voltage vs Temperature



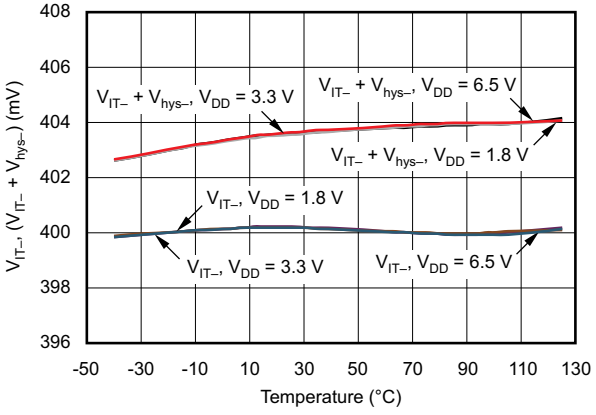
2 mV » 0.5%

Figure 14. TPS386000-Q1 SENSE2 Threshold Voltage vs Temperature



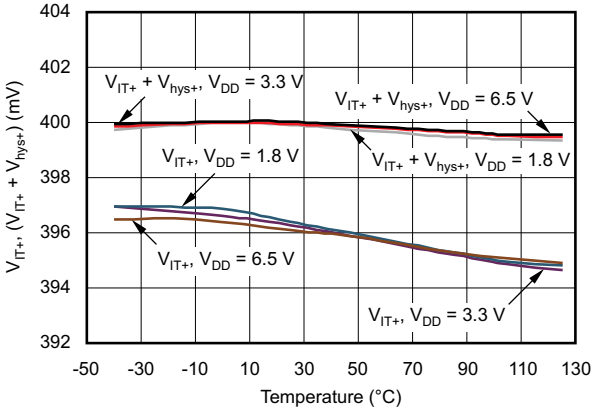
2 mV » 0.5%

Figure 15. TPS386000-Q1 SENSE3 Threshold Voltage vs Temperature



2 mV » 0.5%

Figure 16. TPS386000-Q1 SENSE4L Threshold Voltage vs Temperature



2 mV » 0.5%

Figure 17. TPS386000-Q1 SENSE4H Threshold Voltage vs Temperature

Typical Characteristics (continued)

At T_A = +25°C, and V_{DD} = 3.3 V, unless otherwise noted.

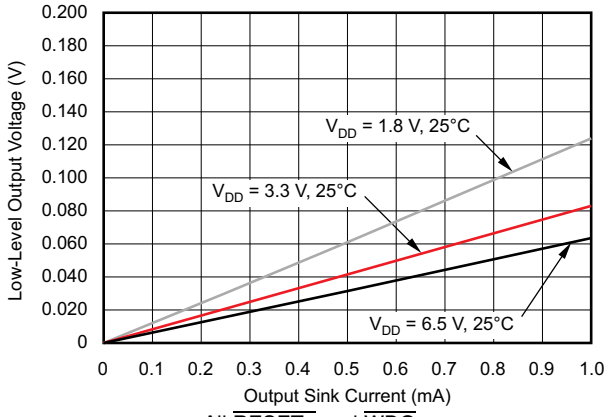


Figure 18. Output Voltage Low vs Output Current

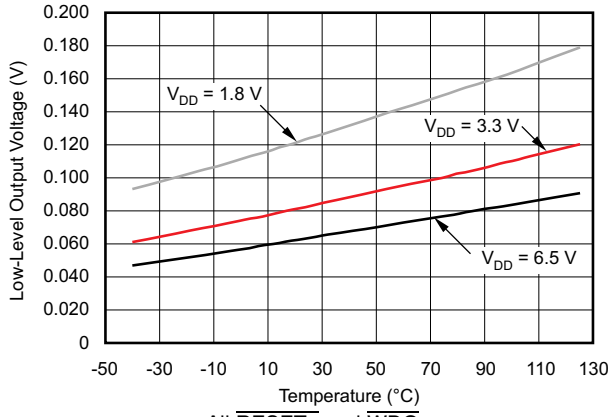


Figure 19. Output Voltage Low at 1 mA vs Temperature

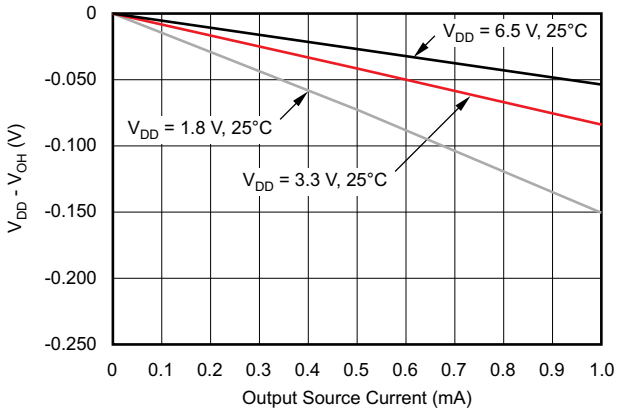


Figure 20. Output Voltage High vs Output Current

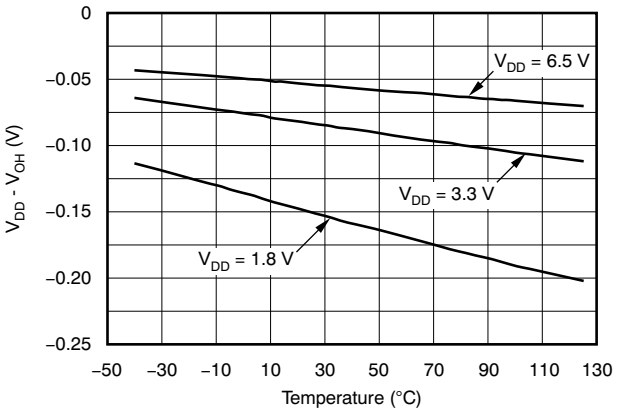


Figure 21. Output Voltage High at 1 mA vs Temperature

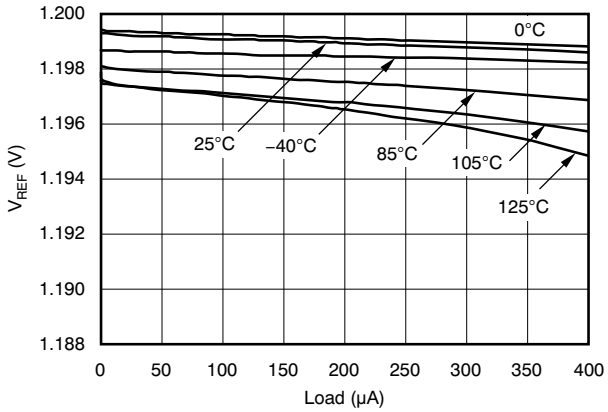


Figure 22. TPS386000-Q1 V_{REF} Output Load Regulation (V_{DD} = 1.8 V)

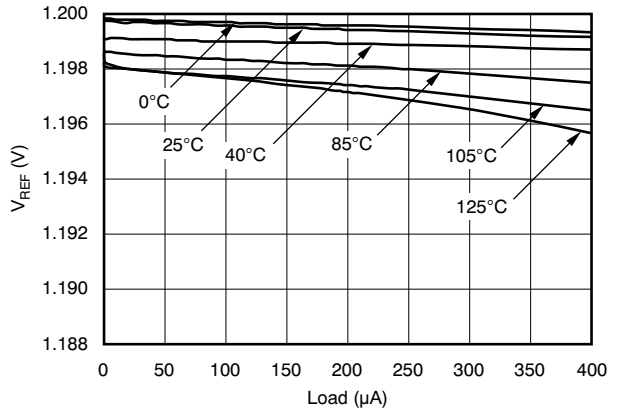
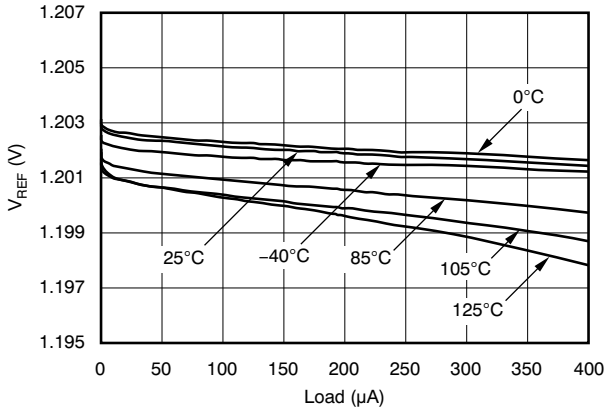


Figure 23. TPS386000-Q1 V_{REF} Output Load Regulation (V_{DD} = 3.3 V)

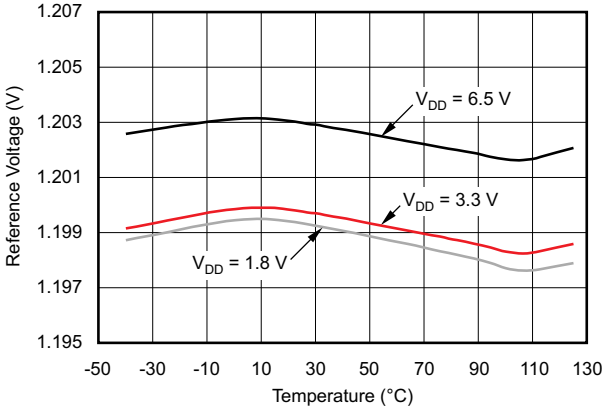
Typical Characteristics (continued)

At T_A = +25°C, and V_{DD} = 3.3 V, unless otherwise noted.



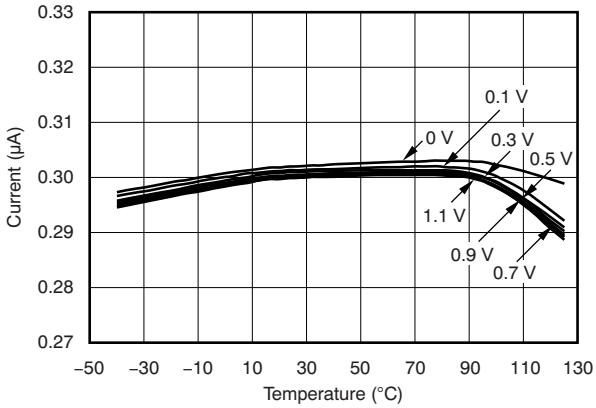
Y-axis (1.195 V to 1.207 V) is 1% of 1.2 V

Figure 24. TPS386000-Q1 V_{REF} Output Load Regulation (V_{DD} = 6.5 V)



Y-axis (1.195 V to 1.207 V) is 1% of 1.2 V

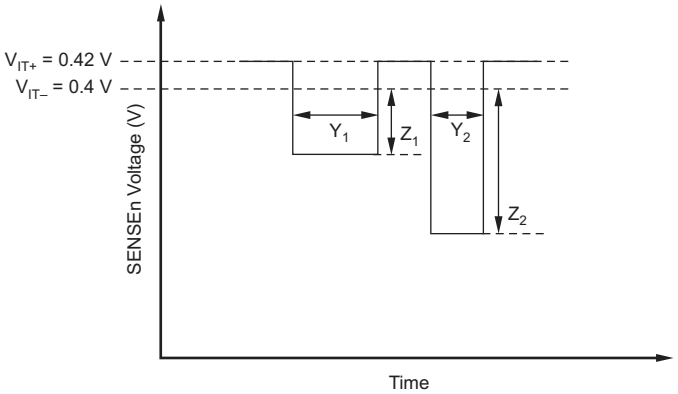
Figure 25. TPS386000-Q1 V_{REF} at 0 µA vs Temperature



Minimum and maximum values of the Y-axis are ±10% of 0.3 mA

Figure 26. TPS386000-Q1 CT1 to CT4 Pin Charging Current vs Temperature Over CT Pin Voltage

7 Parametric Measurement information



$$X_1 = \frac{Z_1}{0.4} \times 100\ (\%)$$

$$X_2 = \frac{Z_2}{0.4} \times 100\ (\%)$$

X_1 and X_2 are overdrive (%) values calculated from the actual SENSEn voltage amplitudes measured as Z_1 and Z_2.

Y_N is the minimum pulse width that gives RESETn or $\overline{\text{RESETn}}$ transition. Greater Z_N produces shorter Y_N.

For SENSE4H, this graph must be inverted 180° on the voltage axis.

Figure 27. Test Circuit

8 Detailed Description

8.1 Overview

The TPS386000-Q1 multi-channel supervisory device family combines four complete SVS function sets into one IC. The design of each SVS channel is based on the single-channel supervisory device series, TPS3808. The TPS386000-Q1 is designed to assert $\overline{\text{RESET}}$n or RESETn signals, as shown in Table 1, Table 2, Table 3, and Table 4. The $\overline{\text{RESET}}$n or RESETn outputs remain asserted during a user-configurable delay time after the event of reset release (see the *Reset Delay Time* section).

8.2 Functional Block Diagram

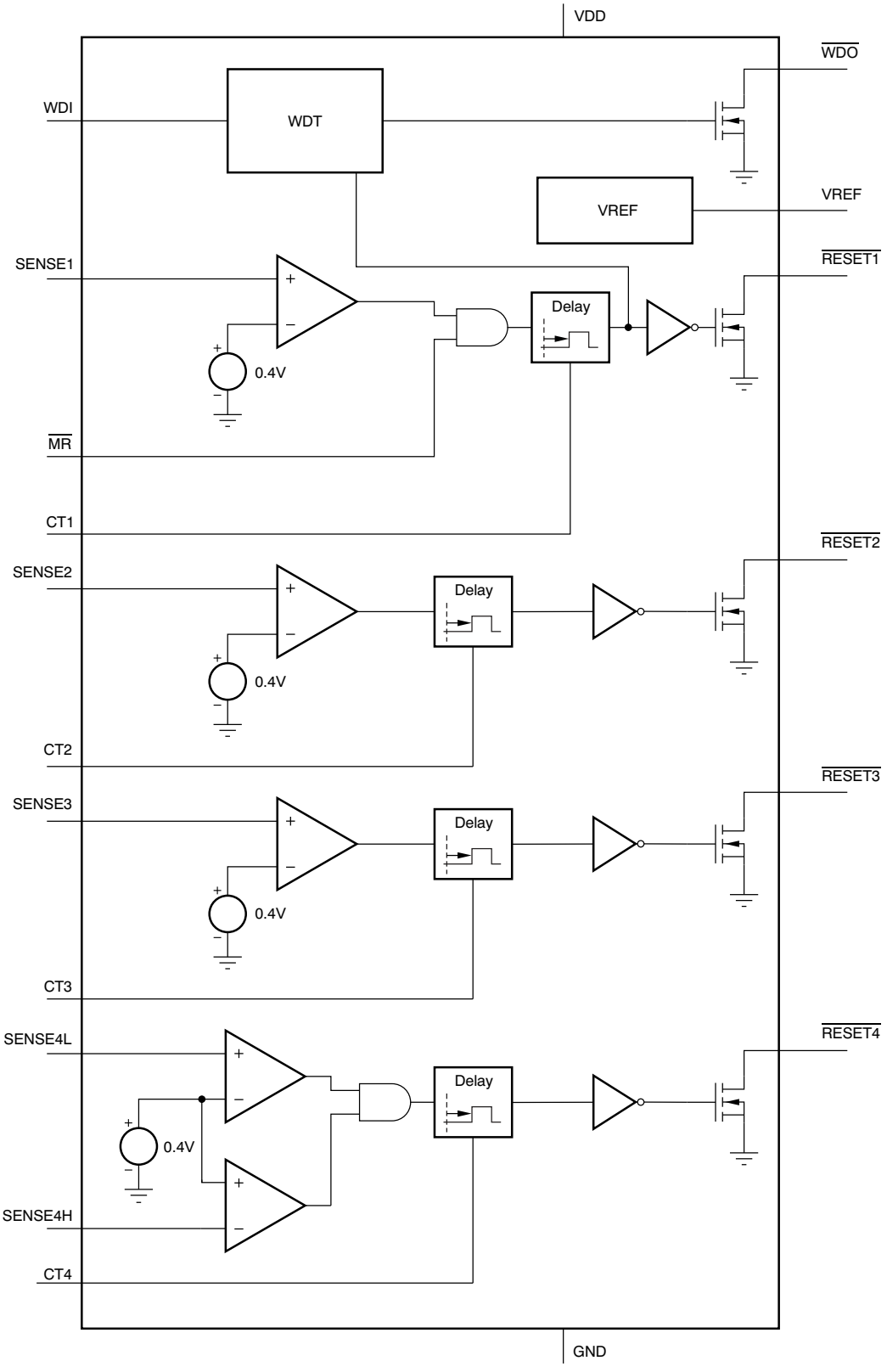


Figure 28. TPS386000-Q1

8.3 Feature Description

8.3.1 Voltage Monitoring

Each SENSEm (m = 1, 2, 3, 4L) pin can be set to any voltage threshold above 0.4 V using an external resistor divider. The SENSE4H pin can be used for any overvoltage detection greater than 0.4 V, or for negative voltage detection using an external resistor divider (see the *Sensing Voltage Less Than 0.4 V* section). A broad range of voltage threshold and reset delay time adjustments can be supported, allowing these devices to be used in a wide array of applications.

8.3.2 RESET Output

In a typical TPS386000-Q1 application, $\overline{\text{RESETn}}$ or RESETn outputs are connected to the reset input of a processor (DSP, CPU, FPGA, ASIC, etc.), or connected to the enable input of a voltage regulator (DC-DC, LDO, etc.)

The TPS386000-Q1 provides open-drain reset outputs. Pullup resistors must be used to hold these lines high when $\overline{\text{RESETn}}$ is not asserted, or when RESETn is asserted. By connecting pullup resistors to the proper voltage rails (up to 6.5 V), $\overline{\text{RESETn}}$ or RESETn output nodes can be connected to the other devices at the correct interface voltage levels. The pullup resistor should be no smaller than 10 kΩ because of the safe operation of the output transistors. By using wired-OR logic, any combination of $\overline{\text{RESETn}}$ can be merged into one logic signal.

All $\overline{\text{RESETn}}$ or RESETn connections must be compatible with the VDD logic level.

The $\overline{\text{RESETn}}$ or RESETn outputs are defined for VDD voltage higher than 0.9 V. To ensure that the target processor(s) are properly reset, the VDD supply input should be fed by the available power rail as early as possible in application circuits. Table 1, Table 2, Table 3, and Table 4 are truth tables that describe how the outputs are asserted or released. Figure 1, Figure 2, Figure 3, and Figure 4 show the SVS-n timing diagrams. When the condition(s) are met, the device changes the state of SVS-n from asserted to released after a user-configurable delay time. However, the transitions from released-state to asserted-state are performed almost immediately with minimal propagation delay. Figure 3 describes relationship between threshold voltages (V_{IT-} and V_{HYS-}) and SENSEm voltage; and all SVS-1, SVS-2, SVS-3, and SVS-4 have the same behavior of Figure 3.

8.3.3 Manual Reset

The manual reset ($\overline{\text{MR}}$) input allows external logic signal from other processors, logic circuits, and/or discrete sensors to initiate a device reset. Because $\overline{\text{MR}}$ is connected to SVS-1, the $\overline{\text{RESET1}}$ or RESET1 pin is intended to be connected to processor(s) as a primary reset source. A logic low at $\overline{\text{MR}}$ causes $\overline{\text{RESET1}}$ or RESET1 to assert. After $\overline{\text{MR}}$ returns to a logic high and SENSE1 is above its reset threshold, $\overline{\text{RESET1}}$ or RESET1 is released after the user-configured reset delay time. Note that unlike the TPS3808 series, the TPS386000-Q1 does not integrate an internal pullup resistor between $\overline{\text{MR}}$ and VDD.

To control the $\overline{\text{MR}}$ function from more than one logic signal, the logic signals can be combined by wired-OR into the $\overline{\text{MR}}$ pin using multiple NMOS transistors and one pullup resistor.

8.3.4 Watchdog Timer

The TPS386000-Q1 provides a watchdog timer with a dedicated watchdog error output, $\overline{\text{WDO}}$ or WDO. The $\overline{\text{WDO}}$ or WDO output enables application board designers to easily detect and resolve the hang-up status of a processor. As with $\overline{\text{MR}}$, the watchdog timer function of the device is also tied to SVS-1. Figure 5 shows the timing diagram of the WDT function. Once $\overline{\text{RESET1}}$ or RESET1 is released, the internal watchdog timer starts its countdown. Inputting a logic level transition at WDI resets the internal timer count and the timer restarts the countdown. If the TPS386000-Q1 fails to receive any WDI rising or falling edge within the WDT period, the WDT times out and asserts $\overline{\text{WDO}}$ or WDO. After $\overline{\text{WDO}}$ or WDO is asserted, the device holds the status with the internal latch circuit. To clear this timeout status, a reset assertion of $\overline{\text{RESET1}}$ or RESET is required. That is, a negative pulse to $\overline{\text{MR}}$, a SENSE1 voltage less than V_{IT-}, or a VDD power-down is required.

To reset the processor by WDT timeout, $\overline{\text{WDO}}$ can be combined with $\overline{\text{RESET1}}$ by using the wired-OR with the TPS386000-Q1 option.

For legacy applications where the watchdog timer timeout causes $\overline{\text{RESET1}}$ to assert, connect $\overline{\text{WDO}}$ to $\overline{\text{MR}}$; see Figure 31 for the connections and see Figure 29 and Figure 30 for the timing diagram. This legacy support configuration is available with the TPS386000-Q1.

Feature Description (continued)

8.3.5 Immunity to SENSEn Voltage Transients

The TPS386000-Q1 is relatively immune to short negative transients on the SENSEn pin. Sensitivity to transients depends on threshold overdrive, as shown in the typical performance graph *TPS386000-Q1 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage* (Figure 12).

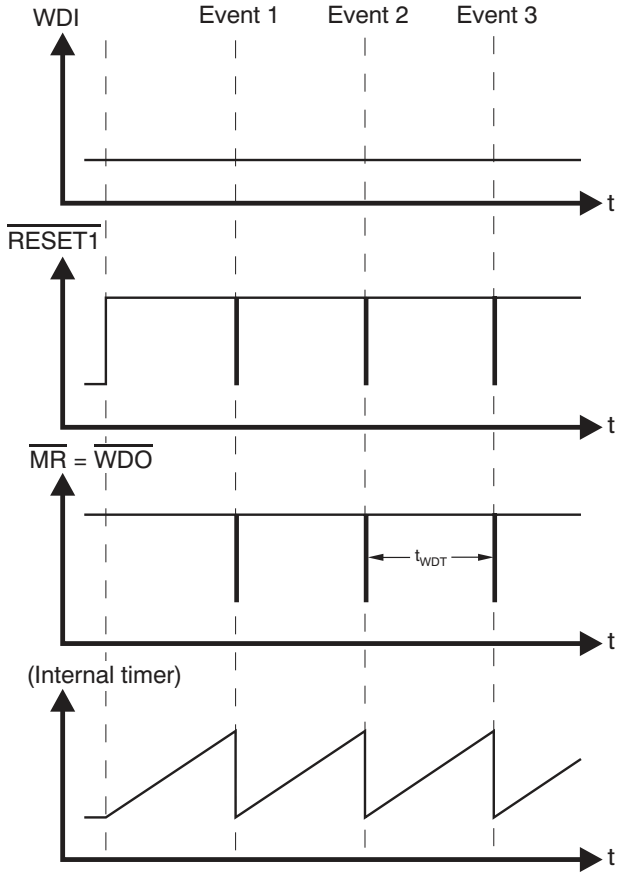


Figure 29. Legacy WDT Configuration Timing Diagram

Feature Description (continued)

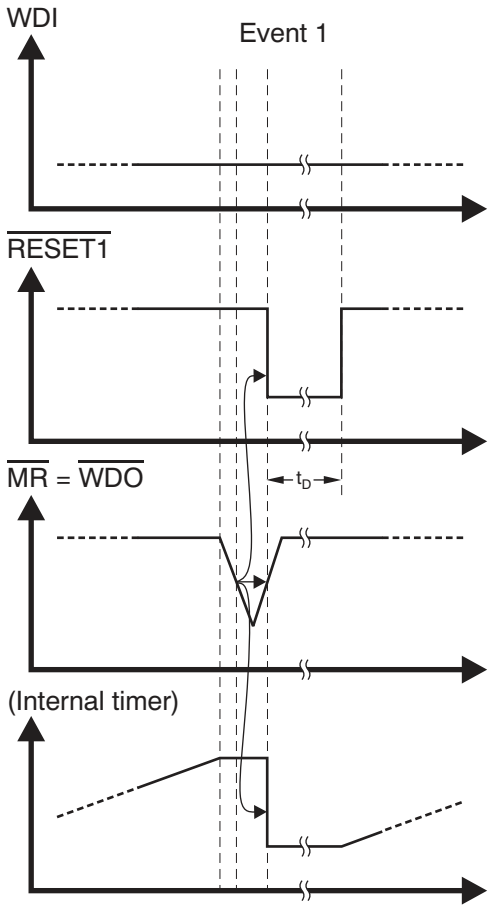


Figure 30. Enlarged View of Event 1 from Figure 29

8.4 Device Functional Modes

8.4.1 Overview

The TPS386000-Q1 multi-channel supervisory device family combines four complete SVS function sets into one IC. The design of each SVS channel is based on the single-channel supervisory device series, TPS3808. The TPS386000-Q1 is designed to assert $\overline{\text{RESET}}$n or RESETn signals, as shown in Table 1, Table 2, Table 3, and Table 4. The $\overline{\text{RESET}}$n or RESETn outputs remain asserted during a user-configurable delay time after the event of reset release (see the *Reset Delay Time* section).

Table 1. SVS-1 Truth Table

CONDITION		OUTPUT	STATUS
		TPS386000-Q1	
$\overline{\text{MR}}$ = Low	SENSE1 < V_{IT-}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = Low	SENSE1 > V_{IT-}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = High	SENSE1 < V_{IT-}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = High	SENSE1 > V_{IT-}	$\overline{\text{RESET1}}$ = High	**Reset released after delay**

Table 2. SVS-2 Truth Table

CONDITION	OUTPUT TPS386000-Q1	STATUS
SENSE2 < V_{IT-}	$\overline{RESET2}$ = Low	Reset asserted
SENSE2 > V_{IT-}	$\overline{RESET2}$ = High	**Reset released after delay**

Table 3. SVS-3 Truth Table

CONDITION	OUTPUT TPS386000-Q1	STATUS
SENSE3 < V_{IT-}	$\overline{RESET3}$ = Low	Reset asserted
SENSE3 > V_{IT-}	$\overline{RESET3}$ = High	**Reset released after delay**

Table 4. SVS-4 Truth Table

CONDITION		OUTPUT TPS386000-Q1	STATUS
SENSE4L < V_{IT-}	SENSE4H > V_{IT+}	$\overline{RESET4}$ = Low	Reset asserted
SENSE4L < V_{IT-}	SENSE4H < V_{IT+}	$\overline{RESET4}$ = Low	Reset asserted
SENSE4L > V_{IT-}	SENSE4H > V_{IT+}	$\overline{RESET4}$ = Low	Reset asserted
SENSE4L > V_{IT-}	SENSE4H < V_{IT+}	$\overline{RESET4}$ = High	**Reset released after delay**

Table 5. Watchdog Timer (WDT) Truth Table

CONDITION				OUTPUT	
$\overline{WDO}$	WDO	$\overline{RESET1}$ OR RESET1	WDI PULSE INPUT	TPS386000-Q1	STATUS
Low	High	Asserted	Toggling	$\overline{WDO}$ = low	Remains in WDT timeout
Low	High	Asserted	610 ms after last WDI↑ or WDI↓	$\overline{WDO}$ = low	Remains in WDT timeout
Low	High	Released	Toggling	$\overline{WDO}$ = low	Remains in WDT timeout
Low	High	Released	610 ms after last WDI↑ or WDI↓	$\overline{WDO}$ = low	Remains in WDT timeout
High	Low	Asserted	Toggling	$\overline{WDO}$ = high	Normal operation
High	Low	Asserted	610 ms after last WDI↑ or WDI↓	$\overline{WDO}$ = high	Normal operation
High	Low	Released	Toggling	$\overline{WDO}$ = high	Normal operation
High	Low	Released	610 ms after last WDI↑ or WDI↓	$\overline{WDO}$ = low	Enters WDT timeout

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 SENSE Input

The SENSEm inputs are pins that allow any system voltages to be monitored. If the voltage at the SENSE1, SENSE2, SENSE3, or SENSE4L pins drops below V_{IT-}, then the corresponding reset outputs are asserted. If the voltage at the SENSE4H pin exceeds V_{IT+}, then $\overline{\text{RESET4}}$ or RESET4 is asserted. The comparators have a built-in hysteresis to ensure smooth reset output assertions and deassertions. Although not required in most cases, for extremely noise applications, it is good analog design practice to place a 1 nF to 10 nF bypass capacitor at the SENSEm input in order to reduce sensitivity to transients, layout parasitics, and interference between power rails monitored by this device. A typical connection of resistor dividers are shown in Figure 31. All the SENSEm pins can be used to monitor voltage rails down to 0.4 V. Threshold voltages can be calculated by following equations:

(1)

$$V_{DD1\_target} = (1 + R_{S1H}/R_{S1L}) \times 0.4\ (V) \quad (2)$$

$$V_{DD2\_target} = (1 + R_{S2H}/R_{S2L}) \times 0.4\ (V) \quad (3)$$

$$V_{DD3\_target} = (1 + R_{S3H}/R_{S3L}) \times 0.4\ (V) \quad (4)$$

$$V_{DD4\_target1} = \{1+ R_{S4H}/R_{S4M} + R_{S4L})\} \times 0.4\ (V)$$

where

- $V_{DD4\_target1}$ is the undervoltage threshold (5)

$$V_{DD4\_target2} = \{1+ R_{S4H} + R_{S4M})/R_{S4L}\} \times 0.4\ (V)$$

where

- $V_{DD4\_target2}$ is the overvoltage threshold (6)

9.1.2 Window Comparator

The comparator at the SENSE4H pin has the opposite comparison polarity to the other SENSEm pins. In the configuration shown in Figure 31, this comparator monitors overvoltage of the VDD4 node; combined with the comparator at SENSE4L, SVS-4 forms a window comparator.

9.1.3 Sensing Voltage Less Than 0.4 V

By using voltage reference output VREF, the SVS-4 comparator can monitor negative voltage or positive voltage lower than 0.4 V. Figure 32 shows this usage in an application circuit. SVS-4 monitors the positive and negative voltage power rail (for example, +15V and –15V supply to an op amp) and the $\overline{\text{RESET4}}$ or RESET4 output status continues to be as described in Table 4. Note that R_{S42H} is located at higher voltage position than R_{S42L}. The threshold voltage calculations are shown in the following equations:

$$VDD41\_target = (1 + R_{S41H}/R_{S41L}) \times 0.4\ (V) \quad (7)$$

$$VDD42\_target = (1 + R_{S42L}/R_{S42H}) \times 0.4 - R_{S42L}/R_{S42H} \times V_{REF} = 0.4 - R_{S42L}/R_{S42H} \times 0.8\ (V) \quad (8)$$

Application Information (continued)

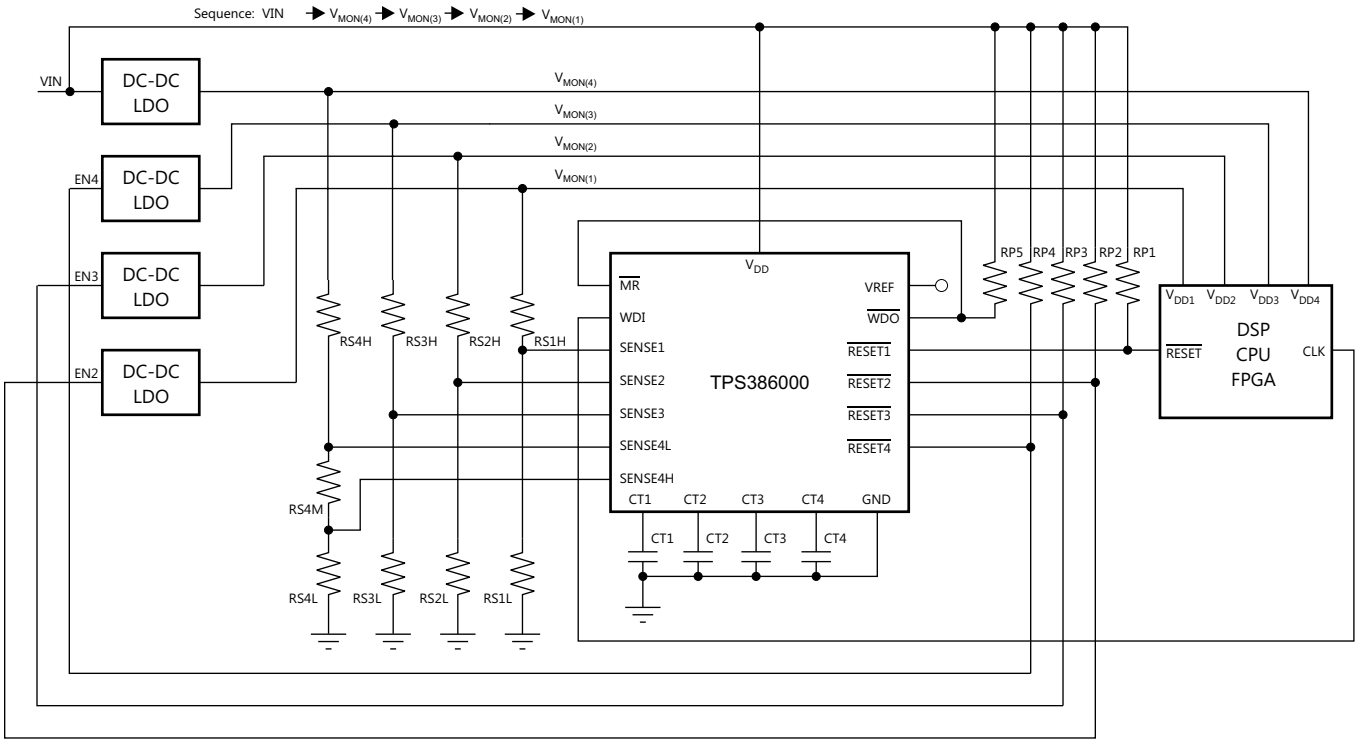


Figure 31. Typical Application Circuit (SVS-4: Window Comparator)

9.1.4 Reset Delay Time

Each of the SVS-n channels can be configured independently in one of three modes. Table 6 describes the delay time settings.

Table 6. Delay Timing Selection

CTn CONNECTION	DELAY TIME
Pullup to V_{DD}	300 ms (typical)
Open	20 ms (typical)
Capacitor to GND	Programmable

To select the 300-ms fixed delay time, the CTn pin should be pulled up to VDD using a resistor from 40 kΩ to 200 kΩ. Note that there is a pulldown transistor from CTn to GND that turns on every time the device powers on to determine and confirm CTn pin status; therefore, a direct connection of CTn to VDD causes a large current flow. To select the 20-ms fixed delay time, the CTn pin should be left open. To program a user-defined adjustable delay time, an external capacitor must be connected between CTn and GND. The adjustable delay time can be calculated by the following equation:

$$C_{CT}\ (nF) = [t_{DELAY}\ (ms) - 0.5(ms)] \times 0.242 \quad (9)$$

Using this equation, a delay time can be set to between 1.4 ms to 10 s. The external capacitor should be greater than 220 pF (nominal), so that the TPS386000-Q1 can distinguish it from an open CT pin. The reset delay time is determined by the time it takes an on-chip, precision 300 nA current source to charge the external capacitor to 1.24 V. When the $\overline{\text{RESET}}$n or $\overline{\text{RESET}}$n outputs are asserted, the corresponding capacitors are discharged. When the condition to release $\overline{\text{RESET}}$n or $\overline{\text{RESET}}$n occurs, the internal current sources are enabled and begin to charge the external capacitors. When the CTn voltage on a capacitor reaches 1.24 V, the corresponding $\overline{\text{RESET}}$n or $\overline{\text{RESET}}$n pins are released. Note that a low leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

9.2 Typical Application

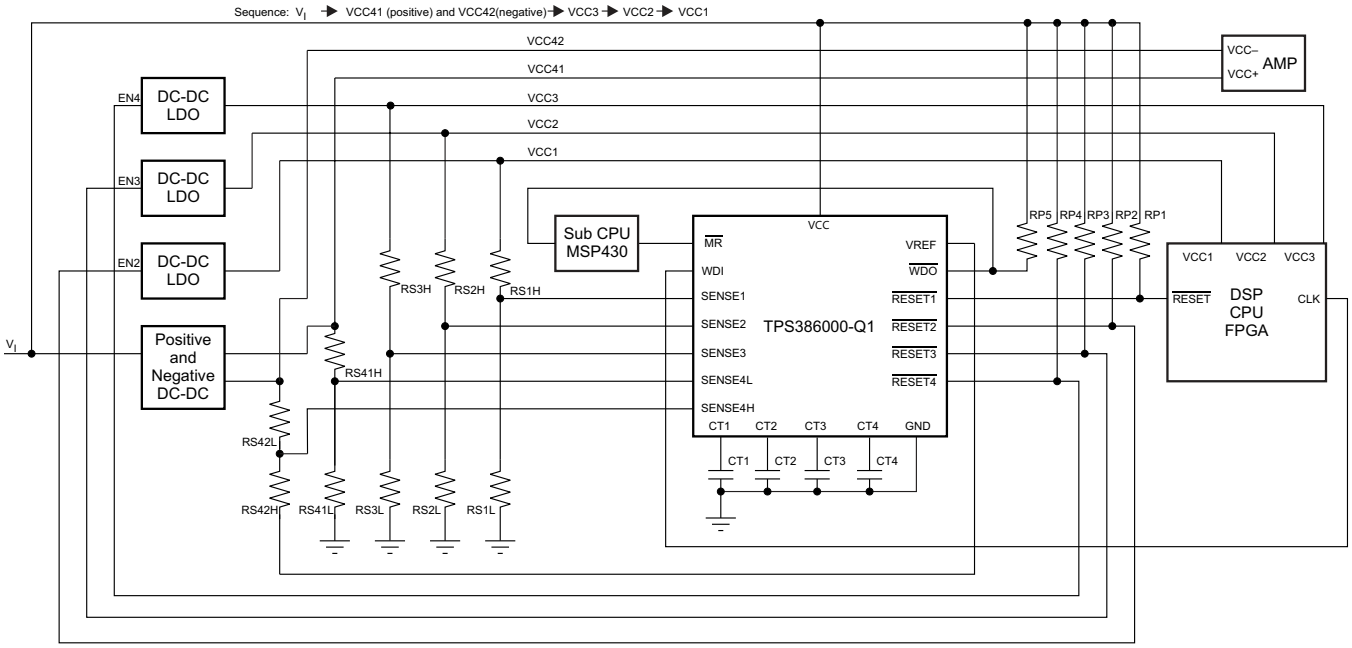


Figure 32. Application Schematic

9.2.1 Design Requirements

This design is intended to monitor the voltage rails for an FPGA. Table 7 summarizes the design requirements.

Table 7. Design Requirements

PARAMETER	DESIGN REQUIREMENT
V_{DD}	5 V
$V_{MON(1)}$	1.8 V –5%
$V_{MON(2)}$	1.5 V –5%
$V_{MON(3)}$	1.2 V –5%
$V_{MON(4)}$	1 V ±5%
Approximate start-up time	100 ms

9.2.2 Detailed Design Procedure

Select the pullup resistors to be 100 kΩ to ensure that $V_{OL} \leq 0.4$ V.

Use Equation 9 to set CT = 22 nF for all channels to obtain an approximate start-up delay of 100 ms.

Select RSnL = 10 kΩ for all channels to ensure DC accuracy.

Use Equation 1 through Equation 6 to determine the values of RSnH and RS4M. Using standard 1% resistors, Table 8 shows the results.

Table 8. Design Results

RESISTOR	VALUE (kΩ)
RS1H	32.4
RS2H	25.5
RS3H	18.7
RS4H	14.3
RS4M	1

The FPGA does not have a separate watchdog failure input, so a legacy connection is used by connecting $\overline{WDO}$ to $\overline{MR}$.

9.2.3 Application Curves

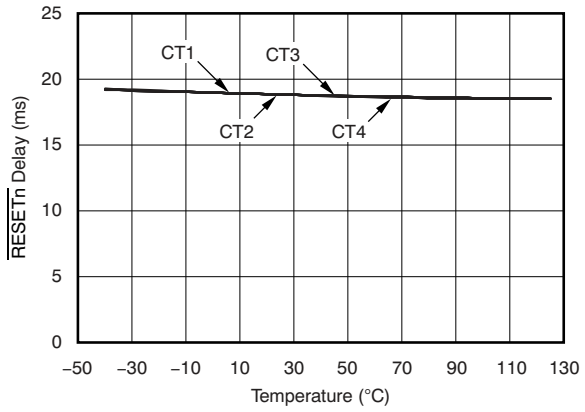
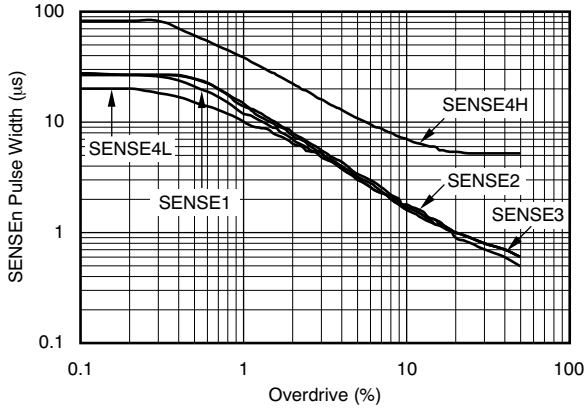


Figure 33. TPS386000-Q1 (CTn = Open) $\overline{RESETn}$ Time-out Period vs Temperature



See Figure 27 for measurement technique

Figure 34. TPS386000-Q1 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage

10 Power Supply Recommendations

The TPS386000-Q1 can operate using a 1.8-V to a 6.5-V input supply. TI recommends placing a 0.1-µF capacitor placed next to the V_{DD} pin to the GND node. This power supply should be less than 1.8 V in normal operation to ensure that the internal UVLO circuit does not assert reset.

11 Layout

11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit-board (PCB) that is used for the TPS386000-Q1 family of devices.

- Keep the traces to the timer capacitors as short as possible to optimize accuracy.
- Avoid long traces from the SENSE pin to the resistor divider. Instead, run the long traces from the RSnH to $V_{MON(n)}$.
- Place the V_{DD} decoupling capacitor (C_{VDD}) close to the device.
- Avoid using long traces for the V_{DD} supply node. The V_{DD} capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum V_{DD} voltage.

11.2 Layout Example

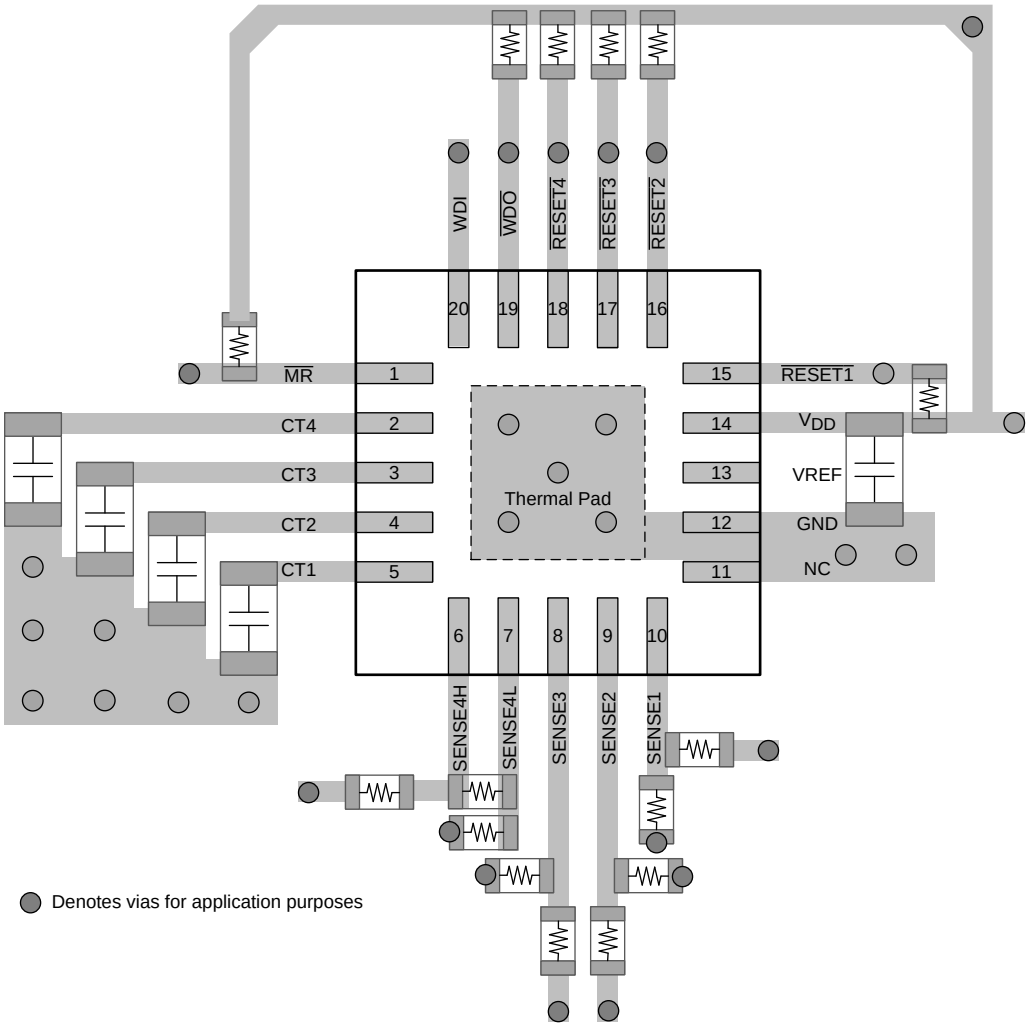


Figure 35. Example Layout (RGP Package)

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *TPS386000-Q1 Pin FMEA,* Application Report, SLVA627
- *Optimizing Resistor Dividers at a Comparator Input*, Application Report, SLVA450

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS386000QRGPRQ1	ACTIVE	QFN	RGP	20	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS 386000Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS386000-Q1 :

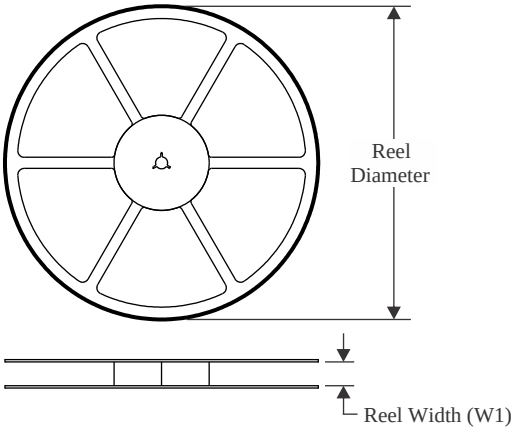
- Catalog: TPS386000

NOTE: Qualified Version Definitions:

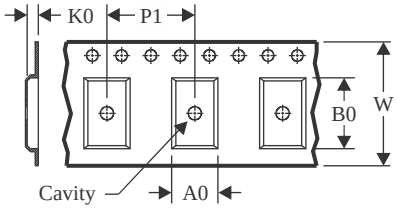
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

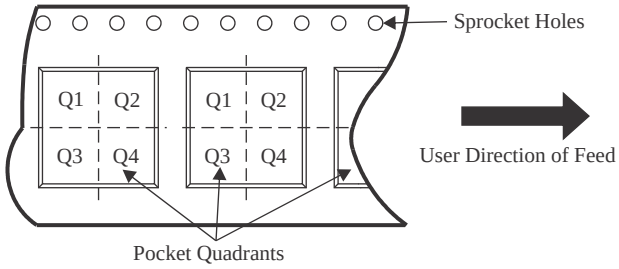


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

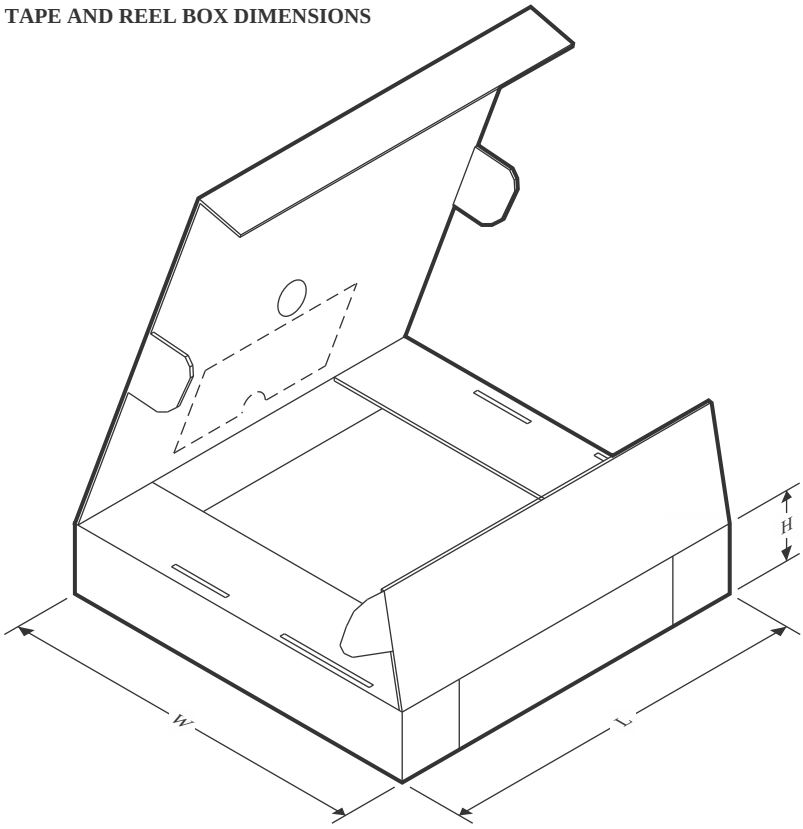
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS386000QRGPRQ1	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS386000QRGPRQ1	QFN	RGP	20	3000	367.0	367.0	35.0

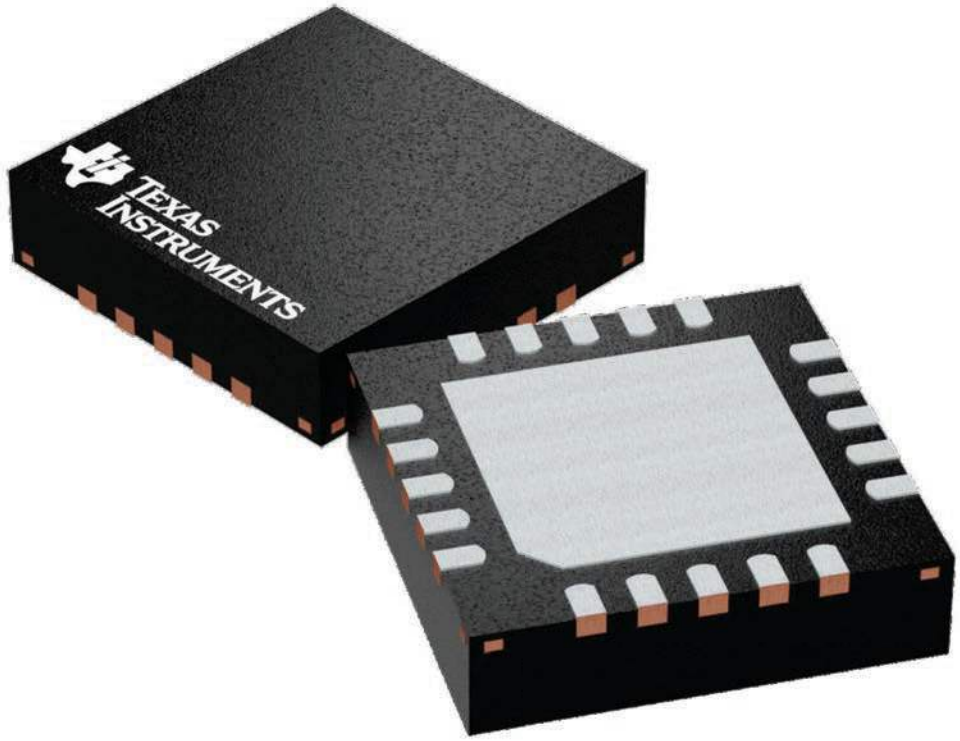
GENERIC PACKAGE VIEW

RGP 20

VQFN - 1 mm max height

4 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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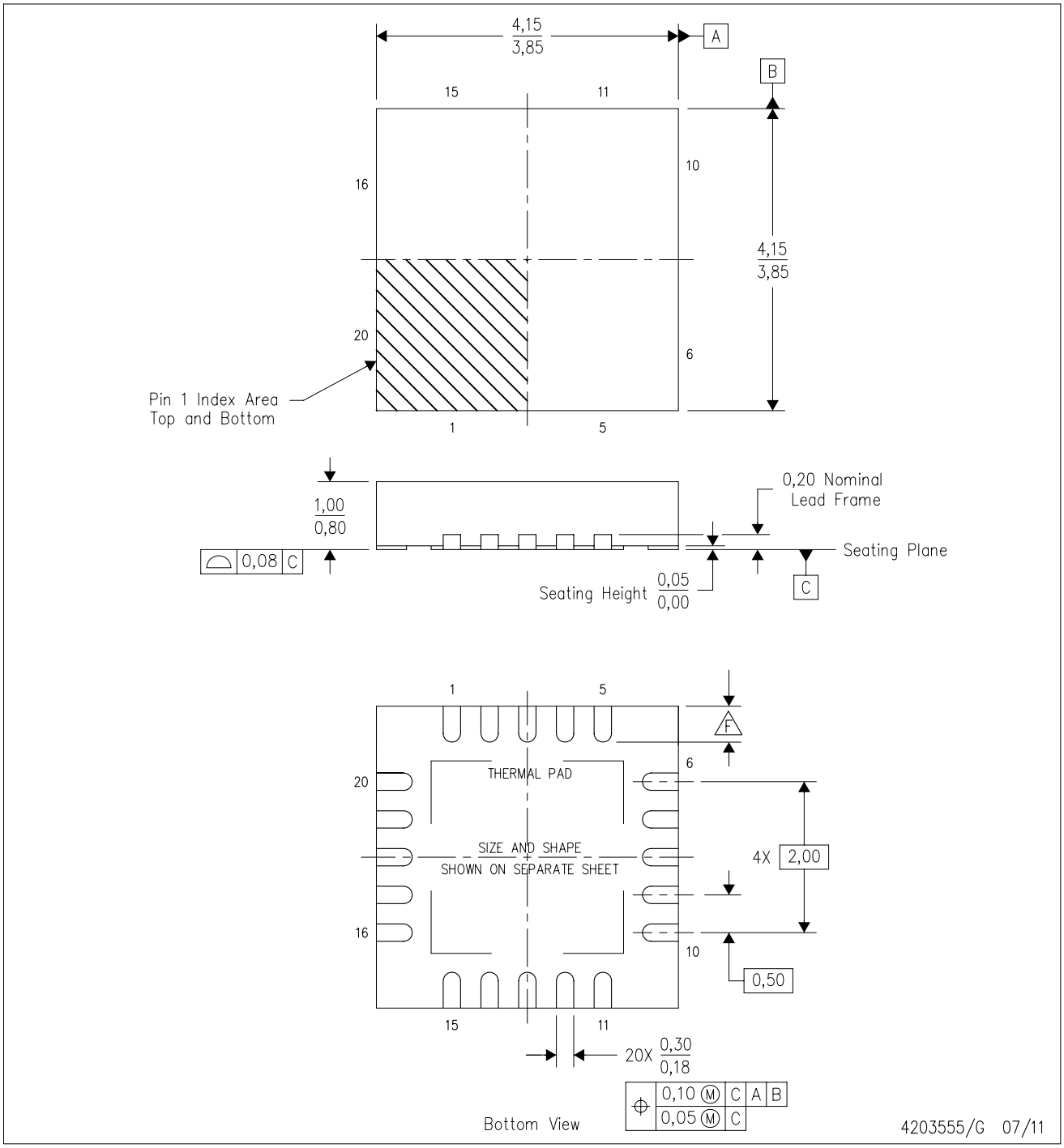
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

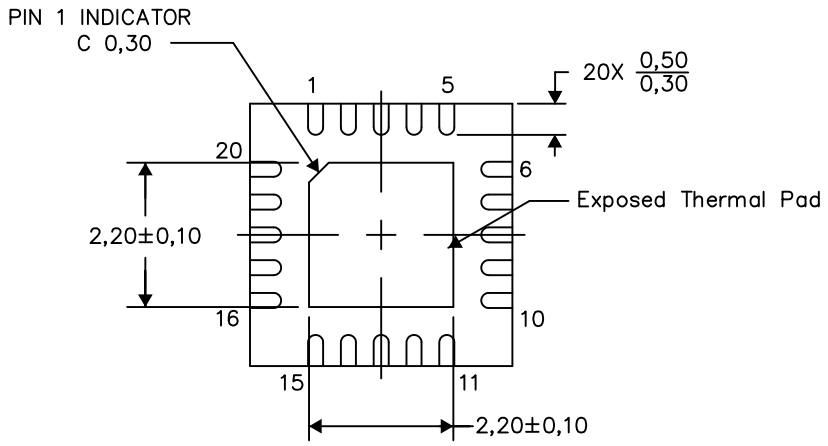
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



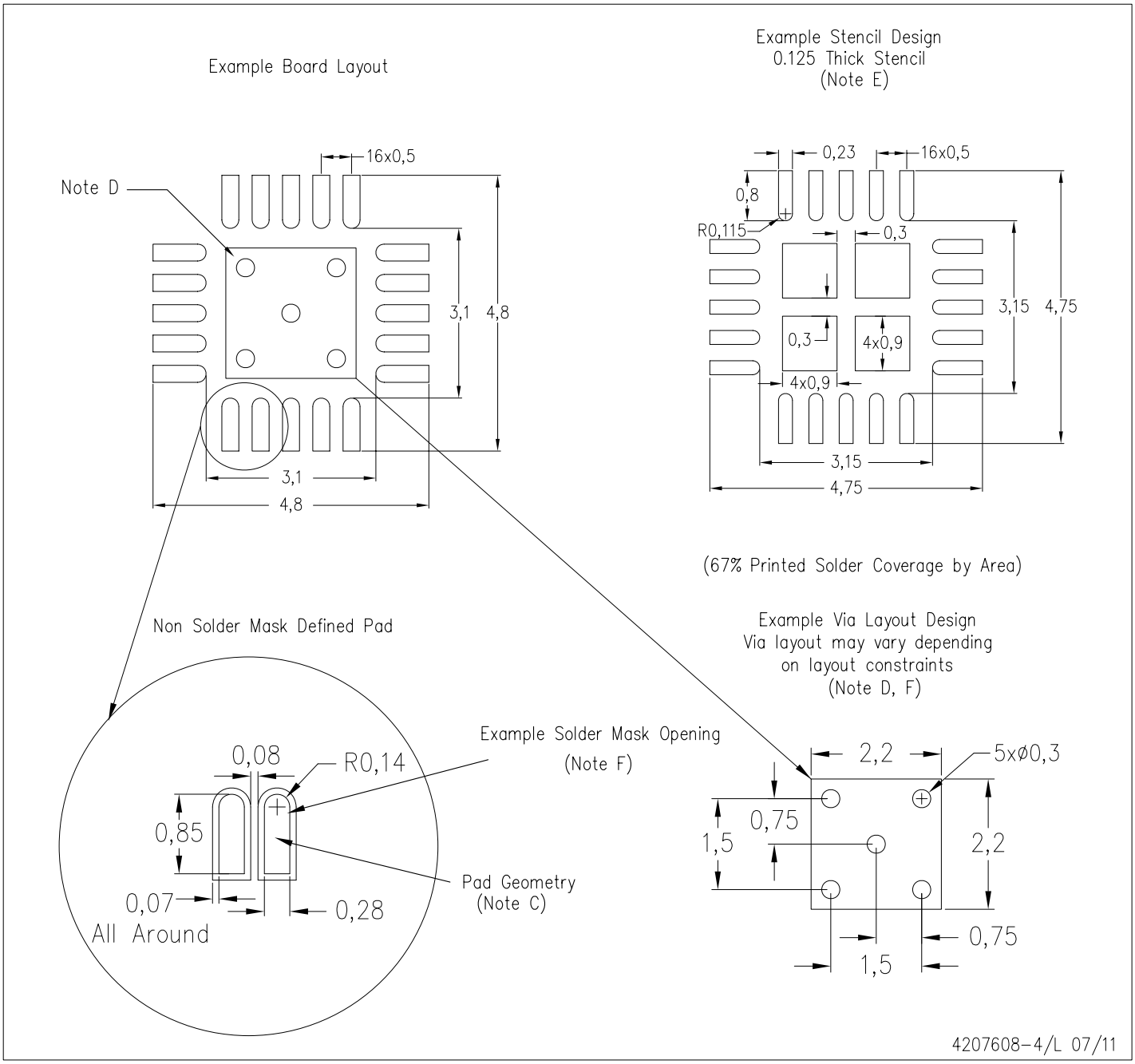
Bottom View

Exposed Thermal Pad Dimensions

4206346–4/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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