

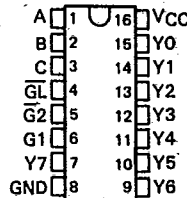
SN54HCT137, SN74HCT137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS
WITH ADDRESS LATCHES

D2804, MARCH 1984—REVISED JUNE 1989

- Inputs are TTL-Voltage Compatible
- Combines Decoder and 3-Bit Address Latch
- Incorporates 2 Output Enables to Simplify Cascading
- Package Options Include Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HCT137 ... J PACKAGE
 SN74HCT137 ... N PACKAGE

(TOP VIEW)



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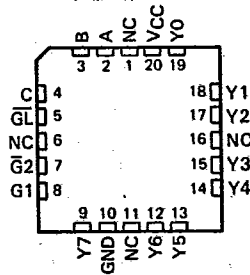
description

The 'HCT137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input (\overline{GL}) is low, the 'HCT137 acts as a decoder/demultiplexer. When \overline{GL} goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as \overline{GL} remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced high if G1 is low or $\overline{G2}$ is high. The 'HCT137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

The SN54HCT137 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT137 is characterized for operation from -40°C to 85°C .

SN54HCT137 ... FK PACKAGE

(TOP VIEW)



NC—No internal connection

HC MOS Devices

NOTICE

SEE ORDER OF DATA FOR ERRATA INFORMATION

FUNCTION TABLE

INPUTS			OUTPUTS										
\overline{GL}	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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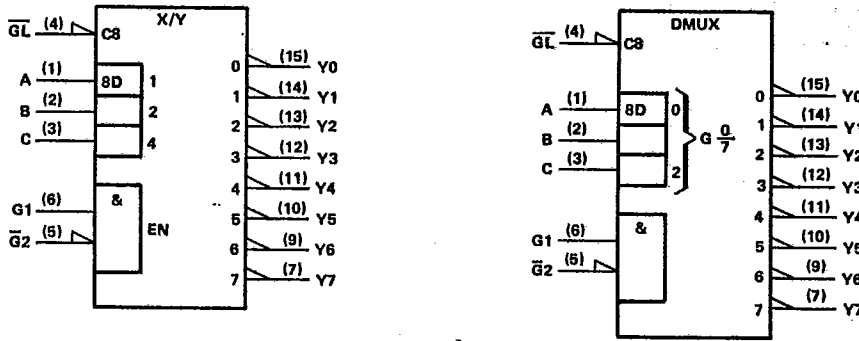
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SN54HCT137, SN74HCT137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS
WITH ADDRESS LATCHES

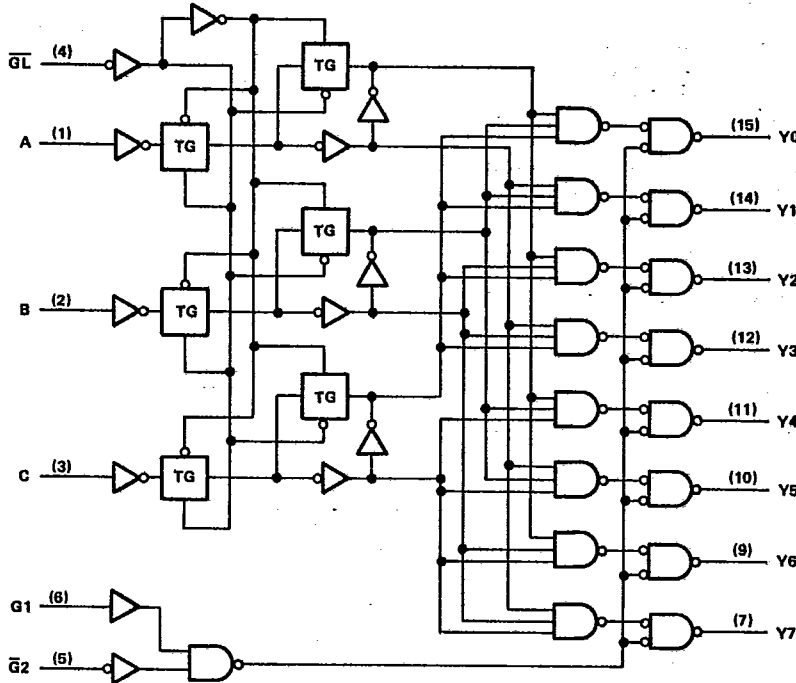
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logic symbols (alternatives)†



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

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 HCMOS Devices

SN54HCT137, SN74HCT137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS
WITH ADDRESS LATCHES

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absolute maximum ratings over operating free-air temperature range†

Supply voltage, VCC	-0.5 V to 7 V
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{CC})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	±20 mA
Continuous output current, I _O (V _O = 0 to V _{CC})	±25 mA
Continuous current through VCC or GND pins	±50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package	260°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HCT137			SN74HCT137			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 4.5 V to 5.5 V			2			V
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V to 5.5 V			0			V
V _I	Input voltage	0	V _{CC}		0	V _{CC}		V
V _O	Output voltage	0	V _{CC}		0	V _{CC}		V
t _t	Input transition (rise and fall) times	0	500		0	500		ns
T _A	Operating free-air temperature	-55	125		-40	85		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54HCT137		SN74HCT137		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	V _I = V _{IH} or V _{IL} , I _{OH} = -20 μA	4.5 V	4.4	4.499		4.4		4.4	V	
	V _I = V _{IH} or V _{IL} , I _{OH} = -4 mA	4.5 V	3.98	4.30		3.7		3.84		
V _{OL}	V _I = V _{IH} or V _{IL} , I _{OH} = 20 μA	4.5 V		0.001	0.1		0.1	0.1	V	
	V _I = V _{IH} or V _{IL} , I _{OL} = 4 mA	4.5 V		0.17	0.26		0.4	0.33		
I _I	V _I = V _{CC} or 0	5.5 V		±0.1	±100		±1000	±1000	nA	
I _{CC}	V _I = V _{CC} or 0, I _O = 0	5.5 V			8		160	80	μA	
ΔI _{CC} ‡	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V _{CC}	5.5 V		1.4	2.4		3.0	2.9	mA	
C _i		4.5 to							pF	
		5.5 V		3	10		10	10		

‡This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

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HCMOS Devices

SN54HCT137, SN74HCT137
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS
WITH ADDRESS LATCHES

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	V _{CC}	T _A = 25°C			SN54HCT137		SN74HCT137		UNIT
		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, $\overline{\text{GL}}$ low	4.5 V	26			39		33		ns
	5.5 V	23			35		30		
t _{su} Setup time, A, B, and C before $\overline{\text{GL}}$	4.5 V	15			23		19		ns
	5.5 V	14			21		17		
t _h Hold time, A, B, and C after $\overline{\text{GL}}$	4.5 V	5			5		5		ns
	5.5 V	5			5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT137		SN74HCT137		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, C	Y	4.5 V		25	38		57		48	ns
			5.5 V		20	34		51		43	
t _{pd}	$\overline{\text{G2}}$	Y	4.5 V		20	29		44		36	ns
			5.5 V		17	25		40		32	
t _{pd}	G1	Y	4.5 V		20	29		44		36	ns
			5.5 V		17	25		40		32	
t _{pd}	$\overline{\text{GL}}$	Y	4.5 V		32	42		63		52	ns
			5.5 V		25	36		57		47	
t _t		Any	4.5 V		12	15		22		19	ns
			5.5 V		11	14		20		17	

C _{pd}	Power dissipation capacitance	No load, T _A = 25°C	85 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.