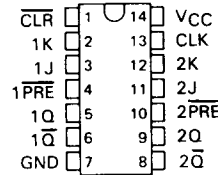


# TYPES SN54ALS114A, SN54AS114, SN74ALS114A, SN74AS114 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

D2661, APRIL 1982—REVISED DECEMBER 1983

- Fully Buffered to Offer Maximum Isolation from External Disturbance
- Package Options Include Both Plastic and Ceramic Carriers in Addition to Plastic and Ceramic DIPs.
- Dependable Texas Instruments Quality and Reliability

SN54ALS114A, SN54AS114 . . . J PACKAGE  
SN74ALS114A, SN74AS114 . . . N PACKAGE  
(TOP VIEW)



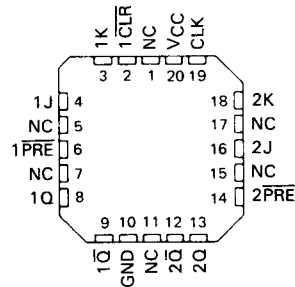
TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'ALS114A	40 MHz ( $C_L = 15$ pF)	6 mW
'AS114	175 MHz ( $C_L = 50$ pF)	95 mW

## description

These devices contain two independent J-K negative-edge-triggered flip-flops. A low level at the Preset or Clear inputs sets or resets the outputs regardless of the levels of the other inputs. When Preset and Clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as toggle flip-flops by tying J and K high.

The SN54ALS114A and SN54AS114 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74ALS114A and SN74AS114 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54ALS114A, SN54AS114 . . . FH PACKAGE  
SN74ALS114A, SN74AS114 . . . FN PACKAGE  
(TOP VIEW)



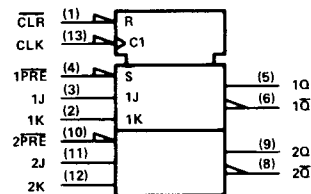
NC — No internal connection

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	$Q_0$	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	TOGGLE
H	H	H	X	X	$Q_0$	$\bar{Q}_0$

\*The output levels in this configuration are not guaranteed to meet the minimum levels for  $V_{OH}$  if the lows at Preset and Clear are near  $V_{IL}$  maximum. Furthermore, this configuration is nonstable; that is, it will not persist when either Preset or Clear returns to its inactive (high) level.

## logic symbol



Pin numbers shown are for J and N packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS114A, SN54AS114	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$
SN74ALS114A, SN74AS114	$0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
Storage temperature range	$-65^{\circ}\text{C}$ to $150^{\circ}\text{C}$

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# TYPES SN54ALS114A, SN74ALS114A

## DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS

### WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

#### recommended operating conditions

		SN54ALS114A			SN74ALS114A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage	2			2			V
V <sub>IL</sub>	Low-level input voltage				0.8			V
I <sub>OH</sub>	High-level output current				-0.4			mA
I <sub>OL</sub>	Low-level output current	4			8			mA
f <sub>clock</sub>	Clock frequency	0			25			MHz
t <sub>w</sub>	Pulse duration	PRE or CLR low		15		10		ns
		CLK high		20		16.5		
		CLK low		20		16.5		
t <sub>su</sub>	Setup time before CLK↓	Data		25		22		ns
		PRE or CLR inactive		22		20		
t <sub>h</sub>	Hold time, data after CLK↓	0			0			ns
T <sub>A</sub>	Operating free-air temperature	-55			125			°C

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54ALS114A		SN74ALS114A		UNIT
			MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA	-1.5		-1.5		V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -0.4 mA	V <sub>CC</sub> -2		V <sub>CC</sub> -2		V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 4 mA	0.25		0.4		V
		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 8 mA			0.35		
I <sub>I</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V			0.1		mA
	PRE or CLR				0.2		
I <sub>IH</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V			20		μA
	PRE or CLR				40		
I <sub>IL</sub>	J, K, or CLK	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V			-0.2		mA
	PRE or CLR				-0.4		
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V	-30	-112	-30	-112	mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, See Note 1	2.5	4.5	2.5	4.5	mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

NOTE 1: I<sub>CC</sub> is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

#### switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX				UNIT
			SN54ALS114A		SN74ALS114A		
			MIN	MAX	MIN	MAX	
f <sub>max</sub>			25		30	MHz	
t <sub>PLH</sub>	PRE or CLR	Q or Q̄	3	20	3	15	ns
t <sub>PHL</sub>			4	22	4	18	
t <sub>PLH</sub>	CLK	Q or Q̄	3	18	3	15	ns
t <sub>PHL</sub>			5	23	5	19	

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

# TYPES SN54AS114, SN74AS114 DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

## recommended operating conditions

		SN54AS114			SN74AS114			UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX		
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V	
V <sub>IH</sub>	High-level input voltage	2			2			V	
V <sub>IL</sub>	Low-level input voltage				0.8			V	
I <sub>OH</sub>	High-level output current				-2			mA	
I <sub>OL</sub>	Low-level output current				20			mA	
f <sub>clock</sub>	Clock frequency	0			0			MHz	
t <sub>w</sub>	Pulse duration	PRE or CLR low						ns	
		CLK high							
		CLK low							
t <sub>su</sub>	Setup time before CLK↓	Data						ns	
		PRE or CLR inactive							
t <sub>h</sub>	Hold time, data after CLK↓							ns	
T <sub>A</sub>	Operating free-air temperature	-55		125		0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS114		SN74AS114		UNIT
				MIN	TYP†	MAX	MIN	
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA		-1.2		-1.2		V
V <sub>OH</sub>		V <sub>CC</sub> = 4.5 V to 5.5 V, I <sub>OH</sub> = -2 mA		V <sub>CC</sub> -2		V <sub>CC</sub> -2		V
V <sub>OL</sub>		V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 20 mA		0.35		0.35		V
I <sub>I</sub>	J or K	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 7 V		0.1		0.1		mA
	PRE			0.5		0.5		
	CLR			1		1		
	CLK			1		1		
I <sub>IH</sub>	J or K	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		0.02		0.02		mA
	PRE			0.1		0.1		
	CLR			0.2		0.2		
	CLK			0.2		0.2		
I <sub>IL</sub>	J or K	V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.4 V		-1		-1		mA
	PRE			-5.5		-5.5		
	CLR			-11.5		-11.5		
	CLK			-10.5		-10.5		
I <sub>O</sub> ‡		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.25 V		-30		-112		mA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V, See Note 1		38		38		mA

†All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I<sub>OS</sub>.

NOTE 1: I<sub>CC</sub> is measured with J, K, CLK, and PRE grounded, then with J, K, CLK, and CLR grounded.

Additional information on these products can be obtained from the factory as it becomes available.

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ALS AND AS CIRCUITS

**TYPES SN54AS114, SN74AS114**  
**DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP FLOPS**  
**WITH PRESET, COMMON CLEAR, AND COMMON CLOCK**

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$ $T_A = \text{MIN to MAX}$						UNIT
			SN54AS114			SN74AS114			
			MIN	TYP <sup>†</sup>	MAX	MIN	TYP <sup>†</sup>	MAX	
$f_{\text{max}}$			175			175			MHz
$t_{\text{PLH}}$	PRE or CLR	Q or $\bar{Q}$	3			3			ns
$t_{\text{PHL}}$			4			4			
$t_{\text{PLH}}$	CLK	Q or $\bar{Q}$	3			3			ns
$t_{\text{PHL}}$			4			4			

<sup>†</sup>All typical values are at  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

NOTE 2: For load circuit and voltage waveforms, see page 1-12.

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**ALS AND AS CIRCUITS**

**PRODUCT PREVIEW**

2-102 This page contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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