

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Phase-out/Discontinued

**SWITCHING
P-CHANNEL POWER MOS FET**

DESCRIPTION

The 2SJ326 is P-channel MOS Field Effect Transistor designed for solenoid, motor and lamp driver.

FEATURES

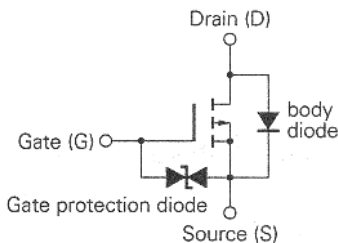
- Low On-state Resistance
 $R_{DS(on)} = 0.28 \Omega$ TYP. ($V_{GS} = -10 V, I_D = -1.0 A$)
 $R_{DS(on)} = 0.50 \Omega$ TYP. ($V_{GS} = -4 V, I_D = -0.8 A$)
- Low C_{iss} : $C_{iss} = 320 pF$ TYP.
- Built-in G-S Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$)

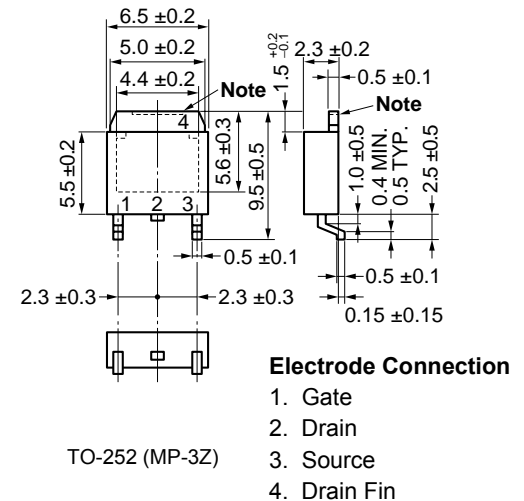
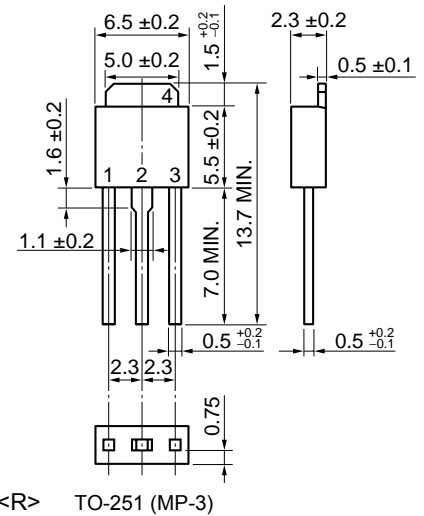
Drain to Source Voltage	V_{DSS}	-60	V
Gate to Source Voltage (AC)	$V_{GSS(AC)}$	± 20	V
Gate to Source Voltage (DC)	$V_{GSS(DC)}$	-20, +10	V
Drain Current (DC)	$I_{D(DC)}$	± 2.0	A
Drain Current (pulse) ^{Note}	$I_{D(pulse)}$	± 8.0	A
Total Power Dissipation ($T_C = 25^\circ C$)	P_{T1}	20	W
Total Power Dissipation ($T_A = 25^\circ C$)	P_{T2}	1.0	W
Channel Temperature	T_{ch}	150	$^\circ C$
Storage Temperature	T_{stg}	-55 to +150	$^\circ C$

Note $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$

EQUIVALENT CIRCUIT



PACKAGE DRAWINGS (Unit: mm)



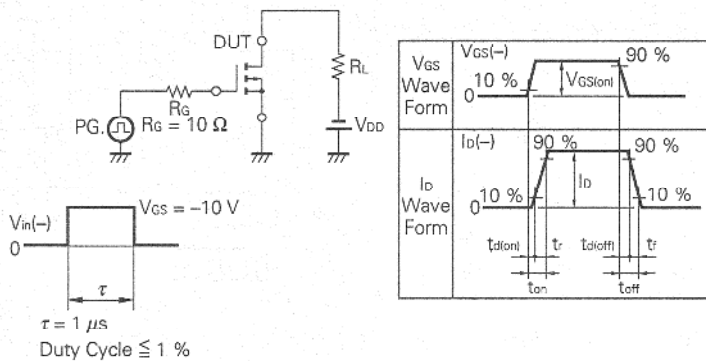
Note The depth of notch at the top of the fin is from 0 to 0.2 mm.

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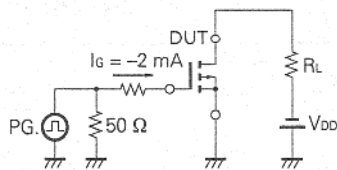
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		0.28	0.37	Ω	V _{GS} = -10 V, I _D = -1.0 A
Drain to Source On-state Resistance	R _{DS(on)}		0.50	0.68	Ω	V _{GS} = -4 V, I _D = -0.8 A
Gate to Source Cutoff Voltage	V _{GS(off)}	-1.0	-1.5	-2.0	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	y _{fs}	1.0	1.8		S	V _{DS} = -10 V, I _D = -1.0 A
Drain Leakage Current	I _{DSS}			-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Input Capacitance	C _{iss}		320		pF	V _{DS} = -10 V
Output Capacitance	C _{oss}		220		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		75		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		5		ns	V _{GS(on)} = -10 V V _{DD} = -30 V I _D = -1.0 A, R _G = 10 Ω R _L = 30 Ω
Rise Time	t _r		15		ns	
Turn-Off Delay Time	t _{d(off)}		40		ns	
Fall Time	t _f		25		ns	
Total Gate Charge	Q _G		12		nC	V _{GS} = -10 V I _D = -2.0 A V _{DD} = -48 V
Gate to Source Charge	Q _{GS}		1		nC	
Gate to Drain Charge	Q _{GD}		5		nC	
Body Diode Forward Voltage	V _F		0.9		V	I _F = 2.0 A, V _{GS} = 0
ESD	V _{ESD}		±130		V	C = 200 pF, R = 0, Single Pulse
Reverse Recovery Time	t _{rr}		72		ns	I _F = 2.0 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		30		nC	di/dt = 50 A/μs

Test Circuit 1: Switching Time

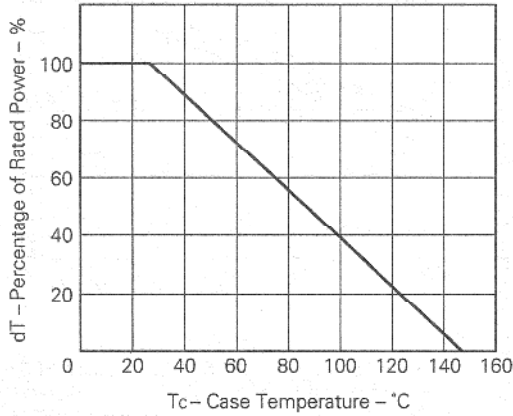


Test Circuit 2: Gate Charge

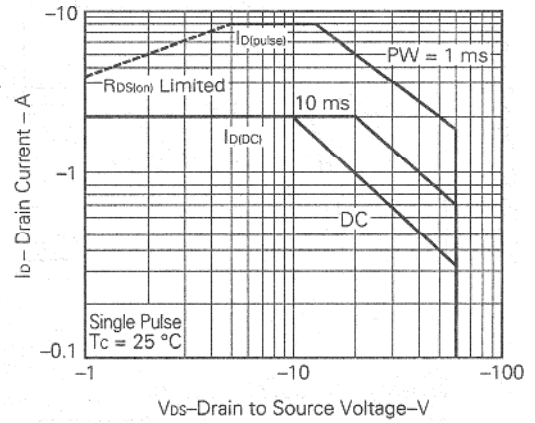


ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

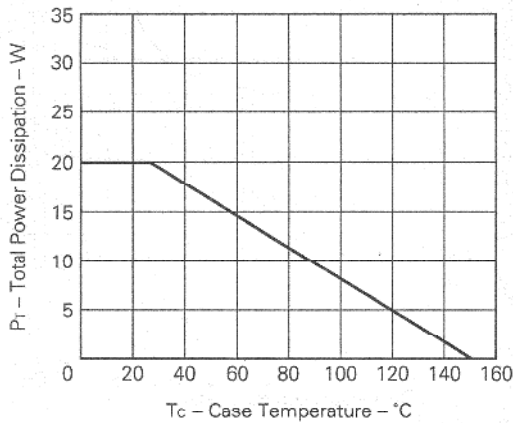
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



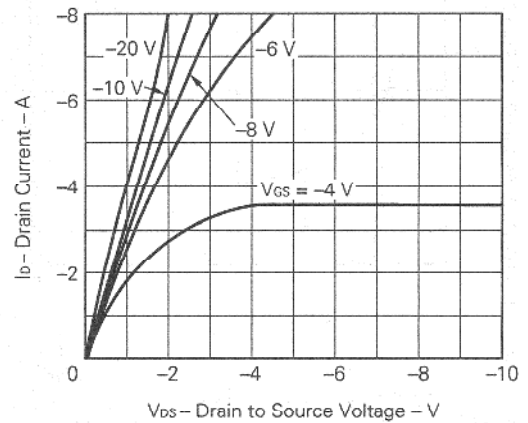
FORWARD BIAS SAFE OPERATING AREA



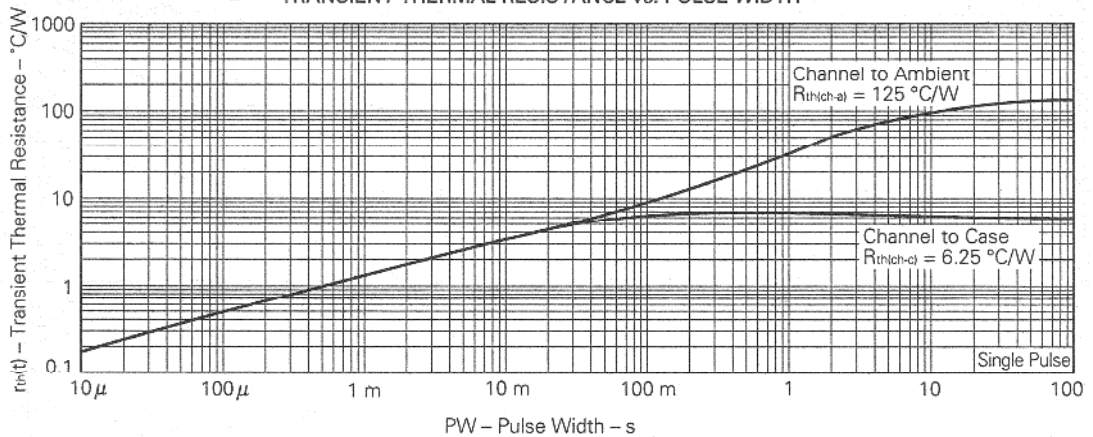
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

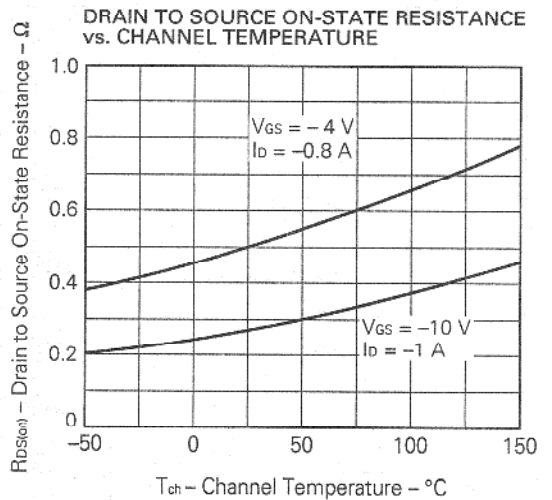
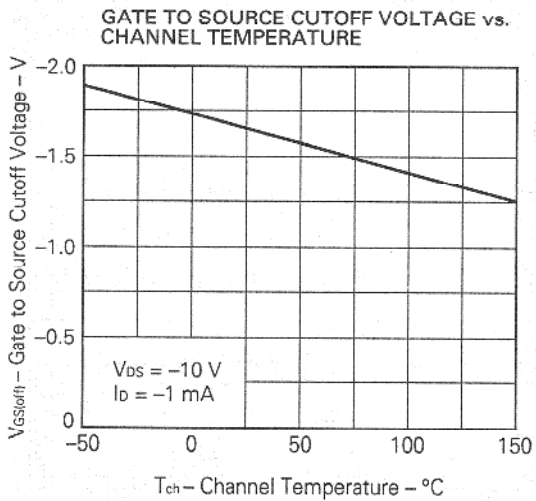
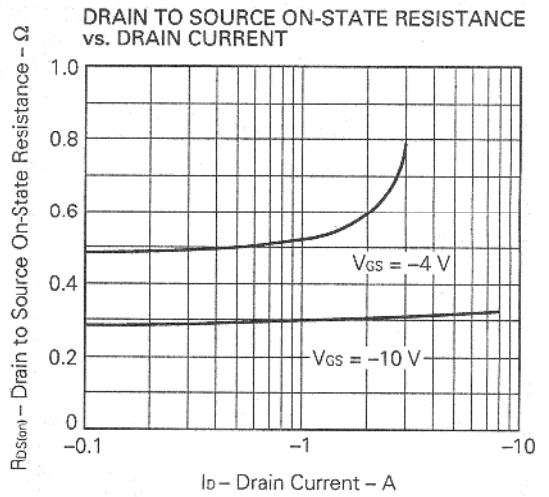
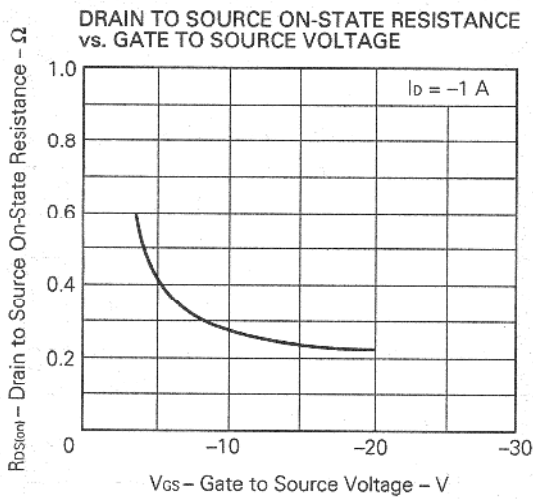
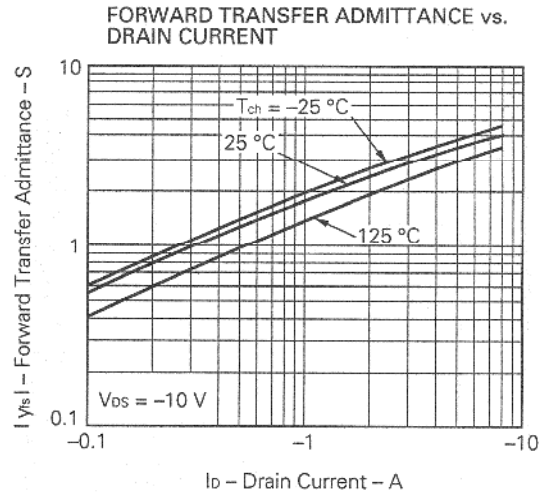
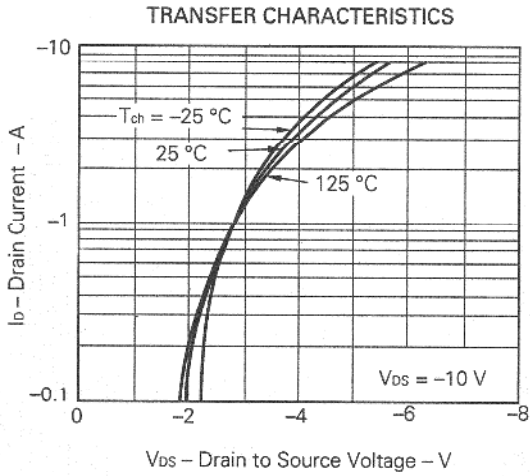


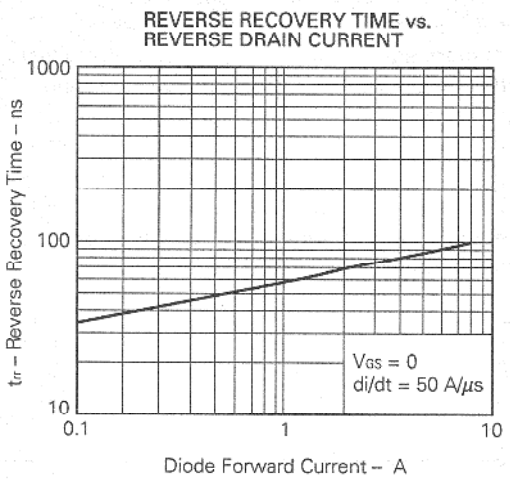
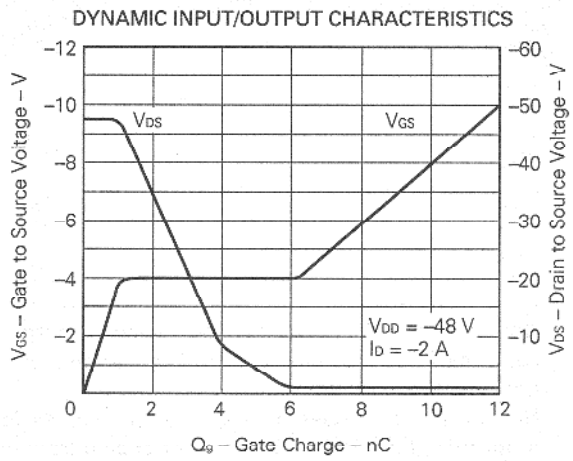
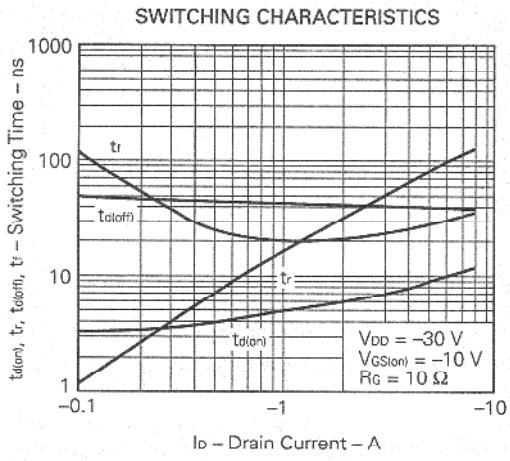
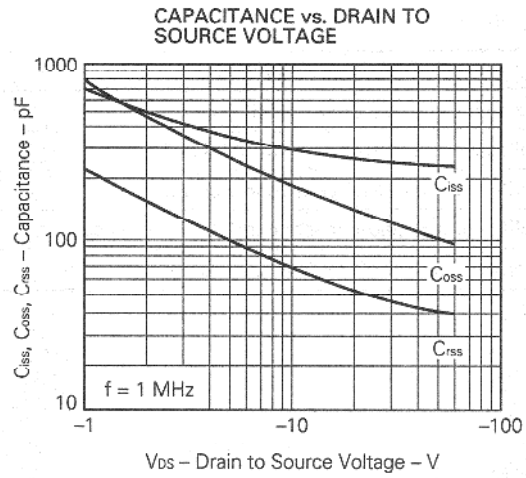
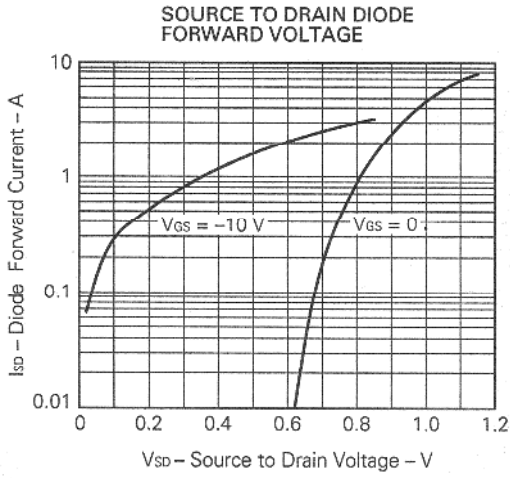
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH







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