UCC39002 Advanced Load-Share Controller User's Guide, HPA027A

User's Guide

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UCC39002 Advanced Load-Share Controller User's Guide, HPA027A

Lisa Dinwoodie *System Power*

ABSTRACT

The UCC39002 is an advanced, high-performance load-share controller that provides all the necessary functions to parallel multiple independent power supplies or dc-to-dc modules. This load-share circuit is based upon the automatic master/slave architecture utilized in the UC3902 and the UC3907 load-share controllers providing better than 1% current-share error between the modules at full load.

Contents

1 Introduction

The UCC39002 load-share controller allows accurate current sharing between paralleled power modules. The evaluation module provides an optimum layout to parallel up to three modules on a board in which most of the reference designators are unpopulated. This user's guide will facilitate component selection for the modules to be current shared. Component values are dependent upon the specific power modules and must be calculated for each load-share system.

2 Caution

Dependent upon the power modules being paralleled, there may be high voltages present on this EVM. Some components under maximum power may be hot. Precautions should be taken. The maximum load current for this evaluation board is recommended to be 10 A from each module being paralleled. Due to the absolute maximum voltage ratings of the current sense amplifier inputs and the adjust pin input, this evaluation module is limited to use with converters whose output voltages do not exceed 15 V.

3 Applications

This user's guide will enable the user to select components to successfully parallel power modules that have the following features:

- Remote sense
- Output voltages greater than 1 V, but less than 15 V
- An output stage that sources output current only, allowing for paralleling of converters and ensuring one converter does not sink current from another converter.
- Available minimum 5-V bus for controller bias voltage, or use of the output voltage of the modules for bias when the output of the modules is between 5 V and 15 V.

4 Features

- High accuracy, better than 1% current-share error at full load
- High-side current sensing
- Ultra-low offset current sense amplifier
- Single wire load-share bus
- Intel® SSI load-share specification compliant
- Disconnect from load-share bus at stand-by
- Load-share bus protection against shorts to GND or to the supply rail
- 8-pin MSOP package option minimizes board space
- External or internal bias selection
- External shutdown switch for each module

5 Schematic

A schematic of a typical load-share design, where the outputs of three modules are being shared, is shown in Figure 1. Note that one load-share controller is required for each module and the circuits are identical when three identical modules are used. Terminals J1 and J2 are connected to the $+V_{OUT}$ and $-V_{OUT}$, respectively, of the first power module. Terminals J3, J4, J5, and J6 correspond to the other two modules positive and negative output pins. Terminal J7 connects the positive output bus to the load and J8 connects the negative output to the load.

The UCC39002 load share controllers require a minimum bias voltage of 4.575 V to ensure enabling the load share bus. Note the maximum bias voltage for this design is 15 V. This enables the under voltage lockout/bias ok internal circuitry of the UCC39002 without exceeding the absolute maximum voltage rating of the current sense amplifier inputs and the adust pin. Modules that have an output voltage of less than 5 V will require external biasing for the load share controllers: jumpers JP1 through JP3 should be shorted to the EXT. position and an external 5-V supply can be used as bias at the terminal block labeled EXTERNAL BIAS. Otherwise, the controllers should be biased from the modules' output bus voltage by shorting these jumpers to the INT. position. Note that the voltage on the current sense input pins and the adjust pin must be equal to or less than the bias voltage on VDD.

Terminal blocks TB1 through TB3 connect to the sense lines from each module. For remote sensing, JP4 and JP5 are left open and remote sense leads from the load are connected to the terminal block labeled REMOTE SENSE. For local voltage sensing, simply jumper JP4 and JP5. This connects the sense lines from the modules to the load terminals on the evaluation board through dedicated, low noise, low current traces.

The available evaluation boards come pre−populated with the load share controllers, VDD decoupling capacitors, and components for external controller shut down. This circuitry is shown in Figure 1 as U1, C5, Q1, R1, and R4 for the first module, U2, C7, Q2, R2, R5 for the second, and U3, C9, Q3, R3, and R6 for the third. By applying a 2-V signal onto the SD terminal of any of the three modules, the 2N7002 transistor is turned on, shorting CS+ to ground, resulting in that module's disconnect feature to be enabled. With the disconnect feature enabled, the UCC39002 disconnects itself from the load share bus and its adjust current is zero.

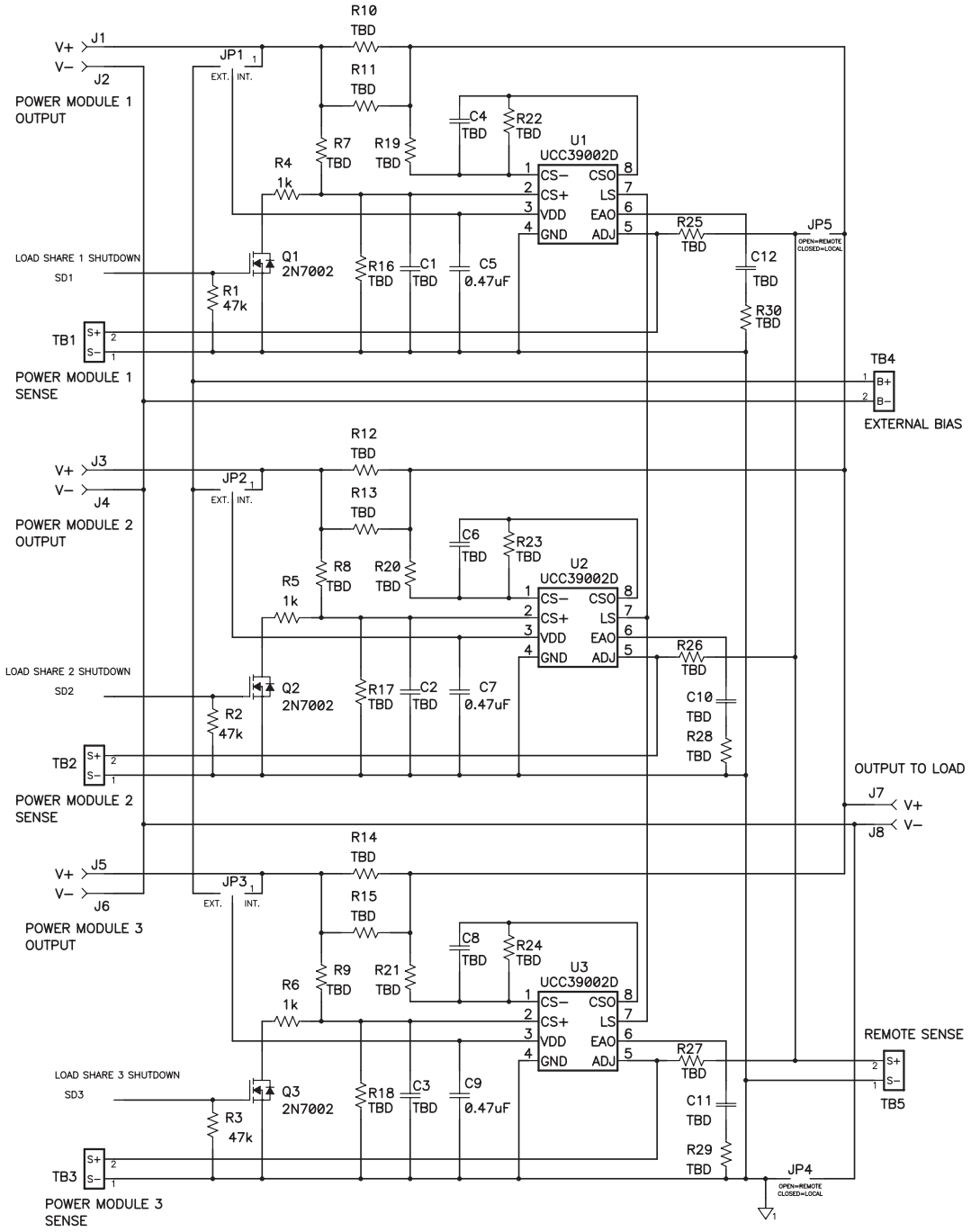

Figure 1. UCC39002 Load-Share Schematic

6 Design Procedure

The following is a step-by-step design procedure on how to determine the appropriate components to parallel power modules for load sharing. The user's guide is stated for the first module and the circuit is repeated for each of the remaining two modules.

In order to accurately current share between power modules, specific parameters must be known:

- V_{OUT} = nominal output voltage of the modules to be paralleled
- $I_{OUT(max)}$ = maximum output current of each module to be paralleled
- $\Delta V_{ADJ(max)}$ = maximum voltage adjustment range of the power module to be paralleled
- N = number of modules to be paralleled
- VDD = bias voltage for the UCC39002 controllers
- The transfer function of the power modules between their positive voltage sense and power output terminals.

6.1 Measuring the Module's Unity Gain Crossover Frequency

Power modules usually have a very low bandwidth to ensure proper operation with a variety of loads. The transfer function is determined using a network analyzer and injecting a small signal across a 20-Ω to 50-Ω resistor placed between the positive sense terminal and the positive voltage output terminal as shown in Figure 2. The resultant bode plot will show the dc gain and the unity gain crossover frequency of the module. Expect the module's crossover frequency to be within the range from 10 Hz to 30 kHz. The desired crossover frequency for the load-share loop is set well before the crossover frequency of the modules. This is accomplished by adding a zero to the compensation of the transconductance error amplifier as described in the error amplifier section. The unity gain crossover frequency is unique to the specific module and must be measured for each module type.

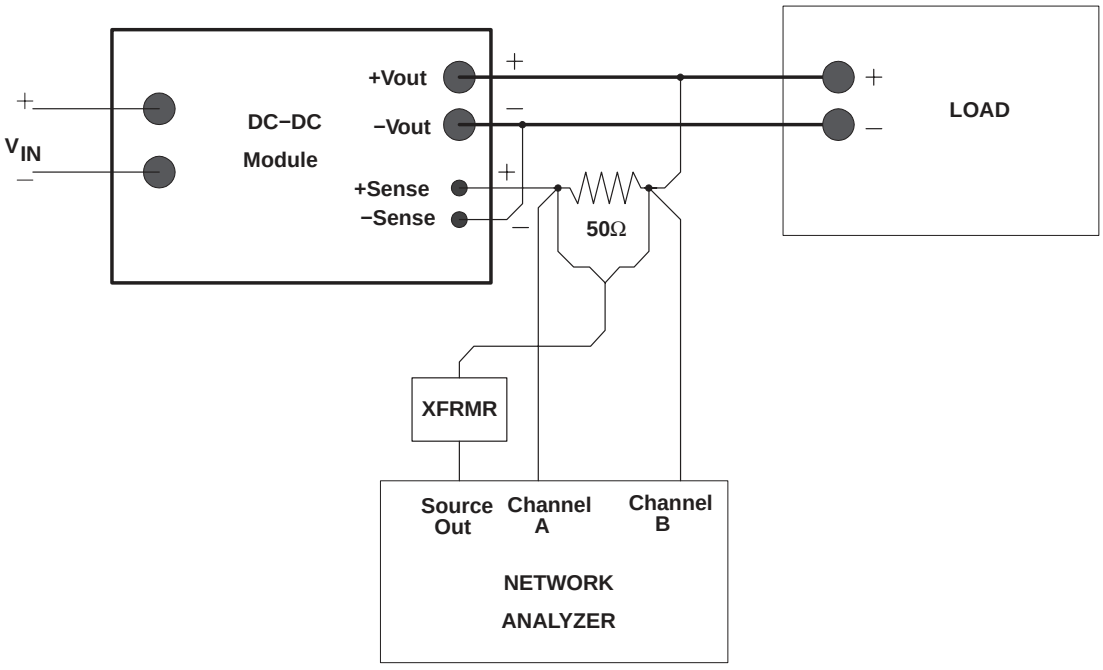

Figure 2. Measuring the Unity Gain Crossover Frequency

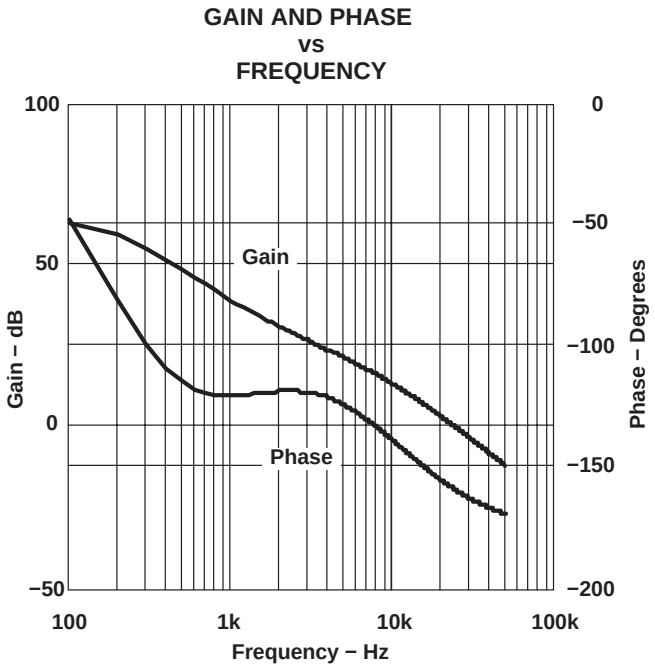

Figure 3

Figure 3 shows an example of the gain and phase frequency response measurement of a power module.

6.2 Choosing the Sense Resistor

The primary concern in the selection of the sense resistor, R_{SENSE}, is to ensure that the sum of the voltage drops across the resistor and the parasitic wire impedances, at maximum module output current, is significantly less than the output voltage adjustment range of the modules, otherwise there would be no room for output voltage adjustment.

$$I_{OUT(max)} \times R_{SENSE} << \Delta V_{ADJ(max)} \quad (1)$$

Other limitations for the sense resistor are the desired minimum power dissipation and available component ratings. The board provided has space for two 1-W 2512 resistors in parallel to be used for current sensing, as shown by R10 and R11 in Figure 1.

6.3 Setting the Gain of the Current Sense Amplifier

The gain of the current-sense amplifier (CSA) is configured by adding compensation components between the inverting input to the amplifier, CS−, and the current sense amplifier output, CSO, of the load-share device. The maximum voltage at the CSO pin, $V_{CSO(max)}$, is limited by the saturation voltage of the internal current sense amplifier and must be at least two volts less than VDD.

$$V_{CSO(max)} < VDD - 2\ V \quad (2)$$

Referring to Figure 1, the CSA gain, A_{CSA}, is equal to:

$$A_{CSA} = \left(\frac{R22}{R19}\right) = \frac{V_{CSO}}{\left(R_{SENSE} \times I_{OUT(max)}\right)} \quad (3)$$

A *high-frequency pole*, f_{POLE} configured with C4, should be added for noise filtering.

$$C4 = \frac{1}{2 \times \pi \times R_{22} \times f_{POLE}} \tag{4}$$

The total impedance at CS− must be mirrored at the non-inverting input, CS+, of the differential amplifier, as shown by R7, R16, and C1 in Figure 1.

The CSA output voltage, V_{CSO}, serves as the input to the internal unity gain LS bus driver. The module with the highest output voltage will forward bias the internal diode located at the output of the LS bus driver and determine the voltage on the load-share bus on the LS pin, V_{LS}, making this module the master. This load-share bus acts as a communication port between the paralleled modules. The LS pin is bi-directional. By forward biasing the internal diode, the master sets the LS bus voltage based upon the voltage across its current sense resistor. Because the internal diode is reverse biased on the other modules, referred to as the slaves, the LS voltage is used as the non-inverting input to the internal LS bus receiver. The master transmits the voltage signal to the slave modules so they can compare their voltages across their own current sense resistors with that of the master module. The slave modules represent a load on the bias current, I_{VDD}, of the master module due to the internal 100-kΩ resistor at the LS pin. This increase in supply current for the master module is equal to:

$$\Delta I_{VDD} = N\left(\frac{V_{LS}}{100\ k\Omega}\right) \tag{5}$$

where N is equal to the number of paralleled modules.

6.4 Determining R_{ADJUST}

The Sense+ terminal of the module is connected to the ADJ pin of the load-share controller. By placing a resistor, R25 in Figure 1, between this ADJ pin and the load, an artificial Sense+ voltage is created from the voltage drop across R_{ADJUST} due to the current sunk by the internal NPN transistor. The voltage at the ADJ pin must be maintained at approximately 1 V above the voltage at the EAO pin. This is necessary in order to keep the transistor at the output of the internal adjust amplifier from saturating. To fulfill this requirement, R_{ADJUST} can be calculated using the following equation:

$$R_{ADJUST} \geq \frac{\left[\Delta V_{ADJ(max)} - \left(I_{OUT(max)} \times R_{SENSE}\right)\right] \times 500\ \Omega}{\left[V_{OUT} - \left(\Delta V_{ADJ(max)} - \left(I_{OUT(max)} \times R_{SENSE}\right)\right) - 1\ V\right]} \tag{6}$$

Also needed for consideration is the actual adjust pin current. The maximum sink current for the ADJ pin, $I_{ADJ(max)}$, is 6 mA as determined by the internal 500-Ω emitter resistor and 3-V clamp. The value of adjust resistor, R_{ADJUST}, is based upon the maximum adjustment range of the module, $\Delta V_{ADJ(max)}$. This adjust resistor is determined using the following formula:

$$R_{ADJUST} \geq \frac{\left[\Delta V_{ADJ(max)} - \left(I_{OUT(max)} \times R_{SENSE}\right)\right]}{I_{ADJ(max)}} \tag{7}$$

By selecting a resistor that meets both of these minimum requirements, the ADJ pin will be at least 1 V greater than the EAO voltage and the adjust pin sink current will not exceed its 6 mA maximum.

6.5 Error Amplifier Compensation

The total load-share loop must be configured for a unity gain crossover frequency well before the crossover frequency of the module, $f_{COmodule}$, as measured in Figure 2 and shown in Figure 3. This is accomplished by placing a zero in the error amplifier compensation at least one decade before the module's crossover frequency. Compensation of the transconductance error amplifier is done by placing the compensation resistor, R_{EAO} shown as R30 in Figure 1, and capacitor, C_{EAO} shown as C12 in Figure 1, between EAO and GND. The values of these components are determined by the following loop gain equation:

$$C_{EAO} = \left(\frac{G_M}{2 \times \pi \times f_{ZERO}}\right) \times A_{CSA} \times A_V \times A_{ADJ} \times A_{PWR(fco)} \quad (8)$$

Where:

1. Gm is the transconductance of the error amplifier, typically 14 mS,
2. f_{zero} is equal to the desired frequency in Hz of the zero to be added to the load-share loop, maximum zero frequency will be equal to $\frac{f_{CO(module)}}{10}$,
3. A_{CSA} equals R22/R19,
4. A_V is the voltage gain, equal to $\frac{R_{SENSE}}{R_{LOAD}}$,
5. A_{ADJ} is the gain associated with the adjust amplifier, equal to $\frac{R_{ADJUST}}{500\ \Omega}$,
6. $A_{PWR(fCO)}$ is the measured gain of the power module at the desired inserted zero frequency, read from Figure 3 and converted from dB to V/V.

The calculated capacitor value will most likely be very large due to the low frequency of the zero. The actual available capacitor used will undoubtedly be of a lower value and this must be taken into consideration when determining the compensation resistor. Once the C_{EAO} capacitor is determined, R_{EAO} is selected to achieve the desired loop response:

$$R_{EAO} = \frac{1}{\left(2 \times \pi \times C_{EAO(actual\ value\ used)} \times f_{ZERO}\right)} \quad (9)$$

7 List of Materials

REFERENCE	QTY	DESCRIPTION	MANUFACTURER	PART NUMBER
C1, C2, C3, C4, C6, C8	6	Capacitor, ceramic, X5R or better, CSA compensation, 0805	TBD	TBD
C10, C11, C12	3	Capacitor, ceramic, X5R or better, EA compensation, 1210	TBD	TBD
C5, C7, C9	3	Capacitor, ceramic, 0.47 μF, 25 V, X7R, ±10%, 0805	TDK Corporation	C2012X7R1E474K
Q1, Q2, Q3	3	MOSFET, N-channel, 60 V, 115 mA, 1.2 Ω, SOT23	Vishay−Liteon	2N7002DICT
R1, R2, R3	3	Resistor, chip, 47 kΩ, 1/10 W, ±5%, 0805	Panasonic − ECG	ERJ−6GEYJ473V
R4, R5, R6,	3	Resistor, chip, 1 kΩ, 1/10 W, ±5%, 0805	Panasonic − ECG	ERJ−6GEYJ102V
R7, R8, R9, R19, R20, R21	6	Resistor, chip, 1/10 W or better, ±5% or better, CSA compensation, 0805	TBD	TBD
R10, R11, R12, R13, R14, R15	6	Resistor, chip, 1 W, ±5% or better, current sense, 2512	TBD	TBD
R16, R17, R18, R22, R23, R24	6	Resistor, chip, 1/10 W or better, ±5% or better, CSA compensation, 0805	TBD	TBD
R25, R26, R27	3	Resistor, chip, 1/10 W or better, ±5% or better, voltage adjustment, 0805	TBD	TBD
R28, R29, R30	3	Resistor, chip, 1/10 W or better, ±5% or better, EA compensation, 0805	TBD	TBD
TB1, TB2, TB3, TB4, TB5	5	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 x 0.35	OST	ED1609
U1, U2, U3 **	3	IC, Advanced Load Share Controller, SO8	Texas Instruments	UCC39002D
JP1, JP2, JP3	3	Header, 3 pin, 100-mil spacing, 36-pin strip, 0.100 x 3”	Sullins	PTC36SAAN
JP4, JP5	2	Header, 2 pin, 100-mil spacing, 36-pin strip, 0.100 x 2”	Sullins	PTC36SAAN
J1, J2, J3, J4, J5, J6, J7, J8	8	Lug, solderless, #10−12 AWG, copper/tin, uninsulated, 0.375 x1.00	AMP	33457
N/A	5	Shunt for JP1, JP2, JP3, JP4, JP5, 0.100”	Sullins	STC02SYAN
N/A	8	Input and output lugs for V+ and V− pads, 0.765”	Solis	8−33457−1
N/A	8	Screw, roundhead, phillips, #8−32 1/4”, 0.35”	Std	Std
N/A	8	Star washer, #8, 0.36”	Std	Std
N/A	8	Nut, medium #8, 0.245”	Std	Std

NOTES:
1. These assemblies are ESD sensitive, ESD precautions shall be observed.
2. These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
3. These assemblies must comply with workmanship standards IPC−A−610 Class 2.
4. Ref designators marked with an asterisk (’**’) cannot be substituted. All other components can be substituted with equivalent MFG’s components.
5. Install lugs with appropriate hardware per Figure 4,below. Ensure the lug is seated on the square pad for good contact.

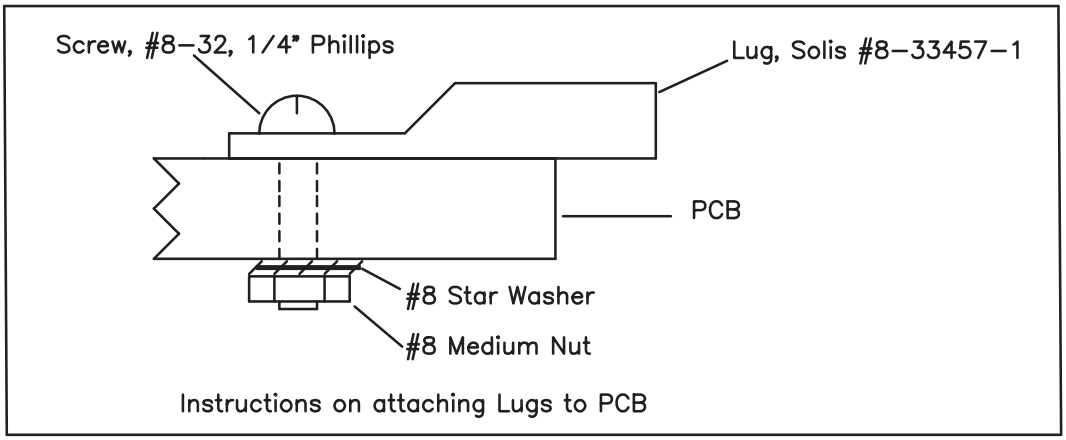

Figure 4. Lug Assembly Detail

8 Board Layout

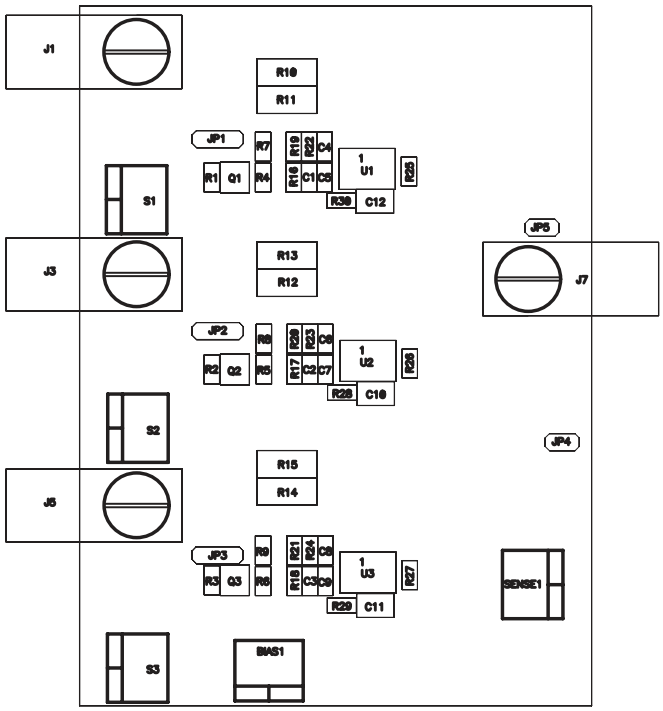

Figure 5. Top View

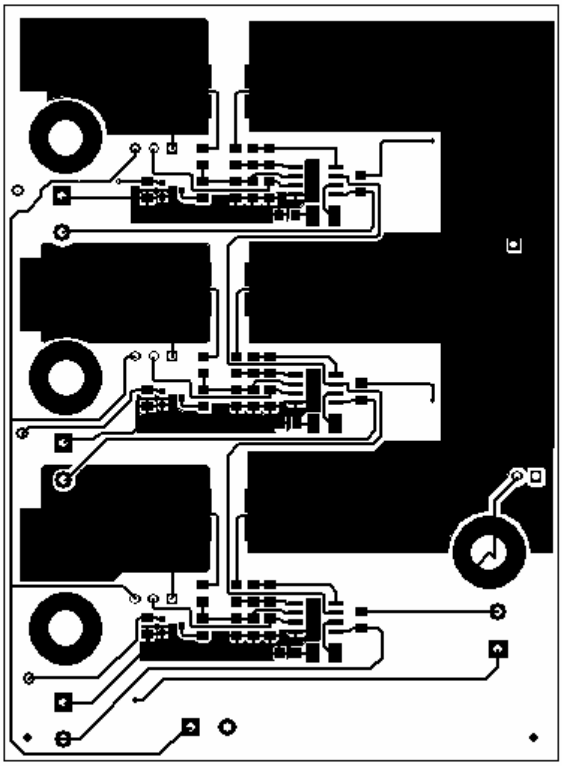

Figure 6. Top Layer Route

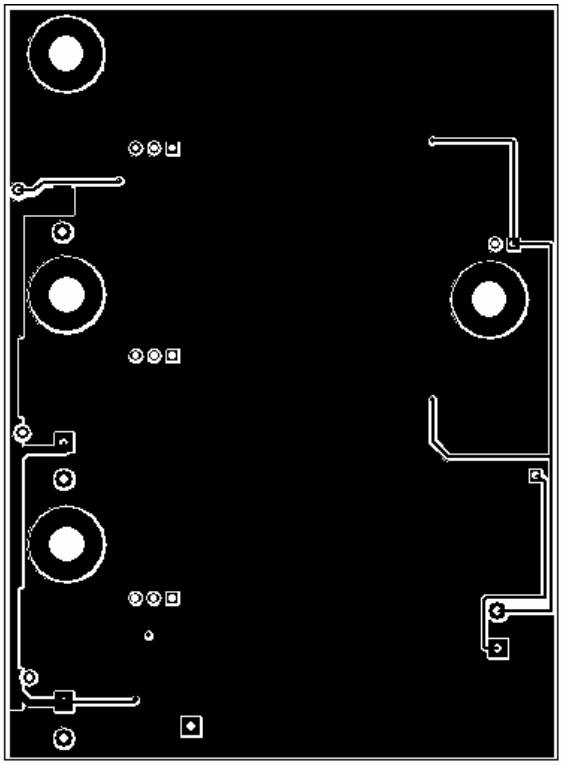

Figure 7. Bottom Layer Route

9 Connection Diagram

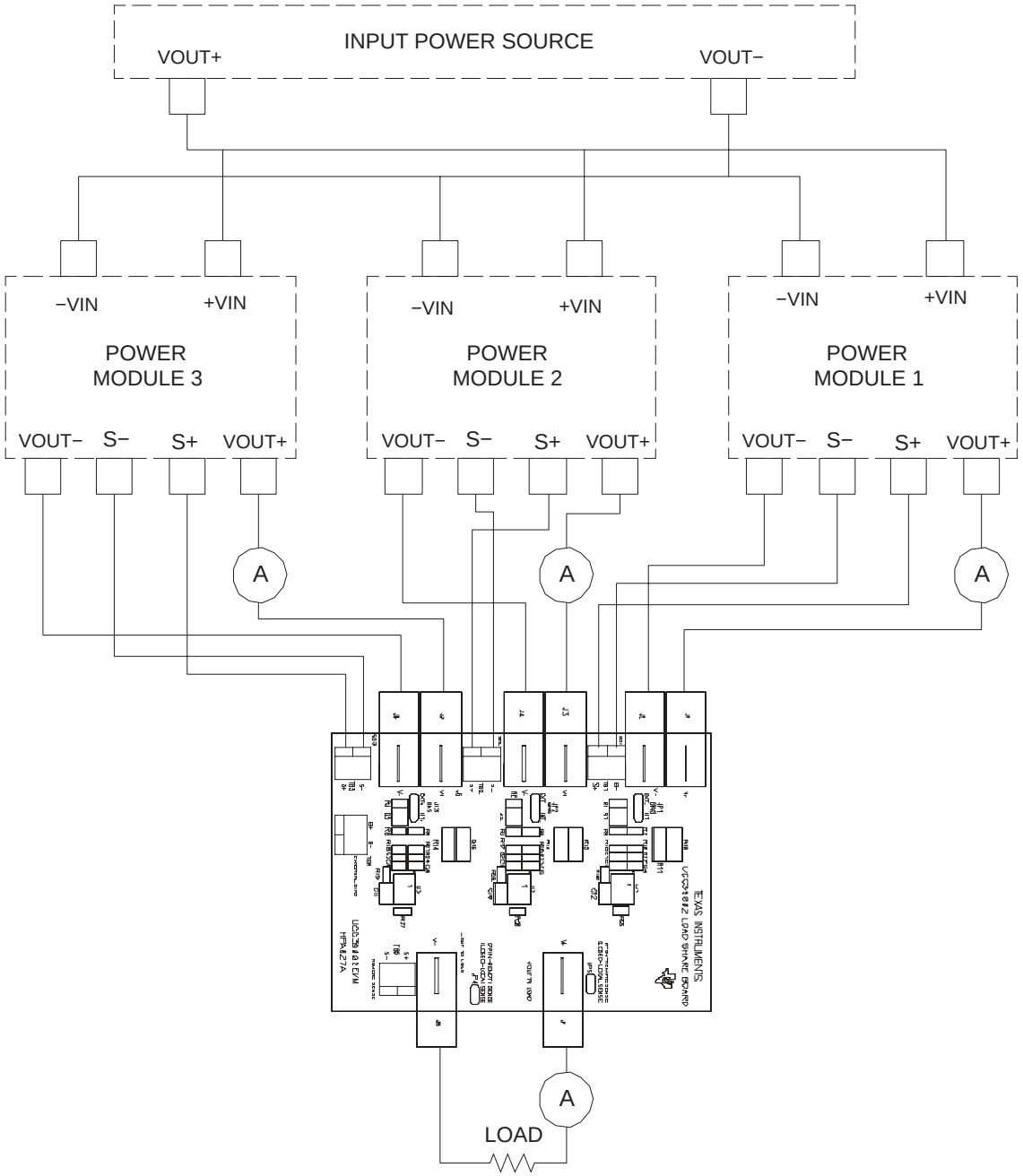

Figure 8. Connection Diagram for Load Share EVM when Paralleling Three Modules

Table 1. Connection Chart for Various Operating Conditions

OPERATING CONDITIONS	JUMPER POSITION		COMMENTS
Power module output voltage greater than 1V but less than 5V	JP1	EXT.	External minimum bias voltage of 4.575V for the Loads Share Controller required at the EXTERNAL BIAS terminal block
	JP2		
	JP3		
Power module output voltage between 5V and 15V	JP1	INT.	Load Share Controller bias from the output bus voltage of each of the modules
	JP2		
	JP3		
Remote sensing	JP4	OPEN	Connect leads from the REMOTE SENSE terminal block directly to the load for voltage sensing at the point of load
	JP5		
Local sensing	JP4	SHORTED	Voltage sensing at the J7/J8 connectors for local sensing on the EVM board
	JP5		

10 Conclusion

This user's guide will help the user determine the appropriate components to populate the available evaluation board in order to current share power modules using the UCC39002 advanced load-share controller. load-share accuracies of better than 1% at full load will be realized. At light load, internal offset voltages and small signal measurement error have a more pronounced effect, which will contribute to a larger current distribution error.

11 References

Balogh, Laszlo, *The UC3902 load-Share Controller and It's Performance in Distributed Power*, TI Literature No. SLUA128A

Dinwoodie, Lisa, *48-V_{IN}, 12-V_{OUT} Loadshare System Using the UCC39002 With Three DC/DC Modules*, TI Literature No. SLUA270A

Advanced 8-Pin Load-Share Controller, TI Literature No. SLUS495B

12 Appendix

Example

NOTE: The following calculations are given as an example. Actual circuit values will vary depending upon the specific modules used

This design uses the UCC39002 to parallel three Texas Instrument PT4484 modules whose output voltages are nominally 5 V, the maximum output current of each module is 20 A, and a maximum output voltage adjustment range of 2% of the output voltage.

Known Variables

N is equal to the number of paralleled units:

$$N = 3$$

V_{OUT} is equal to the nominal output voltage of the modules:

$$V_{OUT} = 5\ V$$

$I_{OUT(max)}$ is equal to the maximum output current of each module:

$$I_{OUT(max)} = 20\ A$$

$\Delta V_{OUTADJ(max)}$ is equal to the maximum output voltage adjustment range of the module by the Sense pins, which is 2% of the output voltage for these modules:

$$\Delta V_{OUTADJ(max)} = 0.02\ V_{OUT}$$

$$\Delta V_{OUTADJ(max)} = 0.1\ V$$

Because the output voltage of the modules is equal to 5 V, the load share controller can be biased directly from this output bus by shorting the JP1, JP2, and JP3 connectors to the INT. positions:

$$V_{DD} = 5\ V$$

Measuring the Module's Unity Gain Crossover Frequency

The unity gain crossover frequency of the module was measured at maximum load exactly as shown in Figure 8. The measured results are displayed in Figure 9. Measurement shows the module has a dc gain of approximately 65 dB, a zero at approximately 1100 Hz, one pole at 10 kHz, and a double pole at approximately 200 Hz, and the crossover frequency of the module, f_{COMOD}, was measured to be 25.6 kHz:

$$f_{COMOD} = 25.6 \text{ kHz}$$

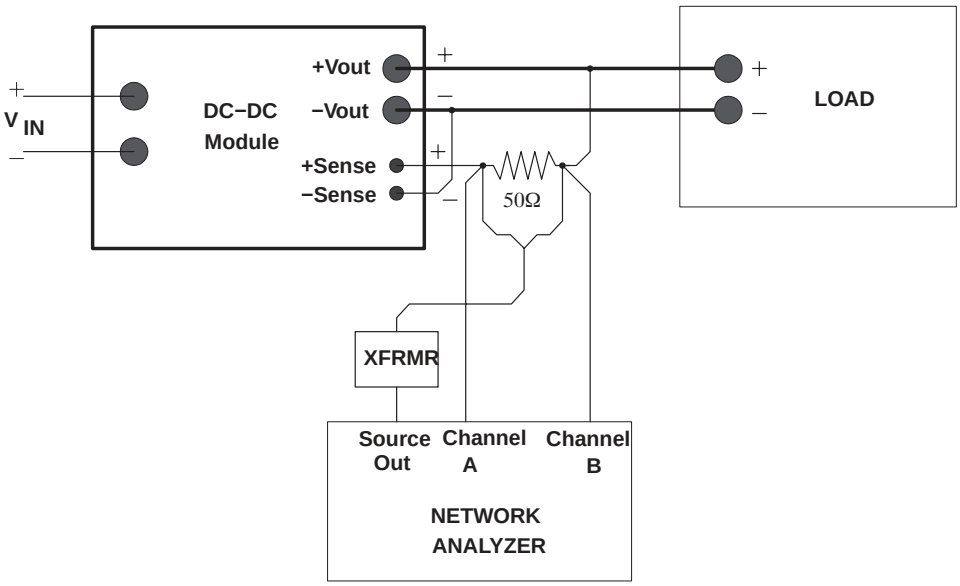

Figure 9. Connection Diagram for Measuring the Unity Gain Crossover Frequency of a Power Module

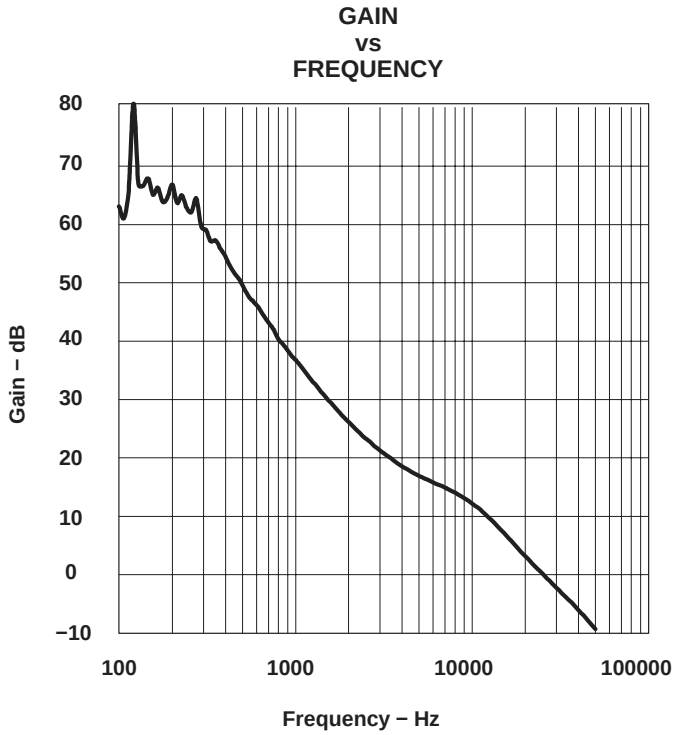

Figure 10. Gain-Frequency Response (PT4484 at Maximum Load)

The results of this gain-frequency measurement are approximated in the following equation and plotted in Figure 10:

$$G_{MOD}(f) = 10^{\frac{65}{20}} \times \frac{1 + s(f) \times \left(\frac{1}{2 \times \pi \times 1100\ Hz}\right)}{\left[1 + s(f) \times \left(\frac{1}{2 \times \pi \times 10000\ Hz}\right)\right] \times \left[1 + s(f) \times \left(\frac{1}{2 \times \pi \times 200\ Hz}\right)\right]^2}$$

where:

$f = 100\ Hz,\ 200\ Hz,\ 50\ kHz$

$s(f) = j \times 2 \times \pi \times f$

$G_{MODULE}(f) = 20 \times \log\left(\left|G_{MOD}(f)\right|\right)$

$\Theta_{MODULE}(f) = \arg\left(G_{MOD}(f)\right) \times \frac{180}{\pi}$

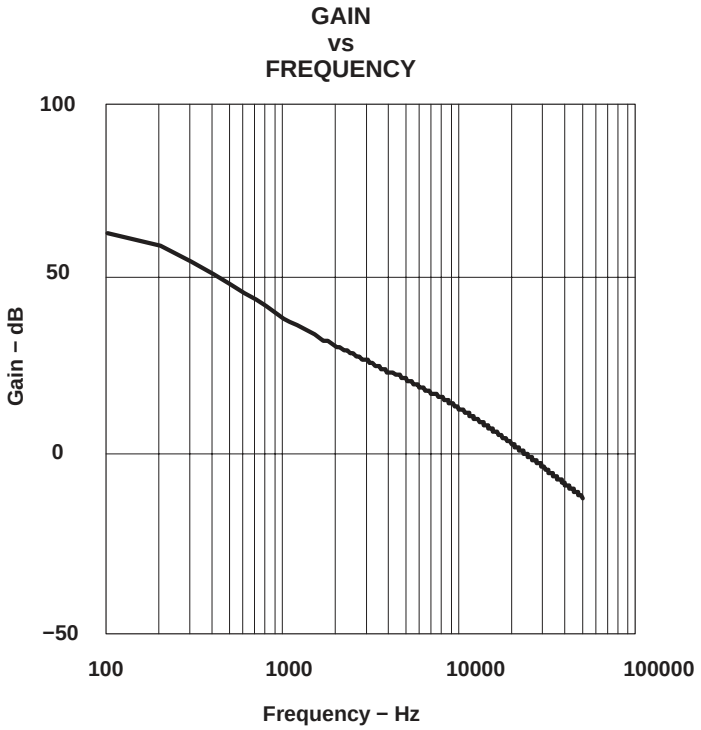

Figure 11. Gain-Frequency Mathematical Approximation of the PT4484 Module

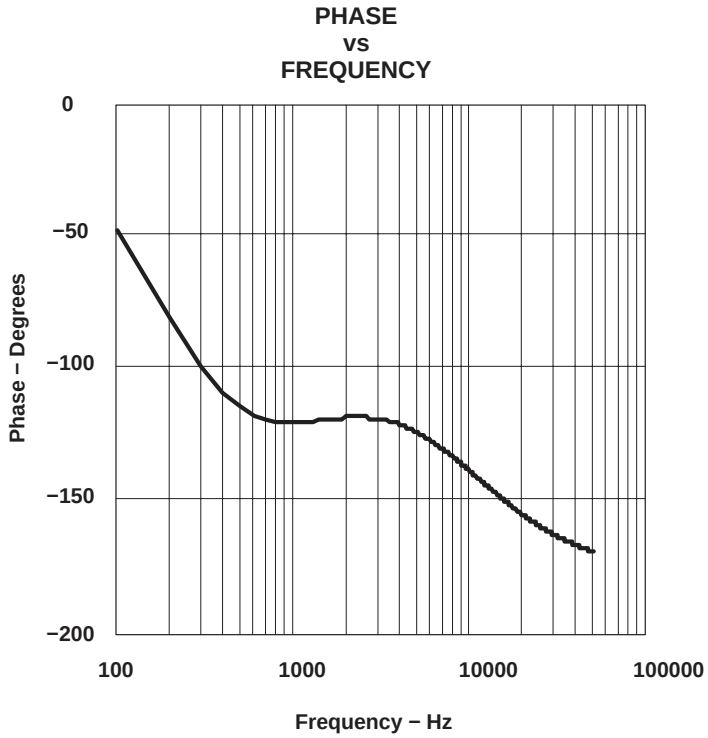

Figure 12. Phase-Frequency Mathematical Approximation of the PT4484 Module

Choosing the Sense Resistor

Because the current sense resistor is in series with the sense lines of the module, the voltage drop across the sense resistor, V_{RSENSE}, must be subtracted from the maximum voltage adjustment range of the module. V_{RSENSE} must be much less than ΔV_{ADJ} otherwise there would be no headroom for the load share controller to adjust the output voltage of the module. The following equation should be true:

$$R_{SENSE} \times I_{OUT(max)} < \Delta V_{ADJ}$$

The evaluation module can accommodate two 1-W resistors in parallel for each load share controller circuit. In order to allow for de-rating, the maximum combined power dissipation is limited to 1 W for the combination. $P_{RSENSE(max)}$ is equal to the desired maximum power dissipation of the sense resistors:

$$P_{RSENSE(max)} = 1\ W$$

$R_{SENSE(max)}$ is equal to the maximum value of the current sense resistor for the given allowable power dissipation:

$$R_{SENSE(max)} = \frac{P_{RSENSE(max)}}{I_{OUT(max)}^{2}}$$

$$R_{SENSE(max)} = 2.5\ m\Omega$$

R_{SENSE} is equal to the actual resistor value used based upon availability of standard values, two 0.002-Ω resistors are used in parallel:

$$R_{SENSE} = 1\ m\Omega$$

P_{RSENSE} is equal to the calculated power dissipation of the actual resistor used and V_{Rsense} is equal to its resultant voltage drop:

$$P_{RSENSE} = R_{SENSE} \times I_{OUT(max)}^{2}$$

$$P_{RSENSE} = 0.4\ W$$

$$V_{RSENSE} = I_{OUT(max)} \times R_{SENSE}$$

$$V_{RSENSE} = 0.02\ V$$

Confirm that V_{RSENSE} is much less than ΔV_{ADJ}.

Setting the Gain of the Current Sense Amplifier

$V_{CSO(max)}$ is equal to the absolute maximum voltage of the CSO pin and, to avoid saturating the internal amplifier, is limited to:

$$V_{CSO(max)} = V_{DD} - 2\ V$$

$A_{CSA(max)}$ is equal to the absolute maximum allowable current sense gain before saturation:

$$A_{CSA(max)} = \frac{V_{CSO(max)}}{R_{SENSE} \times I_{OUT(max)}}$$

$$A_{CSA(max)} = 150$$

A_{CSA} is equal to the actual current sense amplifier gain chosen for this design:

$$A_{CSA} = 100$$

V_{CSO} is equal to the resultant output voltage of the current sense amplifier (CSA) and approximate voltage of the load share (LS) bus:

$$V_{CSO} = A_{CSA} \times R_{SENSE} \times I_{OUT(max)}$$

$$V_{CSO} = 2\ V$$

A_{CSA} is equal to the current sense amplifier gain set by $R_{CSA}1$ (R22) and R_{CSA2} (R19):

$$R_{CSA(1)} = 100\ k\Omega$$

$$R_{CSA(2)} = 1\ k\Omega$$

$$A_{CSA} = \frac{R_{CSA(1)}}{R_{CSA(2)}}$$

$$A_{CSA} = 100$$

f_{POLE} is equal to the added *high frequency* pole for noise roll off:

$$f_{POLE} = 50\ kHz$$

$$C_{CSA} = \frac{1}{2 \times \pi \times R_{CSA(1)} \times f_{POLE}}$$

$$C_{CSA} = 31.831\ pF$$

C_{CSA} is equal to the actual capacitor value selected for this pole:

$$C_{CSA} = 33\ pF$$

The resultant actual pole frequency:

$$f_{POLE} = \frac{1}{2 \times \pi \times R_{CSA(1)} \times C_{CSA}}$$

$$f_{POLE} = 48.229\ kHz$$

Note that these CSA compensation components must be on both input terminals of the differential amplifier.

R_{LS} is equal to the internal resistance of the LS pin, which is seen as a load to the master module and will cause a subsequent increase in supply current and power dissipation of the master module:

$$R_{LS} = 100\ K\Omega$$

$$I_{MASTERINCREASE(max)} = N \times \left(\frac{V_{CSO(max)}}{R_{LS}} \right)$$

$$I_{MASTERINCREASE(max)} = 0.09\ mA$$

$$P_{MASTERINCREASE} = V_{DD} \times I_{MASTERINCREASE(max)}$$

$$P_{MASTERINCREASE} = 0.45\ mW$$

Determining R_{ADJ}

$I_{ADJ(max)}$ is equal to the maximum current that the internal adjust amplifier can sink:

$$I_{ADJ(max)} = \frac{3\ V}{500\ \Omega}$$

$$I_{ADJ(max)} = 6\ mA$$

A resistor, R_{ADJ}, is placed between the power module's Sense+ terminal and the load. The load share controller's adjust amplifier will sink current through this resistor proportional to the error amplifier output voltage, setting up an artificial sense voltage at the module and resulting in the module adjusting its output voltage, and current, accordingly until the error amplifier output turns off the adjust amplifier. The value of R_{ADJ} can be calculated first by assuming the maximum voltage drop across it can be no greater than the maximum output voltage adjustment range of the module by the Sense pins, $\Delta V_{OUTADJ(max)}$, minus the voltage drop across the sense resistor:

$$R_{ADJ} = \frac{\Delta V_{OUTADJ(max)} - I_{OUT(max)} \times R_{SENSE}}{I_{ADJ(max)}}$$

$$R_{ADJ} = 13.3\ \Omega$$

This sets up a voltage at the ADJ pin, V_{ADJ}, equal to:

$$V_{ADJ} = V_{OUT} - R_{ADJ} \times I_{ADJ}$$

$$I_{ADJ} = 6\ mA$$

$$V_{ADJ} = 4.92\ V$$

V_{ADJ} is not only equal to the voltage at the ADJ pin but it must also be greater than or equal to the error amplifier output voltage, V_{EAO}, by at least 1 V in order to keep the internal transistor from saturating:

$$V_{ADJ} \geq V_{EAO} + 1\ V$$

V_{EAO} is clamped to a maximum of 3 V and will be equal to the voltage drop across the internal 500-Ω resistor due to the current sunk by the adjust amplifier at ADJ:

$$V_{EAO} = I_{ADJ} \times 500\ \Omega$$

With V_{EAO} clamped to a maximum of 3 V, and V_{ADJ} approximately equal to the output voltage (minus a small voltage drop across the sense resistor), designs with output voltages of 4 V or greater, such as this one, will easily meet the 1 V greater than V_{EAO} requirement for V_{ADJ}. However, paralleling modules whose output voltage is greater than 1 V but less than 4 V may risk saturating the internal adjust amplifier transistor if the R_{ADJ} does not also meet the following requirement:

$$R_{ADJ} \geq \frac{\left(\Delta V_{OUTADJ(max)} - I_{OUT(max)} \times R_{SENSE}\right) \times 500\ \Omega}{\left[V_{OUT} - \left(\Delta V_{OUTADJ(max)} - I_{OUT(max)} \times R_{SENSE}\right) - 1\ V\right]}$$

$$R_{ADJ} \geq 10.2\ \Omega$$

As pointed out above, this design has an output voltage of 5 V so ADJ pin is approximately equal to 4.92 V which naturally exceeds the maximum voltage on the EAO pin, equal to 3 V, by greater than 1 V by using an adjust resistor that is greater than 10.2 Ω. Utilizing the full range of available adjust amplifier sink current of 6 mA, without exceeding it, requires using an adjust resistor equal to 13.3 Ω, as calculated earlier.

Error Amplifier Compensation

System stability requires the load share circuit's unity gain crossover frequency to be well before the unity gain crossover frequency of the power module, as measured in the first step of this design. In order to compensate the error amplifier so that the load share controller's crossover frequency does not interfere with the power module, a zero is added to the error amplifier at least one decade before the module's crossover frequency. In this design, because the module's crossover frequency is relatively high, at 25.6 kHz, the zero can be easily placed two decades before this. f_{zero} is equal to the desired frequency of the error amplifier compensation zero:

$$f_{ZERO} = \frac{f_{COMOD}}{100}$$

$$f_{ZERO} = 256 \text{ Hz}$$

The absolute value of the gain of the power module is calculated at this zero frequency from the equation used to plot Figure 3, or it can be estimated from the original gain frequency measurement, note this value is unit less, not in dB:

$$\left|G_{MOD}\left(f_{ZERO}\right)\right| = 691.784$$

A_V is equal to the voltage gain:

$$A_V = \frac{R_{SENSE}}{R_{LOAD}}$$

R_{LOAD} is equal to:

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(max)}}$$

$$A_V = 4 \times 10^{-3}$$

A_{ADJ} is equal to the adjust amplifier gain:

$$A_{ADJ} = \frac{R_{ADJ}}{500\ \Omega}$$

$$A_{ADJ} = 0.027$$

G_M is equal to the transconductance of the internal error amplifier:

$$G_M = 0.014 \text{ S}$$

$$S = \frac{1}{\Omega}$$

Combine all of the gains to determine the appropriate capacitor for compensation, C_{EAO}:

$$C_{EAO} = \frac{G_M}{2 \times \pi \times f_{ZERO}} \times A_{CSA} \times A_V \times A_{ADJ} \left| G_{MOD}\left(f_{ZERO}\right) \right|$$

$$C_{EAO} = 64.065\ \mu\text{F}$$

Actual capacitor value used:

$$C_{EAO} = 68\ \mu\text{F}$$

R_{EAO} is equal to the series resistor used in the error amplifier compensation:

$$R_{EAO} = \frac{1}{2 \times \pi \times f_{ZERO} \times C_{EAO}}$$

$$R_{EAO} = 10\ \Omega$$

Actual resistor value used:

$$R_{EAO} = 10\ \Omega$$

A bode plot of the load share open loop gain frequency response and comparing it to the original gain frequency response of the individual module is shown in Figure12:

$$G_{ERRORAMP}(f) = G_M\left(\frac{1}{s(f) \times C_{EAO}} + R_{EAO}\right)$$

$$G_{LSOPENLOOP}(f) =$$

$$20 \times \log\left(\left|G_{CSA}(f)\right|\right) + 20 \times \log\left(\left|A_V\right|\right) + 20 \times \log\left(\left|A_{ADJ}\right|\right) + 20 \times \log\left(\left|G_{ERRORAMP}(f)\right|\right)$$

$$G_{TOTAL}(f) = G_{LSOPENLOOP}(f) + G_{MODULE}(f)$$

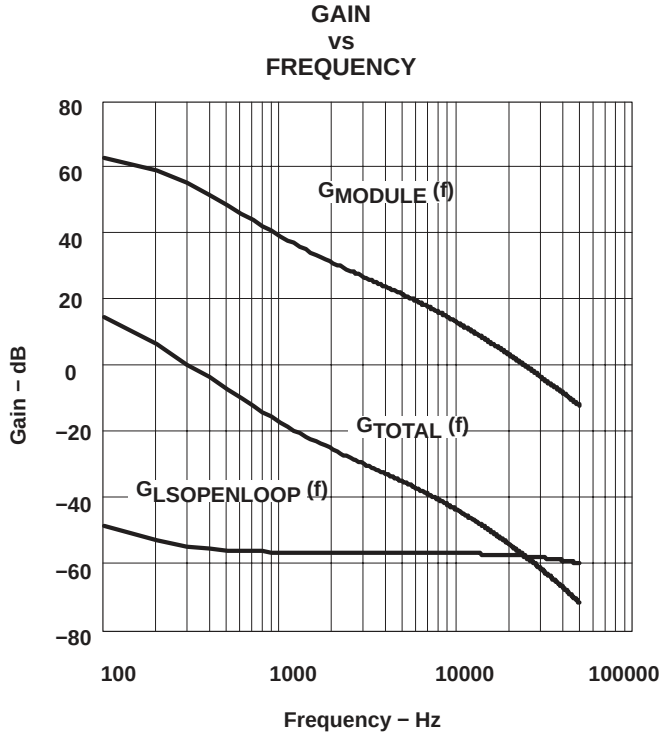

Figure 13. Load Share Open Loop Gain Frequency Response

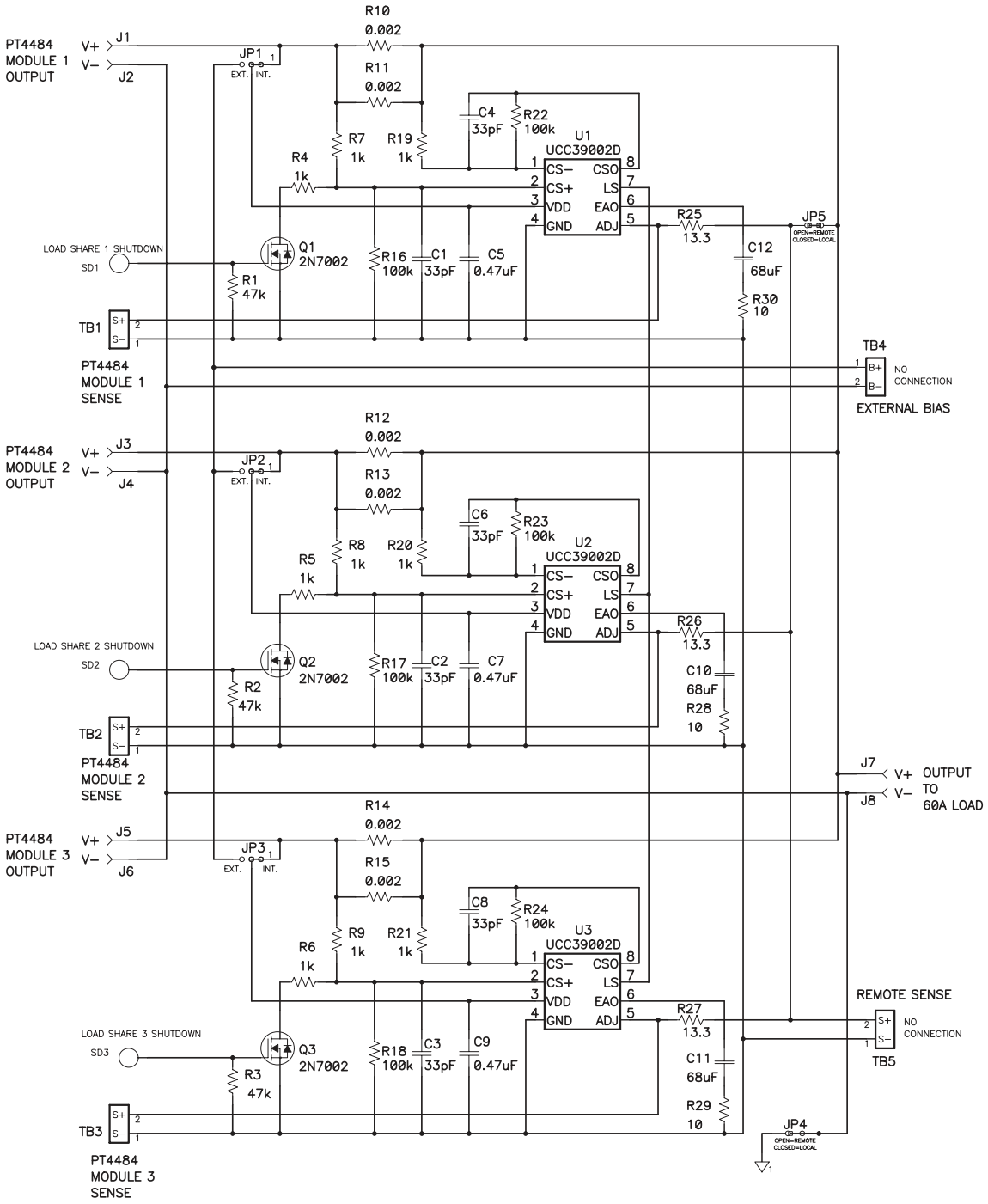

Figure 14. Schematic of Three Paralleled PT4484 Modules

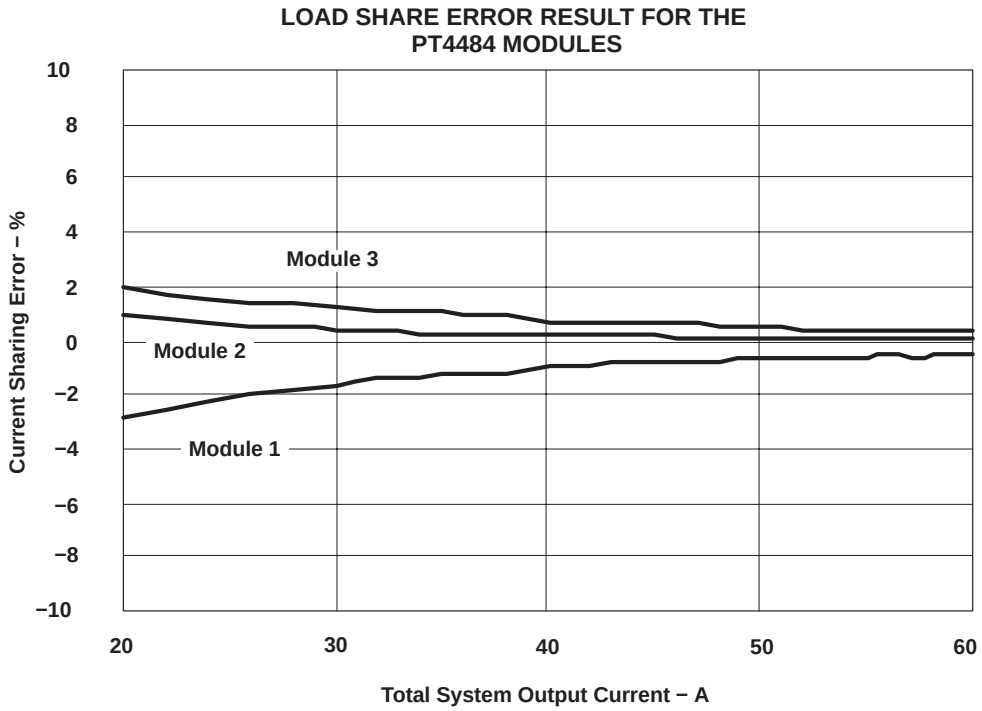

Figure 15. Resultant Load Current Sharing Accuracy, as Measured Across Shunts from the Output of Each Module.

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