

## Real-time Clock Module (3-wire Interface)

### Features

- Using external 32.768kHz quartz crystal
- Real-time clock (RTC) counts seconds, minutes, hours, date of the month, month, day of the week, and year with leap-year compensation valid up to 2099
- 31-byte, nonvolatile (NV) RAM for data storage
- Time keeping voltage: 1.5V to 5.5V
- Uses less than 300nA at 2.0V
- Simple 3-wire interface
- Serial I/O for minimum pin count
- Burst mode for reading/writing successive addresses in clock/RAM
- TTL-compatible ( $V_{CC} = 5V$ )
- Optional industrial temperature range:  $-40^{\circ}C$  to  $+85^{\circ}C$
- Battery backup
- Trickle charger on chip for rechargeable energy source backup

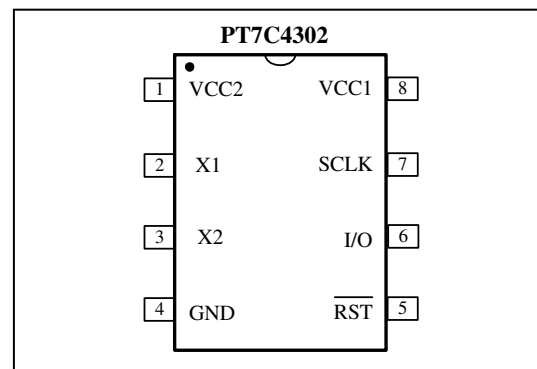
### Description

The PT7C4302 serial real-time clock is a low-power clock/calendar with a programmable square-wave output and 31 bytes of nonvolatile RAM.

Address and data are transferred serially via a 3-wire bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with AM/PM indicator.

Table 1 shows the basic functions of PT7C4302. More details are shown in section: overview of functions.

### Pin Assignment

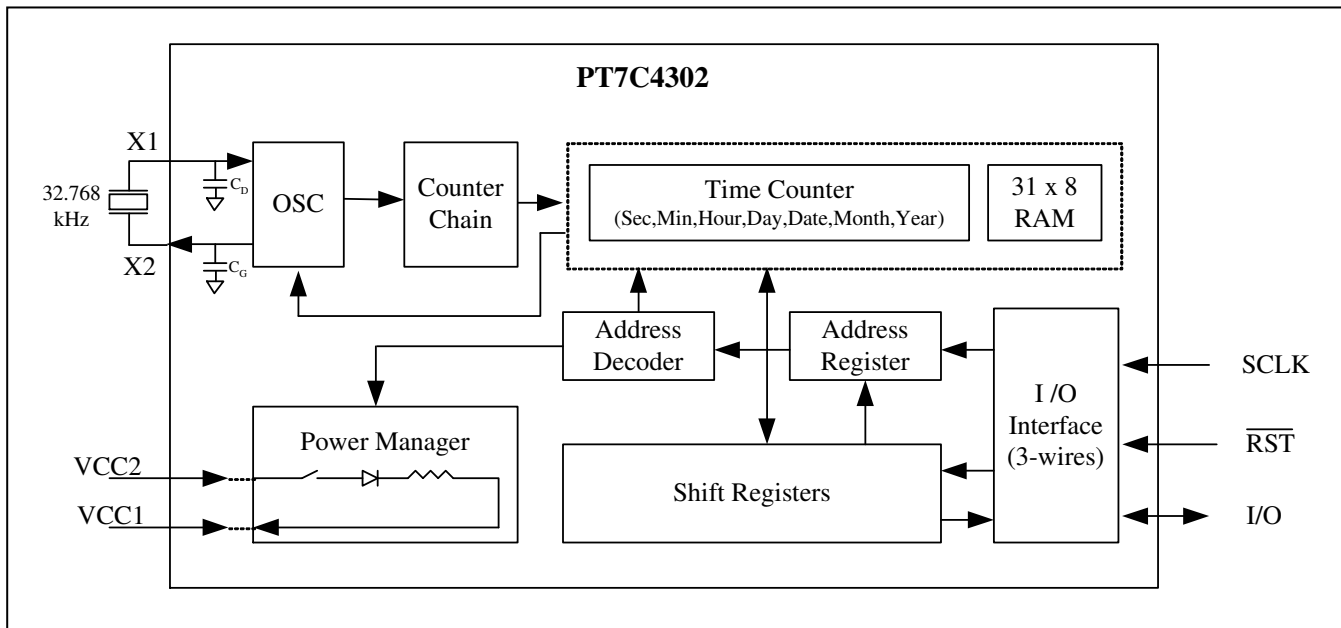


### Pin Description

Pin no.	Pin	Type	Description
1	VCC <sub>2</sub>	P	<b>Primary power.</b> When $V_{CC2}$ is greater than $V_{CC1} + 0.2V$ , $V_{CC2}$ will power the IC. While $V_{CC2} < V_{CC1}$ , $V_{CC1}$ will power the IC. *1
2	X1	I	<b>Oscillator Circuit Input.</b> Together with X2, 32.768kHz crystal is connected between them.
3	X2	O	<b>Oscillator Circuit Output.</b> Together with X1, 32.768kHz crystal is connected between them.
4	GND	P	<b>Ground.</b>
5	$\overline{RST}$	I	<b>Reset.</b> The reset signal must be asserted high during a read or a write. This pin has a 40k $\Omega$ internal pull-down resistor.
6	I/O	I/O	<b>Serial Data Input/Output.</b> I/O is the input/output pin for the 3-wire serial interface. The pin has a 40k $\Omega$ internal pull-down resistor.
7	SCLK	I	<b>Serial Clock Input.</b> SCLK is used to synchronize data movement on the 3-wire serial interface. The pin has a 40k $\Omega$ internal pull-down resistor.
8	VCC <sub>1</sub>	P	<b>Backup power.</b> When $V_{CC2}$ is greater than $V_{CC1} + 0.2V$ , $V_{CC2}$ will power the IC. While $V_{CC2} < V_{CC1}$ , $V_{CC1}$ will power the IC. *1

**Note** \*1: If  $V_{CC1}$  connects to battery, the battery voltage  $V_{CC1}$  has to be lower than  $V_{CC2} - 0.2V$  when IC is read and written.

### Function Block



Note:  $C_D=C_G=11\text{pF}$

### Maximum Ratings

Storage Temperature.....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND) .....	-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND).....	-0.3V to +6.5V
DC Output Voltage (SDA, /INTA, /INTB pins).....	-0.3V to +6.5V
Power Dissipation .....	320mW (Depend on package)

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended Operating Conditions

Symbol	Description	Min	Type	Max	Unit
$V_{CC1}$	Backup power voltage	1.5	-	5.5	V
$V_{CC2}$	Timing data and RAM data maintaining voltage	1.2	-	5.5	
	Timing data writing voltage	1.5	-	5.5	
	Timing data reading voltage	1.5	-	5.5	
	RAM data writing voltage	3.0	-	5.5	
	RAM data reading voltage	1.5	-	5.5	
$V_{IH}$	Input high level	2	-	$V_{CC}+0.3$	
$V_{IL}$	Input low level	-0.3	-	0.3	
$T_A$	Operating temperature	-40	-	85	°C

### DC Electrical Characteristics

Unless otherwise specified, GND = 0V, T<sub>A</sub> = 25 °C, Oscillation frequency = 32.768 kHz.

Sym	Item	Pin	Conditions	Min	Typ	Max	Unit	
V <sub>CC1</sub>	Backup power voltage	VCC1	-	1.5	-	5.5	V	
V <sub>CC2</sub>	Timing and RAM data maintaining	VCC2	-	1.2	-	5.5	V	
	Timing data writing voltage		-	1.5	-	5.5		
	Timing data reading voltage		-	1.5	-	5.5		
	RAM data writing voltage		-	3.0	-	5.5		
	RAM data reading voltage		-	1.5	-	5.5		
I <sub>CC1</sub>	Current consumption	VCC1	OSC on, Note 2, 5	V <sub>CC1</sub> : 2V	-	-	0.4	mA
				V <sub>CC1</sub> : 5V	-	-	1.2	
			OSC on, Note 1, 5	V <sub>CC1</sub> : 2V	-	0.5	-	μA
				V <sub>CC1</sub> : 5V	-	1	-	
			OSC off, Note 4, 5, 7	V <sub>CC1</sub> : 2V	-	100	-	nA
				V <sub>CC1</sub> : 5V	-	100	-	
I <sub>CC2</sub>	Current consumption	VCC2	OSC on, Note 2, 6	V <sub>CC1</sub> : 2V	-	-	0.425	mA
				V <sub>CC1</sub> : 5V	-	-	1.28	
			OSC on, Note 1, 6	V <sub>CC1</sub> : 2V	-	-	25.3	μA
				V <sub>CC1</sub> : 5V	-	-	81	
			OSC off, Note 4, 6	V <sub>CC1</sub> : 2V	-	-	25	μA
				V <sub>CC1</sub> : 5V	-	-	80	
V <sub>IL1</sub>	Low-level input voltage	SCL, /RST	V <sub>CC1</sub> : 5V	-	1.1	0.8	V	
			V <sub>CC1</sub> : 2V	-	0.6	0.4		
V <sub>IH1</sub>	High-level input voltage	SCL, /RST	V <sub>CC1</sub> : 5V	2.0	1.3	-	V	
			V <sub>CC1</sub> : 2V	1.4	0.9	-		
V <sub>IL2</sub>	Low-level input voltage	X1	V <sub>CC1</sub> : 5V	-	1.9	0.8	V	
			V <sub>CC1</sub> : 2V	-	0.9	0.6		
V <sub>IH2</sub>	High-level input voltage	X1	V <sub>CC1</sub> : 5V	2.0	1.9	-	V	
			V <sub>CC1</sub> : 2V	1.4	0.9	-		
V <sub>OL</sub>	Low-level output voltage	I/O	I <sub>OH</sub> = 1.5mA, V <sub>CC</sub> = 2V	-	0.08	0.4	V	
			I <sub>OH</sub> = 4.0mA, V <sub>CC</sub> = 5V	-	0.11	0.4		
V <sub>OH</sub>	High-level output voltage	I/O	I <sub>OH</sub> = -0.4mA, V <sub>CC</sub> = 2V	1.6	1.9	-	V	
			I <sub>OH</sub> = -1.0mA, V <sub>CC</sub> = 5V	2.4	4.9	-		
I <sub>IL</sub>	Input leakage current	/RST, SCLK	Note 3	-	-	500	μA	
I <sub>OZ</sub>	Output current when OFF	I/O	Note 3	-	-	500	μA	
V <sub>TD</sub>	Trickle Charge Diode Voltage Drop	-	-	-	0.7	-	V	
R1	Trickle charge resistors	-	-	-	2	-	kΩ	
R2		-	-	-	4	-		
R3		-	-	-	-	8		-

**Note:** 1. I/O open, /RST set to a logic 0, and /EOSC bit = 0 (oscillator enabled).

2. I/O pin open, /RST high, SCLK=2MHz at V<sub>CC</sub> = 5V; SCLK = 500kHz, V<sub>CC</sub> = 2.0V, and /EOSC bit = 0 (oscillator enabled).
3. /RST, SCLK, and I/O all have 40kΩ pull-down resistors to ground.
4. /RST, I/O, and SCLK open. The /EOSC bit = 1 (oscillator disabled).
5. V<sub>CC2</sub> = 0V.
6. V<sub>CC1</sub> = 0V.
7. Typical values are at 25°C.

## AC Electrical Characteristics

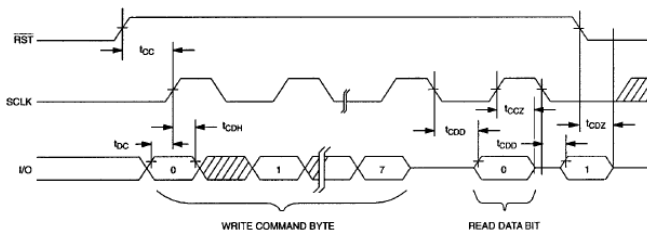


Figure 6 a Timing diagram: Read data transfer

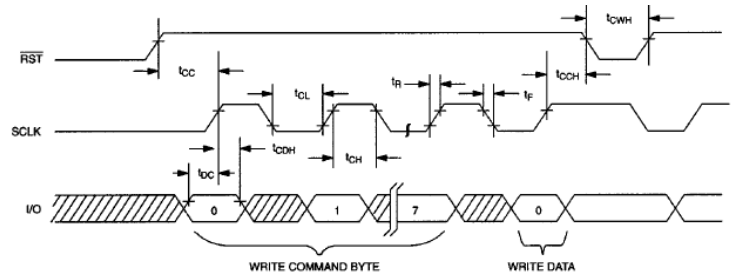


Figure 6 b Timing diagram: Write data transfer

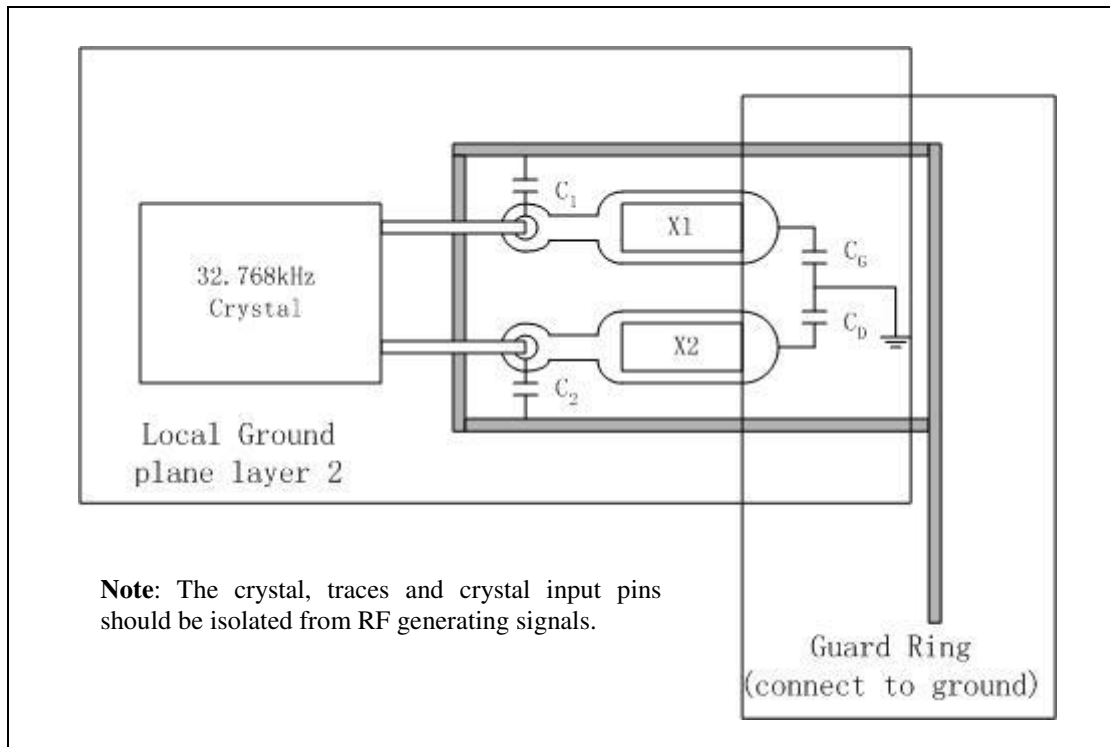
$T_A = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ . Unless otherwise specified.

Parameter	Sym	Min	Typ	Max	Unit	Notes	
Data to CLK Setup	$t_{DC}$	$V_{CC}=2.0V$	200	-	-	ns	1
		$V_{CC}=5.0V$	50	-	-		
CLK to Data Hold	$t_{CDH}$	$V_{CC}=2.0V$	280	-	-	ns	1
		$V_{CC}=5.0V$	70	-	-		
CLK to Data Delay	$t_{CDD}$	$V_{CC}=2.0V$	-	-	800	ns	1,2,3
		$V_{CC}=5.0V$	-	-	200		
CLK Low Time	$t_{CL}$	$V_{CC}=2.0V$	1000	-	-	ns	1
		$V_{CC}=5.0V$	250	-	-		
CLK High Time	$t_{CH}$	$V_{CC}=2.0V$	1000	-	-	ns	1
		$V_{CC}=5.0V$	250	-	-		
CLK Frequency	$t_{CLK}$	$V_{CC}=2.0V$	-	-	0.5	MHz	1
		$V_{CC}=5.0V$	0	-	2.0		
CLK Rise and Fall	$t_R, t_F$	$V_{CC}=2.0V$	-	-	2000	ns	1
		$V_{CC}=5.0V$	-	-	500		
$\overline{RST}$ to CLK Setup	$t_{CC}$	$V_{CC}=2.0V$	4	-	-	$\mu s$	1
		$V_{CC}=5.0V$	1	-	-		
CLK to $\overline{RST}$ Hold	$t_{CCH}$	$V_{CC}=2.0V$	240	-	-	ns	1
		$V_{CC}=5.0V$	60	-	-		
$\overline{RST}$ Inactive Time	$t_{CWH}$	$V_{CC}=2.0V$	4	-	-	$\mu s$	1
		$V_{CC}=5.0V$	1	-	-		
$\overline{RST}$ to I/O High-Z	$t_{CDZ}$	$V_{CC}=2.0V$	-	-	280	ns	1
		$V_{CC}=5.0V$	-	-	70		
SCLK to I/O High-Z	$t_{CCZ}$	$V_{CC}=2.0V$	-	-	280	ns	1
		$V_{CC}=5.0V$	-	-	70		

**Note:**

1. Measured at  $V_{IH} = 2.0V$  or  $V_{IL} = 0.8V$  and 10ns maximum rise and fall time.
2. Measured at  $V_{OH} = 2.4V$  or  $V_{OL} = 0.4V$ .
3. Load capacitance = 50pF.

### Recommended Layout for Crystal



### Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	X1 to GND	C <sub>G</sub>	11	pF
	X2 to GND	C <sub>D</sub>	11	pF
Recommended External capacitors for crystal C <sub>L</sub> =12.5pF	X1 to GND	C <sub>1</sub>	12	pF
	X2 to GND	C <sub>2</sub>	12	pF
Recommended External capacitors for crystal C <sub>L</sub> =6pF	X1 to GND	C <sub>1</sub>	0	pF
	X2 to GND	C <sub>2</sub>	0	pF

**Note:** The frequency of crystal can be optimized by external capacitor C<sub>1</sub> and C<sub>2</sub>, for frequency=32.768 KHz, C<sub>1</sub> and C<sub>2</sub> should meet the equation as below:

$$C_{par} + \frac{[(C_1 + C_G) * (C_2 + C_D)]}{[(C_1 + C_G) + (C_2 + C_D)]} = C_L$$

C<sub>par</sub> is all parasitical capacitor between X1 and X2.

C<sub>L</sub> is crystal's load capacitance.

### Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f <sub>0</sub>	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C <sub>L</sub>	-	6/12.5	-	pF

## Function Description

### Overview of Functions

#### 1. Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

#### 2. Interface with CPU

Simple 3-wire interface.

#### 3. Oscillator enable/disable

Oscillator can be enabled or disabled by /EOSC bit. But time count chain does not shut down when the bit is logic 1.

#### 4. Charger function

The function is controlled by trickle charge register. Customer can select the charge current by selecting the number of diode and resistor value through the register.

For example:

Assume that a system power supply of 5V is applied to VCC2 and a super cap is connected to VCC1. Also assume that the trickle charger has been enabled with one diode and resistor R1 between VCC2 and VCC1. The maximum current I<sub>MAX</sub> would, therefore, be calculated as follows:

$$I_{MAX} = (5.0V - \text{diode drop})/R1 = (5.0V - 0.7V) / 2k\Omega = 2.2mA$$

As the super cap charges, the voltage drop between VCC1 and VCC2 will decrease and, therefore, the charge current will decrease.

## Registers

### 1. Allocation of registers

Addr. (hex) *1	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Seconds (00-59)	/EOSC*2	S40	S20	S10	S8	S4	S2	S1
01	Minutes (00-59)	0	M40	M20	M10	M8	M4	M2	M1
02	Hours (00-23 / 01-12)	12, /24	0	H20 or P /A	H10	H8	H4	H2	H1
03	Dates (01-31)	0	0	D20	D10	D8	D4	D2	D1
04	Months (01-12)	0	0	0	MO10	MO8	MO4	MO2	MO1
05	Days of the week (01-07)	0	0	0	0	0	W4	W2	W1
06	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07	Control	WP*3	0	0	0	0	0	0	0
08	Trickle charger	TCS*4	TCS	TCS	TCS	DS*5	DS	RS*6	RS
1F	Clock burst*7	-	-	-	-	-	-	-	-
20~3E	RAM*9	-	-	-	-	-	-	-	-
3F	RAM burst*8	-	-	-	-	-	-	-	-

#### Caution points:

- \*1. PT7C4302 uses 5 bits for address. It's address byte consists of 1 + RAM/Clock select bit +5-bit addr. + Read/Write select bit.
- \*2. Oscillator Enable bit. When this bit is set to 1, oscillator is stopped but time count chain is still active.
- \*3. WP: Write Protect bit. WP bit should be cleared before attempting to write to the device.
- \*4. TCS: Trickle Charger Select.
- \*5. DS: Diode Select.
- \*6. RS: Resistor Select.
- \*7. Clock burst register address is used as clock/calendar burst mode operation address for consecutively read/write 0~7H registers. Clock/calendar burst mode operation can continuously read 0H to maximum 7H registers in order; write 0~7H registers in order. Less or larger than 8 bytes in clock burst write mode are ignored.
- \*8. RAM burst register address is used as RAM burst mode operation address for consecutively read/write 20~3EH RAM. Less than 31 bytes in RAM burst read/write mode are valid.
- \*9. PT7C4302 has 31×8 static RAM for customer use. It is volatile RAM.
- \*10. All bits marked with "0" are read-only bits. Their value when read is always "0". All bits marked with "-" are customer using space.

## 2. Control and status register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
07	Control (default)	WP 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0

**WP:** Write Protect bit.

WP	Data	Description
Read / Write	0	Write operation is enabled. <span style="float: right;">Default</span>
	1	Prevent a write operation to any other register.

## 3. Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Seconds (default)	/EOSC* 0	S40 Undefined	S20 Undefined	S10 Undefined	S8 Undefined	S4 Undefined	S2 Undefined	S1 Undefined
01	Minutes (default)	0 0	M40 Undefined	M20 Undefined	M10 Undefined	M8 Undefined	M4 Undefined	M2 Undefined	M1 Undefined
02	Hours (default)	12, /24 Undefined	0 0	H20 or P,/A Undefined	H10 Undefined	H8 Undefined	H4 Undefined	H2 Undefined	H1 Undefined

\* **Note:** /EOSC bit must be written into 0 to start the time count.

### a) 12 / 24 bit

This bit is used to select between 12-hour clock operation and 24-hour clock operation.

12, /24	Description	Hours register			
0	24-hour time display	24-hour clock	12-hour clock	24-hour clock	12-hour clock
		00	92 ( AM 12 )	12	B2 ( PM 12 )
		01	81 ( AM 01 )	13	A1 ( PM 01 )
		02	82 ( AM 02 )	14	A2 ( PM 02 )
		03	83 ( AM 03 )	15	A3 ( PM 03 )
		04	84 ( AM 04 )	16	A4 ( PM 04 )
1	12-hour time display	05	85 ( AM 05 )	17	A5 ( PM 05 )
		06	86 ( AM 06 )	18	A6 ( PM 06 )
		07	87 ( AM 07 )	19	A7 ( PM 07 )
		08	88 ( AM 08 )	20	A8 ( PM 08 )
		09	89 ( AM 09 )	21	A9 ( PM 09 )
		10	90 ( AM 10 )	22	B0 ( PM 10 )
		11	91 ( AM 11 )	23	B1 ( PM 11 )

Be sure to select between 12-hour and 24-hour clock operation before writing the time data.



**4. Days of the week Counter**

The day counter is a divide-by-7 counter that counts from 01 to 07 and up 07 before starting again from 01. Values that correspond to the day of week are user defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
05	Days of the week (default)	0 0	0 0	0 0	0 0	0 0	W4 Undefined	W2 Undefined	W1 Undefined

**5. Calendar Counter**

The data format is BCD format.

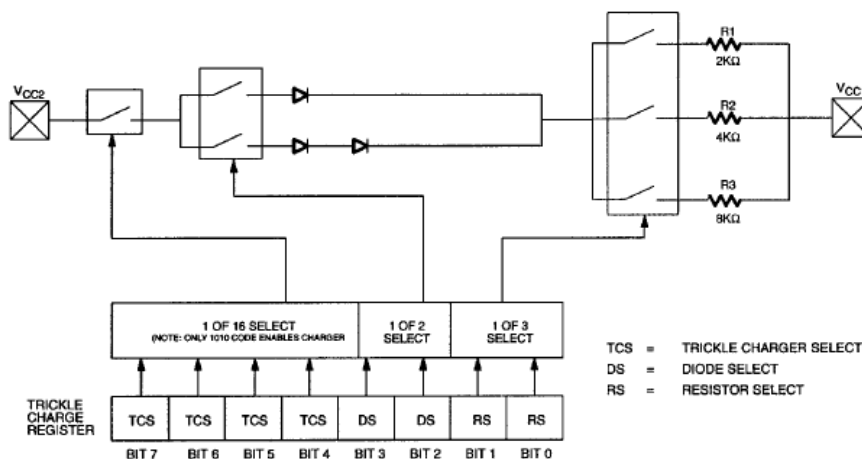
- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).  
                   Range from 1 to 30 (for April, June, September and November).  
                   Range from 1 to 29 (for February in leap years).  
                   Range from 1 to 28 (for February in ordinary years).  
                   Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, ..., 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
03	Dates (default)	0 0	0 0	D20 Undefined	D10 Undefined	D8 Undefined	D4 Undefined	D2 Undefined	D1 Undefined
04	Months (default)	0 0	0 0	0 0	M10 Undefined	M8 Undefined	M4 Undefined	M2 Undefined	M1 Undefined
06	Years (default)	Y80 Undefined	Y40 Undefined	Y20 Undefined	Y10 Undefined	Y8 Undefined	Y4 Undefined	Y2 Undefined	Y1 Undefined

**Note:** Any registered imaginary time should be replaced by correct time, otherwise it will cause the clock counter malfunction.

**6. Trickle Charger**

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
8	Trickle charger (default)	TCS 0	TCS 1	TCS 0	TCS 1	DS 1	DS 1	RS 0	RS 0



**a) Trickle Charger Select**

Control the selection of the trickle charger.

TCS	Data	Description
Read/ Write	Other patent	Disable the trickle charger <span style="float: right;">* Default 0101</span>
	1010	Enable the trickle charger

**b) Diode Select**

Select whether one diode or two diodes are connected between VCC2 and VCC1.

DS	Data	Description
Read/ Write	00 or 11	The trickle charger is disabled independently of TCS. <span style="float: right;">* Default</span>
	01	One diode is selected.
	10	Two diodes are selected.

**c) Resistor Select**

Select whether one diode or two diodes are connected between VCC2 and VCC1.

RS	Data	Description
Read/ Write	00	No resistor. <span style="float: right;">* Default</span>
	01	R1 with typ. 2kΩ
	10	R2 with typ. 4kΩ
	11	R3 with typ. 8kΩ

## Communication

**1. 3-wire Interface**

**a) Command Byte**

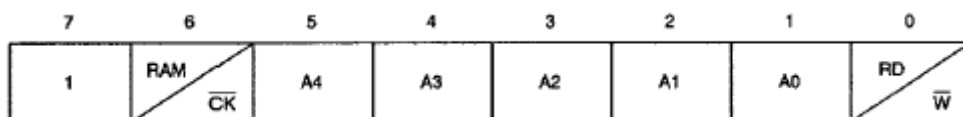


Figure 1 Command byte

The command byte is shown in Figure 1. Each data transfer is initiated by a command byte. The MSB (Bit 7) must be a logic 1. If it is 0, writes to the PT7C4302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 through 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic 1. The command byte is always input starting with the LSB (bit 0).

**b)  $\overline{\text{RST}}$  and SCL Signal**

All data transfers are initiated by driving the  $\overline{\text{RST}}$  input high and terminated by driving the  $\overline{\text{RST}}$  input low. A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the  $\overline{\text{RST}}$  input is low all data transfer terminates and the SDA pin goes to a high impedance state. Data transfer is illustrated in Figure 2 and Figure 3. At power-up,  $\overline{\text{RST}}$  must be a logic 0 until VCC > 2.0V. Also SCLK must be at a logic 0 when  $\overline{\text{RST}}$  is driven to a logic 1 state.

**c) Single Byte Read**

**SINGLE BYTE READ**

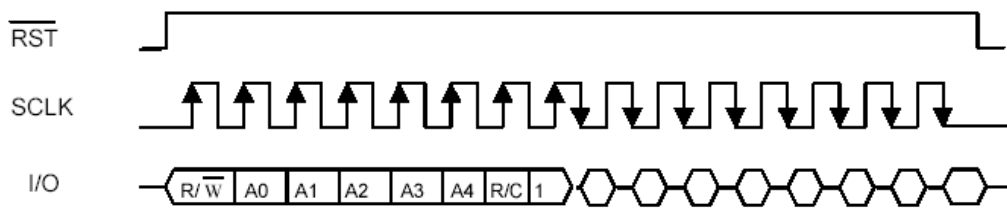


Figure 2 Single byte read

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written.

Additional SCLK cycles will transmit the same data bytes by PT7C4302 so long as  $\overline{\text{RST}}$  remains high. This operation permits continuous burst mode read capability. Also, the SDA pin is tri-stated upon each rising edge of SCLK. Data is output starting with bit 0.

**d) Single Byte Write**

**SINGLE BYTE WRITE**

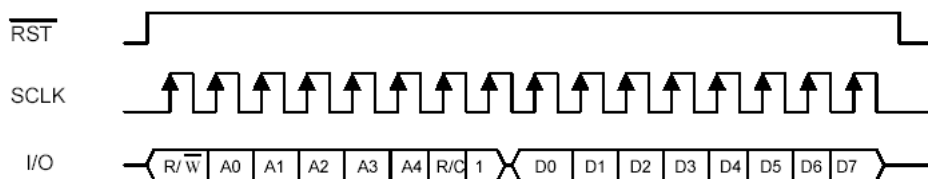


Figure 3 Signal byte write

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored. Data is input starting with bit 0.

**e) Burst Mode**

Burst mode is specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (Address bits: A4 A3 A2 A1 A0 = 1 1 1 1 1 showed in Figure 1). As before, bit 6 specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit 0 of address 0.

When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. If the number of transferred bytes is less than eight, the data will be ignored. However, when writing to RAM in burst mode, it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written will be transferred to RAM regardless of whether all 31 bytes are written or not. Additional SCLK cycles are ignored.

• **Clock/Calendar Burst Mode**

The clock/calendar command byte specifies burst mode operation. In this mode the first eight clock/calendar registers can be consecutively read or written starting with bit 0 of address 0.

If the write protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

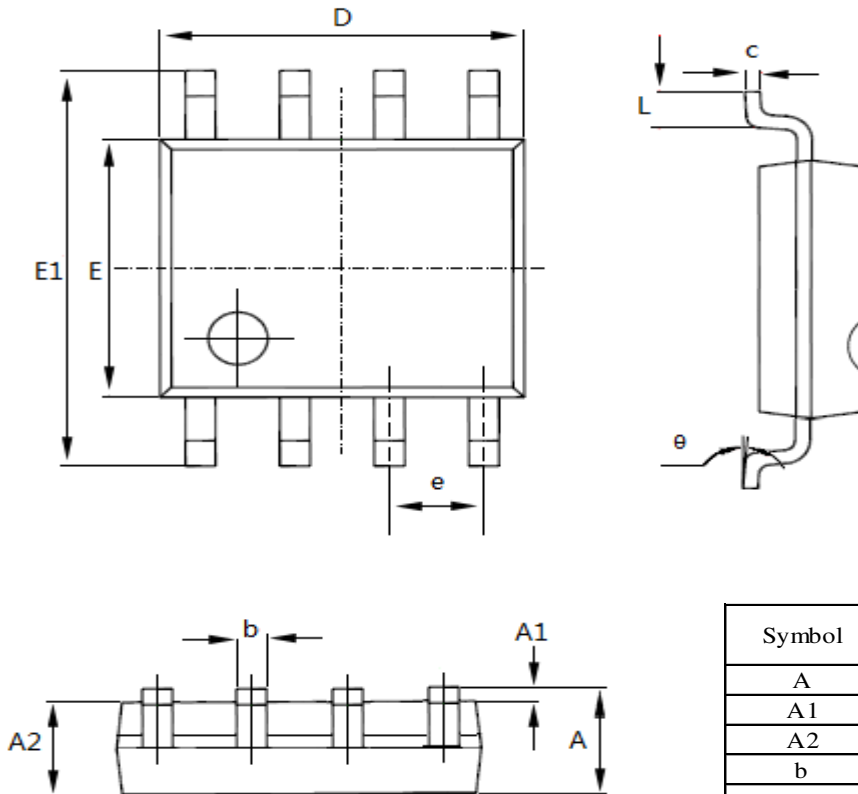
• **RAM Burst Mode**

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written starting with bit 0 of address 0.

**Note:** PT7C4302 use 94H, 96H as test mode address. Customer should not use the address.

**Mechanical Information**

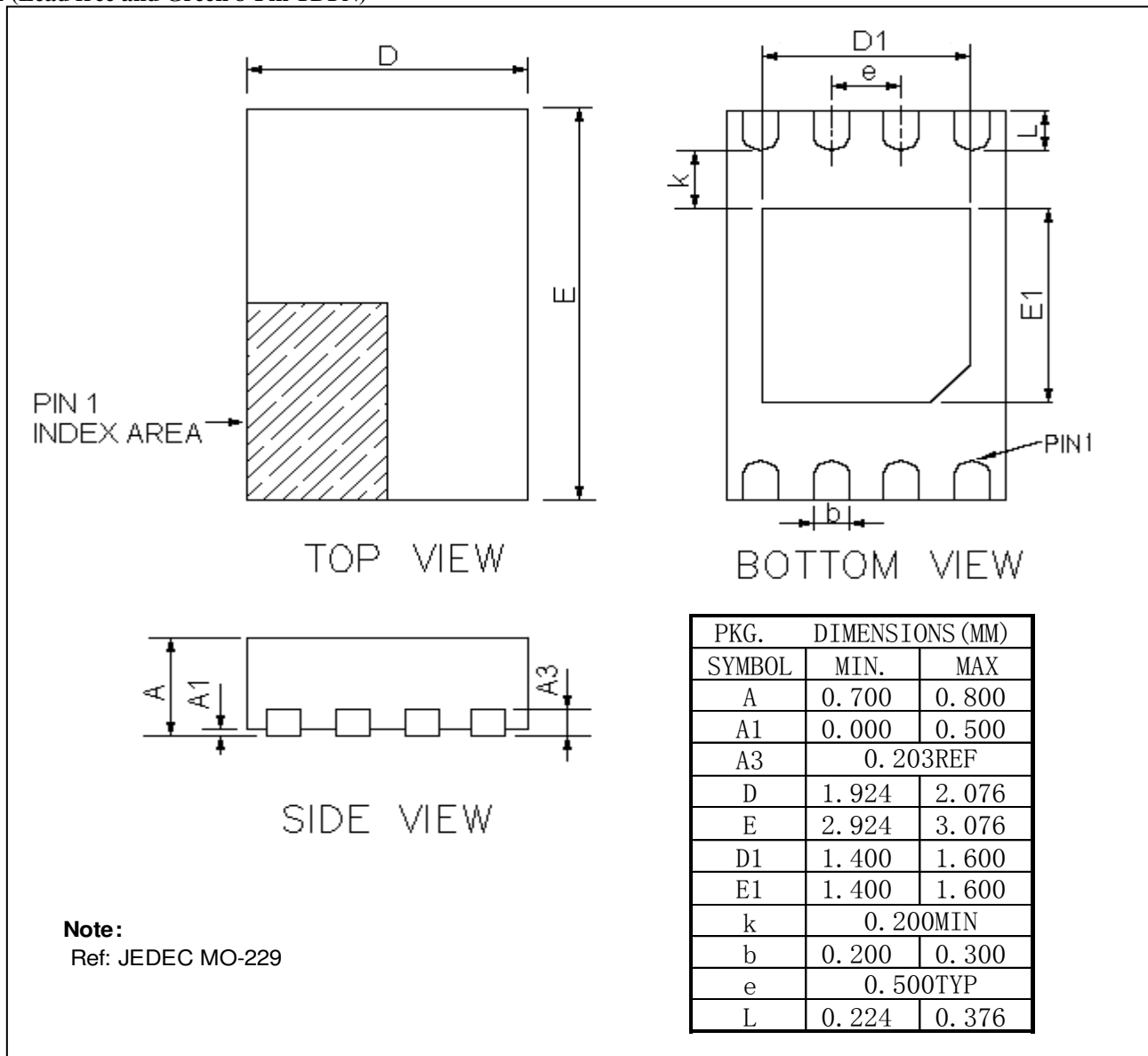
WE (8-Pin SOIC)



Symbol	Dimensions In Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
e	1.27 BSC	
L	0.400	1.270
$\theta$	0°	8°

**Note:**

- 1) Controlling dimensions in millimeters.
- 2) Ref: JEDEC MS-012E/AA

**ZEE (Lead free and Green 8-Pin TDFN)**


**Ordering Information**

<b>Part Number</b>	<b>Package Code</b>	<b>Package</b>
PT7C4302WE	W	Lead Free and Green 8-Pin SOIC (W)
PT7C4302WEX	W	Lead Free and Green 8-Pin SOIC (W) Tape/Reel
PT7C4302ZEE	ZE	Lead free and Green 8-Pin TDFN (ZE)
PT7C4302ZEEX	ZE	Lead free and Green 8-Pin TDFN (ZE) Tape/Reel

**Notes:**

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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