

Phase-Aligned Clock Multiplier

Features

- 3-multiplier configuration (1x, 2x, 4x Ref)
- 10 MHz to 166.67 MHz operating range (reference input from 10 MHz to 41.67 MHz)
- Phase Alignment
- 80 ps typical period jitter
- Output enable pin
- 3.3V operation
- 5V Tolerant input
- 8-pin 150-mil SOIC package
- Commercial and Industrial Temperature available

Functional Description

The CY2303 is a 3 output 3.3V phase-aligned system clock designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part allows user to obtain 1x, 2x, and 4x Ref output frequencies on respective output pins.

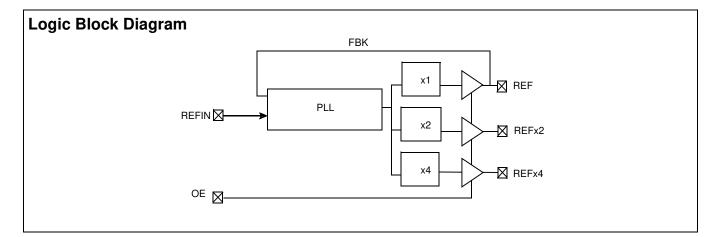
The CY2303 has an on-chip PLL, which locks to an input clock presented on the REFIN pin. The PLL feedback is internally connected to the REF output. The input-to-output skew is guaranteed to be less than ± 200 ps, and output-to-output skew is guaranteed to be less than 200 ps.

Multiple CY2303 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 400 ps.

The CY2303 is available in commercial and industrial temperature ranges.

Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2303SXC	3	10 MHz–41.67 MHz	10 MHz–166.67 MHz	Commercial Temperature
CY2303SXI	3	10 MHz–41.67 MHz	10 MHz–166.67 MHz	Industrial Temperature



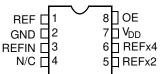
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Pinouts

Figure 1. CY2303 - 8-pin SOIC Top View



Pin Description

Pin	Signal ^[1]	Description
1	REF	REF output (1x Reference input)
2	GND	Ground
3	REFIN	Input reference frequency, 5V tolerant input
4	N/C	No Connect
5	REFx2	2x Reference input
6	REFx4	4x Reference input
7	VDD	3.3V Supply
8	OE	Output Enable (weak pull up)

Maximum Ratings

Supply Voltage to Ground Potential0.5V to +7.0V	
DC Input Voltage (Except Ref)0.5V to V_{DD} + 0.5V	
DC Input Voltage REFIN0.5 to 7V	

Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Static Discharge Voltage	. 2000)/
(per MIL-STD-883, Method 3015)	>2000 v

Operating Conditions for CY2303SC Commercial Temperature Devices

Parameter	Description	Min	Max	Unit
V _{DD}	Supply Voltage	3.0	3.6	V
T _A	Operating Temperature (Ambient Temperature)	0	70	°C
CL	Load Capacitance, Fout < 133.33 MHz	-	18	pF
	Load Capacitance, 133.33 MHz < Fout < 166.67 MHz	-	12	pF
C _{IN}	Input Capacitance	-	7	pF
t _{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for CY2303SC Commercial Temperature Devices

Parameter	Description	Test Conditions	Min.	Max.	Unit
V _{IL}	Input LOW Voltage		_	0.8	V
V _{IH}	Input HIGH Voltage		2.0	_	V
IIL	Input LOW Current	$V_{IN} = 0V$	_	100	μA
IIH	Input HIGH Current	$V_{IN} = V_{DD}$	_	50	μA
V _{OL}	Output LOW Voltage ^[2]	I _{OL} = 8 mA	-	0.4	V

Notes

1. Weak pull-down on all outputs.

^{2.} Parameter is guaranteed by design and characterization. It is not 100% tested in production.



Electrical Characteristics for CY2303SC Commercial Temperature Devices

V _{OH}	Output HIGH Voltage ^[2]	I _{OH} = -8 mA	2.4	_	V
I _{DD}	Supply Current	Unloaded outputs, REFIN = 41.67 MHz	-	45	mA
		Unloaded outputs, REFIN = 25 MHz	-	32	mA
		Unloaded outputs, REFIN = 10 MHz	_	18	mA

Switching Characteristics for CY2303SC Commercial Temperature Devices

Parameter	Name	Test Conditions	Min	Тур.	Max	Unit
1/t ₁	Output Frequency	18-pF load	10	-	133.33	MHz
		12-pF load	-	—	166.67	MHz
	Duty Cycle ^[3] = $t_2 \div t_1$	Measured at $V_{DD}/2$	40	50	60	%
t ₃	Rise Time ^[3]	Measured between 0.8V and 2.0V	-	-	1.20	ns
t ₄	Fall Time ^[3]	Measured between 0.8V and 2.0V	-	-	1.20	ns
t ₅	Output to Output Skew on rising edges ^[3]	All outputs equally loaded Measured at V _{DD} /2	-	_	200	ps
t ₆	Delay, REFIN Rising Edge to REF Rising Edge ^[3]	Measured at $V_{DD}/2$ from REFIN to any output	-	_	±200	ps
t ₇	Device to Device Skew ^[3]	Measured at $V_{DD}/2$ on the REF pin of the device (pin 1)	-	-	400	ps
tj	Period Jitter ^[3]	Measured at Fout < 133.33 MHz, loaded outputs, 18-pF load	-	80	±175	ps
t _{LOCK}	PLL Lock Time ^[3]	Stable power supply, valid clocks presented on REFIN	-	_	1.0	ms

Operating Conditions for CY2303SI Industrial Temperature Devices

Parameter	Description	Min.	Max.	Unit
V _{DD}	Supply Voltage	3.0	3.6	V
Τ _Α	Operating Temperature (Ambient Temperature)	-40	85	°C
CL	Load Capacitance, Fout <133.33 MHz	-	15	pF
	Load Capacitance, 133.33 MHz < Fout < 166.67 MHz,	-	10	pF
t _{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

Electrical Characteristics for CY2303SI Industrial Temperature Devices

Parameter	Description	Test Conditions	Min	Max.	Unit
V _{IL}	Input LOW Voltage		-	0.8	V
V _{IH}	Input HIGH Voltage		2.0	-	V
IIL	Input LOW Current	$V_{IN} = 0V$	-	100	μA
I _{IH}	Input HIGH Current	$V_{IN} = V_{DD}$	-	50	μA
V _{OL}	Output LOW Voltage ^[2]	I _{OL} = 8 mA	-	0.4	V
V _{OH}	Output HIGH Voltage ^[2]	I _{OH} = -8 mA	2.4	-	V
I _{DD}	Supply Current	Unloaded outputs, REFIN = 41.67 MHz	-	48	mA
		Unloaded outputs, REFIN = 25 MHz	-	35	mA
		Unloaded outputs, REFIN = 10 MHz	_	20	mA

Note

3. All parameters are specified with loaded outputs.



Parameter	Name	Test Conditions	Min	Тур.	Max	Unit
1/t ₁	Output Frequency	15-pF load	10	-	133.33	MHz
		10-pF load	-	-	166.67	MHz
	Duty Cycle ^[3] = $t_2 \div t_1$	Measured at V _{DD} /2	40	50	60	%
t ₃	Rise Time ^[3]	Measured between 0.8V and 2.0V	-	-	1.20	ns
t ₄	Fall Time ^[3]	Measured between 0.8V and 2.0V	-	-	1.20	ns
t ₅	Output to Output Skew on rising edges ^[3]	All outputs equally loaded Measured at V _{DD} /2	_	-	200	ps
t ₆	Delay, REFIN Rising Edge to REF Rising Edge ^[3]	Measured at $V_{DD}/2$ from REFIN to any output	_	-	±200	ps
t ₇	Device to Device Skew ^[3]	Measured at $V_{DD}/2$ on the REF pin of the device (pin 1)	_	-	400	ps
tj	Period Jitter ^[3]	Measured at Fout < 133.33 MHz, loaded outputs, 15-pF load	_	80	±175	ps
t _{LOCK}	PLL Lock Time ^[3]	Stable power supply, valid clocks presented on REFIN	_	-	1.0	ms

Switching Characteristics for CY2303SI Industrial Temperature Devices

Switching Waveforms

Figure 2. Duty Cycle Timing

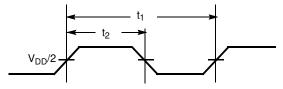


Figure 3. All Outputs Rise/Fall Time

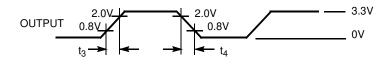
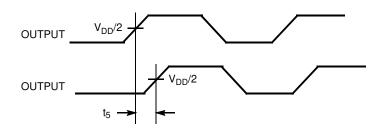


Figure 4. Output-Output Skew





Switching Waveforms (continued)

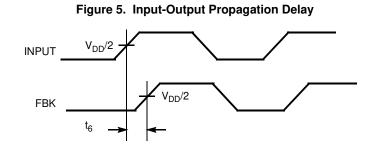
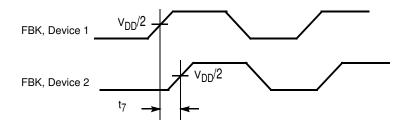
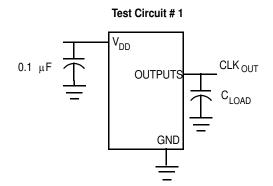


Figure 6. Device-Device Skew



Test Circuits



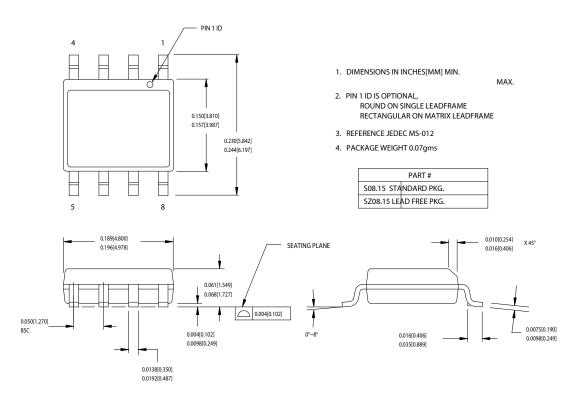
Ordering Information

Ordering Code	Package Type	Operating Range
Pb-free		
CY2303SXC	8-Pin 150-mil SOIC	Commercial
CY2303SXCT	8-Pin 150-mil SOIC - Tape and Reel	Commercial
CY2303SXI	8-Pin 150-mil SOIC	Industrial
CY2303SXIT	8-Pin 150-mil SOIC - Tape and Reel	Industrial



Package Diagram

Figure 7. 8-Pin (150-Mil) SOIC S8



51-85066-*C



Document History Page

Document Title: CY2303 Phase-Aligned Clock Multiplier Document Number: 38-07249					
REV.	ECN	Orig. of Change	Submission Date	Description of Change	
**	110514	SZV	01/07/02	Change from Spec number: 38-01036 to 38-07249	
*A	121852	RBI	12/14/02	Power up requirements added to Operating Conditions Information	
*B	390413	RGL	08/10/05	Added Lead-free devices Added typical values for jitter	
*C	2568533	AESA	09/23/08	Updated template. Removed part number CY2303SC and CY2303SI from Selector Guide table. Removed part number CY2303SC, CY2303SCT, CY2303SI, and CY2303SIT.	

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