XC95144XV High-Performance CPLD

DS051 (v3.0) June 25, 2007

Product Specification

Note: This product is being discontinued. You cannot order parts after May 14, 2008. Xilinx recommends replacing XC95144XV devices with equivalent XC95144XL devices in all designs as soon as possible. Recommended replacements are pin compatible, however require a V_{CC} change to 3.3V, and a recompile of the design file. In addition, there is no 1.8V I/O support, and only one output bank is supported. See **XCN07010** for details regarding this discontinuation, including device replacement recomendations for the XC95144XV CPLD.

Features

- 144 macrocells with 3,200 usable gates
- Available in small footprint packages
  - 100-pin TQFP (81 user I/O pins)
  - 144-pin TQFP (117 user I/O pins)
  - 144-pin CSP (117 user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Two separate output banks
  - Superior pin-locking and routability with Fast CONNECT™ II switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - 20 year data retention
  - ESD protection exceeding 2,000V

Description

The XC95144XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of eight 54V18 Function Blocks, providing 3,200 usable gates with propagation delays of 5 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

$$P_{TOTAL} = P_{INT} + P_{IO} = I_{CCINT} \times V_{CCINT} + P_{IO}$$

Separating internal and I/O power here is convenient because XC9500XV CPLDs also separate the corresponding power pins. P_{IO} is a strong function of the load capacitance driven, so it is handled by I = CVf. I_{CCINT} is another situation that reflects the actual design considered and the internal switching speeds. An estimation expression for I_{CCINT} (taken from simulation) is:

$I_{CCINT}(mA) = MC_{HS}(0.122 \text{ X } PT_{HS} + 0.238) + MC_{LP}(0.042 \text{ x } PT_{LP} + 0.171) + 0.04(MC_{HS} + MC_{LP}) \text{ x } f_{MAX} \text{ x } MC_{TOG}$

where:

MC_{HS} = # macrocells used in high speed mode

MC_{LP} = #macrocells used in low power mode

PT_{HS} = average p-terms used per high speed macrocell

PT_{LP} = average p-terms used over low power macrocell

f_{MAX} = max clocking frequency in the device

MC_{TOG} = % macrocells toggling on each clock (12% is frequently a good estimate

This calculation was derived from laboratory measurements of an XC9500XV part filled with 16-bit counters and allowing a single output (the LSB) to be enabled. The actual I_{CC} value varies with the design application and should be verified during normal system operation. Figure 1 shows the above estimation in a graphical form. For a more detailed discussion of power consumption in this device, see Xilinx

application note **XAPP361, "Planning for High Speed XC9500XV Designs."**

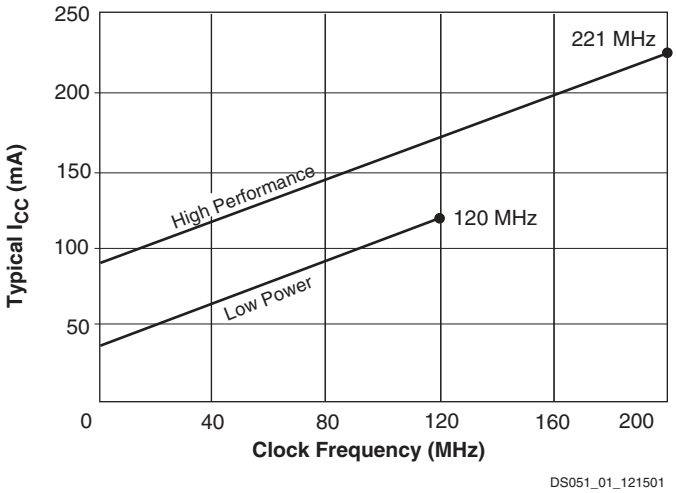


Figure 1: **Typical I_{CC} vs. Frequency for XC95144XV**

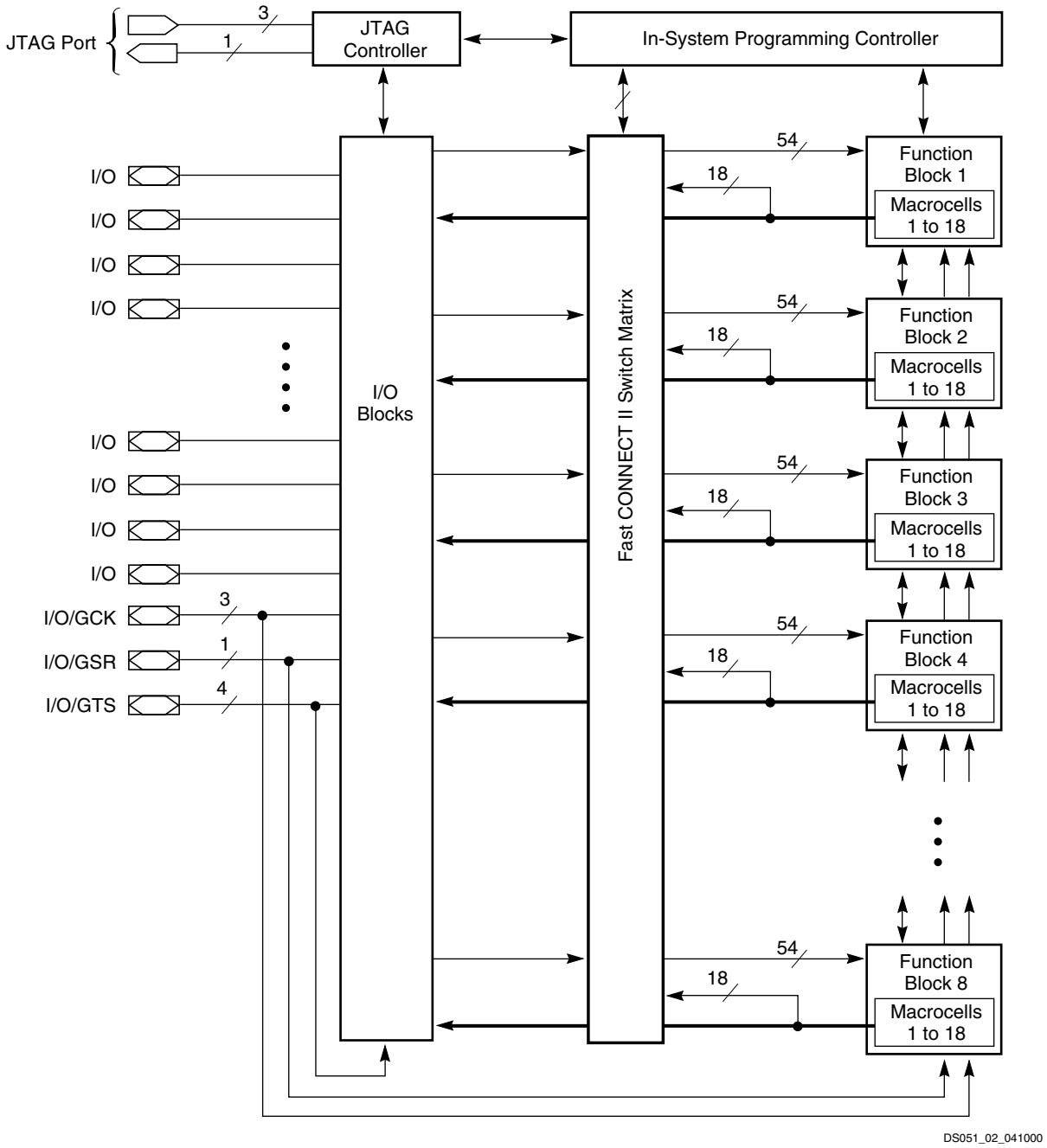


Figure 2: **XC95144XV Architecture**
Function Block outputs (indicated by the bold line) drive the I/O Blocks directly.

Supported I/O Standards

Table 1: **IOSTANDARD Options**

IOSTANDARD	V_{CCIO}
LVTTL	3.3V
LVCMOS2	2.5V
X25TO18	1.8V

The XC95144XV CPLD features both LVCMOS and LVTTL I/O implementations. See Table 1 for I/O standard voltages. The LVTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTL input buffer and Push-Pull output buffer. The LVCMOS2 standard is used in 2.5V applications.

XC9500XV CPLDs are also 1.8V I/O compatible. The X25TO18 setting is provided for generating 1.8V compatible outputs from a CPLD normally operating in a 2.5V environ-

ment. The ISE software automatically groups outputs with matching IOSTANDARD settings into the same V_{CCIO} bank when no location constraints are specified. The default I/O Standard for pads without IOSTANDARD attributes is LVTTL for XC9500XV devices.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to 2.7	V
V_{CCIO}	Supply voltage for output drivers	–0.5 to 3.6	V
V_{IN}	Input voltage relative to GND(1)	–0.5 to 3.6	V
V_{TS}	Voltage applied to 3-state output(1)	–0.5 to 3.6	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_J	Junction temperature	+150	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to +3.6V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
3. For solder specifications, see **Xilinx Packaging**.

Recommended Operation Conditions

Symbol	Parameter		Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffers	Commercial T_A = 0°C to +70°C	2.37	2.62	V
		Industrial T_A = –40°C to +85°C	2.37	2.62	
V_{CCIO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.37	2.62	V
	Supply voltage for output drivers for 1.8V operation		1.71	1.89	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		1.7	3.6	V
V_O	Output voltage		0	V_{CCIO}	V

Quality and Reliability Characteristics

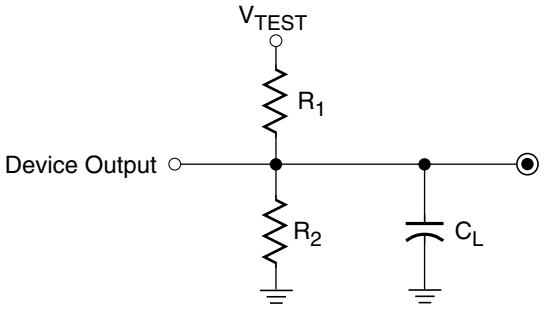
Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/Erase cycles (endurance)	1,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

DC Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 3.3V outputs	I_{OH} = –4.0 mA	2.4	-	V
	Output high voltage for 2.5V outputs	I_{OH} = –1.0 mA	2.0	-	V
	Output high voltage for 1.8V outputs	I_{OH} = –100 µA	90% V_{CCIO}	-	V
V_{OL}	Output low voltage for 3.3V outputs	I_{OL} = 8.0 mA	-	0.4	V
	Output low voltage for 2.5V outputs	I_{OL} = 1.0 mA	-	0.4	V
	Output low voltage for 1.8V outputs	I_{OL} = 100 µA	-	0.4	V
I_{IL}	Input leakage current	V_{CC} = 2.62V V_{CCIO} = 3.6V V_{IN} = GND or 3.6V	-	±10	µA
I_{IH}	Input high-Z leakage current	V_{CC} = 2.62V V_{CCIO} = 3.6V V_{IN} = GND or 3.6V	-	±10	µA
		V_{CC} min < V_{IN} < 3.6V	-	±150	µA
C_{IN}	I/O capacitance	V_{IN} = GND f = 1.0 MHz	-	10	pF
I_{CC}	Operating Supply Current (low power mode, active)	V_I = GND, No load f = 1.0 MHz	29		mA

AC Characteristics

Symbol	Parameter	XC95144XV-5		XC95144XV-7		Units
		Min	Max	Min	Max	
T_{PD}	I/O to output valid	-	5.0	-	7.5	ns
T_{SU}	I/O setup time before GCK	3.5	-	4.8	-	ns
T_H	I/O hold time after GCK	0	-	0	-	ns
T_{CO}	GCK to output valid	-	3.5	-	4.5	ns
f_{SYSTEM}	Multiple FB internal operating frequency	-	222.2	-	125.0	MHz
T_{PSU}	I/O setup time before p-term clock input	1.0	-	1.6	-	ns
T_{PH}	I/O hold time after p-term clock input	2.5	-	3.2	-	ns
T_{PCO}	P-term clock output valid	-	6.0	-	7.7	ns
T_{OE}	GTS to output valid	-	4.0	-	5.0	ns
T_{OD}	GTS to output disable	-	4.0	-	5.0	ns
T_{POE}	Product term OE to output enabled	-	7.0	-	9.5	ns
T_{POD}	Product term OE to output disabled	-	7.0	-	9.5	ns
T_{AO}	GSR to output valid	-	10.0	-	12.0	ns
T_{PAO}	P-term S/R to output valid	-	10.7	-	12.6	ns
T_{WLH}	GCK pulse width (High or Low)	2.2	-	4.0	-	ns
T_{PLH}	P-term clock pulse width (High or Low)	5.0	-	6.5	-	ns
T_{APRPW}	Asynchronous preset/reset pulse width (High or Low)	5.0	-	6.5	-	ns



Output Type	V_{CCIO}	V_{TEST}	R_1	R_2	C_L
	3.3V	3.3V	320Ω	360Ω	35 pF
	2.5V	2.5V	250Ω	660Ω	35 pF
	1.8V	1.8V	10KΩ	14KΩ	35 pF

DS051_03_0601000

Figure 3: **AC Load Circuit**

Internal Timing Parameters

Symbol	Parameter	XC95144XV-5		XC95144XV-7		Units
		Min	Max	Min	Max	
Buffer Delays						
T_{IN}	Input buffer delay	-	2.0	-	2.3	ns
T_{GCK}	GCK buffer delay	-	1.2	-	1.5	ns
T_{GSR}	GSR buffer delay	-	2.0	-	3.1	ns
T_{GTS}	GTS buffer delay	-	4.0	-	5.0	ns
T_{OUT}	Output buffer delay	-	2.1	-	2.5	ns
T_{EN}	Output buffer enable/disable delay	-	0	-	0	ns
Product Term Control Delays						
T_{PTCK}	Product term clock delay	-	1.7	-	2.4	ns
T_{PTSR}	Product term set/reset delay	-	0.7	-	1.4	ns
T_{PTTS}	Product term 3-state delay	-	5.0	-	7.2	ns
Internal Register and Combinatorial Delays						
T_{PDI}	Combinatorial logic propagation delay	-	0.2	-	1.3	ns
T_{SUI}	Register setup time	2.0	-	2.6	-	ns
T_{HI}	Register hold time	1.5	-	2.2	-	ns
T_{ECSU}	Register clock enable setup time	2.0	-	2.6	-	ns
T_{ECHO}	Register clock enable hold time	1.5	-	2.2	-	ns
T_{COI}	Register clock to output valid time	-	0.2	-	0.5	ns
T_{AOI}	Register async. S/R to output delay	-	5.9	-	6.4	ns
T_{RAI}	Register async. S/R recover before clock	5.0		7.5		ns
T_{LOGI}	Internal logic delay	-	0.7	-	1.4	ns
T_{LOGILP}	Internal low power logic delay	-	5.7	-	6.4	ns
Feedback Delays						
T_F	Fast CONNECT II feedback delay	-	1.6	-	3.5	ns
Time Adders						
T_{PTA}	Incremental product term allocator delay	-	0.7	-	0.8	ns
T_{PTA2}	Adjacent macrocell p-term allocator delay	-	0.3	-	0.3	ns
T_{SLEW}	Slew-rate limited delay	-	3.0	-	4.0	ns

XC95144XV I/O Pins

Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Bank
1	1	-	23	H3	429	1
1	2	11	16	F1	426	1
1	3	12	17	G2	423	1
1	4	-	25	J1	420	1
1	5	13	19	G3	417	1
1	6	14	20	G4	414	1
1	7	-	-	-	411	-
1	8	15	21	H1	408	1
1	9	16	22	H2	405	1
1	10	-	31	K3	402	1
1	11	17	24	H4	399	1
1	12	18	26	J2	396	1
1	13	-	-	-	393	-
1	14	19	27	J3	390	1
1	15	20	28	J4	387	1
1	16	-	35	M1	384	1
1	17	22(1)	30(1)	K2(1)	381	1
1	18	-	-	-	378	-
2	1	-	142	C3	375	2
2	2	99(1)	143(1)	A2(1)	372	2
2	3	-	-	-	369	-
2	4	-	4	C1	366	2
2	5	1(1)	2(1)	B1(1)	363	2
2	6	2(1)	3(1)	C2(1)	360	2
2	7	-	-	-	357	-
2	8	3(1)	5(1)	D4(1)	354	2
2	9	4(1)	6(1)	D3(1)	351	2
2	10	-	7	D2	348	2
2	11	6	9	E4	345	2
2	12	7	10	E3	342	2
2	13	-	12	E1	339	2
2	14	8	11	E2	336	2
2	15	9	13	F4	333	2
2	16	-	14	F3	330	2
2	17	10	15	F2	327	2
2	18	-	-	-	324	-

Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Bank
3	1	-	39	M3	321	1
3	2	23(1)	32(1)	L1(1)	318	1
3	3	-	41	K4	315	1
3	4	-	44	N4	312	1
3	5	24	33	L2	309	1
3	6	25	34	L3	306	1
3	7	-	46	L5	303	1
3	8	27(1)	38(1)	N2(1)	300	1
3	9	28	40	N3	297	1
3	10	-	48	N5	294	1
3	11	29	43	M4	291	1
3	12	30	45	K5	288	1
3	13	-	-	-	285	-
3	14	32	49	K6	282	1
3	15	33	50	L6	279	1
3	16	-	-	-	276	-
3	17	34	51	M6	273	1
3	18	-	-	-	270	-
4	1	-	118	C9	267	2
4	2	87	126	A7	264	2
4	3	-	133	A5	261	2
4	4	-	-	-	258	-
4	5	89	128	D7	255	2
4	6	90	129	A6	252	2
4	7	-	-	-	249	-
4	8	91	130	B6	246	2
4	9	92	131	C6	243	2
4	10	-	135	C5	240	2
4	11	93	132	D6	237	2
4	12	94	134	B5	234	2
4	13	-	137	A4	231	2
4	14	95	136	D5	228	2
4	15	96	138	B4	225	2
4	16	-	139	C4	222	2
4	17	97	140	A3	219	2
4	18	-	-	-	216	-

Notes:
1. Global control pin.

XC95144XV I/O Pins *(Continued)*

Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Bank
5	1	-	-	-	213	-
5	2	35	52	N6	210	1
5	3	-	59	L8	207	1
5	4	-	-	-	204	-
5	5	36	53	M7	201	1
5	6	37	54	N7	198	1
5	7	-	66	M10	195	1
5	8	39	56	K7	192	1
5	9	40	57	N8	189	1
5	10	-	68	N11	186	1
5	11	41	58	M8	183	1
5	12	42	60	K8	180	1
5	13	-	70	L11	177	1
5	14	43	61	N9	174	1
5	15	46	64	K9	171	1
5	16	-	-	-	168	-
5	17	49	69	M11	165	1
5	18	-	-	-	162	-
6	1	-	-	-	159	-
6	2	74	106	C11	156	2
6	3	-	-	-	153	-
6	4	-	111	B11	150	2
6	5	76	110	A12	147	2
6	6	77	112	A11	144	2
6	7	-	-	-	141	-
6	8	78	113	D10	138	2
6	9	79	116	A10	135	2
6	10	-	115	B10	132	2
6	11	80	119	B9	129	2
6	12	81	120	A9	126	2
6	13	-	-	-	123	-
6	14	82	121	D8	120	2
6	15	85	124	A8	117	2
6	16	-	117	D9	114	2
6	17	86	125	B7	111	2
6	18	-	-	-	108	-

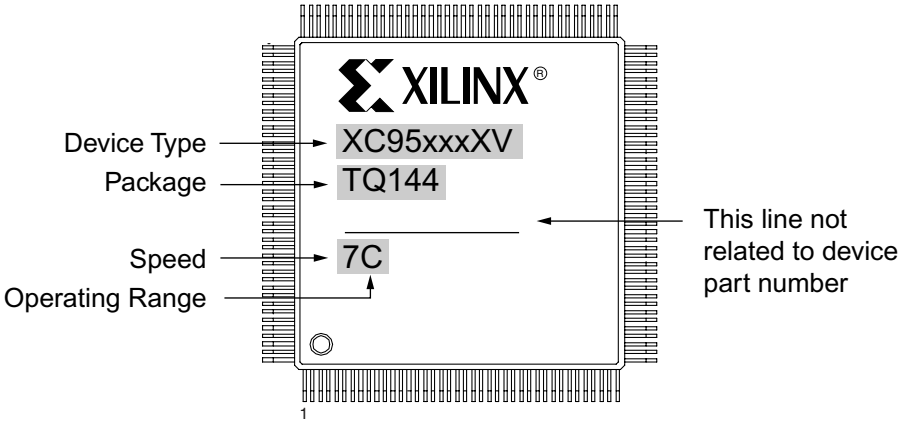
Function Block	Macro-cell	TQ100	TQ144	CS144	BScan Order	Bank
7	1	-	-	-	105	-
7	2	50	71	N12	102	1
7	3	-	75	L12	99	1
7	4	-	-	-	96	-
7	5	52	74	M13	93	1
7	6	53	76	L13	90	1
7	7	-	77	K10	87	1
7	8	54	78	K11	84	1
7	9	55	80	K13	81	1
7	10	-	79	K12	78	1
7	11	56	82	J11	75	1
7	12	58	85	H10	72	1
7	13	-	81	J10	69	1
7	14	59	86	H11	66	1
7	15	60	87	H12	63	1
7	16	-	83	J12	60	1
7	17	61	88	H13	57	1
7	18	-	-	-	54	-
8	1	-	-	-	51	-
8	2	63	91	G11	48	2
8	3	-	95	F11	45	2
8	4	-	97	E13	42	2
8	5	64	92	G10	39	2
8	6	65	93	F13	36	2
8	7	-	-	-	33	-
8	8	66	94	F12	30	2
8	9	67	96	F10	27	2
8	10	-	101	D13	24	2
8	11	68	98	E12	21	2
8	12	70	100	E10	18	2
8	13	-	103	D11	15	2
8	14	71	102	D12	12	2
8	15	72	104	C13	9	2
8	16	-	107	B13	6	2
8	17	73	105	C12	3	2
8	18	-	-	-	0	-

XC95144XV Global, JTAG and Power Pins

Pin Type	TQ100	TQ144	CS144
I/O/GCK1	22	30	K2
I/O/GCK2	23	32	L1
I/O/GCK3	27	38	N2
I/O/GTS1	3	5	D4
I/O/GTS2	4	6	D3
I/O/GTS3	1	2	B1
I/O/GTS4	2	3	C2
I/O/GSR	99	143	A2
TCK	48	67	L10
TDI	45	63	L9
TDO(1)	83	122	C8
TMS	47	65	N10
V_{CCINT} 2.5V	5, 57, 98	8, 42, 84, 141	B3, D1, J13, L4
V_{CCIO1}	26, 38, 51	37, 55, 73	L7, N1, N13
V_{CCIO2}	88	1, 109, 127	A1, A13, C7
GND	21, 31, 44, 62, 69, 75, 84, 100	18, 29, 36, 47, 62, 72, 89, 90, 99, 108, 114, 123, 144	B2, B8, B12, C10, E11, G1, G12, G13, K1, M2, M5, M9, M12
No Connects	-	-	-

Notes:
1. TDO voltage is controlled by V_{CCIO2}.

Device Part Marking and Ordering Combination Information



Sample package with part marking.

Device Ordering and Part Marking Number	Speed (pin-to-pin delay)	Pkg. Symbol	No. of Pins	Package Type	Operating Range(1)
XC95144XV-5TQ100C	5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XV-5TQ144C	5 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XV-5CS144C	5 ns	CS144	144-ball	Chip Scale Package (CSP)	C
XC95144XV-7TQ100C	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XV-7TQ144C	7.5 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	C
XC95144XV-7CS144C	7.5 ns	CS144	144-ball	Chip Scale Package (CSP)	C
XC95144XV-7TQ100I	7.5 ns	TQ100	100-pin	Thin Quad Flat Pack (TQFP)	I
XC95144XV-7TQ144I	7.5 ns	TQ144	144-pin	Thin Quad Flat Pack (TQFP)	I
XC95144XV-7CS144I	7.5 ns	CS144	144-ball	Chip Scale Package (CSP)	I

Notes:
1. C = Commercial: T_A = 0° to +70°C; I = Industrial: T_A = –40° to +85°C
2. Some packages available in Pb-free option. See **Xilinx Packaging** for more information.

Revision History

The following table shows the revision history for this document..

Date	Version	Revision
06/28/00	1.0	Initial Xilinx release. Advance information specification.
01/25/01	2.0	Added -4 performance specifications.Updated I_{CC} vs. Frequency Figure 1.
05/15/01	2.1	Updated I_{CC} formula, Recommended Operation Conditions, -4 and -5 AC Characteristics and Internal Timing Parameters
08/27/01	2.2	Changed V_{CCIO} 3.3V from 3.13 to 3.0 (min), 3.46 to 3.60 (max); DC characteristics: I_{IL} - added "low" current, I_{IH} - changed to "Input leakage high current"; Internal Timing: -5 T_{AOI} from 6.5 to 5.9.
06/20/02	2.3	Updated I_{CC} equation on page 1. Updated Component Availability chart. Changed to Preliminary. Added second test condition and max measurement to I_{IH} DC Characteristics. Added Part Marking Information to Ordering Information. Removed -4 device.
06/25/02	2.4	Fixed Note 1 in XC95144XV Global, JTAG and Power Pins table.
01/08/03	2.5	Corrected link on first page.
06/18/03	2.6	Updated T_{SOL} from 260 to 220ºC. Updated Device Part Marking.
08/21/03	2.7	Updated Package Device Marking Pin 1 orientation.
04/15/05	2.8	Added T_{APRPW} specification to AC Characteristics. Added IOSTANDARD information.
06/25/07	3.0	Notice of discontinuance.