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## NTE4032B & NTE4038B Integrated Circuit CMOS, Triple Serial Logic Adder 16-Lead DIP Type Package

**Description:**

The NTE4032B (Positive Logic) and NTE4038B (Negative Logic) are monolithic integrated circuits consisting of three serial adder circuits with common CLOCK and CARRY-RESET inputs. Each adder has two provisions for two serial DATA INPUT signals and an INVERT command signal. When the command signal is a logical "1", the sum is complemented. Data words enter the adder with the least significant bit first; the sign bit trails. The output is the MOD 2 sum of the input bits plus the carry from the previous bit position. The carry is only added at the positive-going clock transition for the NTE4032B or at the negative-going clock for the NTE4038B, thus, for spike-free operation the input data transitions should occur as soon as possible after the triggering edge. The CARRY is reset to a logical "0" at the end of each word by applying a logical "1" signal to a CARRY-RESET input one-bit-position before the application of the first bit of the next word.

**Features:**

- Inverts Inputs on All Adders for Sum Complementing Applications
- Fully Static Operation: DC to 10Mhz (Typ) at  $V_{DD} = 10V$
- Buffered Inputs and Outputs
- Single-Phase Clocking
- Standardized Symmetrical Output Characteristics
- Quiescent Current Specified to 20V
- 5V, 10V, and 15V Parametric Ratings
- Input Current of 100nA at 18V and +25°C

**Absolute Maximum Ratings:** (Note 1)

Supply Voltage (Voltages Referenced to $V_{SS}$ ), $V_{DD}$ .....	-0.5 to +20V
Input Voltage, $V_I$ .....	-0.5 to $V_{DD}+0.5V$
DC Input Current (Any One Input), $I_I$ .....	$\pm 10mA$
Total Power Dissipation (Per Package), $P_{tot}$ .....	200mW
Device Dissipation (Per Output Transistor)	
For $T_{opr} =$ Full Package Temperature Range .....	100mW
Operating Temperature Range, $T_{opr}$ .....	-55° to +125°C
Storage Temperature Range, $T_{stg}$ .....	-65° to +150°C

Note 1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for external periods may affect device reliability.

**Recommended Operating Conditions:**

Supply Voltage,  $V_{DD}$  ..... 3 to 18V  
 Input Voltage,  $V_I$  ..... 0 to  $V_{DD}$  V  
 Operating Temperature Range,  $T_{opr}$  .....  $-55^{\circ}$  to  $+125^{\circ}$ C

**Static Electrical Characteristics:**

Characteristic	Conditions				Limits at Indicated Temperature ( $^{\circ}$ C)						Units	
	$V_I$ (V)	$V_O$ (V)	$ I_O $ ( $\mu$ A)	$V_{DD}$ (V)	$-55^{\circ}$ C		$+25^{\circ}$ C			$+125^{\circ}$ C		
					Min	Max	Min.	Typ.	Max.	Min		Max
Quiescent Current, $I_L$	0,5	-	-	5	-	5	-	0.04	5.0	-	150	$\mu$ A
	0,10	-	-	10	-	10	-	0.04	10	-	300	$\mu$ A
	0,15	-	-	15	-	20	-	0.04	20	-	600	$\mu$ A
	0,20	-	-	20	-	100	-	0.08	100	-	3000	$\mu$ A
Output High Voltage, $V_{OH}$	0,5	-	< 1	5	4.95	-	4.95	5.0	-	4.95	-	V
	0,10	-	< 1	10	9.95	-	9.95	10	-	9.95	-	V
	0,15	-	< 1	15	14.95	-	14.95	15	-	14.95	-	V
Output Low Voltage, $V_{OL}$	5,0	-	< 1	5	-	0.05	-	-	0.05	-	0.05	V
	10,0	-	< 1	10	-	0.05	-	-	0.05	-	0.05	V
	15,0	-	< 1	15	-	0.05	-	-	0.05	-	0.05	V
Input High Voltage, $V_{IH}$	-	0,5,4,5	< 1	5	3.5	-	3.5	-	-	3.5	-	V
	-	1,9	< 1	10	7.0	-	7.0	-	-	7.0	-	V
	-	1,5,13,5	< 1	15	11.0	-	11.0	-	-	11.0	-	V
Input Low Voltage, $V_{IL}$	-	0,5,4,5	< 1	5	-	1.5	-	-	1.5	-	1.5	V
	-	9,1	< 1	10	-	3.0	-	-	3.0	-	3.0	V
	-	1,5,13,5	< 1	15	-	4.0	-	-	4.0	-	4.0	V
Output Drive Current, $I_{OH}$	0,5	2,5	-	5	-2.0	-	-1.6	-3.2	-	-1.15	-	mA
	0,5	4,6	-	5	-0.64	-	-0.51	-1.0	-	-0.36	-	mA
	0,10	9,5	-	10	-1.6	-	-1.3	-2.6	-	-0.9	-	mA
	0,15	13,5	-	15	-4.2	-	-3.4	-6.8	-	-2.4	-	mA
Output Sink Current, $I_{OL}$	0,5	0,4	-	5	0.64	-	0.51	1.0	-	0.36	-	mA
	0,10	0,5	-	10	1.6	-	1.3	2.6	-	0.9	-	mA
	0,15	1,5	-	15	4.2	-	3.4	6.8	-	2.4	-	mA
Input Current, $I_{IH}, I_{IL}$	0,18	Any Input		18	-	$\pm 0.1$	-	$\pm 10^{-5}$	$\pm 0.1$	-	$\pm 1.0$	$\mu$ A
Input Capacitance, $C_I$	-	Any Input		-	-	-	-	5.0	7.5	-	-	pF

**Dynamic Electrical Characteristics:**

( $T_A = +25^{\circ}$ C,  $C_L = 50$ pF,  $R_L = 200$ k $\Omega$ ,  $t_r$  and  $t_f = 20$ ns, unless otherwise specified)

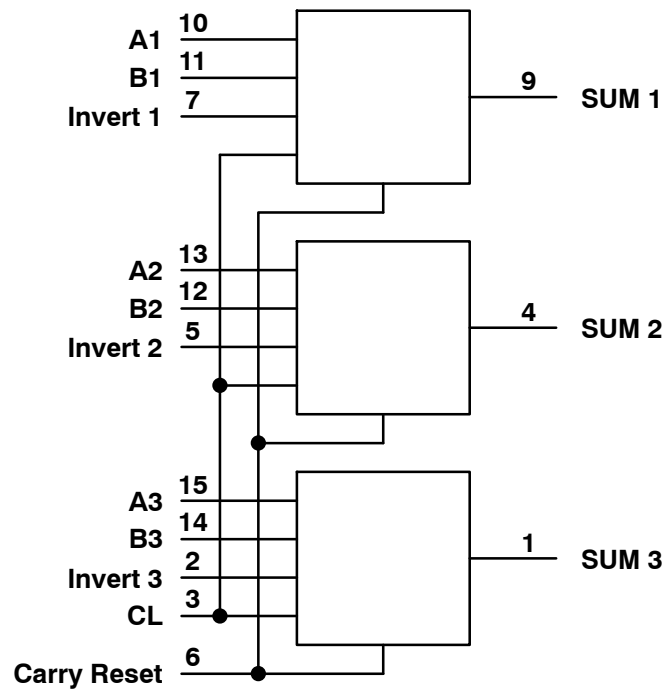
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time A, B, or Inverter Inputs to Sum Outputs	$t_{PHL}$ or $t_{PLH}$	$V_{DD} = 5$ V	-	260	520	ns
		$V_{DD} = 10$ V	-	120	240	ns
		$V_{DD} = 15$ V	-	90	180	ns
Clock Input to Sum Outputs		$V_{DD} = 5$ V	-	325	650	ns
		$V_{DD} = 10$ V	-	175	350	ns
		$V_{DD} = 15$ V	-	150	300	ns

**Dynamic Electrical Characteristics (Cont'd):** ( $T_A = +25^\circ\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}\Omega$ ,  $t_r$  and  $t_f = 20\text{ns}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Transition Time	$t_{\text{THL}}$ or $t_{\text{TLH}}$	$V_{\text{DD}} = 5\text{V}$	–	100	200	ns
		$V_{\text{DD}} = 10\text{V}$	–	50	100	ns
		$V_{\text{DD}} = 15\text{V}$	–	40	80	ns
Data Input Hold Time Clock Edge to A, B, or reset Inputs	$t_{\text{hold}}$	$V_{\text{DD}} = 5\text{V}$	–	120	200	ns
		$V_{\text{DD}} = 10\text{V}$	–	50	80	ns
		$V_{\text{DD}} = 15\text{V}$	–	40	60	ns
Maximum Clock Input Frequency	$f_{\text{max}}$	$V_{\text{DD}} = 5\text{V}$	2.5	4.5	–	MHz
		$V_{\text{DD}} = 10\text{V}$	5.0	10.0	–	MHz
		$V_{\text{DD}} = 15\text{V}$	7.5	15.0	–	MHz
Clock Input Rise or Fall Time (Note 2)	$t_r$ , $t_f$	$V_{\text{DD}} = 5\text{V}$	–	–	500	ns
		$V_{\text{DD}} = 10\text{V}$	–	–	500	ns
		$V_{\text{DD}} = 15\text{V}$	–	–	500	ns

Note 2. If more than one unit is cascaded,  $t_r$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving state for the estimated capacitive load.

### Functional Diagram



### Pin Connection Diagram

