QUALITY SEMICONDUCTOR, INC.

High Speed CMOS 16-Bit Registers (3-State)

QS74FCT16374T
QS74FCT162374T

ADVANCE INFORMATION

FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <1μW typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5ns $t_{SK(O)}$
- Flow-through pinout for easy layout
- Power off disable allows hot plugging
- Industrial temperature: –40°C to +85°C
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- Std., A, and C speed grades: 5.2ns t_{PD} for C

FCT16374T

- High drive standard FCT-T outputs: I_{OL} = +64mA, I_{OH} = –32mA
- Incident switching for driving buses and large loads

FCT162374T

- Balanced output drivers: ±24mA
- Reduced switching noise for point to point signals

DESCRIPTION

The FCT16374 family of products are 16-bit buffered registers with three-state outputs that are ideal for driving address and data buses. The output enable (x$\overline{OE}$) and clock (xCLK) controls are organized to operate each device as two 8-bit registers, or one 16-bit register with common clock. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01) and many power and ground pins provide low ground bounce. To accommodate hot-plug or live insertion applications, both versions of this product were designed not to load an active bus when V_{CC} is removed. In applications where bus signals are point-to-point or driving light capacitance loads, the balanced drive FCT162374 is recommended.

Figure 1. Functional Block Diagram

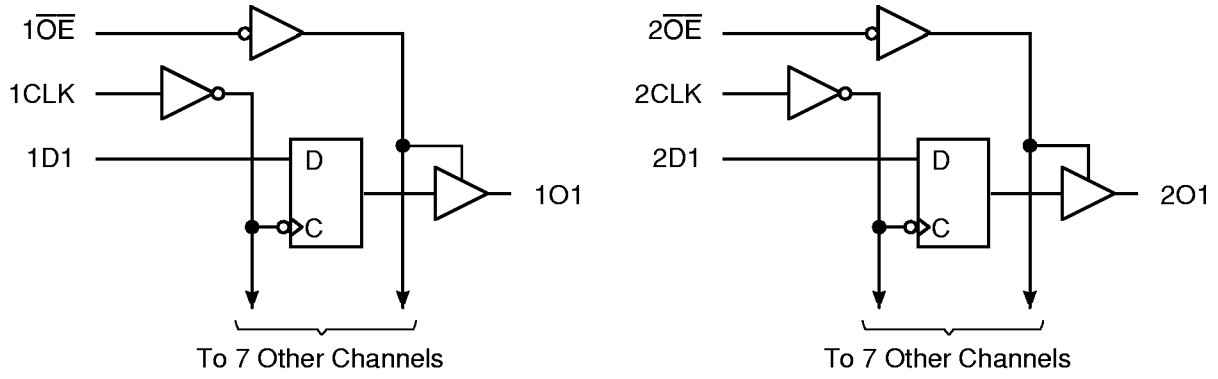

Figure 2. Pin Configuration
(All Pins Top View)

SSOP, TSSOP

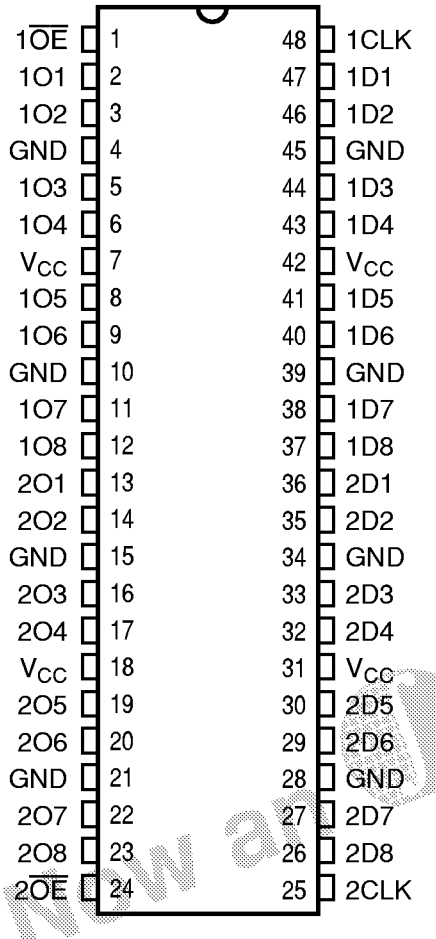

Table 1. Pin Description

Name	I/O	Description
xDx	I	Data Inputs
xOx	O	Data Outputs
xCLK	I	Clock Input
$x\overline{OE}$	I	Output Enable

Table 2. Function Table

Inputs $x\overline{OE}$	Inputs xCLK	Inputs xDx	Internal Q Value	Outputs xOx	Function
H	X	X	X	Hi-Z	Disable Outputs
L	↑	L	L	L	Load Input Data
L	↑	H	H	H	Enable Outputs
H	↑	L	L	Hi-Z	Load Input Data
H	↑	H	H	Hi-Z	Disable Outputs

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	Typ	Max	Unit
All	6.0	9.0	pF

Note: Capacitance is characterized but not tested.

Table 4. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Diode Current with $V_{OUT} < 0$	–50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	1.0 watts
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}	Input Voltage	–0.5	5.5	V
V_{OUT}	Voltage Applied to Output or I/O	0	V_{CC}	V
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
T_A	Operating Free Air Tempeature	–40	+85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise noted.

Symbol	Parameter	Test Conditions[1]	Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs[4]	—	100	—	mV
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{OUT} \le V_{CC}$	—	—	1	µA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND[3,4]	–80	–140	–225	mA
V_{IK}	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18mA	–	–0.7	–1.2	V

Notes:
1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
3. Not more than one output should be tested at one time. Duration of test should not exceed one second.
4. These parameters are guaranteed by design but not tested.

Table 7. Output Drive Characteristics for FCT16374T

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
I_O	Output Drive Current	V_{CC} = Max, V_{OUT} = 2.5V[3]		–50	—	–180	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –3mA	2.5	—	—	V
		V_{IN} = V_{IH} or VIL	I_{OH} = –15mA	2.4	—	—	V
			I_{OH} = –32mA[4]	2.0	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		—	—	±1.0	µA

Table 8. Output Drive Characteristics for FCT162374T

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		60	115	200	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V[3]		–60	–115	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.55	V

Notes:
1. For conditions shown as Min. or Max. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
3. Not more than one output should be shorted and the duration is ≤1 second.
4. Duration of the condition should not exceed one second.

Table 9. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ[2]	Max	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., Freq = 0 V_{IN} = GND or V_{CC}		5	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		0.5	1.5	mA
Q_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open One Bit Toggling @ 50% Duty Cycle x$\overline{OE}$ = GND		60	100	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open One Bit Toggling @ 50% Duty Cycle x$\overline{OE}$ = GND, f_i = 10MHz	V_{IN} = V_{CC} V_{IN} = GND	0.6	1.5	mA
			V_{IN} = 3.4V V_{IN} = GND	0.9	2.3	mA
		V_{CC} = Max., Outputs Open Sixteen Bits Toggling @ 50% Duty Cycle x$\overline{OE}$ = GND, f_i = 2.5MHz	V_{IN} = V_{CC} V_{IN} = GND	2.4	4.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND	6.4	16.5[5]	mA

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All Other Inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} = I_{DYNAMIC}$.
   $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$.
   I_{CCQ} = Quiescent Current (I_{CCL}, I_{CCH}, and I_{CCZ}).
   ΔI_{CC} = Power Supply Current for a TTL-High Input (V_{IN} = 3.4V).
   D_H = Duty Cycle for TTL High Inputs.
   N_T = Number of TTL High Inputs.
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f_{CP} = Clock Frequency for Register devices (Zero for Non-Register Devices).
   N_{CP} = Number of Clock Inputs at f_{CP}.
   f_i = Input Frequency.
   N_i = Number of Inputs at f_i.

Table 10. Switching Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise specified.
C_{LOAD} = 50pF, R_{LOAD} = 500Ω unless otherwise noted.

Symbol	Description[1]	FCT16374T FCT162374T		FCT16374AT FCT162374AT		FCT16374CT FCT162374CT		Unit
		Min	Max	Min	Max	Min	Max	
t_{PHL} t_{PLH}	Propagation Delay xCLK to xOx	2.0	10	2.0	6.5	2.0	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xOx	1.5	12.5	1.5	6.5	1.5	5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time[2] x$\overline{OE}$ to xOx	1.5	8	1.5	5.5	1.5	5	ns
t_S	Data Setup Time xDx to xCLK	2.0	—	2.0	—	2.0	—	ns
t_H	Data Hold Time xDx to xCLK	1.5	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width HIGH or LOW	7.0	—	5.0	—	5.0	—	ns
$t_{SK(O)}$	Output Skew[3]	—	0.5	—	0.5	—	0.5	ns

Notes:
1. Minimums guaranteed but not tested on propagation delays. See Test Circuit and Waveforms.
2. Guaranteed by design, but not tested.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design but not tested.