

HALOGEN FREE



Improved Quad SPST CMOS Analog Switches

DESCRIPTION

The DG444B, DG445B are monolithic quad analog switches designed to provide high speed, low error switching of analog and audio signals. The DG444B, DG445B are upgrades to the original DG444, DG445.

Combing low on-resistance (45 Ω , typ.) with high speed (t_{ON} 120 ns, typ.), the DG444B, DG445B are ideally suited for Data Acquisition, Communication Systems, Automatic Test Equipment, or Medical Instrumentation. Charge injection has been minimized on the drain for use in sample-and-hold circuits.

The DG444B, DG445B are built using Vishay Siliconix's high-voltage silicon-gate process. An epitaxial layer prevents

When on, each switch conducts equally well in both directions and blocks input voltages to the supply levels when off.

FEATURES

- Low On-Resistance: 45 W
- Low Power Consumption: 1 mW
- Fast Switching Action t_{ON}: 120 ns
- Low Charge Injection
- TTL/CMOS-Compatible Logic
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

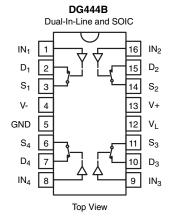
BENEFITS

- Low Signal Errors and Distortion
- Reduced Power Supply Consumption
- Faster Throughput
- Reduced Pedestal Errors
- Simple Interfacing

APPLICATIONS

- Audio Switching
- **Data Acquisition**
- Sample-and-Hold Circuits
- Communication Systems
- Automatic Test Equipment
- Medical Instruments

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



	DG444B	
	QFN16 (4 x 4 mm)	
	D_1 IN_1 IN_2 D_2	
	16 15 14 13	
	• TŢŢT	
S ₁	112	S ₂
V-	2 11	V+
GND	3 10	V_{L}
S_4	4-4-9	S_3
	5 6 7 8	
	D ₄ IN ₄ IN ₃ D ₃	
	Top View	

TRUTH TABLE								
Logic	DG444B	DG445B						
0	ON	OFF						
1	OFF	ON						

Logic "0" ≤ 0.8 V Logic "1" ≥ 2.4 V

ORDERING INFORMATION									
Temp Range	Package	Part Number							
		DG444BDJ							
	16-pin Plastic DIP	DG444BDJ-E3							
	10-pii11 lastic Dii	DG445BDJ							
		DG445BDJ-E3							
- 40 °C to 85 °C	16-pin Narrow SOIC	DG444BDY-E3							
40 0 10 05 0		DG444BDY-T1-E3							
	10-piii Nariow 3010	DG445BDY-E3							
		DG445BDY-T1-E3							
	16 pin QFN 4 x 4 mm	DG444BDN-T1-E4							
	(Variation 1)	DG445BDN-T1-E4							

DG444B, DG445B

Vishay Siliconix



ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)								
Parameter		Symbol	Limit	Unit				
V+ to V-			44					
GND to V-			25	1				
V _L			(GND - 0.3 V) to (V+) + 0.3 V	V				
Digital Inputs ^a , V _S , V _D			(V-) - 2 to (V+) + 2 or 30 mA, whichever occurs first					
Continuous Current (Any Termin	nuous Current (Any Terminal)		30	mΛ				
Current, S or D (Pulsed at 1 ms,	10 % duty cycle)		100	mA				
Storage Temperature			- 65 to 125	°C				
	16-pin Plastic DIP ^c		470					
Power Dissipation (Package) ^b	16-pin Narrow Body SOIC ^d		640	mW				
	QFN-16		850	1				

Notes: a. Signals on S_X , D_X , or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 6 mW/°C above 75 °C.

d. Derate 8 mW/°C above 75 °C.



SPECIFICATIONS (for du		Test Conditions			Limits		
		Unless Otherwise Specified V+ = 15 V, V- = - 15 V		- 40 °C to 85 °C			=
Parameter	Symbol	$V_L = 5 \text{ V}, V_{IN} = 2.4 \text{ V}, 0.8 \text{ V}^e$	Temp.a	Min.b	Typ. ^c	Max.b	Unit
Analog Switch					l	•	
Analog Signal Range ^d	V _{ANALOG}		Full	- 15		15	V
Drain-Source On-Resistance	R _{DS(on)}	$I_S = 1 \text{ mA}, V_D = \pm 10 \text{ V}$	Room Full		45	80 95	Ω
Switch Off Leakage Current	I _{S(off)}	$V_D = \pm 14 \text{ V}, V_S = \pm 14 \text{ V}$	Room Full	- 0.5 - 5	± 0.01	0.5 5	
Owner on Leakage ourient	I _{D(off)}	D-111, V, VS-111V	Room Full	- 0.5 - 5	± 0.01	0.5 5	nA
Channel On Leakage Current	I _{D(on)}	$V_S = V_D = \pm 14 \text{ V}$	Room Full	- 0.5 - 10	± 0.02	0.5 10	
Digital Control							
Input Voltage Low	V _{INL}		Full			0.8	V
Input Voltage High	V _{INH}		Full	2.4			V
Input Current V _{IN} Low	I _{INL}	V _{IN} under test = 0.8 V All Other = 2.4 V	Full	- 1	- 0.01	1	μА
Input Current V _{IN} High	I _{INH}	V _{IN} under test = 2.4 V All Other = 0.8 V	Full	- 1	0.01	1	μι
Dynamic Characteristics							
Turn-On Time	t _{ON}	$R_L = 1 \text{ k}\Omega, C_L = 35 \text{ pF}$	Room			300	ns
Turn-Off Time	t _{OFF}	$V_S = \pm 10 \text{ V}$, See Figure 2	Room			200	113
Charge Injection ^e	Q	$C_L = 1 \text{ nF, } V_S = 0 \text{ V}$ $V_{gen} = 0 \text{ V, } R_{gen} = 0 \Omega$	Room		1		рС
Off Isolation ^e	OIRR	$R_L = 50 \Omega$, $C_L = 15 pF$	Room		- 90		dB
Crosstalk (Channel-to-Channel) ^d	X _{TALK}	$V_S = 1 V_{RMS}$, $f = 100 kHz$	Room		- 95		uБ
Source Off Capacitance	C _{S(off)}	V _S = 0 V, f = 100 kHz	Room		5		
Drain Off Capacitance	C _{D(off)}	-	Room		5		pF
Channel On Capacitance	C _{D(on)}	$V_S = V_D = 0 V$, $f = 1 MHz$	Room		16		
Power Supplies							
Positive Supply Current	l+		Room Full			1 5	
Negative Supply Current	l-	$V_{IN} = 0 V \text{ or } 5 V$	Room Full	- 1 - 5			μΑ
Logic Supply Current	I _{IN}		Room Full			1 5	



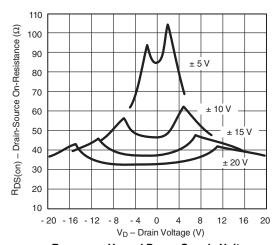
SPECIFICATIONS (for unipolar supplies)									
		Test Conditions Unless Otherwise Specified		D Suffix - 40 °C to 85 °C					
		V + = 12 V, V - = 0 V							
Parameter	Symbol	$V_L = 5 \text{ V}, V_{IN} = 2.4 \text{ V}, 0.8 \text{ V}^e$	Temp. ^a	Min. ^b	Typ. ^c	Max.b	Unit		
Analog Switch									
Analog Signal Range ^d	V _{ANALOG}		Full	0		12	V		
Drain-Source	D	I _S = 1 mA, V _D = 3 V, 8 V			90	160	0		
On-Resistance ^d	R _{DS(on)}					200	Ω		
Dynamic Characteristics									
Turn-On Time	t _{ON}	$R_L = 1 \text{ k}\Omega$, $C_L = 35 \text{ pF}$, $V_S = 8 \text{ V}$	Room		120	300	no		
Turn-Off Time	t _{OFF}	See Figure 2	Room		60	200	ns		
Charge Injection	Q	$C_L = 1 \text{ nF, } V_{gen} = 6 \text{ V, } R_{gen} = 0 \Omega$	Room		4		рC		
Power Supplies	•					1	ı		
Positive Supply Current	l+		Room			1			
1 ositive ouppry ourient	17	$V_{IN} = 0 \text{ or } 5 \text{ V}$	Full			5			
Negative Supply Current	I-		Room	- 1			μΑ		
gaara capp., curron			Full	- 5			, r.,		
Logic Supply Current	I _{IN}	$V_1 = 5.25 \text{ V}, V_{IN} = 0 \text{ or } 5 \text{ V}$	Room			1			
9	TIN	L, - IIV	Full			5			

Notes:

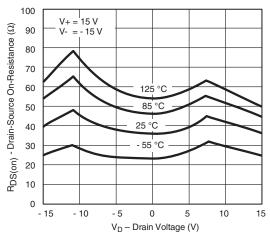
- a. Room = 25 °C, Full = as determined by the operating temperature suffix.
- b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. Guaranteed by design, not subject to production test.
- e. V_{IN} = input voltage to perform proper function.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



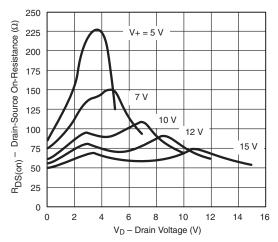
 $R_{DS(on)}$ vs. V_D and Power Supply Voltages



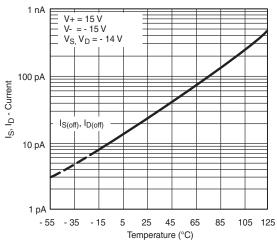
 $R_{DS(on)} \ vs. \ V_D$ and Temperature



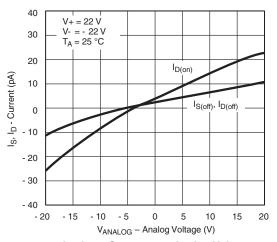
TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



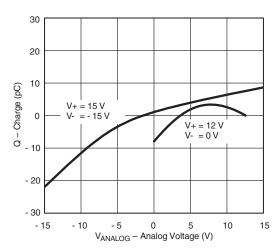
 $\mathbf{R}_{\mathrm{DS(on)}}$ vs. \mathbf{V}_{D} and Single Power Supply Voltages



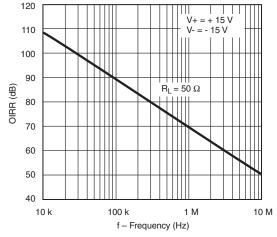
Leakage Current vs. Temperature



Leakage Currents vs. Analog Voltage

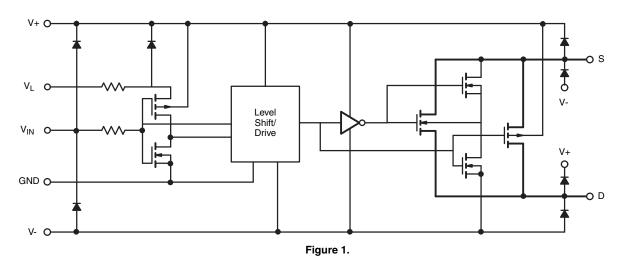


Q_S, Q_D - Charge Injection vs. Analog Voltage

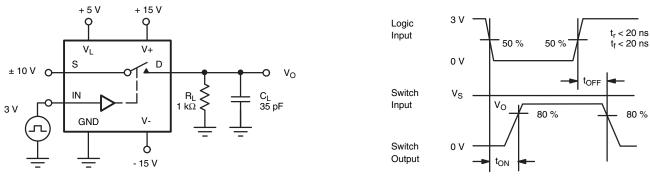


Off Isolation vs. Frequency

SCHEMATIC DIAGRAM (typical channel)



TEST CIRCUITS



C_L (includes fixture and stray capacitance)

Note: Logic input waveform is inverted for DG445.

Figure 2. Switching Time

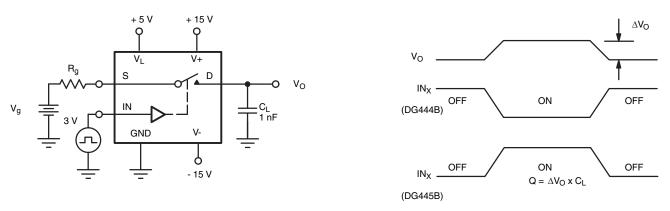


Figure 3. Charge Injection



TEST CIRCUITS

C = 1 mF tantalum in parallel with 0.01 mF ceramic

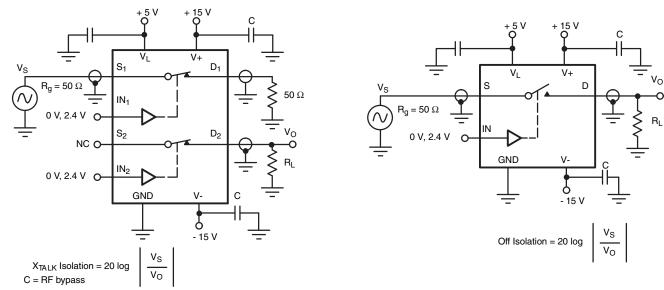


Figure 4. Crosstalk

Figure 5. Off Isolation

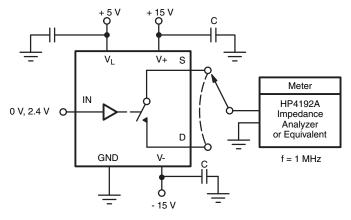


Figure 6. Source/Drain Capacitances

APPLICATIONS

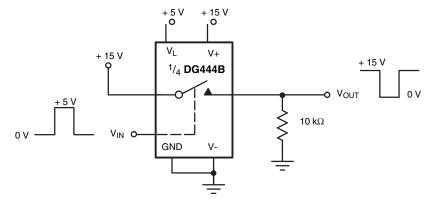


Figure 7. Level Shifter



APPLICATIONS

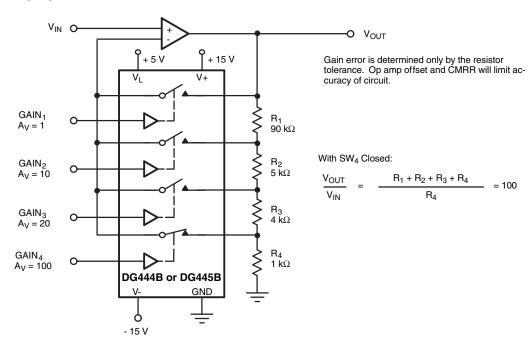


Figure 8. Precision-Weighted Resistor Programmable-Gain Amplifier

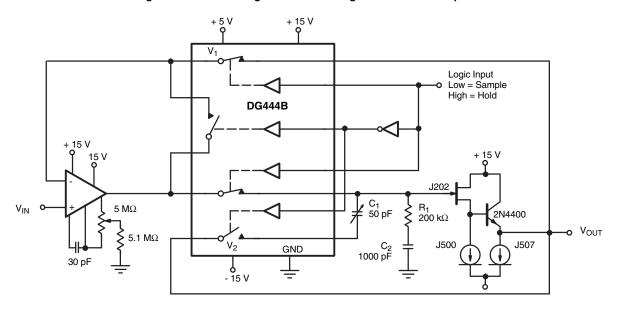


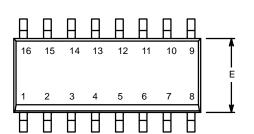
Figure 9. Precision Sample-and-Hold

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?72626.





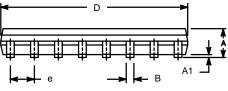
SOIC (NARROW): 16-LEAD JEDEC Part Number: MS-012

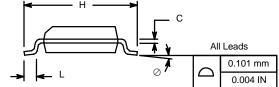


	MILLIN	IETERS	INCHES							
Dim	Min	Max	Min	Max						
Α	1.35	1.75	0.053	0.069						
A ₁	0.10	0.20	0.004	0.008						
В	0.38	0.51	0.015	0.020						
С	0.18	0.23	0.007	0.009						
D	9.80	10.00	0.385	0.393						
E	3.80	4.00	0.149	0.157						
е	1.27	BSC	0.050	BSC						
H 5.80		6.20	0.228	0.244						
L	0.50	0.93	0.020	0.037						
0	0°	0° 8°		8°						
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ECN: S-03946-Rev. F, 09-Jul-01

DWG: 5300

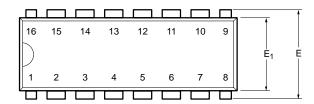


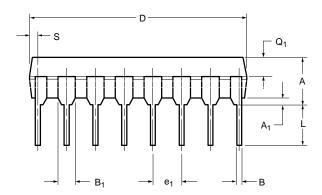


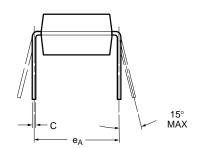
www.vishay.com 02-Jul-01



PDIP: 16-LEAD



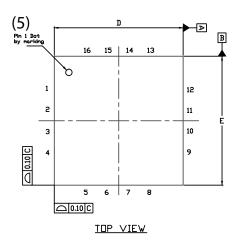


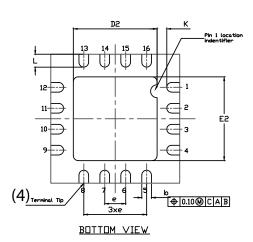


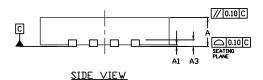
	MILLIN	IETERS	INC	HES				
Dim	Min	Max	Min	Max				
Α	3.81	5.08	0.150	0.200				
A ₁	0.38	1.27	0.015	0.050				
В	0.38	0.51	0.015	0.020				
B ₁	0.89	1.65	0.035	0.065				
С	0.20	0.30	0.008	0.012				
D	18.93	21.33	0.745	0.840				
Е	7.62	8.26	0.300	0.325				
E ₁	5.59	7.11	0.220	0.280				
e ₁	2.29	2.79	0.090	0.110				
e _A	7.37	7.87	0.290	0.310				
L	2.79	3.81	0.110	0.150				
Q_1	1.27	2.03	0.050	0.080				
S	0.38	1.52	.015	0.060				
ECN: S-03946—Rev. D, 09-Jul-01								

Document Number: 71261 www.vishay.com 06-Jul-01 1

QFN 4x4-16L Case Outline







	VARIATION 1					VARIATION 2						
DIM	МІ	MILLIMETERS ⁽¹⁾		INCHES		МІ	MILLIMETERS ⁽¹⁾		INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α	0.75	0.85	0.95	0.029	0.033	0.037	0.75	0.85	0.95	0.029	0.033	0.037
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
A3		0.20 ref.			0.008 ref.		0.20 ref.				0.008 ref.	
b	0.25	0.30	0.35	0.010	0.012	0.014	0.25	0.30	0.35	0.010	0.012	0.014
D		4.00 BS0	1.00 BSC 0.157 BSC 4.00 BSC			0.157 BSC						
D2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
е		0.65 BS0)		0.026 BSC		0.65 BSC 0.026 BSC					
E	4.00 BSC)	0.157 BS				4.00 BSC			0.157 BSC	
E2	2.0	2.1	2.2	0.079	0.083	0.087	2.5	2.6	2.7	0.098	0.102	0.106
K		0.20 min.			0.008 min.			0.20 min.			0.008 min.	
L	0.5	0.6	0.7	0.020	0.024	0.028	0.3	0.4	0.5	0.012	0.016	0.020
N ⁽³⁾		16		16		16		16				
Nd ⁽³⁾		4		4		4		4				
Ne ⁽³⁾		4			4		4			4		

Notes

- (1) Use millimeters as the primary measurement.
- (2) Dimensioning and tolerances conform to ASME Y14.5M. 1994.
- (3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.
- (4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.
- (5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.
- (6) Package warpage max. 0.05 mm.

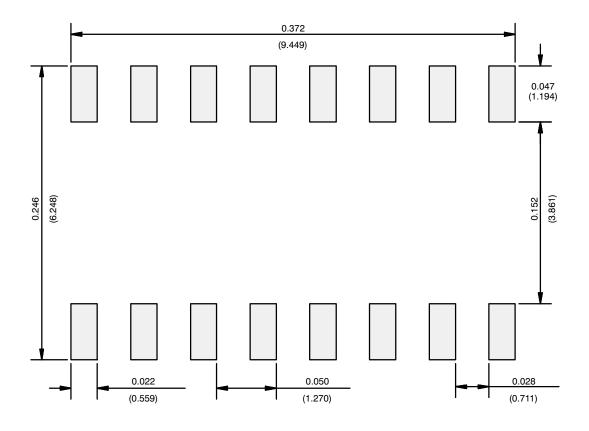
ECN: S13-0893-Rev. B, 22-Apr-13

DWG: 5890

Revision: 22-Apr-13



RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads Dimensions in Inches/(mm)

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