HARRIS

RFM8N18L/20L
RFP8N18L/20L

N-Channel Logic Level Power Field-Effect Transistors (L^2FET)

August 1991

Features

- 8A, 180V and 200V
- $r_{DS(ON)} = 0.5\Omega$
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from QMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power-Dissipation Limited
- Nanoscecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

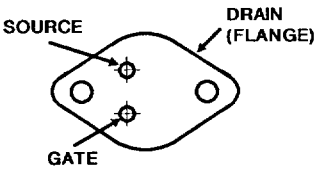
Description

The RFM8N18L and RFM8N20L and the RFP8N18L and RFP8N20L are N-channel enhancmement-mode silicon-gate power field-effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V - 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

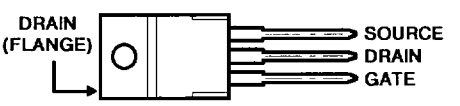
The RFM series types are supplied in the JEDEC TO-204AA steel package and the RFP series types in the JEDEC TO-220AB plastic package.

Package

TO-204AA
BOTTOM VIEW

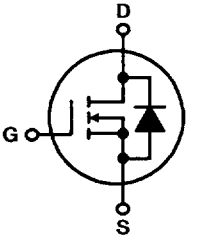


TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

	RFM8N18L	RFM8N20L	RFP8N18L	RFP8N20L	UNITS
Drain-Source Voltage ..... V_{DS}	180	200	180	200	V
Drain-Gate Voltage (R_{GS} = 1MΩ) ..... V_{DGR}	180	200	180	200	V
Continuous Drain Current					
RMS Continuous ..... I_D	8	8	8	8	A
Pulsed Drain Current ..... I_{DM}	20	20	20	20	A
Gate-Source Voltage ..... V_{GS}	±10	±10	±10	±10	V
Maximum Power Dissipation					
T_C = +25°C ..... P_D	75	75	60	60	W
Above T_C = +25°C, Derate Linearly	0.6	0.6	0.48	0.48	W/°C
Operating and Storage Junction Temperature Range ..... TJ, TSTG	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **1514.1**

ELECTRICAL CHARACTERISTICS, *At Case Temperature (T_C)=25° C unless otherwise specified.*

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Drain-Source Breakdown Voltage	BV_{DDS}	I_D=1 mA V_{GS}=0	180	—	200	—	V
Gate Threshold Voltage	$V_{GS}(th)$	V_{GS}=V_{DS} I_D=1 mA	1	2	1	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=145 V V_{DS}=160 V	— —	1 —	— —	— 1	μA
		T_C=125° C V_{DS}=145 V V_{DS}=160 V	— —	50 —	— —	— 50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±10 V V_{DS}=0	—	100	—	100	nA
Drain-Source On Voltage	$V_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	2.0	—	2.0	V
		I_D=8 A V_{GS}=5 V	—	4.6	—	4.6	V
Static Drain-Source On Resistance	$r_{DS}(on)$[a]	I_D=4 A V_{GS}=5 V	—	0.5	—	0.6	Ω
Forward Transconductance	g_{fs}[a]	V_{DS}=10 V I_D=4 A	3.0	—	3.0	—	mho
Input Capacitance	C_{iss}	V_{DS}=25 V V_{GS}=0 V f=1MHz	—	900	—	900	pF
Output Capacitance	C_{oss}		—	250	—	250	pF
Reverse-Transfer Capacitance	C_{rss}		—	120	—	120	pF
Turn-On Delay Time	$t_d(on)$	V_{DD}=50 V I_D=4A R_{gen}=∞ R_{gs}=6.25 Ω V_{GS}=5 V	15(typ)	45	15(typ)	45	ns
Rise Time	t_r		45(typ)	150	45(typ)	150	ns
Turn-Off Delay Time	$t_d(off)$		100(typ)	135	100(typ)	135	ns
Fall Time	t_f		60(typ)	105	60(typ)	105	ns
Thermal Resistance Junction-to-Case	$R\theta_{JC}$	RFM8N18L, RFM8N20L	—	1.67	—	1.67	°C/W
		RFP8N18L, RFP8N20L	—	2.083	—	2.083	°C/W

[a]Pulsed: Pulse duration = 300 μs max., duty cycle = 2%.

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS				UNITS
			RFM8N18L RFP8N18L		RFM8N20L RFP8N20L		
			MIN.	MAX.	MIN.	MAX.	
Diode Forward Voltage	V_{SD}	I_{SD}=4 A	—	1.4	—	1.4	V
Reverse Recovery Time	t_{rr}	I_F=4 A d_{IF}/d_t=100 A/μs	250(typ)		250(typ)		ns

*Pulse Test: Width ≤ 300 μs, duty cycle ≤ 2%.

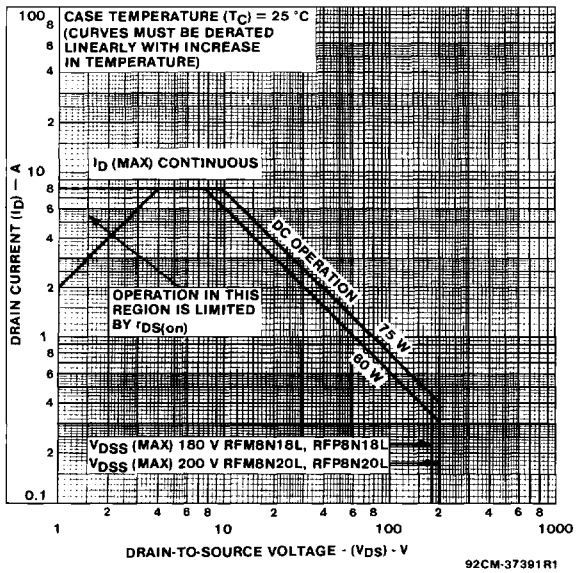


Fig. 1 — Maximum safe operating areas for all types.

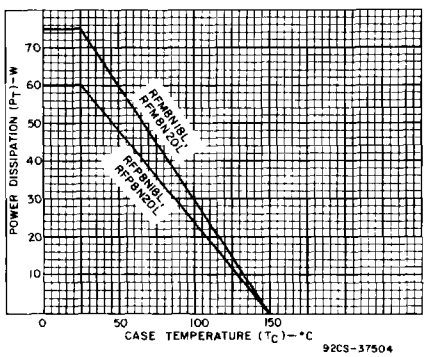


Fig. 2 — Power vs. temperature derating curve for all types.

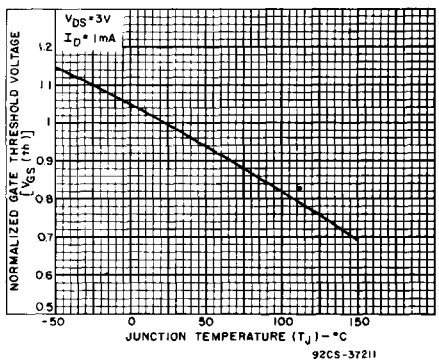


Fig. 3 — Typical normalized gate threshold voltage as a function of junction temperature for all types.

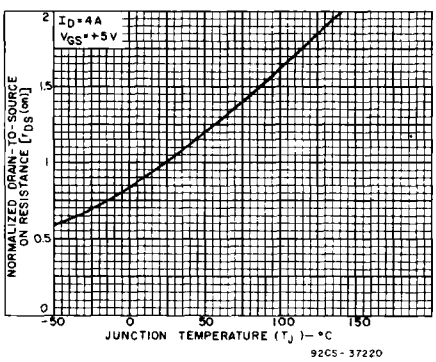


Fig. 4 — Normalized drain-to-source on resistance to junction temperature for all types.

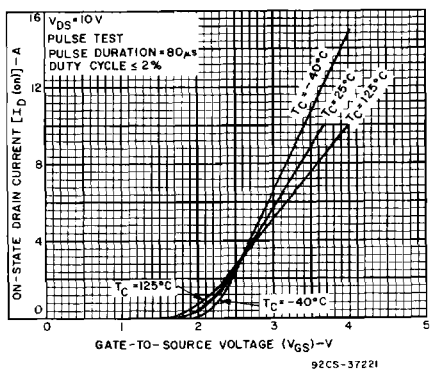


Fig. 5 — Typical transfer characteristics for all types.

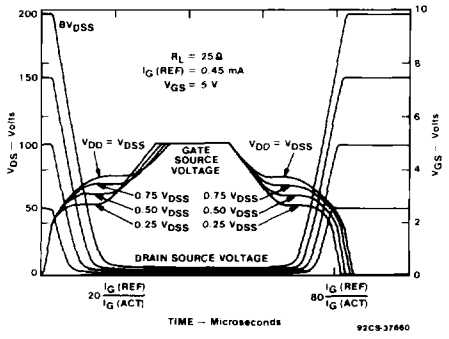


Fig. 6 - Normalized switching waveforms for constant gate-current. Refer to Harris application notes AN7254 and AN-7260.

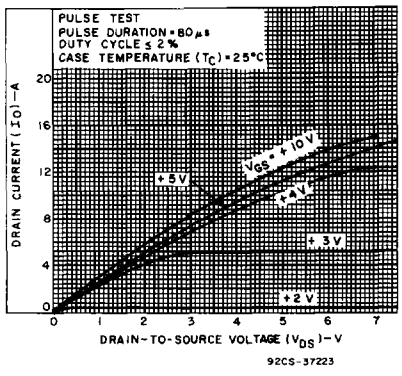


Fig. 7 — Typical saturation characteristics for all types.

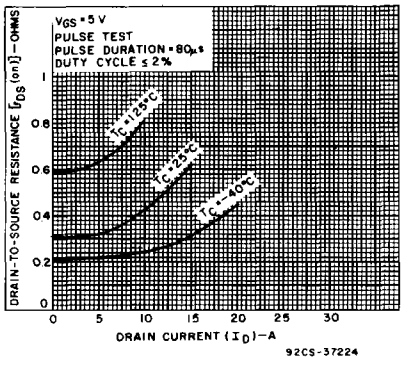


Fig. 8 — Typical drain-to-source on resistance as a function of drain current for all types.

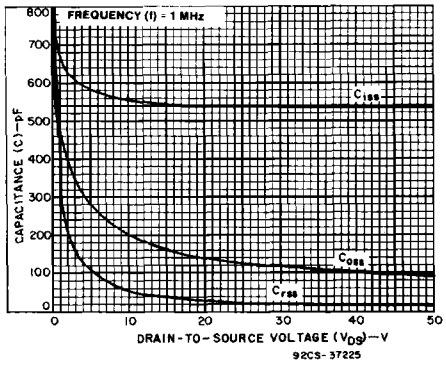


Fig. 9 — Capacitance as a function of drain-to-source voltage for all types.

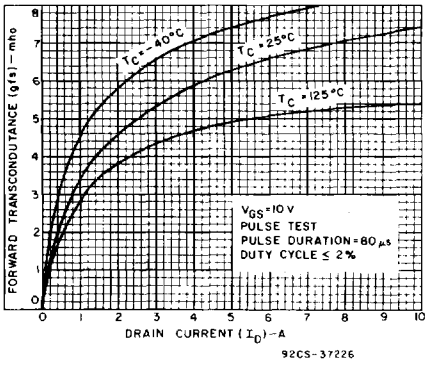


Fig. 10 — Typical forward transconductance as a function of drain current for all types.

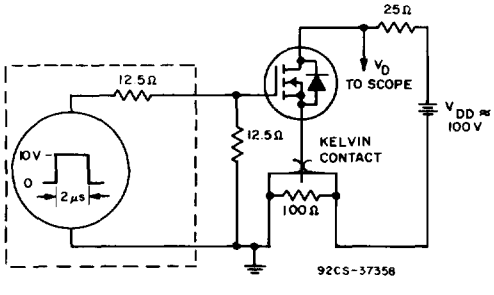


Fig. 11 — Switching Time Test Circuit.