To our customers,

## Old Company Name in Catalogs and Other Documents

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Renesas Electronics Corporation

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RENESAS

## 72M-BIT DDR II+ SRAM
## 2.0 & 2.5 CLOCK CYCLES READ LATENCY
## 2-WORD BURST OPERATION

### Description

The $\mu$PD44646092A-A and $\mu$PD44646093A-A are 8,388,608-word by 9-bit, the $\mu$PD44646182A-A and $\mu$PD44646183A-A are 4,194,304-word by 18-bit and the $\mu$PD44646362A-A and $\mu$PD44646363A-A are 2,097,152-word by 36-bit synchronous double data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The $\mu$PD44646xx2A-A is for 2.0 clock cycles and the $\mu$PD44646xx3A-A is for 2.5 clock cycles read latency. The $\mu$PD44646092A-A, $\mu$PD44646093A-A, $\mu$PD44646182A-A, $\mu$PD44646183A-A, $\mu$PD44646362A-A and $\mu$PD44646363A-A integrate unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and K#) are latched on the positive edge of K and K#.

These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

These products are packaged in 165-pin PLASTIC BGA.

### Features

- 1.8 ± 0.1 V power supply
- 165-pin PLASTIC BGA (15 x 17)
- HSTL interface
- DLL/PLL circuitry for wide output data valid window and future frequency scaling
- Pipelined double data rate operation
- Common data input/output bus
- Two-tick burst for low DDR transaction size
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two Echo clocks (CQ and CQ#)
- Data Valid pin (QVLD) supported
- Read latency : 2.0 & 2.5 clock cycles (Not selectable by user)
- Internally self-timed write control
- Clock-stop capability.  Normal operation is restored in 20 $\mu$s after clock is resumed.
- User programmable impedance output (35 to 70 $\Omega$)
- Fast clock cycle time : 2.5 ns (400 MHz) for 2.0 clock cycles read latency,
           2.0 ns (500 MHz) for 2.5 clock cycles read latency
- Simple control logic for easy depth expansion
- JTAG 1149.1 compatible test access port
- On-Die Termination (ODT) for better signal quality (Selectable ON/OFF by user)

## Ordering Information

### 2.0 Clock Cycles Read Latency

| Part number | Cycle Time ns | Clock Frequency MHz | Organization (word x bit) | Core Supply Voltage V | I/O Interface | Package |
|---|---|---|---|---|---|---|
| $\mu$PD44646092AF5-E25-FQ1-A [Note] | 2.5 | 400 | 8M x 9 | 1.8 ± 0.1 | HSTL | 165-pin PLASTIC BGA (15 x 17) Lead-free |
| $\mu$PD44646092AF5-E30-FQ1-A | 3.0 | 333 | | | | |
| $\mu$PD44646092AF5-E33-FQ1-A | 3.3 | 300 | | | | |
| $\mu$PD44646182AF5-E25-FQ1-A [Note] | 2.5 | 400 | 4M x 18 | | | |
| $\mu$PD44646182AF5-E30-FQ1-A | 3.0 | 333 | | | | |
| $\mu$PD44646182AF5-E33-FQ1-A | 3.3 | 300 | | | | |
| $\mu$PD44646362AF5-E25-FQ1-A [Note] | 2.5 | 400 | 2M x 36 | | | |
| $\mu$PD44646362AF5-E30-FQ1-A | 3.0 | 333 | | | | |
| $\mu$PD44646362AF5-E33-FQ1-A | 3.3 | 300 | | | | |

**Note** Please contact our sales.

### 2.5 Clock Cycles Read Latency

| Part number | Cycle Time ns | Clock Frequency MHz | Organization (word x bit) | Core Supply Voltage V | I/O Interface | Package |
|---|---|---|---|---|---|---|
| $\mu$PD44646093AF5-E20-FQ1-A [Note] | 2.0 | 500 | 8M x 9 | 1.8 ± 0.1 | HSTL | 165-pin PLASTIC BGA (15 x 17) Lead-free |
| $\mu$PD44646093AF5-E22-FQ1-A | 2.2 | 450 | | | | |
| $\mu$PD44646093AF5-E25-FQ1-A | 2.5 | 400 | | | | |
| $\mu$PD44646093AF5-E30-FQ1-A | 3.0 | 333 | | | | |
| $\mu$PD44646183AF5-E20-FQ1-A [Note] | 2.0 | 500 | 4M x 18 | | | |
| $\mu$PD44646183AF5-E22-FQ1-A | 2.2 | 450 | | | | |
| $\mu$PD44646183AF5-E25-FQ1-A | 2.5 | 400 | | | | |
| $\mu$PD44646183AF5-E30-FQ1-A | 3.0 | 333 | | | | |
| $\mu$PD44646363AF5-E20-FQ1-A [Note] | 2.0 | 500 | 2M x 36 | | | |
| $\mu$PD44646363AF5-E22-FQ1-A | 2.2 | 450 | | | | |
| $\mu$PD44646363AF5-E25-FQ1-A | 2.5 | 400 | | | | |
| $\mu$PD44646363AF5-E30-FQ1-A | 3.0 | 333 | | | | |

**Note** Please contact our sales.

**Feature Differences between DDR II and DDR II+**

| Features | DDR II | DDR II+ | Note |
|---|---|---|---|
| Frequency (DLL/PLL ON) | 200 MHz to 333 MHz | 300 MHz to 500 MHz | |
| Organization | x9 / x18 / x36 | x9 / x18 / x36 | |
| $V_{DD}$ | 1.8 ± 0.1 V | 1.8 ± 0.1 V | |
| $V_{DD}Q$ | 1.8 ± 0.1 V or 1.5 ± 0.1 V | 1.8 ± 0.1 V or 1.5 ± 0.1 V | |
| Read Latency | 1.5 clock cycles | 2.0 & 2.5 clock cycles | 1 |
| Write Latency | 1.0 clock cycle | 1.0 clock cycle | 2 |
| Input Clocks (K, K#) | Single Ended (K, K#) | Single Ended (K, K#) | |
| Output Clocks (C, C#) | Yes | No | |
| Echo Clock Number (CQ, CQ#) | 1 Pair | 1 Pair | 3 |
| Package | 165-pin PLASTIC BGA (15 x 17) | 165-pin PLASTIC BGA (15 x 17) | |
| Fixed Burst Address for DDR CIO; A0 for burst 2 | Yes | No | 4 |
| QVLD | No | Yes | 5 |
| ODT | No | Yes | 6 |

**Notes 1.** DDR II+ read latency is not user selectable. Offered as two different devices. 2.5 clock cycle is consortium standard, and 2.0 clock cycle is vendor option.

   **2.** DDR II+ write latency is 1.0 clock cycle regardless of read latency.

   **3.** Echo Clocks are single-ended outputs.

   **4.** Linear burst is not supported at DDR II + CIO.

   **5.** Edge aligned with Echo Clocks.

   **6.** ODT ON/OFF is user selectable.

## Pin Configurations

**165-pin PLASTIC BGA (15 x 17)**

**(Top View)**

**[μPD44646092A-A], [μPD44646093A-A]**

**8M x 9**

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|----|----|
| **A** | CQ# | A | A | R, W# | NC | K# | NC/144M | LD# | A | A | CQ |
| **B** | NC | NC | NC | A | NC/288M | K | BW0# | A | NC | NC | DQ4 |
| **C** | NC | NC | NC | Vss | A | A | A | Vss | NC | NC | NC |
| **D** | NC | NC | NC | Vss | Vss | Vss | Vss | Vss | NC | NC | NC |
| **E** | NC | NC | DQ5 | VDDQ | Vss | Vss | Vss | VDDQ | NC | NC | DQ3 |
| **F** | NC | NC | NC | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | NC |
| **G** | NC | NC | DQ6 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | NC |
| **H** | DLL# | VREF | VDDQ | VDDQ | VDD | Vss | VDD | VDDQ | VDDQ | VREF | ZQ |
| **J** | NC | NC | NC | VDDQ | VDD | Vss | VDD | VDDQ | NC | DQ2 | NC |
| **K** | NC | NC | NC | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | NC |
| **L** | NC | DQ7 | NC | VDDQ | Vss | Vss | Vss | VDDQ | NC | NC | DQ1 |
| **M** | NC | NC | NC | Vss | Vss | Vss | Vss | Vss | NC | NC | NC |
| **N** | NC | NC | NC | Vss | A | A | A | Vss | NC | NC | NC |
| **P** | NC | NC | DQ8 | A | A | QVLD | A | A | NC | NC | DQ0 |
| **R** | TDO | TCK | A | A | A | ODT | A | A | A | TMS | TDI |

| A | : Address inputs | TMS | : IEEE 1149.1 Test input |
|---|---|---|---|
| DQ0 to DQ8 | : Data inputs / outputs | TDI | : IEEE 1149.1 Test input |
| LD# | : Synchronous load | TCK | : IEEE 1149.1 Clock input |
| R, W# | : Read Write input | TDO | : IEEE 1149.1 Test output |
| BW0# | : Byte Write data select | VREF | : HSTL input reference input |
| K, K# | : Input clock | VDD | : Power Supply |
| CQ, CQ# | : Echo clock | VDDQ | : Power Supply |
| ZQ | : Output impedance matching | Vss | : Ground |
| DLL# | : DLL/PLL disable | NC | : No connection |
| QVLD | : Q Valid output | NC/xxM | : Expansion address for xxMb |
| ODT | : ODT Control Input | | |

**Remarks  1.** ×××# indicates active LOW signal.

　　　　**2.** Refer to **Package Drawing** for the index mark.

　　　　**3.** 7A and 5B are expansion addresses: 7A for 144Mb

　　　　　　　　　　　　　　　　　　: 7A and 5B for 288Mb

**165-pin PLASTIC BGA (15 x 17)**

**(Top View)**

**[μPD44646182A-A], [μPD44646183A-A]**

**4M x 18**

|   | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **A** | CQ# | A | A | R, W# | BW1# | K# | NC/144M | LD# | A | A | CQ |
| **B** | NC | DQ9 | NC | A | NC/288M | K | BW0# | A | NC | NC | DQ8 |
| **C** | NC | NC | NC | Vss | A | NC | A | Vss | NC | DQ7 | NC |
| **D** | NC | NC | DQ10 | Vss | Vss | Vss | Vss | Vss | NC | NC | NC |
| **E** | NC | NC | DQ11 | VDDQ | Vss | Vss | Vss | VDDQ | NC | NC | DQ6 |
| **F** | NC | DQ12 | NC | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | DQ5 |
| **G** | NC | NC | DQ13 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | NC |
| **H** | DLL# | VREF | VDDQ | VDDQ | VDD | Vss | VDD | VDDQ | VDDQ | VREF | ZQ |
| **J** | NC | NC | NC | VDDQ | VDD | Vss | VDD | VDDQ | NC | DQ4 | NC |
| **K** | NC | NC | DQ14 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | DQ3 |
| **L** | NC | DQ15 | NC | VDDQ | Vss | Vss | Vss | VDDQ | NC | NC | DQ2 |
| **M** | NC | NC | NC | Vss | Vss | Vss | Vss | Vss | NC | DQ1 | NC |
| **N** | NC | NC | DQ16 | Vss | A | A | A | Vss | NC | NC | NC |
| **P** | NC | NC | DQ17 | A | A | QVLD | A | A | NC | NC | DQ0 |
| **R** | TDO | TCK | A | A | A | ODT | A | A | A | TMS | TDI |

| A | : Address inputs | TMS | : IEEE 1149.1 Test input |
|---|---|---|---|
| DQ0 to DQ17 | : Data inputs / outputs | TDI | : IEEE 1149.1 Test input |
| LD# | : Synchronous load | TCK | : IEEE 1149.1 Clock input |
| R, W# | : Read Write input | TDO | : IEEE 1149.1 Test output |
| BW0#, BW1# | : Byte Write data select | VREF | : HSTL input reference input |
| K, K# | : Input clock | VDD | : Power Supply |
| CQ, CQ# | : Echo clock | VDDQ | : Power Supply |
| ZQ | : Output impedance matching | Vss | : Ground |
| DLL# | : DLL/PLL disable | NC | : No connection |
| QVLD | : Q Valid output | NC/xxM | : Expansion address for xxMb |
| ODT | : ODT Control Input | | |

**Remarks 1.** ×××# indicates active LOW signal.

   **2.** Refer to **Package Drawing** for the index mark.

   **3.** 7A and 5B are expansion addresses: 7A for 144Mb

   : 7A and 5B for 288Mb

**165-pin PLASTIC BGA (15 x 17)**

**(Top View)**

**[μPD44646362A-A], [μPD44646363A-A]**

**2M x 36**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | CQ# | NC/144M | A | R, W# | BW2# | K# | BW1# | LD# | A | A | CQ |
| B | NC | DQ27 | DQ18 | A | BW3# | K | BW0# | A | NC | NC | DQ8 |
| C | NC | NC | DQ28 | Vss | A | NC | A | Vss | NC | DQ17 | DQ7 |
| D | NC | DQ29 | DQ19 | Vss | Vss | Vss | Vss | Vss | NC | NC | DQ16 |
| E | NC | NC | DQ20 | VDDQ | Vss | Vss | Vss | VDDQ | NC | DQ15 | DQ6 |
| F | NC | DQ30 | DQ21 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | DQ5 |
| G | NC | DQ31 | DQ22 | VDDQ | VDD | Vss | VDD | VDDQ | NC | NC | DQ14 |
| H | DLL# | VREF | VDDQ | VDDQ | VDD | Vss | VDD | VDDQ | VDDQ | VREF | ZQ |
| J | NC | NC | DQ32 | VDDQ | VDD | Vss | VDD | VDDQ | NC | DQ13 | DQ4 |
| K | NC | NC | DQ23 | VDDQ | VDD | Vss | VDD | VDDQ | NC | DQ12 | DQ3 |
| L | NC | DQ33 | DQ24 | VDDQ | Vss | Vss | Vss | VDDQ | NC | NC | DQ2 |
| M | NC | NC | DQ34 | Vss | Vss | Vss | Vss | Vss | NC | DQ11 | DQ1 |
| N | NC | DQ35 | DQ25 | Vss | A | A | A | Vss | NC | NC | DQ10 |
| P | NC | NC | DQ26 | A | A | QVLD | A | A | NC | DQ9 | DQ0 |
| R | TDO | TCK | A | A | A | ODT | A | A | A | TMS | TDI |

| | | | | |
|---|---|---|---|---|
| A | : Address inputs | TMS | : IEEE 1149.1 Test input |
| DQ0 to DQ35 | : Data inputs / outputs | TDI | : IEEE 1149.1 Test input |
| LD# | : Synchronous load | TCK | : IEEE 1149.1 Clock input |
| R, W# | : Read Write input | TDO | : IEEE 1149.1 Test output |
| BW0# to BW3# | : Byte Write data select | VREF | : HSTL input reference input |
| K, K# | : Input clock | VDD | : Power Supply |
| CQ, CQ# | : Echo clock | VDDQ | : Power Supply |
| ZQ | : Output impedance matching | Vss | : Ground |
| DLL# | : DLL/PLL disable | NC | : No connection |
| QVLD | : Q Valid output | NC/xxM | : Expansion address for xxMb |
| ODT | : ODT Control Input | | |

**Remarks** **1.** ×××# indicates active LOW signal.

**2.** Refer to **Package Drawing** for the index mark.

**3.** 2A is expansion address for 144Mb.

**Pin Identification**

| Symbol | Type | Description |
|---|---|---|
| A | Input | Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K.  All transactions operate on a burst of two words (one clock period of bus activity). These inputs are ignored when device is deselected, i.e., NOP (LD# = HIGH). |
| DQ0 to DQxx | Input/Output | Synchronous Data IOs: Input data must meet setup and hold times around the rising edges of K and K#. Output data is synchronized to the respective K and K#.<br> x9 device uses DQ0 to DQ8.<br> x18 device uses DQ0 to DQ17.<br> x36 device uses DQ0 to DQ35. |
| LD# | Input | Synchronous Load: This input is brought LOW when a bus cycle sequence is to be defined. This definition includes address and read/write direction. All transactions operate on a burst of 2 data (one clock period of bus activity). |
| R, W# | Input | Synchronous Read/Write Input: When LD# is LOW, this input designates the access type (READ when R, W# is HIGH, WRITE when R, W# is LOW) for the loaded address. R, W# must meet the setup and hold times around the rising edge of K. |
| BWx# | Input | Synchronous Byte Writes: When LOW these inputs cause their respective byte to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and K# for each of the two rising edges comprising the WRITE cycle. See **Pin Configurations** for signal to data relationships.<br> x9 device uses BW0#.<br> x18 device uses BW0#, BW1#.<br> x36 device uses BW0# to BW3#.<br>See **Byte Write Operation** for relation between BWx# and DQxx. |
| K, K# | Input | Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. |
| CQ, CQ# | Output | Synchronous Echo Clock Outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when DQ tristates. If K and K# are stopped in the single clock mode, CQ and CQ# will also stop. |
| ZQ | Input | Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. DQ, CQ, CQ# and QVLD output impedance are set to 0.2 x RQ, where RQ is a resistor from this bump to ground.  The output impedance can be minimized by directly connect ZQ to V$_{DD}$Q.  This pin cannot be connected directly to GND or left unconnected. The output impedance is adjusted every 20 μs upon power-up to account for drifts in supply voltage and temperature. After replacement for a resistor, the new output impedance is reset by implementing power-on sequence. |
| DLL# | Input | DLL/PLL Disable: When DLL# is LOW, the operation can be performed at a clock frequency slower than TKHKH (MAX.) without the DLL/PLL circuit being used. The AC/DC characteristics cannot be guaranteed. For normal operation, DLL# must be HIGH and it can be connected to V$_{DD}$Q through a 10 kΩ or less resistor. |
| QVLD | Output | Q valid Output: The Q Valid indicates valid output data. QVLD is edge aligned with CQ and CQ#. |
| ODT | Input | ODT Control Input: When the ODT control pin is HIGH, the ODT function is turned on at DQxx and BWx# pins. The ODT resistors are set to 0.6 x RQ, where RQ is a resistor from ZQ pin bump to ground. When the ODT Control pin is LOW or No Connect, the ODT function is turned off. The ODT ON/OFF is set at power-on sequence. The ODT can not change the state after power-on. To enable ODT function, ODT pin must be HIGH and it can be connected to V$_{DD}$Q through a 10 kΩ or less resistor. |
| TMS<br>TDI | Input | IEEE 1149.1 Test Inputs: 1.8 V I/O level.  These balls may be left Not Connected if the JTAG function is not used in the circuit. |
| TCK | Input | IEEE 1149.1 Clock Input: 1.8 V I/O level.  This pin must be tied to V$_{SS}$ if the JTAG function is not used in the circuit. |
| TDO | Output | IEEE 1149.1 Test Output: 1.8 V I/O level.<br>When providing any external voltage to TDO signal, it is recommended to pull up to V$_{DD}$. |
| V$_{REF}$ | – | HSTL Input Reference Voltage: Nominally V$_{DD}$Q/2. Provides a reference voltage for the input buffers. |
| V$_{DD}$ | Supply | Power Supply: 1.8 V nominal.  See **Recommended DC Operating Conditions** and **DC Characteristics** for range. |
| V$_{DD}$Q | Supply | Power Supply: Isolated Output Buffer Supply. Nominally 1.5 V. 1.8 V is also permissible. See **Recommended DC Operating Conditions** and **DC Characteristics** for range. |
| V$_{SS}$ | Supply | Power Supply: Ground |
| NC | – | No Connect: These signals are not connected internally. |

**Block Diagram**
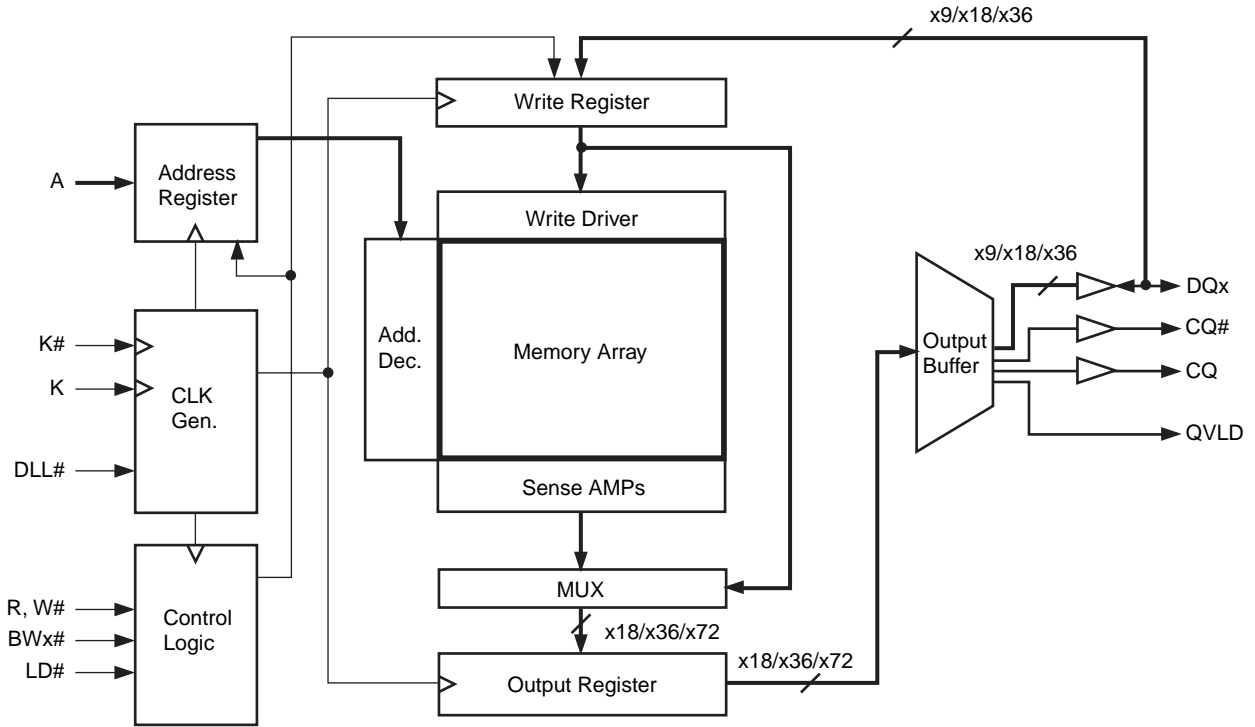
### Power-On Sequence in DDR II+ SRAM

DDR II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations. The following timing charts show the recommended power-on sequence.

The following power-up supply voltage application is recommended: $V_{SS}$, $V_{DD}$, $V_{DD}Q$, $V_{REF}$, then $V_{IN}$. $V_{DD}$ and $V_{DD}Q$ can be applied simultaneously, as long as $V_{DD}Q$ does not exceed $V_{DD}$ by more than 0.5 V during power-up. The following power-down supply voltage removal sequence is recommended: $V_{IN}$, $V_{REF}$, $V_{DD}Q$, $V_{DD}$, $V_{SS}$. $V_{DD}$ and $V_{DD}Q$ can be removed simultaneously, as long as $V_{DD}Q$ does not exceed $V_{DD}$ by more than 0.5 V during power-down.

#### Power-On Sequence

Apply power and tie DLL# to HIGH.

- Apply $V_{DD}$ before $V_{DD}Q$.
- Apply $V_{DD}Q$ before $V_{REF}$ or at the same time as $V_{REF}$.

Select ODT ON/OFF.

Provide stable clock for more than 20 $\mu$s to lock the DLL/PLL.

#### DLL/PLL Constraints

The DLL/PLL uses K clock as its synchronizing input and the input should have low phase jitter which is specified as TKC var. The DLL/PLL can cover 190 MHz as the lowest frequency. If the input clock is unstable and the DLL/PLL is enabled, then the DLL/PLL may lock onto an undesired clock frequency.

#### ODT initialization

The ODT ON/OFF is set at power-on sequence. When the ODT Control pin is HIGH before applying stable clock, the ODT function is turn on. When the ODT Control pin is LOW or No Connect, the ODT function is off. The ODT can not change the state after power-on.

#### Power-On Waveforms
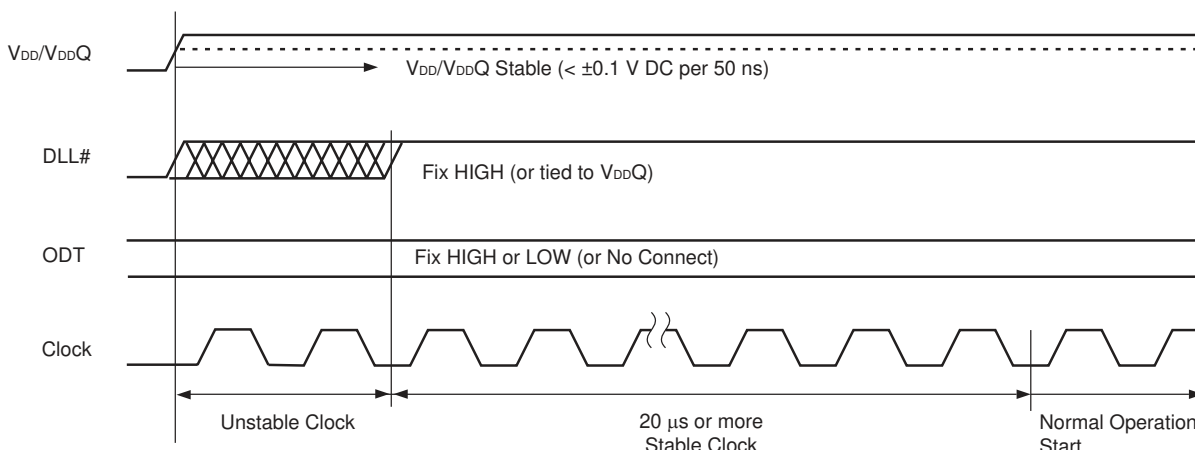
**On-Die Termination (ODT)**

On-Die Termination (ODT) is enabled by setting ODT control pin to HIGH at power-on sequence. The ODT resistors ($R_{TT}$) are set to 0.6 x RQ, where RQ is a resistor from ZQ pin bump to ground. With ODT on, all the DQs and BW#s are terminated to $V_{DD}Q$ and $V_{SS}$ with a resistance $R_{TT}$ x 2. The command, address, and clock signals are not terminated. Figure below shows the equivalent circuit of a DQxx and BWx# receiver with ODT. ODT of DQs are dynamically switched off before a half cycle when READ commands starts and are designed to be off prior to the product driving the bus. ODT of BW#s are always on. Similarly, ODTs are designed to switch on after a half cycle when the product has issued the last piece of data.

When the ODT control pin is LOW or No Connect at power-on sequence, the ODT function is always off.

When the ODT be changed the state after power-on, the AC/DC characteristics cannot be guaranteed.

**On-Die Termination DC Parameters**

| Description | Symbol | MIN. | TYP. | MAX. | Units |
|---|---|---|---|---|---|
| On-Die termination | $R_{TT}$ | 105 | 150 | 210 | Ω |
| External matching resistor | RQ | 175 | 250 | 350 | Ω |

Remark    The allowable range of RQ to guarantee impedance matching a tolerance of ± 20 % is between 175 Ω and 350 Ω.

**On- Die Termination-Equivalent Circuit**
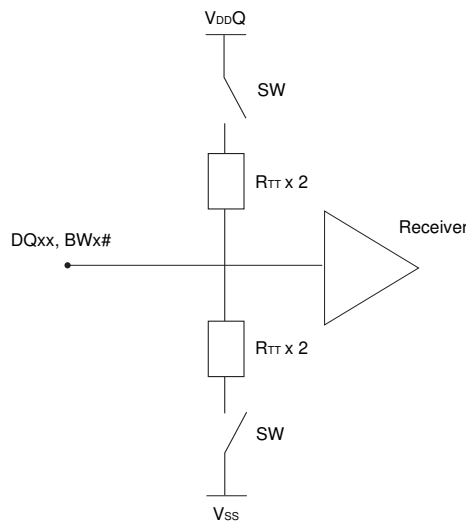


$QDR^{TM}$ Consortium specification for ODT is defined when 6R is HIGH and vendor specification when 6R is LOW or Floating. NEC specification is "Disabled" with 6R LOW or Floating as follows.

**ODT-option clarification**

| 6R input | ODT function | | Termination value | |
|---|---|---|---|---|
| | Consortium specification | NEC specification | Consortium specification | NEC specification |
| HIGH | Active | Active | $R_{TT}$ = 0.6 x RQ | $R_{TT}$ = 0.6 x RQ |
| LOW | Vendor specification | Disabled | Vendor specification | – |
| Floating | Vendor specification | Disabled | Vendor specification | – |

Note    In case of nominal value (RQ = 250 Ω), $R_{TT}$ = 150 Ω.

**Truth Table**

### 2.0 Clock Cycles Read Latency

**[$\mu$PD44646092A-A], [$\mu$PD44646182A-A], [$\mu$PD44646362A-A]**

| Operation | CLK | LD# | R,W# | DQ | | | |
|---|---|---|---|---|---|---|---|
| WRITE cycle | $L \rightarrow H$ | L | L | Data in | | | |
| Load address, input write data on | | | | | Input data | $D_A(A+0)$ | $D_A(A+1)$ |
| consecutive K and K# rising edge | | | | | Input clock | $K(t+1)\uparrow$ | $K\#(t+1)\uparrow$ |
| READ cycle | $L \rightarrow H$ | L | H | Data out | | | |
| Load address, read data on | | | | | Output data | $Q_A(A+0)$ | $Q_A(A+1)$ |
| consecutive K and K# rising edge | | | | | Output clock | $K(t+2)\uparrow$ | $K\#(t+2)\uparrow$ |
| NOP (No operation) | $L \rightarrow H$ | H | X | DQ = High-Z | | | |
| Clock stop | Stopped | X | X | Previous state | | | |

### 2.5 Clock Cycles Read Latency

**[$\mu$PD44646093A-A], [$\mu$PD44646183A-A], [$\mu$PD44646363A-A]**

| Operation | CLK | LD# | R,W# | DQ | | | |
|---|---|---|---|---|---|---|---|
| WRITE cycle | $L \rightarrow H$ | L | L | Data in | | | |
| Load address, input write data on | | | | | Input data | $D_A(A+0)$ | $D_A(A+1)$ |
| consecutive K and K# rising edge | | | | | Input clock | $K(t+1)\uparrow$ | $K\#(t+1)\uparrow$ |
| READ cycle | $L \rightarrow H$ | L | H | Data out | | | |
| Load address, read data on | | | | | Output data | $Q_A(A+0)$ | $Q_A(A+1)$ |
| consecutive K and K# rising edge | | | | | Output clock | $K\#(t+2)\uparrow$ | $K(t+3)\uparrow$ |
| NOP (No operation) | $L \rightarrow H$ | H | X | DQ = High-Z | | | |
| Clock stop | Stopped | X | X | Previous state | | | |

**Remarks**   Remarks listed below are for both products with 2.0 and 2.5 Clock Cycles Read Latency.

1.  H : HIGH, L : LOW, $\times$ : don't care, $\uparrow$ : rising edge.
2.  Data inputs are registered at K and K# rising edges. Data outputs are delivered at K and K# rising edges.
3.  All control inputs in the truth table must meet setup/hold times around the rising edge (LOW to HIGH) of K. All control inputs are registered during the rising edge of K.
4.  This device contains circuitry that ensure the outputs to be in high impedance during power-up.
5.  Refer to state diagram and timing diagrams for clarification.
6.  A+0 refers to the address input during a WRITE or READ cycle.
    A+1 refers to the next internal burst address in accordance with the burst sequence.
7.  It is recommended that K = K# when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.

**Byte Write Operation**

**[μPD44646092A-A], [μPD44646093A-A]**

| Operation | K | K# | BW0# |
|---|---|---|---|
| Write DQ0 to DQ8 | L → H | – | 0 |
|  | – | L → H | 0 |
| Write nothing | L → H | – | 1 |
|  | – | L → H | 1 |

**Remarks 1.** H : HIGH, L : LOW, → : rising edge.

**2.** Assumes a WRITE cycle was initiated. BW0# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

**[μPD44646182A-A], [μPD44646183A-A]**

| Operation | K | K# | BW0# | BW1# |
|---|---|---|---|---|
| Write DQ0 to DQ17 | L → H | – | 0 | 0 |
|  | – | L → H | 0 | 0 |
| Write DQ0 to DQ8 | L → H | – | 0 | 1 |
|  | – | L → H | 0 | 1 |
| Write DQ9 to DQ17 | L → H | – | 1 | 0 |
|  | – | L → H | 1 | 0 |
| Write nothing | L → H | – | 1 | 1 |
|  | – | L → H | 1 | 1 |

**Remarks 1.** H : HIGH, L : LOW, → : rising edge.

**2.** Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

**[μPD44646362A-A], [μPD44646363A-A]**

| Operation | K | K# | BW0# | BW1# | BW2# | BW3# |
|---|---|---|---|---|---|---|
| Write DQ0 to DQ35 | L → H | – | 0 | 0 | 0 | 0 |
|  | – | L → H | 0 | 0 | 0 | 0 |
| Write DQ0 to DQ8 | L → H | – | 0 | 1 | 1 | 1 |
|  | – | L → H | 0 | 1 | 1 | 1 |
| Write DQ9 to DQ17 | L → H | – | 1 | 0 | 1 | 1 |
|  | – | L → H | 1 | 0 | 1 | 1 |
| Write DQ18 to DQ26 | L → H | – | 1 | 1 | 0 | 1 |
|  | – | L → H | 1 | 1 | 0 | 1 |
| Write DQ27 to DQ35 | L → H | – | 1 | 1 | 1 | 0 |
|  | – | L → H | 1 | 1 | 1 | 0 |
| Write nothing | L → H | – | 1 | 1 | 1 | 1 |
|  | – | L → H | 1 | 1 | 1 | 1 |

**Remarks 1.** H : HIGH, L : LOW, → : rising edge.

**2.** Assumes a WRITE cycle was initiated. BW0# to BW3# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

**Bus Cycle State Diagram**
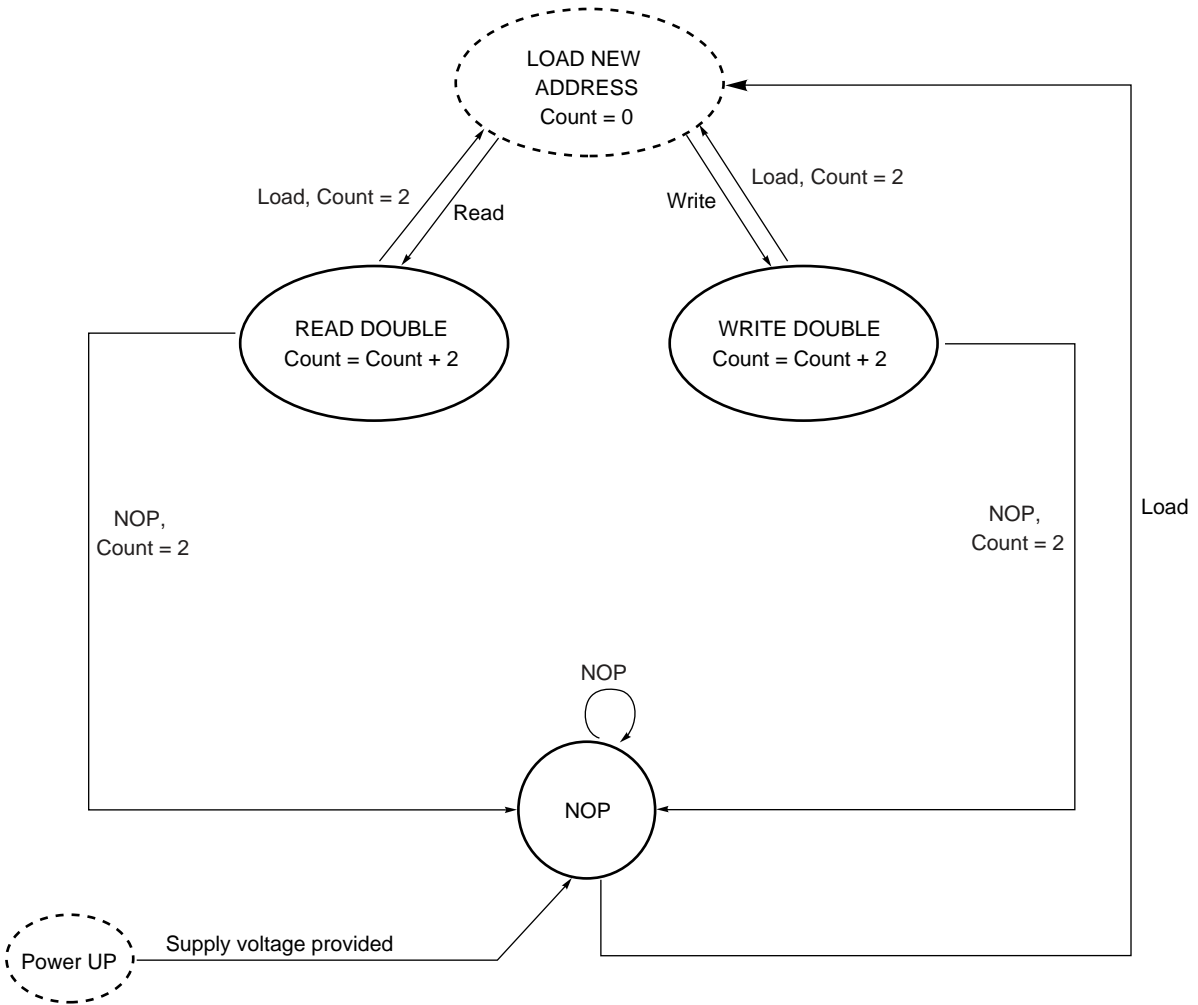


**Remarks 1.** Bus cycle is terminated after burst count = 2.

**2.** State machine control timing sequence is controlled by K.

## Electrical Specifications

### Absolute Maximum Ratings

| Parameter | Symbol | Conditions | Rating | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | −0.5 to +2.5 | V |
| Output supply voltage | $V_{DD}Q$ | | −0.5 to $V_{DD}$ | V |
| Input voltage | $V_{IN}$ | | −0.5 to $V_{DD}$ + 0.5 (2.5 V MAX.) | V |
| Input / Output voltage | $V_{I/O}$ | | −0.5 to $V_{DD}Q$ + 0.5 (2.5 V MAX.) | V |
| Operating ambient temperature | $T_A$ | | 0 to 70 | °C |
| Storage temperature | $T_{stg}$ | | −55 to +125 | °C |

**Caution  Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### Recommended DC Operating Conditions ($T_A$ = 0 to 70°C)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit | Note |
|---|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | 1.7 | 1.8 | 1.9 | V | |
| Output supply voltage | $V_{DD}Q$ | | 1.4 | | $V_{DD}$ | V | 1 |
| Input HIGH voltage | $V_{IH (DC)}$ | | $V_{REF}$ + 0.1 | | $V_{DD}Q$ + 0.3 | V | 1, 2 |
| Input LOW voltage | $V_{IL (DC)}$ | | −0.3 | | $V_{REF}$ − 0.1 | V | 1, 2 |
| Clock input voltage | $V_{IN}$ | | −0.3 | | $V_{DD}Q$ + 0.3 | V | 1, 2 |
| Reference voltage | $V_{REF}$ | | 0.68 | | 0.95 | V | |

**Notes 1.**  During normal operation, $V_{DD}Q$ must not exceed $V_{DD}$.

**2.**  Power-up: $V_{IH} \leq V_{DD}Q$ + 0.3 V and $V_{DD} \leq$ 1.7 V and $V_{DD}Q \leq$ 1.4 V for t $\leq$ 200 ms

### Recommended AC Operating Conditions ($T_A$ = 0 to 70°C)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit | Note |
|---|---|---|---|---|---|---|
| Input HIGH voltage | $V_{IH (AC)}$ | | $V_{REF}$ + 0.2 | | V | 1 |
| Input LOW voltage | $V_{IL (AC)}$ | | | $V_{REF}$ − 0.2 | V | 1 |

**Note 1.**  Overshoot: $V_{IH (AC)} \leq V_{DD}$ + 0.7 V (2.5 V MAX.) for t $\leq$ TKHKH/2

Undershoot: $V_{IL (AC)} \geq$ − 0.5 V for t $\leq$ TKHKH/2

Control input signals may not have pulse widths less than TKHKL (MIN.) or operate at cycle rates less than TKHKH (MIN.).

**DC Characteristics** ($T_A$ = 0 to 70°C, $V_{DD}$ = 1.8 ± 0.1 V)

| Parameter | Symbol | Test condition | | MIN. | MAX. | | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | x9 | x18 | x36 | | |
| Input leakage current | $I_{LI}$ | | | –2 | +2 | | | $\mu$A | 4, 5 |
| I/O leakage current | $I_{LO}$ | | | –2 | +2 | | | $\mu$A | 4 |
| Operating supply current (Read cycle / Write cycle) | $I_{DD}$ | $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$ $I_{I/O}$ = 0 mA Cycle = MAX. | -E20 [Note1] | | 690 | 740 | 850 | mA | |
| | | | -E22 [Note1] | | 650 | 695 | 790 | | |
| | | | -E25 | | 610 | 650 | 730 | | |
| | | | -E30 | | 530 | 590 | 670 | | |
| | | | -E33 | | 490 | 560 | 640 | | |
| Standby supply current (NOP) | $I_{SB1}$ | $V_{IN} \leq V_{IL}$ or $V_{IN} \geq V_{IH}$ $I_{I/O}$ = 0 mA Cycle = MAX. Inputs static | -E20 [Note1] | | 440 | 470 | 530 | mA | |
| | | | -E22 [Note1] | | 430 | 450 | 505 | | |
| | | | -E25 | | 410 | 430 | 480 | | |
| | | | -E30 | | 380 | 400 | 450 | | |
| | | | -E33 | | 370 | 390 | 430 | | |
| Output HIGH voltage | $V_{OH(Low)}$ | $\|I_{OH}\| \leq 0.1$ mA | | $V_{DDQ} - 0.2$ | $V_{DDQ}$ | | | V | 6, 7 |
| | $V_{OH}$ | **Note2** | | $V_{DDQ}/2 - 0.12$ | $V_{DDQ}/2 + 0.12$ | | | | 6, 7 |
| Output LOW voltage | $V_{OL(Low)}$ | $I_{OL} \leq 0.1$ mA | | $V_{SS}$ | 0.2 | | | V | 6, 7 |
| | $V_{OL}$ | **Note3** | | $V_{DDQ}/2 - 0.12$ | $V_{DDQ}/2 + 0.12$ | | | | 6, 7 |

**Notes 1.** -E20 and -E22 are valid for 2.5 Clock Cycles Read Latency products.

   **2.** Outputs are impedance-controlled. | $I_{OH}$ | = ($V_{DDQ}/2$)/(RQ/5) ±15% for values of 175 Ω ≤ RQ ≤ 350 Ω.

   **3.** Outputs are impedance-controlled. $I_{OL}$ = ($V_{DDQ}/2$)/(RQ/5) ±15% for values of 175 Ω ≤ RQ ≤ 350 Ω.

   **4.** Measured with ODT off.

   **5.** ODT pin is internally tied to $V_{SS}$, so input leakage current value is ±5 $\mu$A.

   **6.** AC load current is higher than the shown DC values.

   **7.** HSTL outputs meet JEDEC HSTL Class I standards.

**Capacitance** ($T_A$ = 25°C, f = 1 MHz)

| Parameter | Symbol | Test conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Input capacitance (Address, Control) | $C_{IN}$ | $V_{IN}$ = 0 V | | 4 | pF |
| Input / Output capacitance (DQ, CQ, CQ#, QVLD) | $C_{I/O}$ | $V_{I/O}$ = 0 V | | 5 | pF |
| Clock Input capacitance | $C_{clk}$ | $V_{clk}$ = 0 V | | 4 | pF |

**Remark** These parameters are periodically sampled and not 100% tested.

**Thermal Characteristics**

| Parameter | Symbol | Substrate | Airflow | TYP. | Unit |
|---|---|---|---|---|---|
| Thermal resistance from junction to ambient air | $\theta_{ja}$ | 4-layer | 0 m/s | 19.5 | °C/W |
| | | | 1 m/s | 12.0 | °C/W |
| | | 8-layer | 0 m/s | 18.1 | °C/W |
| | | | 1 m/s | 11.3 | °C/W |
| Thermal characterization parameter from junction to the top center of the package surface | $\Psi_{jt}$ | 4-layer | 0 m/s | 0.01 | °C/W |
| | | | 1 m/s | 0.05 | °C/W |
| | | 8-layer | 0 m/s | 0.01 | °C/W |
| | | | 1 m/s | 0.04 | °C/W |
| Thermal resistance from junction to case | $\theta_{jc}$ | | | 2.14 | °C/W |

**AC Characteristics (T$_A$ = 0 to 70°C, V$_{DD}$ = 1.8 ± 0.1 V)**

**AC Test Conditions (V$_{DD}$ = 1.8 ± 0.1 V, V$_{DD}$Q = 1.4 to V$_{DD}$)**

**Input waveform (Rise / Fall time ≤ 0.3 ns)**
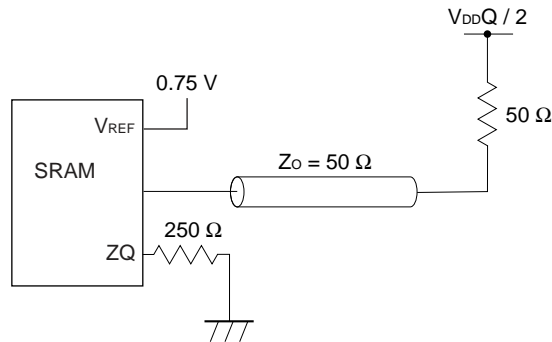
```
1.25 V
                  0.75 V ←——————— Test Points ———————→ 0.75 V
0.25 V
```

**Output waveform**

```
          V$_{DD}$Q / 2 ←——————— Test Points ———————→ V$_{DD}$Q / 2
```
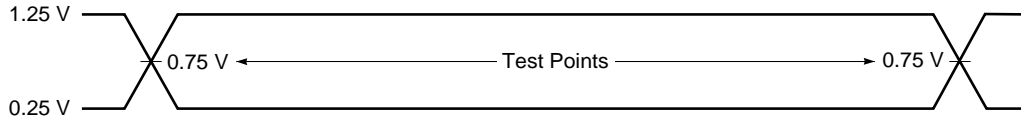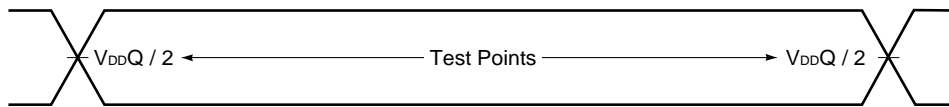
**Output load condition**

**Figure 1.  External load at test**

**Read and Write Cycle**

| Parameter | Symbol | -E20 [Note1] (500 MHz) | | -E22 [Note1] (450 MHz) | | -E25 (400 MHz) | | -E30 (333 MHz) | | -E33 (300 MHz) | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Clock | | | | | | | | | | | | | |
| Average Clock cycle time (K, K#) | TKHKH | 2.0 | 5.25 | 2.2 | 5.25 | 2.5 | 5.25 | 3.0 | 5.25 | 3.3 | 5.25 | ns | 2 |
| Clock phase jitter (K, K#) | TKC var | | 0.15 | | 0.15 | | 0.20 | | 0.20 | | 0.20 | ns | 3 |
| Clock HIGH time (K, K#) | TKHKL | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | TKHKH | |
| Clock LOW time (K, K#) | TKLKH | 0.4 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | TKHKH | |
| Clock HIGH to Clock# HIGH (K → K#) | TKHK#H | 0.85 | | 0.95 | | 1.06 | | 1.28 | | 1.40 | | ns | |
| Clock# HIGH to Clock HIGH (K# → K) | TK#HKH | 0.85 | | 0.95 | | 1.06 | | 1.28 | | 1.40 | | ns | |
| DLL/PLL lock time (K) | TKC lock | 20 | | 20 | | 20 | | 20 | | 20 | | μs | 4 |
| K static to DLL/PLL reset | TKC reset | 30 | | 30 | | 30 | | 30 | | 30 | | ns | 5 |
| | | | | | | | | | | | | | |
| Output Times | | | | | | | | | | | | | |
| CQ HIGH to CQ# HIGH (CQ → CQ#) | TCQHCQ#H | 0.6 | | 0.7 | | 0.81 | | 1.03 | | 1.15 | | ns | 6 |
| CQ# HIGH to CQ HIGH (CQ# → CQ) | TCQ#HCQH | 0.6 | | 0.7 | | 0.81 | | 1.03 | | 1.15 | | ns | 6 |
| K, K# HIGH to output valid | TKHQV | | 0.45 | | 0.45 | | 0.45 | | 0.45 | | 0.45 | ns | |
| K, K# HIGH to output hold | TKHQX | – 0.45 | | – 0.45 | | – 0.45 | | – 0.45 | | – 0.45 | | ns | |
| K, K# HIGH to echo clock valid | TKHCQV | | 0.45 | | 0.45 | | 0.45 | | 0.45 | | 0.45 | ns | |
| K, K# HIGH to echo clock hold | TKHCQX | – 0.45 | | – 0.45 | | – 0.45 | | – 0.45 | | – 0.45 | | ns | |
| CQ, CQ# HIGH to output valid | TCQHQV | | 0.15 | | 0.15 | | 0.20 | | 0.20 | | 0.20 | ns | 7 |
| CQ, CQ# HIGH to output hold | TCQHQX | – 0.15 | | – 0.15 | | – 0.20 | | – 0.20 | | – 0.20 | | ns | 7 |
| K HIGH to output High-Z | TKHQZ | | 0.45 | | 0.45 | | 0.45 | | 0.45 | | 0.45 | ns | |
| K HIGH to output Low-Z | TKHQX1 | – 0.45 | | – 0.45 | | – 0.45 | | – 0.45 | | – 0.45 | | ns | |
| CQ, CQ# HIGH to QVLD valid | TCQHQVLD | – 0.15 | 0.15 | – 0.15 | 0.15 | – 0.20 | 0.20 | – 0.20 | 0.20 | – 0.20 | 0.20 | ns | |
| | | | | | | | | | | | | | |
| Setup Times | | | | | | | | | | | | | |
| Address valid to K rising edge | TAVKH | 0.33 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | ns | 8 |
| Synchronous load input (LD#), read write input (R, W#) valid to K rising edge | TIVKH | 0.33 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | ns | 8 |
| Data inputs and write data select inputs (BWx#) valid to K, K# rising edge | TDVKH | 0.25 | | 0.28 | | 0.28 | | 0.28 | | 0.28 | | ns | 8 |
| | | | | | | | | | | | | | |
| Hold Times | | | | | | | | | | | | | |
| K rising edge to address hold | TKHAX | 0.33 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | ns | 8 |
| K rising edge to synchronous load input (LD#), read write input (R, W#) hold | TKHIX | 0.33 | | 0.4 | | 0.4 | | 0.4 | | 0.4 | | ns | 8 |
| K, K# rising edge to data inputs and write data select inputs (BWx#) hold | TKHDX | 0.25 | | 0.28 | | 0.28 | | 0.28 | | 0.28 | | ns | 8 |

**Notes 1.** -E20 and –E22 are valid for 2.5 Clock Cycles Read Latency products.

   **2.** When debugging the system or board, these products can operate at a clock frequency slower than TKHKH (MAX.) without the DLL/PLL circuit being used, if DLL# = LOW. Read latency (RL) is changed to 1.0 clock cycle regardless of RL = 2.0 and 2.5 clock cycles products in this operation. The AC/DC characteristics cannot be guaranteed, however.

   **3.** Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge. TKC var (MAX.) indicates a peak-to-peak value.

**4.** V$_{DD}$ slew rate must be less than 0.1 V DC per 50 ns for DLL/PLL lock retention.

DLL/PLL lock time begins once V$_{DD}$ and input clock are stable.

It is recommended that the device is kept NOP (LD# = HIGH) during these cycles.

**5.** K input is monitored for this operation. See below for the timing.
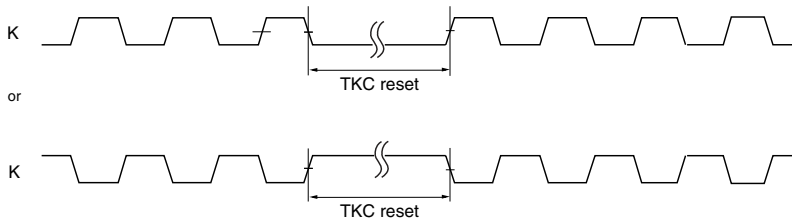


**6.** Guaranteed by design.

**7.** Echo clock is very tightly controlled to data valid / data hold. By design, there is a ± 0.1 ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.

**8.** This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

**Remarks 1.** This parameter is sampled.

**2.** Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.

**3.** Control input signals may not be operated with pulse widths less than TKHKL (MIN.).

**4.** V$_{DD}$Q is 1.5 V DC.

**Read and Write Timing**

**2.0 Clock Cycles Read Latency**

**[μPD44646092A-A], [μPD44646182A-A], [μPD44646362A-A]**
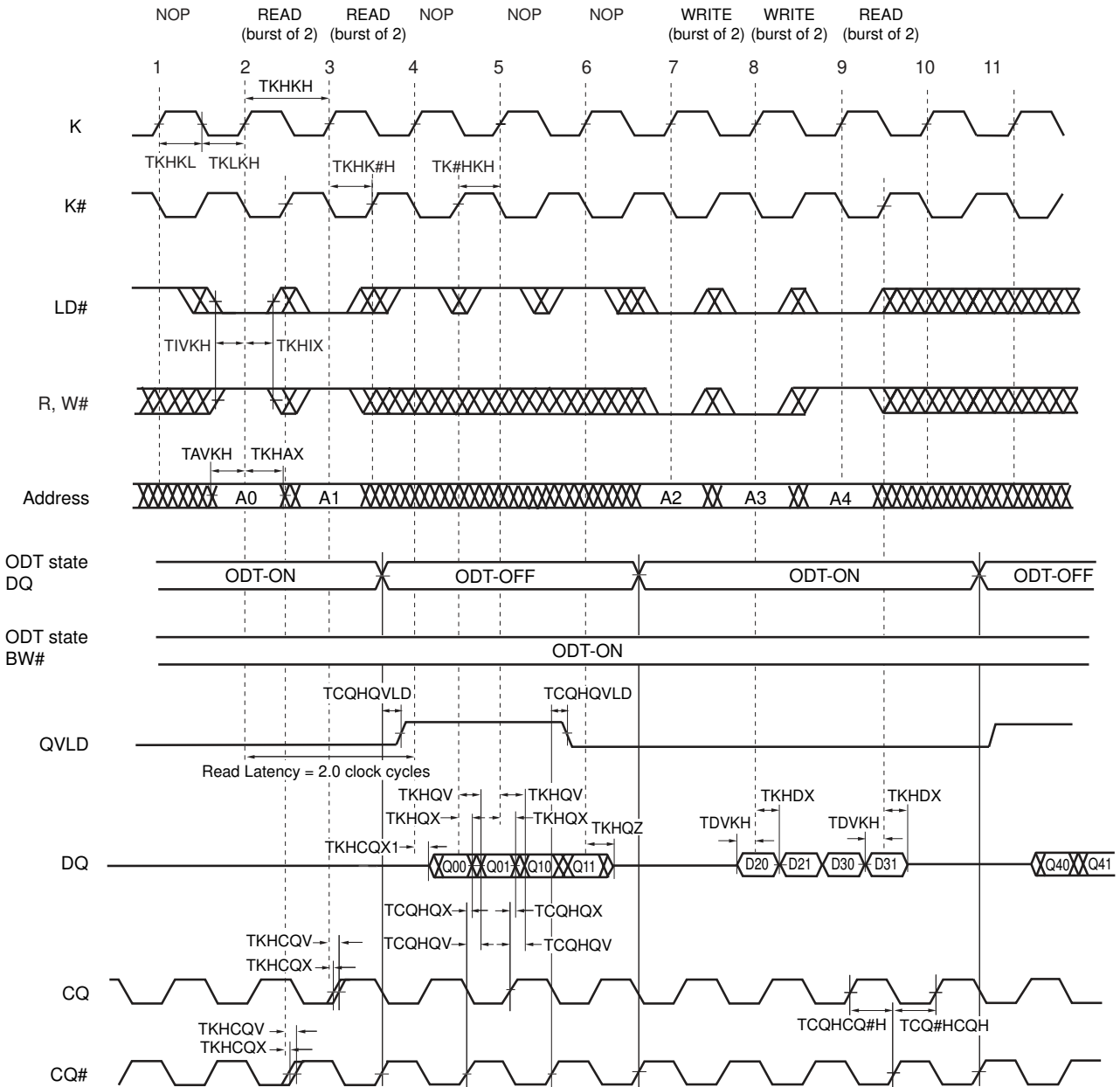


**Remarks 1.** Q00 refers to output from address A0.

Q01 refers to output from the next internal burst address following A0, etc.

**2.** Outputs are disabled (high impedance) 3 clock cycles after the last READ (LD# = LOW, R, W# = HIGH) is input in the sequences of [READ]-[NOP].

**3.** The third NOP cycle between Read to Write transition may not be necessary for correct device operation when Read latency = 2.0 clock cycles. However, it may be required to avoid bus contention.

**4.** When the ODT control pin is LOW or No Connect, the ODT function is always off.

**2.5 Clock Cycles Read Latency**

**[μPD44646093A-A], [μPD44646183A-A], [μPD44646363A-A]**
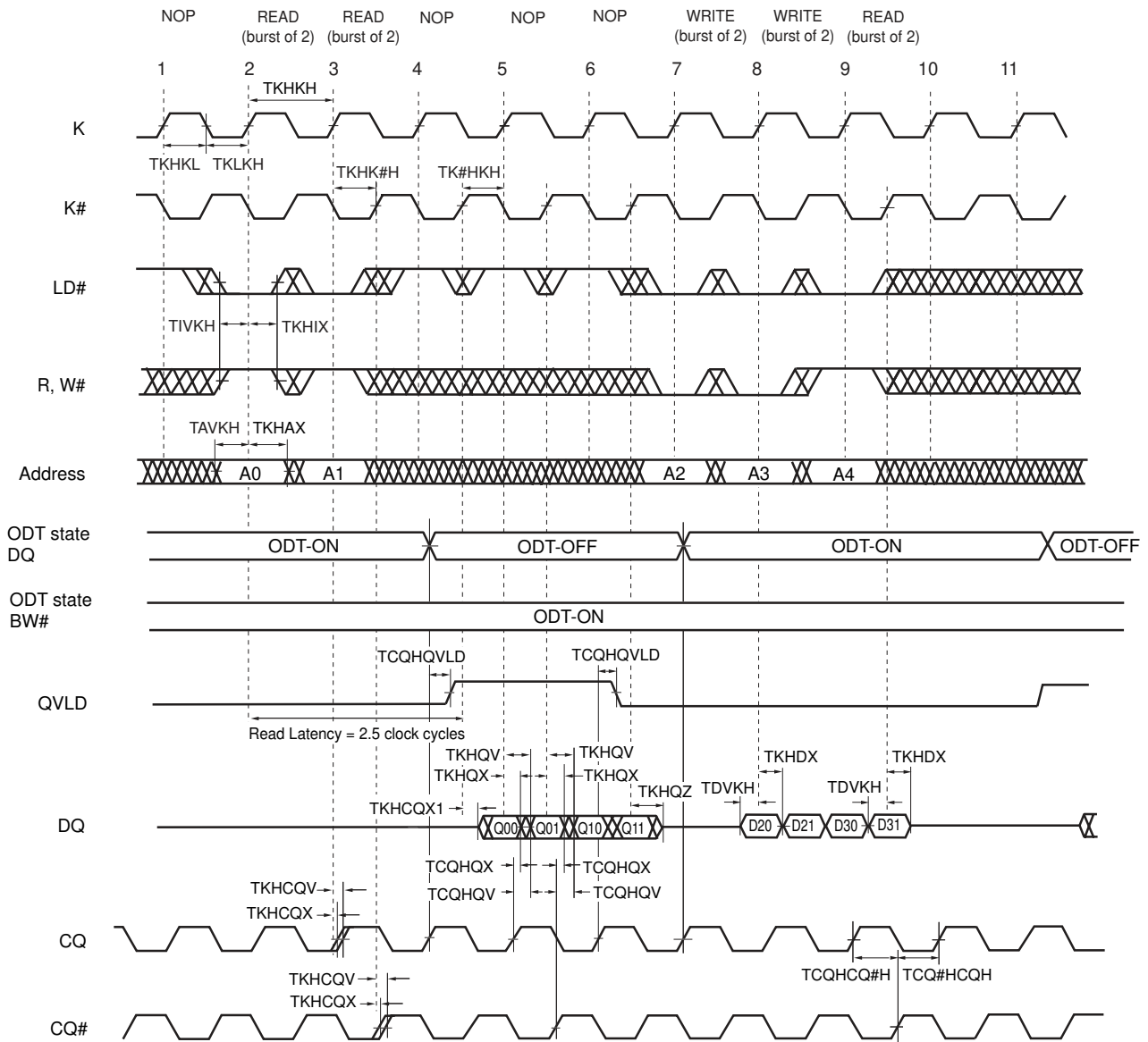


**Remarks 1.** Q00 refers to output from address A0.

Q01 refers to output from the next internal burst address following A0, etc.

**2.** Outputs are disabled (high impedance) 3.5 clock cycles after the last READ (LD# = LOW, R, W# = HIGH) is input in the sequences of [READ]-[NOP].

**3.** When the ODT control pin is LOW or No Connect, the ODT function is always off.

**Application Example**



R = 50 Ω   Vt = Vref
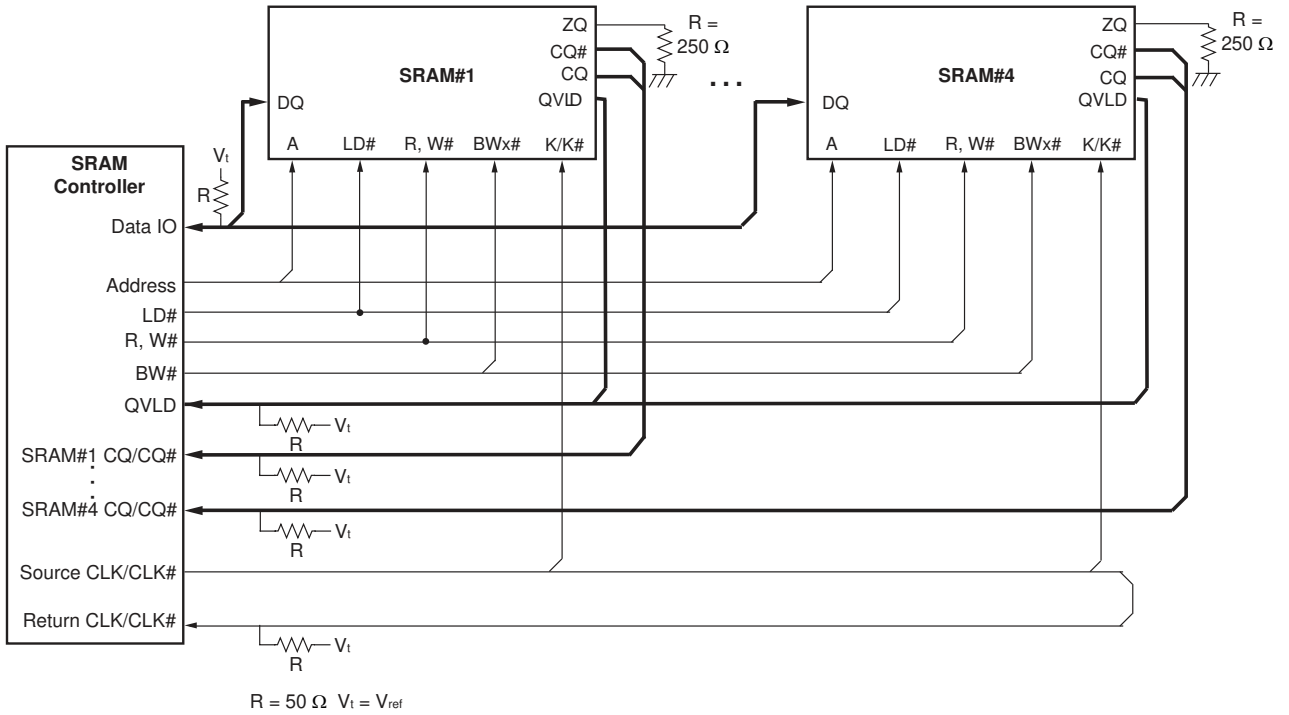
**Remark**   AC specifications are defined at the condition of SRAM outputs, CQ, CQ#, QVLD and DQ with termination. DQs and BW#s have ODT.

## JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

### Test Access Port (TAP) Pins

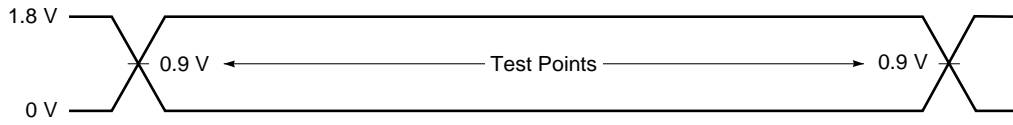| Pin name | Pin assignments | Description |
|---|---|---|
| TCK | 2R | Test Clock Input.  All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK. |
| TMS | 10R | Test Mode Select.  This is the command input for the TAP controller state machine. |
| TDI | 11R | Test Data Input.  This is the input side of the serial registers placed between TDI and TDO.  The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction. |
| TDO | 1R | Test Data Output.  This is the output side of the serial registers placed between TDI and TDO.  Output changes in response to the falling edge of TCK. |

**Remark**  The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held HIGH for five rising edges of TCK.  The TAP controller state is also reset on the SRAM POWER-UP.

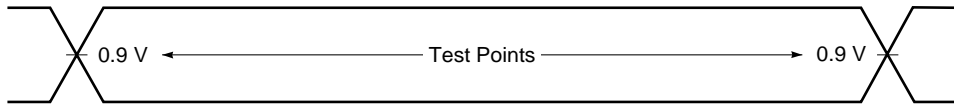### JTAG DC Characteristics ($T_A$ = 0 to 70°C, $V_{DD}$ = 1.8 ± 0.1 V, unless otherwise noted)

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| JTAG Input leakage current | $I_{LI}$ | 0 V ≤ $V_{IN}$ ≤ $V_{DD}$ | −5.0 | +5.0 | µA |
| JTAG I/O leakage current | $I_{LO}$ | 0 V ≤ $V_{IN}$ ≤ $V_{DD}Q$, Outputs disabled | −5.0 | +5.0 | µA |
| JTAG input HIGH voltage | $V_{IH}$ | | 1.3 | $V_{DD}$+0.3 | V |
| JTAG input LOW voltage | $V_{IL}$ | | −0.3 | +0.5 | V |
| JTAG output HIGH voltage | $V_{OH1}$ | \| $I_{OHC}$ \| = 100 µA | 1.6 | | V |
| | $V_{OH2}$ | \| $I_{OHT}$ \| = 2 mA | 1.4 | | V |
| JTAG output LOW voltage | $V_{OL1}$ | $I_{OLC}$ = 100 µA | | 0.2 | V |
| | $V_{OL2}$ | $I_{OLT}$ = 2 mA | | 0.4 | V |

**JTAG AC Test Conditions**

**Input waveform (Rise / Fall time ≤ 1 ns)**

```
1.8 V ─┐   ┌──────────────────────────────────────┐   ┌─
       ╳─ 0.9 V ◄──────── Test Points ────────► 0.9 V ─╳
  0 V ─┘   └──────────────────────────────────────┘   └─
```

**Output waveform**

```
   ┐   ┌──────────────────────────────────────┐   ┌─
   ╳─ 0.9 V ◄──────── Test Points ────────► 0.9 V ─╳
   ┘   └──────────────────────────────────────┘   └─
```

**Output load**

**Figure 2. External load at test**

$V_{TT} = 0.9$ V

$50\ \Omega$

$Z_O = 50\ \Omega$

TDO ◄

$20$ pF
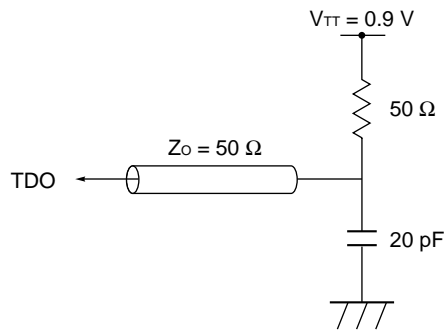
**JTAG AC Characteristics (T<sub>A</sub> = 0 to 70°C)**

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Clock | | | | | |
| Clock cycle time | $t_{THTH}$ | | 50 | | ns |
| Clock frequency | $f_{TF}$ | | | 20 | MHz |
| Clock HIGH time | $t_{THTL}$ | | 20 | | ns |
| Clock LOW time | $t_{TLTH}$ | | 20 | | ns |
| | | | | | |
| Output time | | | | | |
| TCK LOW to TDO unknown | $t_{TLOX}$ | | 0 | | ns |
| TCK LOW to TDO valid | $t_{TLOV}$ | | | 10 | ns |
| | | | | | |
| Setup time | | | | | |
| TMS setup time | $t_{MVTH}$ | | 5 | | ns |
| TDI valid to TCK HIGH | $t_{DVTH}$ | | 5 | | ns |
| Capture setup time | $t_{CS}$ | | 5 | | ns |
| | | | | | |
| Hold time | | | | | |
| TMS hold time | $t_{THMX}$ | | 5 | | ns |
| TCK HIGH to TDI invalid | $t_{THDX}$ | | 5 | | ns |
| Capture hold time | $t_{CH}$ | | 5 | | ns |

**JTAG Timing Diagram**
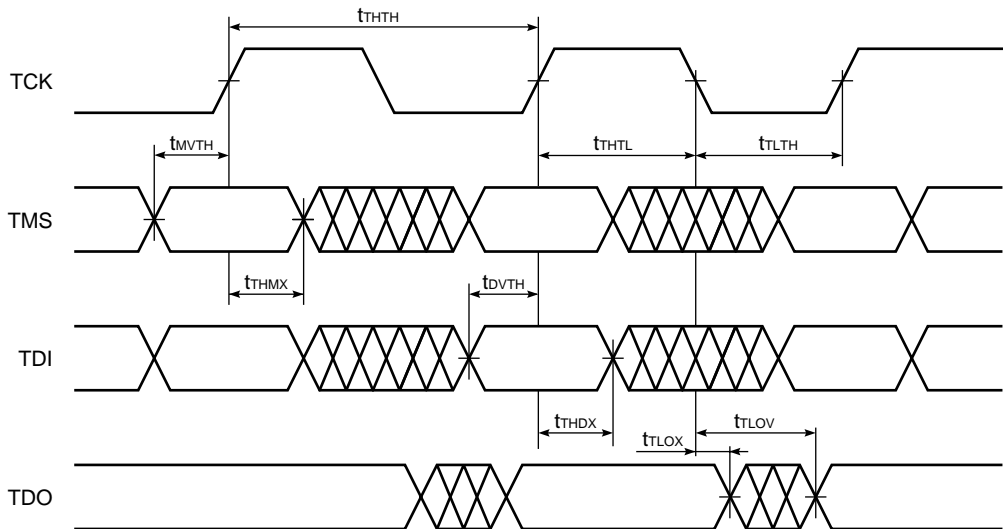
**Scan Register Definition (1)**

| Register name | Description |
|---|---|
| Instruction register | The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state. |
| Bypass register | The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible. |
| ID register | The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state. |
| Boundary register | The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register.<br>The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number. |

**Scan Register Definition (2)**

| Register name | Bit size | Unit |
|---|---|---|
| Instruction register | 3 | bit |
| Bypass register | 1 | bit |
| ID register | 32 | bit |
| Boundary register | 109 | bit |

**ID Register Definition**

**2.0 Clock Cycles Read Latency**

| Part number | Organization | ID [31:28] vendor revision no. | ID [27:12] part no. | ID [11:1] vendor ID no. | ID [0] fix bit |
|---|---|---|---|---|---|
| μPD44646092A-A | 8M x 9 | XXXX | 0000 0000 1000 1100 | 00000010000 | 1 |
| μPD44646182A-A | 4M x 18 | XXXX | 0000 0000 1000 1101 | 00000010000 | 1 |
| μPD44646362A-A | 2M x 36 | XXXX | 0000 0000 1000 1110 | 00000010000 | 1 |

**2.5 Clock Cycles Read Latency**

| Part number | Organization | ID [31:28] vendor revision no. | ID [27:12] part no. | ID [11:1] vendor ID no. | ID [0] fix bit |
|---|---|---|---|---|---|
| μPD44646093A-A | 8M x 9 | XXXX | 0000 0000 1001 1000 | 00000010000 | 1 |
| μPD44646183A-A | 4M x 18 | XXXX | 0000 0000 1001 1001 | 00000010000 | 1 |
| μPD44646363A-A | 2M x 36 | XXXX | 0000 0000 1001 1010 | 00000010000 | 1 |

**SCAN Exit Order**

| Bit no. | Signal name x9 | x18 | x36 | Bump ID | Bit no. | Signal name x9 | x18 | x36 | Bump ID | Bit no. | Signal name x9 | x18 | x36 | Bump ID |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | ODT | | | 6R | 37 | NC | | | 10D | 73 | NC | | | 2C |
| 2 | QVLD | | | 6P | 38 | NC | | | 9E | 74 | DQ5 | DQ11 | DQ20 | 3E |
| 3 | A | | | 6N | 39 | NC | DQ7 | DQ17 | 10C | 75 | NC | NC | DQ29 | 2D |
| 4 | A | | | 7P | 40 | NC | NC | DQ16 | 11D | 76 | NC | | | 2E |
| 5 | A | | | 7N | 41 | NC | | | 9C | 77 | NC | | | 1E |
| 6 | A | | | 7R | 42 | NC | | | 9D | 78 | NC | DQ12 | DQ30 | 2F |
| 7 | A | | | 8R | 43 | DQ4 | DQ8 | DQ8 | 11B | 79 | NC | NC | DQ21 | 3F |
| 8 | A | | | 8P | 44 | NC | NC | DQ7 | 11C | 80 | NC | | | 1G |
| 9 | A | | | 9R | 45 | NC | | | 9B | 81 | NC | | | 1F |
| 10 | DQ0 | | | 11P | 46 | NC | | | 10B | 82 | DQ6 | DQ13 | DQ22 | 3G |
| 11 | NC | NC | DQ9 | 10P | 47 | CQ | | | 11A | 83 | NC | NC | DQ31 | 2G |
| 12 | NC | | | 10N | 48 | A | | | 10A | 84 | DLL# | | | 1H |
| 13 | NC | | | 9P | 49 | A | | | 9A | 85 | NC | | | 1J |
| 14 | NC | DQ1 | DQ11 | 10M | 50 | A | | | 8B | 86 | NC | | | 2J |
| 15 | NC | NC | DQ10 | 11N | 51 | A | | | 7C | 87 | NC | DQ14 | DQ23 | 3K |
| 16 | NC | | | 9M | 52 | A | NC | NC | 6C | 88 | NC | NC | DQ32 | 3J |
| 17 | NC | | | 9N | 53 | LD# | | | 8A | 89 | NC | | | 2K |
| 18 | DQ1 | DQ2 | DQ2 | 11L | 54 | NC | NC | BW1# | 7A | 90 | NC | | | 1K |
| 19 | NC | NC | DQ1 | 11M | 55 | BW0# | | | 7B | 91 | DQ7 | DQ15 | DQ33 | 2L |
| 20 | NC | | | 9L | 56 | K | | | 6B | 92 | NC | NC | DQ24 | 3L |
| 21 | NC | | | 10L | 57 | K# | | | 6A | 93 | NC | | | 1M |
| 22 | NC | DQ3 | DQ3 | 11K | 58 | NC | NC | BW3# | 5B | 94 | NC | | | 1L |
| 23 | NC | NC | DQ12 | 10K | 59 | NC | BW1# | BW2# | 5A | 95 | NC | DQ16 | DQ25 | 3N |
| 24 | NC | | | 9J | 60 | R, W# | | | 4A | 96 | NC | NC | DQ34 | 3M |
| 25 | NC | | | 9K | 61 | A | | | 5C | 97 | NC | | | 1N |
| 26 | DQ2 | DQ4 | DQ13 | 10J | 62 | A | | | 4B | 98 | NC | | | 2M |
| 27 | NC | NC | DQ4 | 11J | 63 | A | | | 3A | 99 | DQ8 | DQ17 | DQ26 | 3P |
| 28 | ZQ | | | 11H | 64 | A | A | NC | 2A | 100 | NC | NC | DQ35 | 2N |
| 29 | NC | | | 10G | 65 | CQ# | | | 1A | 101 | NC | | | 2P |
| 30 | NC | | | 9G | 66 | NC | DQ9 | DQ27 | 2B | 102 | NC | | | 1P |
| 31 | NC | DQ5 | DQ5 | 11F | 67 | NC | NC | DQ18 | 3B | 103 | A | | | 3R |
| 32 | NC | NC | DQ14 | 11G | 68 | NC | | | 1C | 104 | A | | | 4R |
| 33 | NC | | | 9F | 69 | NC | | | 1B | 105 | A | | | 4P |
| 34 | NC | | | 10F | 70 | NC | DQ10 | DQ19 | 3D | 106 | A | | | 5P |
| 35 | DQ3 | DQ6 | DQ6 | 11E | 71 | NC | NC | DQ28 | 3C | 107 | A | | | 5N |
| 36 | NC | NC | DQ15 | 10E | 72 | NC | | | 1D | 108 | A | | | 5R |
| | | | | | | | | | | 109 | – | | | Internal |

**JTAG Instructions**

| Instructions | Description |
|---|---|
| EXTEST | The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins. |
| IDCODE | The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state. |
| BYPASS | When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path. |
| SAMPLE / PRELOAD | SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and DQ pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time ($t_{CS}$ plus $t_{CH}$). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins. |
| SAMPLE-Z | If the SAMPLE-Z instruction is loaded in the instruction register, all RAM DQ pins are forced to an inactive drive state (high impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state. |

**JTAG Instruction Coding**

| IR2 | IR1 | IR0 | Instruction | Note |
|---|---|---|---|---|
| 0 | 0 | 0 | EXTEST | |
| 0 | 0 | 1 | IDCODE | |
| 0 | 1 | 0 | SAMPLE-Z | 1 |
| 0 | 1 | 1 | RESERVED | 2 |
| 1 | 0 | 0 | SAMPLE / PRELOAD | |
| 1 | 0 | 1 | RESERVED | 2 |
| 1 | 1 | 0 | RESERVED | 2 |
| 1 | 1 | 1 | BYPASS | |

**Notes 1.** TRISTATE all DQ pins and CAPTURE the pad values into a SERIAL SCAN LATCH.

**2.** Do not use this instruction code because the vendor uses it to evaluate this product.

**Output Pin States of CQ, CQ#, QVLD and DQ**

| Instructions | Control-Register Status | Output Pin Status | |
|---|---|---|---|
| | | CQ, CQ#, QVLD | DQ |
| EXTEST | 0 | Update | High-Z |
| | 1 | Update | Update |
| IDCODE | 0 | SRAM | SRAM |
| | 1 | SRAM | SRAM |
| SAMPLE-Z | 0 | High-Z | High-Z |
| | 1 | High-Z | High-Z |
| SAMPLE | 0 | SRAM | SRAM |
| | 1 | SRAM | SRAM |
| BYPASS | 0 | SRAM | SRAM |
| | 1 | SRAM | SRAM |

**Remark**    The output pin statuses during each instruction vary according to the Control-Register status (value of Boundary Scan Register, bit no. 109).
There are three statuses:

   Update : Contents of the "Update Register" are output to the output pin (DDR Pad).
   SRAM  : Contents of the SRAM internal output "SRAM Output" are output to the output pin (DDR Pad).
   High-Z : The output pin (DDR Pad) becomes high impedance by controlling of the "High-Z JTAG ctrl".

The Control-Register status is set during Update-DR at the EXTEST or SAMPLE instruction.

In case checking the QVLD output status in EXTEST mode, please make sure stay DLL# pin HIGH.
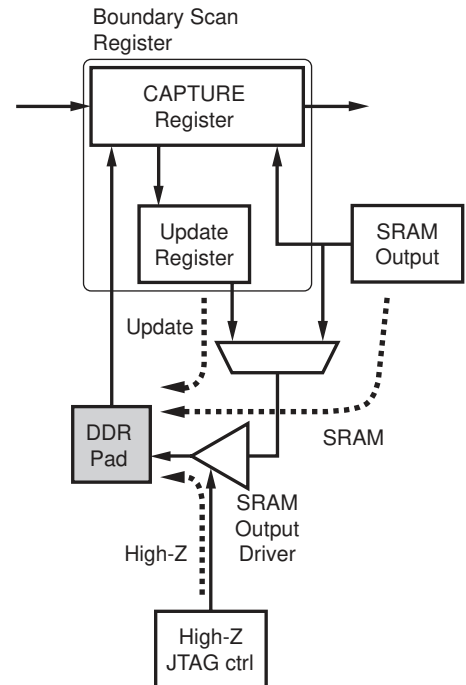
**Boundary Scan Register Status of Output Pins CQ, CQ#, QVLD and DQ**

| Instructions | SRAM Status | Boundary Scan Register Status | | Note |
|---|---|---|---|---|
| | | CQ, CQ#, QVLD | DQ | |
| EXTEST | READ (Low-Z) | Pad | Pad | |
| | NOP (High-Z) | Pad | Pad | |
| IDCODE | READ (Low-Z) | – | – | No definition |
| | NOP (High-Z) | – | – | |
| SAMPLE-Z | READ (Low-Z) | Pad | Pad | |
| | NOP (High-Z) | Pad | Pad | |
| SAMPLE | READ (Low-Z) | Internal | Internal | |
| | NOP (High-Z) | Internal | Pad | |
| BYPASS | READ (Low-Z) | – | – | No definition |
| | NOP (High-Z) | – | – | |

**Remark** The Boundary Scan Register statuses during execution each instruction vary according to the instruction code and SRAM operation mode.
There are two statuses:

Pad : Contents of the output pin (DDR Pad) are captured in the "CAPTURE Register" in the Boundary Scan Register.
Internal : Contents of the SRAM internal output "SRAM Output" are captured in the "CAPTURE Register" in the Boundary Scan Register.
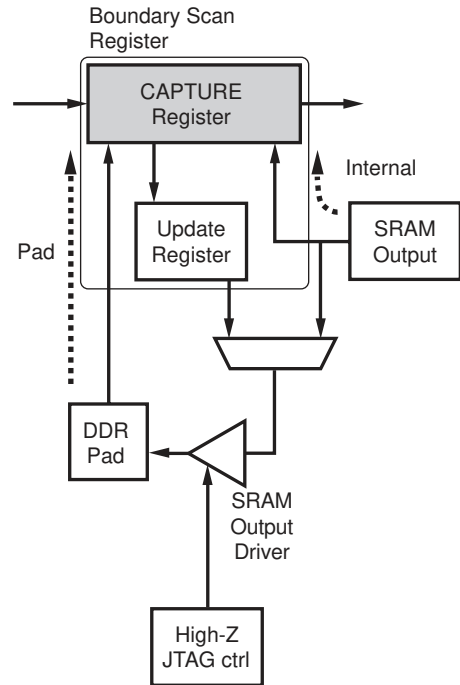
**TAP Controller State Diagram**
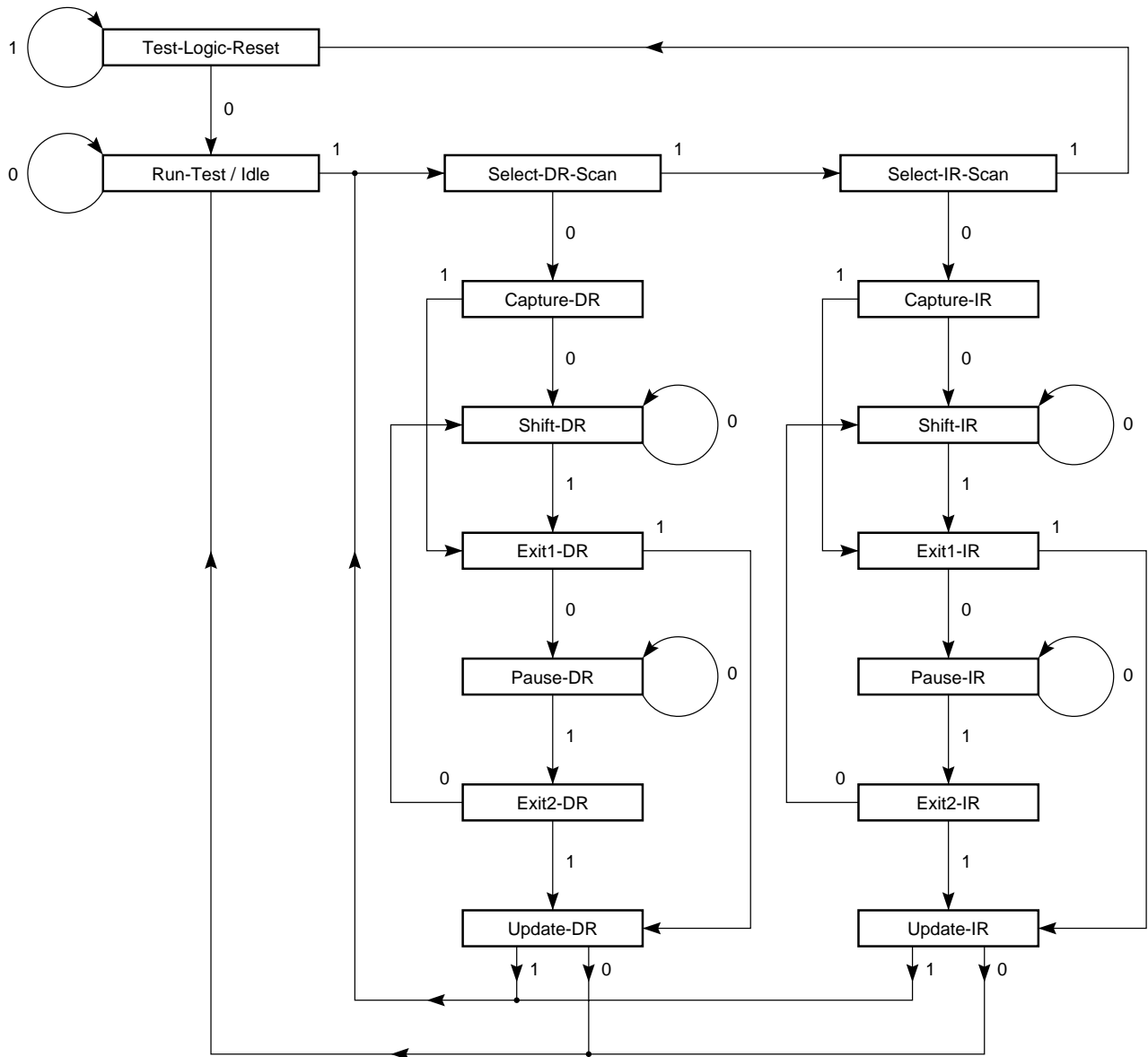


**Disabling the Test Access Port**

It is possible to use this device without utilizing the TAP.  To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to Vss to preclude mid level inputs.  TDI and TMS may be left open but fix them to VDD via a resistor of about 1 kΩ when the TAP controller is not used.  TDO should be left unconnected also when the TAP controller is not used.

**Test Logic Operation (Instruction Scan)**

TCK

TMS

Controller state

| Test-Logic-Reset | Run-Test/Idle | Select-DR-Scan | Select-IR-Scan | Capture-IR | Shift-IR | Exit1-IR | Pause-IR | Exit2-IR | Shift-IR | Exit1-IR | Update-IR | Run-Test/Idle |

TDI

Instruction Register state: IDCODE | New Instruction

TDO: Output Inactive

**Test Logic (Data Scan)**

| | |
|---|---|
| TCK | |
| TMS | |
| Controller state | Test-Logic-Reset / Select-IR-Scan / Select-DR-Scan / Run-Test/Idle / Update-DR / Exit1-DR / Shift-DR / Exit2-DR / Pause-DR / Exit1-DR / Shift-DR / Capture-DR / Select-DR-Scan / Run-Test/Idle |
| TDI | |
| Instruction Register state | IDCODE / Instruction |
| TDO | Output Inactive |

**Package Drawing**

165-PIN PLASTIC BGA(15x17)



INDEX MARK

ZD ← → ← ZE →B

w S B

w S A

R P N M L K J H G F E D C B A

11
10
9
8
7
6
5
4
3
2
1

// y1 S

A2

S

y S

e

A1

φb  φx Ⓜ S A B
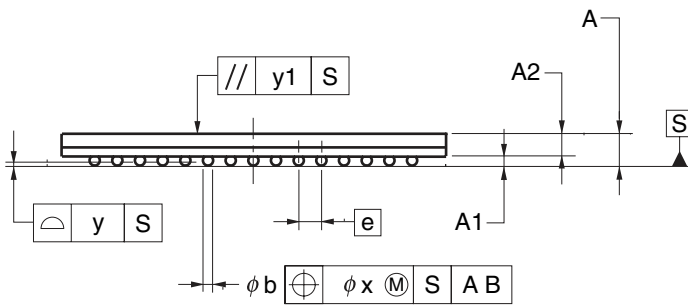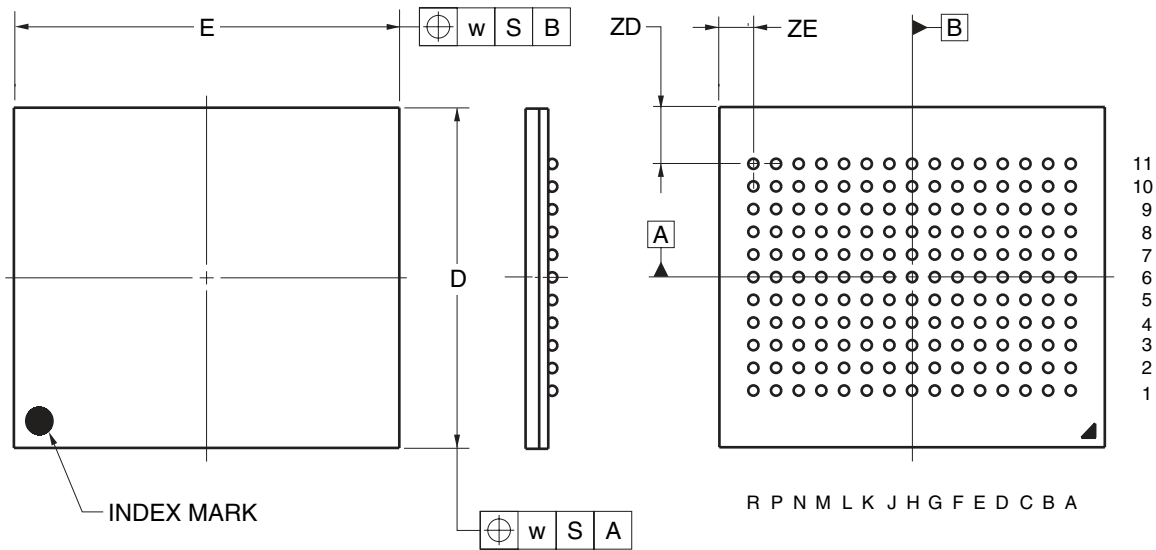
| ITEM | DIMENSIONS |
|------|-----------|
| | (UNIT:mm) |
| D | 15.00±0.10 |
| E | 17.00±0.10 |
| w | 0.30 |
| A | 1.35±0.11 |
| A1 | 0.37±0.05 |
| A2 | 0.98 |
| e | 1.00 |
| b | $0.50^{+0.10}_{-0.05}$ |
| x | 0.10 |
| y | 0.15 |
| y1 | 0.25 |
| ZD | 2.50 |
| ZE | 1.50 |

P165F5-100-FQ1-1

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## Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

## Types of Surface Mount Devices

μPD44646092AF5-FQ1-A  : 165-pin PLASTIC BGA (15 x 17), Lead free

μPD44646182AF5-FQ1-A  : 165-pin PLASTIC BGA (15 x 17), Lead free

μPD44646362AF5-FQ1-A  : 165-pin PLASTIC BGA (15 x 17), Lead free

μPD44646093AF5-FQ1-A  : 165-pin PLASTIC BGA (15 x 17), Lead free

μPD44646183AF5-FQ1-A  : 165-pin PLASTIC BGA (15 x 17), Lead free

μPD44646363AF5-FQ1-A  : 165-pin PLASTIC BGA (15 x 17), Lead free

## Related Document

| Document Name | Document Number |
|---|---|
| μPD44646092A, 44646182A, 44646362A, 44646093A, 44646183A, 44646363A<br>Data Sheet  (Leaded products) | M19060 |

## Quality Grade

• A quality grade of the products is "Standard".

• Anti-radioactive design is not implemented in the products.

• Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the
  ground and so forth.

**Revision History**

| Edition/ Date | Page | | Type of revision | Location | Description (Previous edition → This edition) |
|---|---|---|---|---|---|
| | This edition | Previous edition | | | |
| 2nd edition/ Mar. 2010 | Throughout | Throughout | Modification | | Preliminary Data Sheet → Data Sheet |

[MEMO]

[MEMO]

─── **NOTES FOR CMOS DEVICES** ───

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (MAX) and $V_{IH}$ (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

QDR RAMs and Quad Data Rate RAMs comprise a new series of products developed by Cypress Semiconductor, Renesas, IDT, NEC Electronics, and Samsung.