National Semiconductor

8-Pin Dual Op Amp Eval. Boards

Part Numbers CLC730038, CLC730036

September 1997

The CLC730038 and CLC730036 evaluation boards are designed to aid in the characterization of Comlinear's 8-pin, dual monolithic amplifiers.

- CLC730038 - DIP packages
  Uses all through-hole components
- CLC730036 - SOIC packages
  Uses all surface-mount components

Both boards have identical circuit configurations and are designed for non-inverting gains. Inverting gains or other circuit configurations can be obtained with slight modifications to the boards. Use the evaluation boards as a:

- Guide for high frequency layout
- Tool to aid in device testing and characterization

Basic Operation

Figure 1 shows the non-inverting schematic for both boards. The input signal is brought into the board through SMA connectors to the non-inverting input of the amplifier. The resistor R_{in} is used to set the input termination resistance to the op amp. The non-inverting gain is set by the following equation:

$$\text{Non-inverting Gain:} \quad 1+\frac{R_f}{R_g}$$

The value of the feedback resistor, R_f, has a strong influence on AC performance. Refer to the product data sheet for feedback resistor selection. The output of the op amp travels through a series resistance, R_{out}, and then leaves the board through an SMA connector. The series resistance, R_{out}, matches transmission lines or isolates the output from capacitive loads.

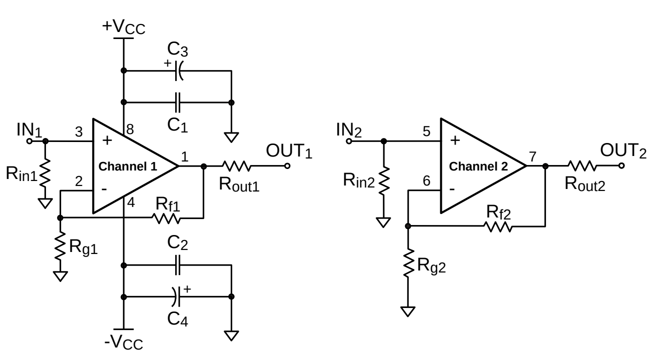


Figure 1: Non-inverting Gain Configurations

Inverting Gain Operation

The evaluation boards can be modified to provide an inverting gain configuration. Complete these steps to modify the board:

1. Cut the input trace as shown in Figure 2
2. Use 25Ω for R_{in}
3. Terminate R_g at the input trace instead of ground (See Figure 2)
4. Add R_t for desired input impedance (input impedance = $R_g||R_t$)

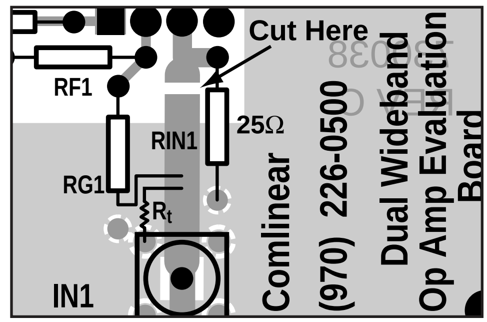


Figure 2: Modifications for Inverting Gains (CLC730038 board shown)

Figure 3 illustrates the inverting schematic for both boards.

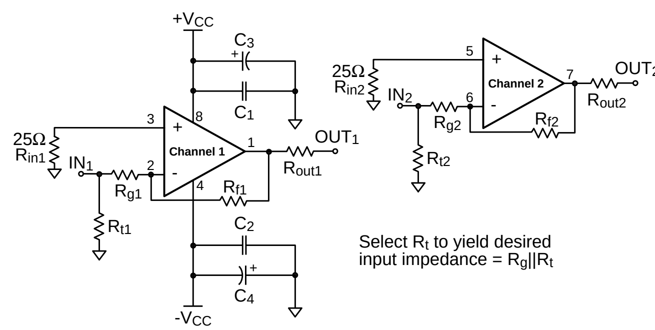


Figure 3: Inverting Gain Configurations

Isolation and Channel Matching Performance

For maximum isolation between channels, proper power supply decoupling is required. Always include the bypass capacitors C1, C2, C3, and C4. The use of good quality capacitors also helps to achieve better isolation performance.

The evaluation boards have also been designed to minimize channel-to-channel crosstalk. The input and output pins of the amplifier are sensitive to the coupling of parasitic capacitances caused by power or ground planes and traces. To reduce the influence of these parasitics, the ground plane has been removed around these sensitive nodes. In multilayer boards, remove both the ground and power traces and planes around the input and output pins.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. When designing your own board, use the evaluation board as a guide and follow these steps as a basis for high frequency layout:

1. Use a ground plane.
2. Include 6.8μF tantalum and 0.1μF ceramic capacitors on both supplies.
3. Place the 6.8μF capacitors within 0.75 inches of the power pins.
4. Place the 0.1μF capacitors less than 0.1 inches from the power pins.
5. Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
6. Minimize all trace lengths to reduce series inductances.
7. Use individual flush-mount sockets, for prototyping.

Measurement Hints

If 50Ω coax and 50Ω R_{in}/R_{out} resistors are used, many of the typical performance plots found in the product data sheets can be reproduced.

When SMA connectors and cables are not available to evaluate the amplifier, do not use normal oscilloscope probes. Use low impedance resistive divider probes of 100 to 500Ω. If a low impedance probe is not available, then a section of 50Ω coaxial cable and a low impedance resistor (10Ω to 50Ω) may be used. Follow these 3 steps to create a "cable/resistor" probe:

1. Connect one end of the coax's center to a test measurement box terminated in 50Ω.
2. Connect the other end of the cable's center conductor to the low impedance resistor. (The open side of the resistor is now a probe.)
3. Connect the ground shield of the cable to evaluation board ground and test box ground.

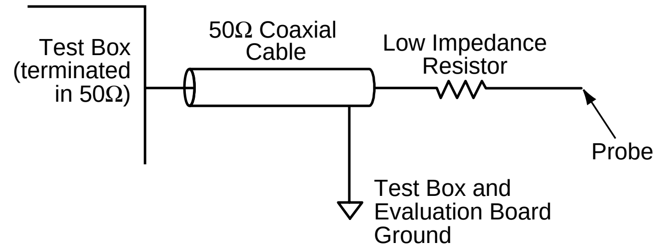


Figure 4: "Cable/Resistor" Probe Configuration

This "cable/resistor" probe, shown in Figure 4, forms a voltage attenuator between the resistor and the 50Ω termination resistance of the test box. This method allows measurements to be performed directly on the output pin of the amplifier.

When evaluating only one channel on the board, complete the following on the unused channel:

1. Included R_f and R_g as shown in Figure 1
2. Ground the input
3. Load the output with 50Ω to ground

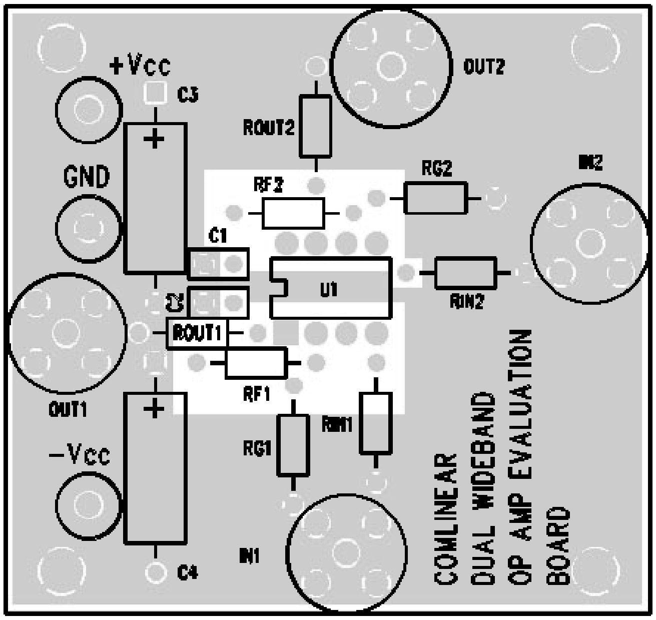
Power Supplies

Refer to the product data sheet for the recommended supply voltages.

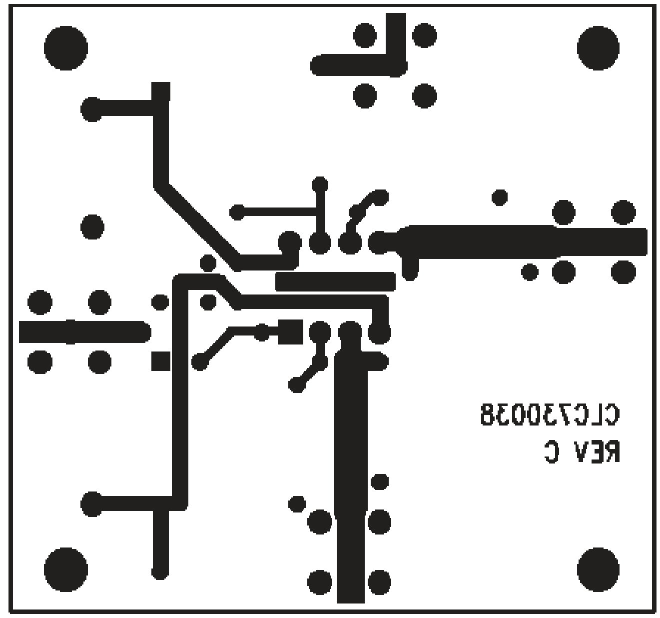
Component Values

- R_f, R_g - Use the product data sheet to select values
- R_{in}, R_{out} - 50Ω (Refer to ***Basic Operation*** section for details)
- R_t - Optional resistor for inverting gain configurations (Refer ***Inverting Gain Operation*** section for details)
- C3, C4 - 6.8μF tantalum capacitors
- C1, C2 - 0.1μF ceramic capacitors

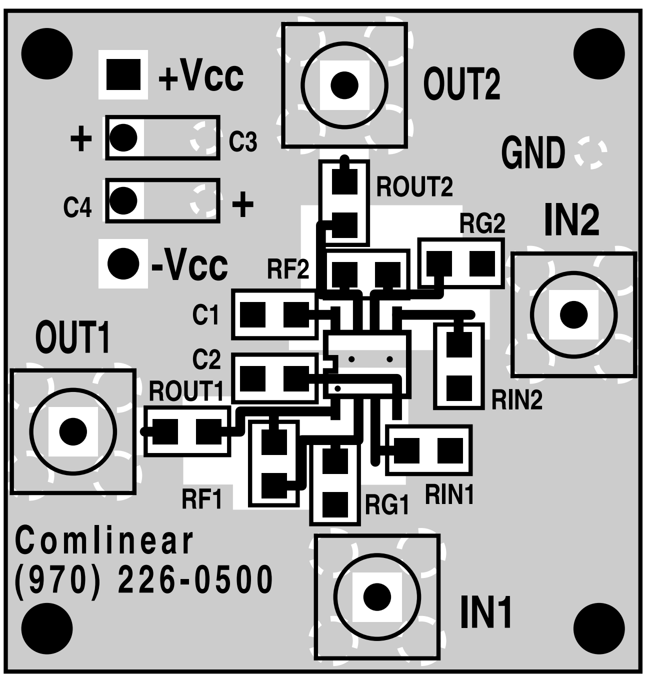
DIP – Top Side



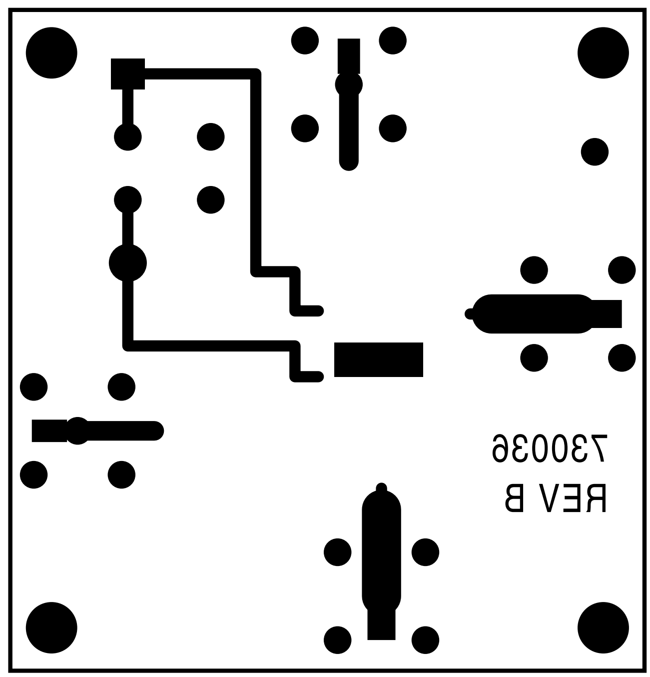
DIP – Bottom Side



SOIC – Top Side



SOIC – Bottom Side



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