ZL30157
Two Channel Universal Clock Translator
Short Form Data Sheet

February 2013

Features

- Two independent clock channels
- Programmable synthesizers generate any clock-rate from 1 kHz to 720 MHz
- One precision synthesizers generate clocks with jitter below 0.7 ps RMS for 10 G PHYs
- One general purpose synthesizers generate a wide range of digital bus clocks
- Programmable digital PLLs synchronize to any clock rate from 1 kHz to 720 MHz
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter from 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Automatic hitless reference switching and digital holdover on reference fail
- Four reference inputs configurable as single ended or differential
- Eight LVPECL outputs and four LVCMOS outputs

Ordering Information

ZL30157GGG2	100 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper
-40°C to +85°C

- Eight outputs configurable as LVCMOS or LVDS/LVPECL/HCSL
- Operates from a single crystal resonator or clock oscillator
- Configurable via SPI/I2C interface

Applications

- 10 Gigabit line cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- OTN multiplexers and transponders
- SONET/SDH, Fibre Channel, XAUI

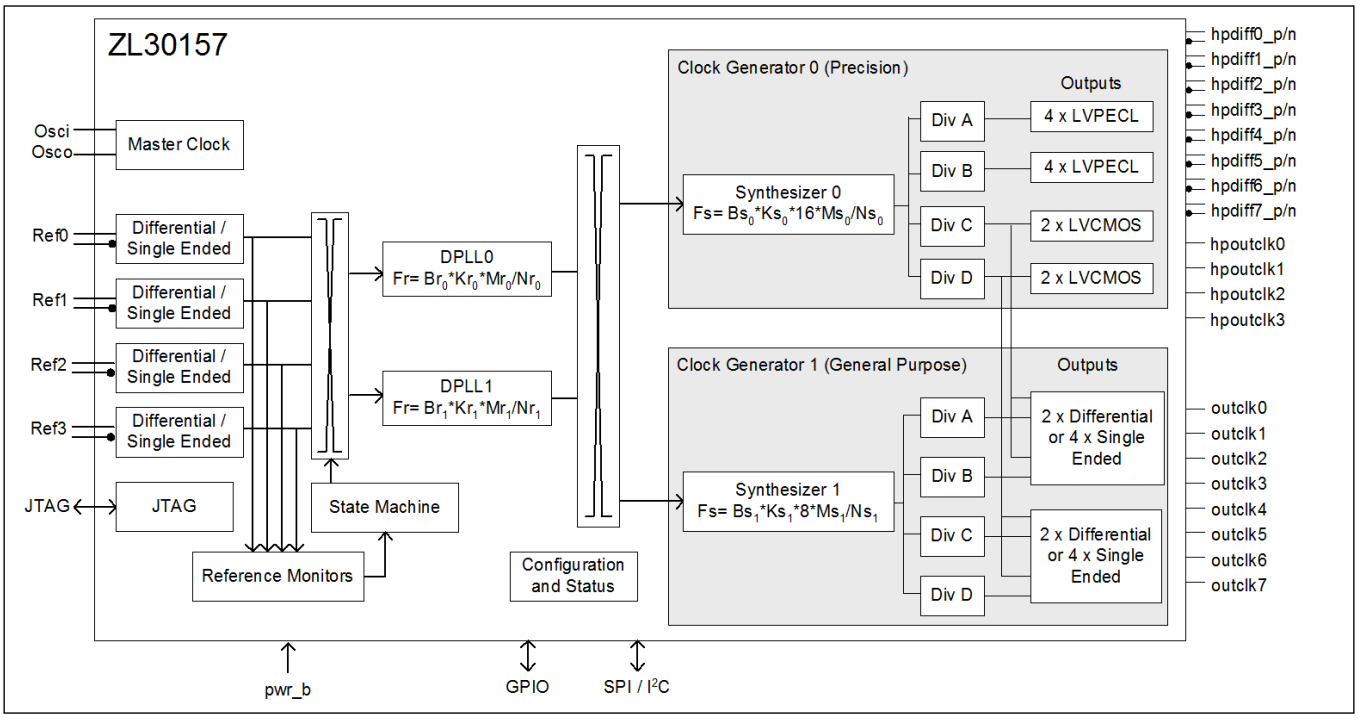


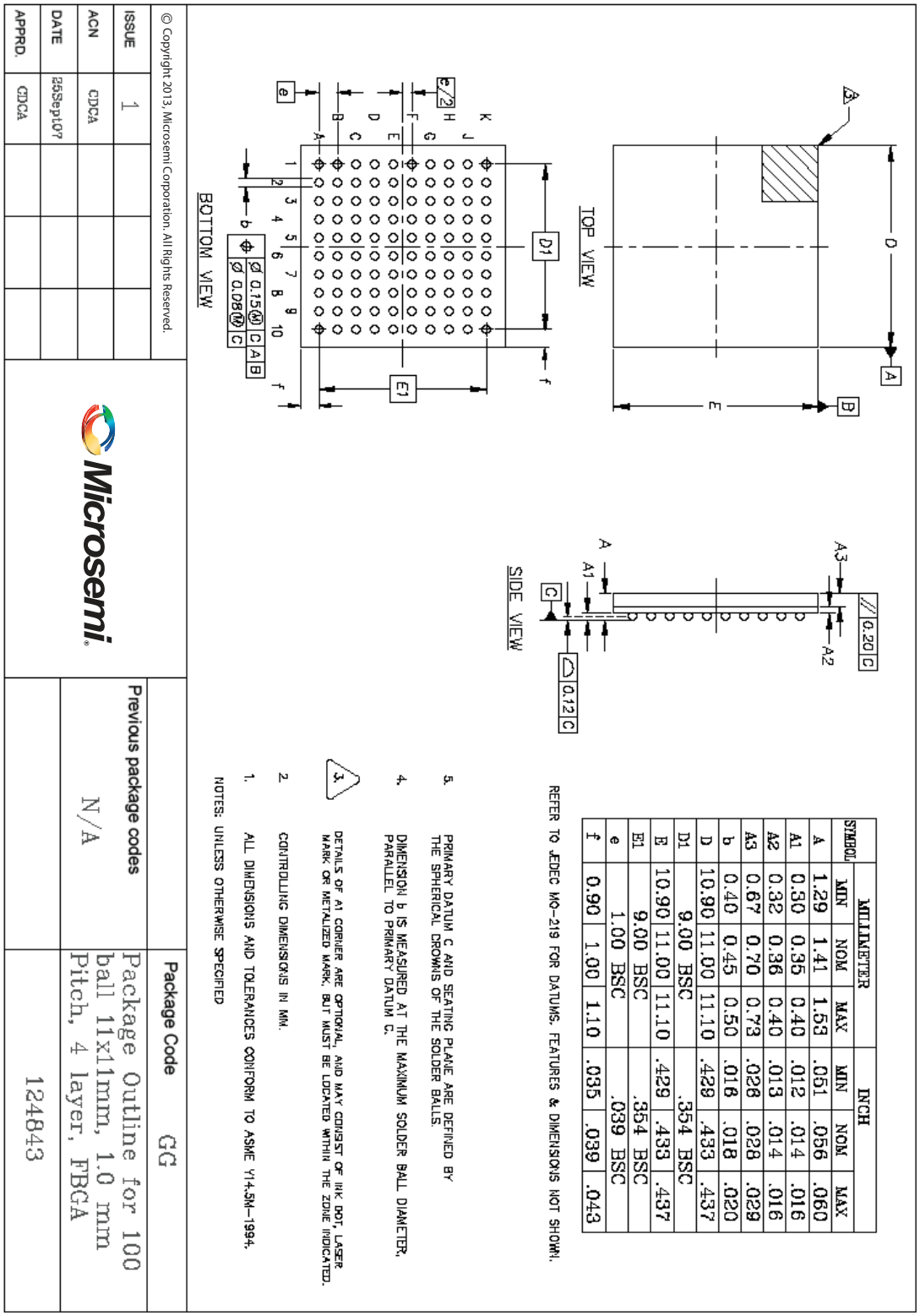
Figure 1 - Functional Block Diagram

Description

The ZL30157 Dual Channel Universal Clock Translator, part of ClockCenter platform of Synchronous Clock devices by Microsemi®, delivers industry leading synchronization performance for high-speed complex applications. The highly integrated and programmable solution provides translation from any input reference frequency to any output clock frequency and allows designers to replace multiple components with a single chip, simplifying design, and reducing component count and power.

The ZL30157 integrates two independent digital phase-locked loops (PLLs), accepts 4 input references, and generates 12 programmable clock outputs. One precision synthesizers generates clocks with jitter performance that can directly drive 10 G PHY devices. One general purpose synthesizers generates a wide range of digital bus clocks.

1.0 Mechanical Drawing



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.29	1.41	1.53	.051	.056	.060
A1	0.30	0.35	0.40	.012	.014	.016
A2	0.32	0.36	0.40	.013	.014	.016
A3	0.67	0.70	0.73	.026	.028	.029
b	0.40	0.45	0.50	.016	.018	.020
D	10.90	11.00	11.10	.429	.433	.437
D1		9.00 BSC			.354 BSC	
E	10.90	11.00	11.10	.429	.433	.437
E1		9.00 BSC			.354 BSC	
e		1.00 BSC			.039 BSC	
f	0.90	1.00	1.10	.035	.039	.043

REFER TO JEDEC MO-219 FOR DATUMS, FEATURES & DIMENSIONS NOT SHOWN.

5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
3. DETAILS OF A1 CORNER ARE OPTIONAL, AND MAY CONSIST OF INK DOT, LASER MARK OR METALIZED MARK, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
2. CONTROLLING DIMENSIONS IN MM.
1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1			
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Microsemi

Previous package codes	Package Code GG
N/A	Package Outline for 100 ball 11x11mm, 1.0 mm Pitch, 4 layer, FBGA
	124843

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