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# MC14557B

## 1-to-64 Bit Variable Length Shift Register

The MC14557B is a static clocked serial shift register whose length may be programmed to be any number of bits between 1 and 64. The number of bits selected is equal to the sum of the subscripts of the enabled Length Control inputs (L1, L2, L4, L8, L16, and L32) plus one. Serial data may be selected from the A or B data inputs with the A/B select input. This feature is useful for recirculation purposes. A Clock Enable (CE) input is provided to allow gating of the clock or negative edge clocking capability.

The device can be effectively used for variable digital delay lines or simply to implement odd length shift registers.

- 1–64 Bit Programmable Length
- Q and  $\bar{Q}$  Serial Buffered Outputs
- Asynchronous Master Reset
- All Inputs Buffered
- No Limit On Clock Rise and Fall Times
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or one Low-power Schottky TTL Load Over the Rated Temperature Range
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

| Symbol            | Parameter   | Value                  | Unit               |
|-------------------|---|------------------------|--------------------|
| $V_{DD}$          | DC Supply Voltage Range                           | -0.5 to +18.0          | V                  |
| $V_{in}, V_{out}$ | Input or Output Voltage Range (DC or Transient)   | -0.5 to $V_{DD} + 0.5$ | V                  |
| $I_{in}, I_{out}$ | Input or Output Current (DC or Transient) per Pin | $\pm 10$               | mA                 |
| $P_D$             | Power Dissipation, per Package (Note 2)           | 500                    | mW                 |
| $T_A$             | Ambient Temperature Range                         | -55 to +125            | $^{\circ}\text{C}$ |
| $T_{stg}$         | Storage Temperature Range                         | -65 to +150            | $^{\circ}\text{C}$ |
| $T_L$             | Lead Temperature (8-Second Soldering)             | 260                    | $^{\circ}\text{C}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

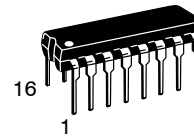
1.  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.
2. Temperature Derating:  
Plastic "P and D/DW" Packages: - 7.0 mW/ $^{\circ}\text{C}$  From 65 $^{\circ}\text{C}$  To 125 $^{\circ}\text{C}$



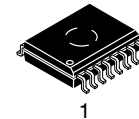
ON Semiconductor®

<http://onsemi.com>

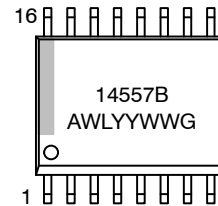
### MARKING DIAGRAMS



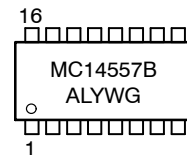
PDIP-16  
P SUFFIX  
CASE 648



SO-16 WB  
DW SUFFIX  
CASE 751G



SOEIAJ-16  
F SUFFIX  
CASE 966



- A = Assembly Location
- WL, L = Wafer Lot
- YY, Y = Year
- WW, W = Work Week
- G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC14557B

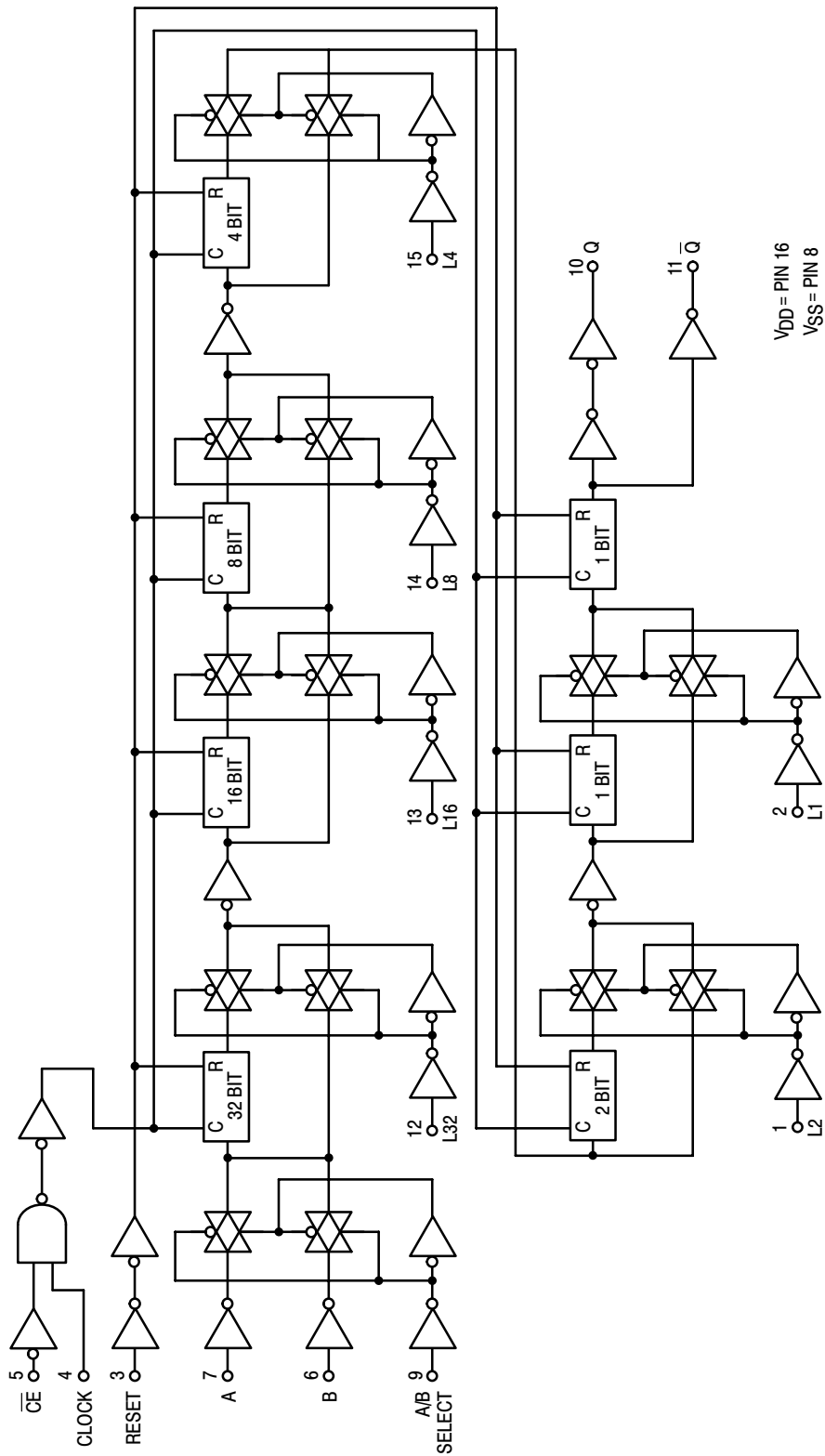


Figure 1. Logic Diagram

# MC14557B

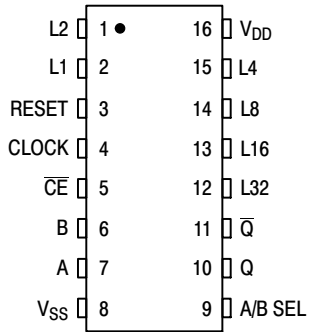


Figure 2. Pin Assignment

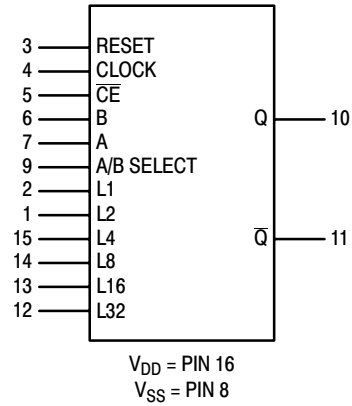


Figure 3. Block Diagram

## TRUTH TABLE

| Inputs |     |        |              | Output |
|--------|-----|--------|--------------|--------|
| Rst    | A/B | Clock  | CE           | Q      |
| 0      | 0   | $\int$ | 0            | B      |
| 0      | 1   | $\int$ | 0            | A      |
| 0      | 0   | 1      | $\downarrow$ | B      |
| 0      | 1   | 1      | $\downarrow$ | A      |
| 1      | X   | X      | X            | 0      |

Q is the output of the first selected shift register stage.  
X = Don't Care

## LENGTH SELECT TRUTH TABLE

| L32 | L16 | L8 | L4 | L2 | L1 | Register Length |
|-----|-----|----|----|----|----|-----------------|
| 0   | 0   | 0  | 0  | 0  | 0  | 1 Bit           |
| 0   | 0   | 0  | 0  | 0  | 1  | 2 Bits          |
| 0   | 0   | 0  | 0  | 1  | 0  | 3 Bits          |
| 0   | 0   | 0  | 0  | 1  | 1  | 4 Bits          |
| 0   | 0   | 0  | 1  | 0  | 0  | 5 Bits          |
| 0   | 0   | 0  | 1  | 0  | 1  | 6 Bits          |
| •   | •   | •  | •  | •  | •  | •               |
| •   | •   | •  | •  | •  | •  | •               |
| •   | •   | •  | •  | •  | •  | •               |
| 1   | 0   | 0  | 0  | 0  | 0  | 33 Bits         |
| 1   | 0   | 0  | 0  | 0  | 1  | 34 Bits         |
| •   | •   | •  | •  | •  | •  | •               |
| •   | •   | •  | •  | •  | •  | •               |
| •   | •   | •  | •  | •  | •  | •               |
| 1   | 1   | 1  | 1  | 0  | 0  | 61 Bits         |
| 1   | 1   | 1  | 1  | 0  | 1  | 62 Bits         |
| 1   | 1   | 1  | 1  | 1  | 0  | 63 Bits         |
| 1   | 1   | 1  | 1  | 1  | 1  | 64 Bits         |

NOTE: Length equals the sum of the binary length control subscripts plus one.

# MC14557B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

| Symbol   | Characteristic   | $V_{DD}$<br>Vdc | - 55°C                                    |           | 25°C |                 |           | 125°C |           | Unit      |      |
|----------|--|-----------------|---|-----------|------|-----------------|-----------|-------|-----------|-----------|------|
|          |  |                 | Min                                       | Max       | Min  | Typ<br>(Note 3) | Max       | Min   | Max       |           |      |
| $V_{OL}$ | Output Voltage<br>$V_{in} = V_{DD}$ or 0   | "0" Level       | 5.0                                       | -         | 0.05 | -               | 0         | 0.05  | -         | 0.05      | Vdc  |
|          |  |                 | 10  | -         | 0.05 | -               | 0         | 0.05  | -         | 0.05      |      |
|          |  |                 | 15  | -         | 0.05 | -               | 0         | 0.05  | -         | 0.05      |      |
| $V_{OH}$ | $V_{in} = 0$ or $V_{DD}$   | "1" Level       | 5.0                                       | 4.95      | -    | 4.95            | 5.0       | -     | 4.95      | -         | Vdc  |
|          |  |                 | 10  | 9.95      | -    | 9.95            | 10        | -     | 9.95      | -         |      |
|          |  |                 | 15  | 14.95     | -    | 14.95           | 15        | -     | 14.95     | -         |      |
| $V_{IL}$ | Input Voltage<br>( $V_O = 4.5$ or $0.5$ Vdc)<br>( $V_O = 9.0$ or $1.0$ Vdc)<br>( $V_O = 13.5$ or $1.5$ Vdc)                          | "0" Level       | 5.0                                       | -         | 1.5  | -               | 2.25      | 1.5   | -         | 1.5       | Vdc  |
|          |  |                 | 10  | -         | 3.0  | -               | 4.50      | 3.0   | -         | 3.0       |      |
|          |  |                 | 15  | -         | 4.0  | -               | 6.75      | 4.0   | -         | 4.0       |      |
| $V_{IH}$ | ( $V_O = 0.5$ or $4.5$ Vdc)<br>( $V_O = 1.0$ or $9.0$ Vdc)<br>( $V_O = 1.5$ or $13.5$ Vdc)   | "1" Level       | 5.0                                       | 3.5       | -    | 3.5             | 2.75      | -     | 3.5       | -         | Vdc  |
|          |  |                 | 10  | 7.0       | -    | 7.0             | 5.50      | -     | 7.0       | -         |      |
|          |  |                 | 15  | 11        | -    | 11              | 8.25      | -     | 11        | -         |      |
| $I_{OH}$ | Output Drive Current<br>( $V_{OH} = 2.5$ Vdc)<br>( $V_{OH} = 4.6$ Vdc)<br>( $V_{OH} = 9.5$ Vdc)<br>( $V_{OH} = 13.5$ Vdc)            | Source          | 5.0                                       | -3.0      | -    | -2.4            | -4.2      | -     | -1.7      | -         | mAdc |
|          |  |                 | 5.0                                       | -0.64     | -    | -0.51           | -0.88     | -     | -0.36     | -         |      |
|          |  |                 | 10  | -1.6      | -    | -1.3            | -2.25     | -     | -0.9      | -         |      |
|          |  |                 | 15  | -4.2      | -    | -3.4            | -8.8      | -     | -2.4      | -         |      |
| $I_{OL}$ | ( $V_{OL} = 0.4$ Vdc)<br>( $V_{OL} = 0.5$ Vdc)<br>( $V_{OL} = 1.5$ Vdc)  | Sink            | 5.0                                       | 0.64      | -    | 0.51            | 0.88      | -     | 0.36      | -         | mAdc |
|          |  |                 | 10  | 1.6       | -    | 1.3             | 2.25      | -     | 0.9       | -         |      |
|          |  |                 | 15  | 4.2       | -    | 3.4             | 8.8       | -     | 2.4       | -         |      |
| $I_{in}$ | Input Current  | 15              | -   | $\pm 0.1$ | -    | $\pm 0.00001$   | $\pm 0.1$ | -     | $\pm 1.0$ | $\mu$ Adc |      |
| $C_{in}$ | Input Capacitance<br>( $V_{in} = 0$ )  | -               | -   | -         | -    | 5.0             | 7.5       | -     | -         | pF        |      |
| $I_{DD}$ | Quiescent Current<br>(Per Package)   | 5.0             | -   | 5.0       | -    | 0.010           | 5.0       | -     | 150       | $\mu$ Adc |      |
|          |  | 10              | -   | 10        | -    | 0.020           | 10        | -     | 300       |           |      |
|          |  | 15              | -   | 20        | -    | 0.030           | 20        | -     | 600       |           |      |
| $I_T$    | Total Supply Current (Notes 4, 5)<br>(Dynamic plus Quiescent, Per Package)<br>( $C_L = 50$ pF on all outputs, all buffers switching) | 5.0             | $I_T = (1.75 \mu\text{A/kHz}) f + I_{DD}$ |           |      |                 |           |       |           | $\mu$ Adc |      |
|          |  | 10              | $I_T = (3.50 \mu\text{A/kHz}) f + I_{DD}$ |           |      |                 |           |       |           |           |      |
|          |  | 15              | $I_T = (5.25 \mu\text{A/kHz}) f + I_{DD}$ |           |      |                 |           |       |           |           |      |

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

4. The formulas given are for the typical characteristics only at 25°C.

5. To calculate total supply current at loads other than 50 pF:  $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$  where:  $I_T$  is in  $\mu\text{A}$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.001$ .

# MC14557B

## SWITCHING CHARACTERISTICS (Note 6) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ )

| Symbol                   | Characteristic   | $V_{DD}$                       | Min                                   | Typ<br>(Note 7)                      | Max                        | Unit          |
|--------------------------|--|--------------------------------|---------------------------------------|--------------------------------------|----------------------------|---------------|
| $t_{TLH}$ ,<br>$t_{THL}$ | Rise and Fall Time, Q or $\bar{Q}$ Output<br>$t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$             | 5<br>10<br>15                  | –<br>–<br>–                           | 100<br>50<br>40                      | 200<br>100<br>80           | ns            |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay, Clock or $\bar{CE}$ to Q or $\bar{Q}$<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 65 \text{ ns}$ | 5<br>10<br>15                  | –<br>–<br>–                           | 300<br>130<br>90                     | 600<br>260<br>180          | ns            |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay, Reset to Q or $\bar{Q}$<br>$t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 215 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 97 \text{ ns}$<br>$t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 70 \text{ ns}$               | 5<br>10<br>15                  | –<br>–<br>–                           | 300<br>130<br>95                     | 600<br>260<br>190          | ns            |
| $t_{WH(cl)}$             | Pulse Width, Clock   | 5<br>10<br>15                  | 200<br>100<br>75                      | 95<br>45<br>35                       | –<br>–<br>–                | ns            |
| $t_{WH(rst)}$            | Pulse Width, Reset   | 5<br>10<br>15                  | 300<br>140<br>100                     | 150<br>70<br>50                      | –<br>–<br>–                | ns            |
| $f_{cl}$                 | Clock Frequency (50% Duty Cycle)   | 5<br>10<br>15                  | –<br>–<br>–                           | 3.0<br>7.5<br>13.0                   | 1.7<br>5.0<br>6.7          | MHz           |
| $t_{su}$                 | Setup Time, A or B to Clock or $\bar{CE}$<br>Worst case condition: $L1 = L2 = L4 = L8 = L16 = L32 = V_{SS}$ (Register Length = 1)<br><br>Best case condition: $L32 = V_{DD}$ , L1 through L16 = Don't Care (Any register length from 33 to 64)             | 5<br>10<br>15<br>5<br>10<br>15 | 700<br>290<br>145<br>400<br>165<br>60 | 350<br>130<br>85<br>45<br>5<br>0     | –<br>–<br>–<br>–<br>–<br>– | ns            |
| $t_h$                    | Hold Time, Clock or $\bar{CE}$ to A or B<br>Best case condition: $L1 = L2 = L4 = L8 = L16 = L32 = V_{SS}$ (Register Length = 1)<br><br>Worst case condition: $L32 = V_{DD}$ , L1 through L16 = Don't Care (Any register length from 33 to 64)              | 5<br>10<br>15<br>5<br>10<br>15 | 200<br>100<br>10<br>400<br>185<br>85  | –150<br>–60<br>–50<br>50<br>25<br>22 | –<br>–<br>–<br>–<br>–<br>– | ns            |
| $t_r$ ,<br>$t_f$         | Rise and Fall Time, Clock  | 5<br>10<br>15                  | No Limit                              |                                      |                            | –             |
| $t_r$ ,<br>$t_f$         | Rise and Fall Time, Reset or $\bar{CE}$  | 5<br>10<br>15                  | –<br>–<br>–                           | –<br>–<br>–                          | 15<br>5<br>4               | $\mu\text{s}$ |
| $t_{rem}$                | Removal Time, Reset to Clock or $\bar{CE}$   | 5<br>10<br>15                  | 160<br>80<br>70                       | 80<br>40<br>35                       | –<br>–<br>–                | ns            |

6. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14557B

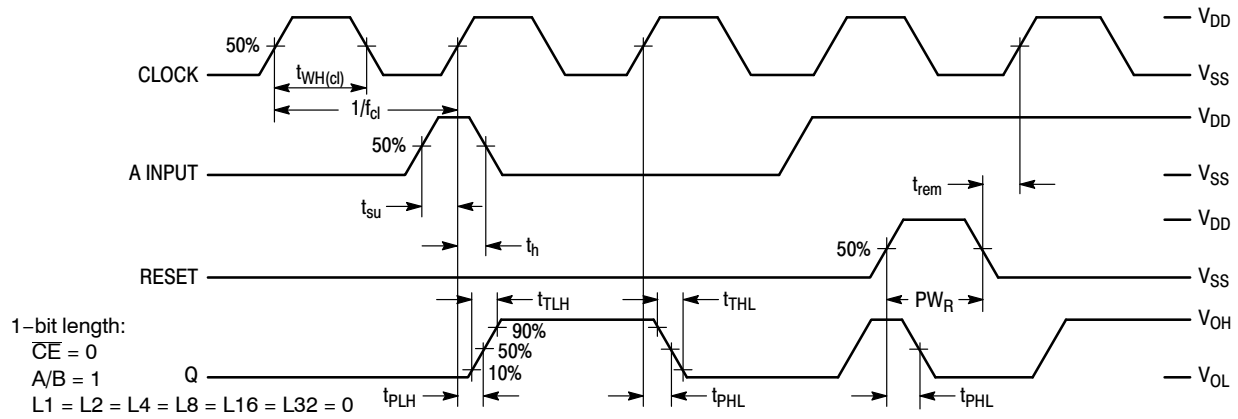


Figure 4. Timing Diagram

## ORDERING INFORMATION

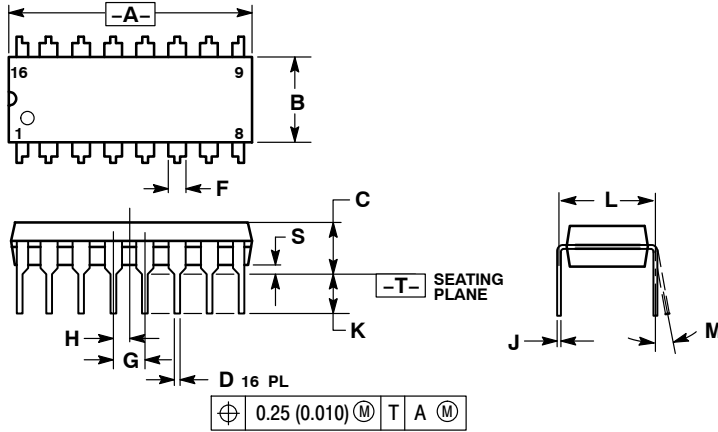
| Device        | Package                | Shipping <sup>†</sup> |
|---------------|------------------------|-----------------------|
| MC14557BFELG  | SOEIAJ-16<br>(Pb-Free) | 2000 / Tape & Reel    |
| MC14557BDWR2G | SO-16 (WB)             | 1000 / Tape & Reel    |
| MC14557BCPG   | PDIP-16<br>(Pb-Free)   | 500 Units / Rail      |
| MC14557BDWG   | SO-16 (WB)             | 47 Units / Rail       |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MC14557B

## PACKAGE DIMENSIONS

PDIP-16  
P SUFFIX  
CASE 648-08  
ISSUE T

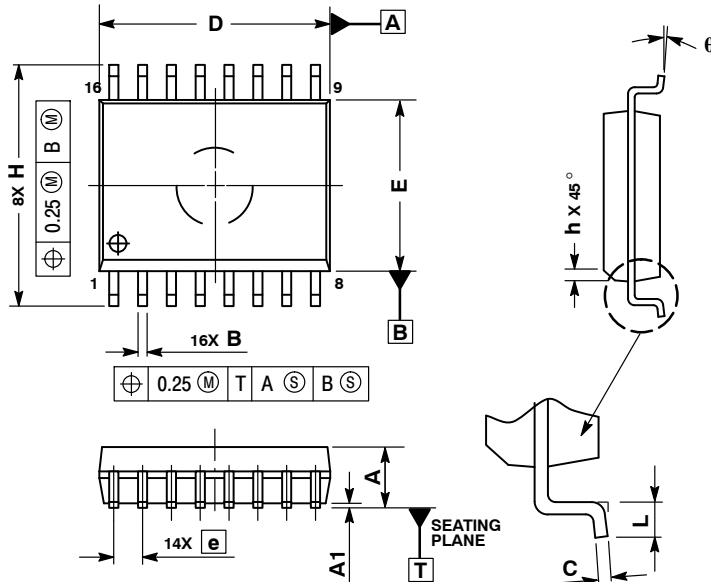


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 0.740     | 0.770 | 18.80       | 19.55 |
| B   | 0.250     | 0.270 | 6.35        | 6.85  |
| C   | 0.145     | 0.175 | 3.69        | 4.44  |
| D   | 0.015     | 0.021 | 0.39        | 0.53  |
| F   | 0.040     | 0.70  | 1.02        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| H   | 0.050 BSC |       | 1.27 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.130 | 2.80        | 3.30  |
| L   | 0.295     | 0.305 | 7.50        | 7.74  |
| M   | 0°        | 10°   | 0°          | 10°   |
| S   | 0.020     | 0.040 | 0.51        | 1.01  |

SO-16 WB  
DW SUFFIX  
CASE 751G-03  
ISSUE C



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

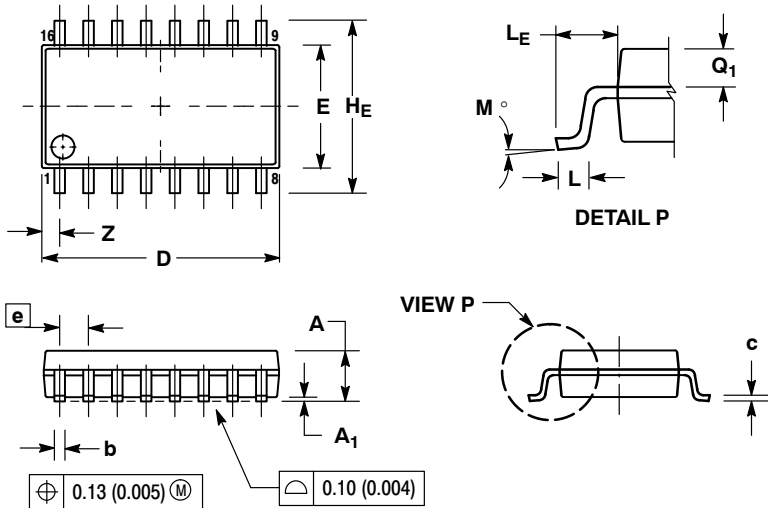
| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN         | MAX   |
| A   | 2.35        | 2.65  |
| A1  | 0.10        | 0.25  |
| B   | 0.35        | 0.49  |
| C   | 0.23        | 0.32  |
| D   | 10.15       | 10.45 |
| E   | 7.40        | 7.60  |
| e   | 1.27 BSC    |       |
| H   | 10.05       | 10.55 |
| h   | 0.25        | 0.75  |
| L   | 0.50        | 0.90  |
| q   | 0°          | 7°    |



# MC14557B

## PACKAGE DIMENSIONS

SOEIAJ-16  
CASE 966-01  
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.10        | 0.20  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.78  | ---       | 0.031 |

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