GENERAL DESCRIPTION

The XRT83VL38 is a fully integrated Octal (eight channel) long-haul and short-haul line interface unit for T1 (1.544Mbps) 100Ω, E1 (2.048Mbps) 75Ω or 120Ω, J1 110Ω or BITS Timing applications.

In long-haul applications the XRT83VL38 accepts signals that have been attenuated from 0 to 36dB at 772kHz in T1 mode (equivalent of 0 to 6000 feet of cable loss) or 0 to 43dB at 1024kHz in E1 mode.

In T1 applications, the XRT83VL38 can generate five transmit pulse shapes to meet the short-haul Digital Cross-Connect (DSX-1) template requirements as well as for Channel Service Units (CSU) Line Build Out (LBO) filters of 0dB, -7.5dB -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions (The arbitrary pulse generators are available in both T1 and E1 modes).

The XRT83VL38 provides both a parallel/serial **Host** microprocessor interface as well as a **Hardware** mode for programming and control.

Both the B8ZS and HDB3 encoding and decoding functions are selectable as well as AMI. Two on-chip crystal-less jitter attenuators with a 32 or 64 bit FIFO can be placed in the receive and the transmit paths with loop bandwidths of less than 3Hz. The XRT83VL38 provides a variety of loop-back and diagnostic features as well as transmit driver short circuit detection and receive loss of signal monitoring. It supports internal impedance matching for 75Ω, 100Ω, 110Ω and 120Ω for both transmitter and receiver. In the absence of the power supply, the transmit outputs and receive inputs are tri-stated allowing for redundancy applications The chip includes an integrated programmable clock multiplier that can synthesize T1 or E1 master.

APPLICATIONS

- BITS Timing
- T1 Digital Cross-Connects (DSX-1)
- ISDN Primary Rate Interface
- CSU/DSU E1/T1/J1 Interface
- T1/E1/J1 LAN/WAN Routers
- Public switching Systems and PBX Interfaces
- T1/E1/J1 Multiplexer and Channel Banks

Features (See Page 2)

FIGURE 1. BLOCK DIAGRAM OF THE XRT83VL38 T1/E1/J1 LIU (HOST MODE)

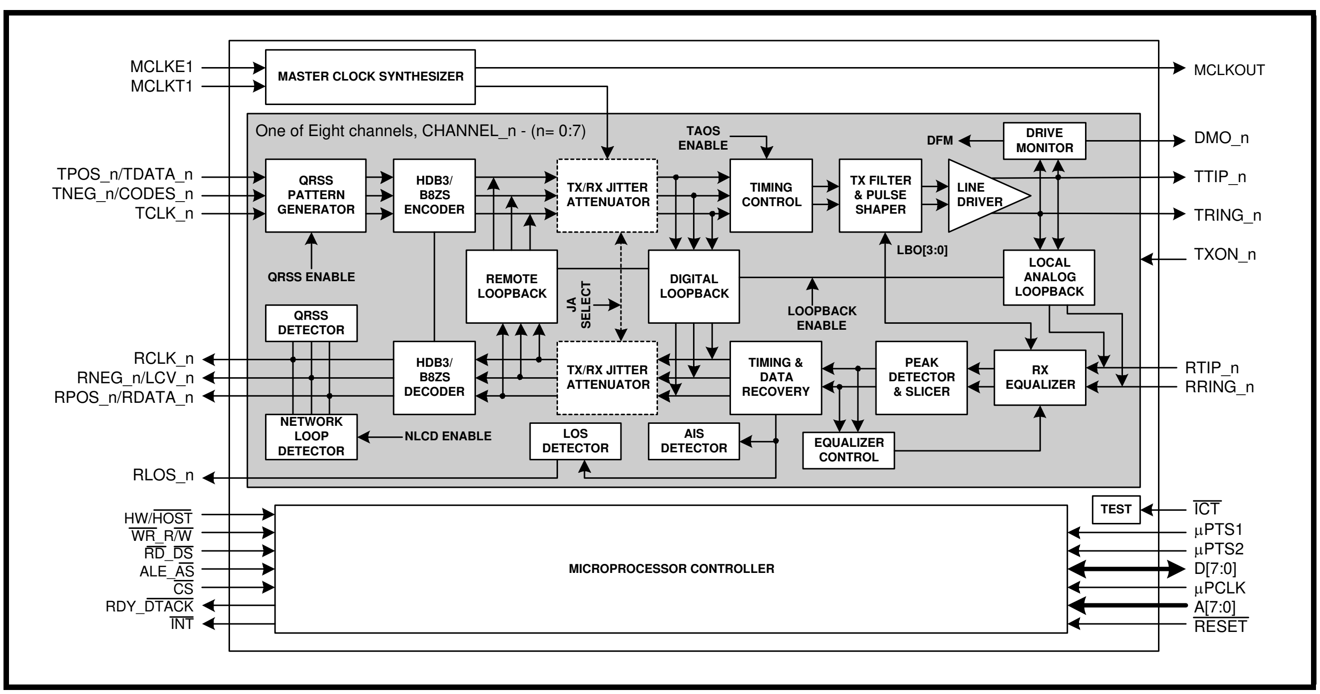
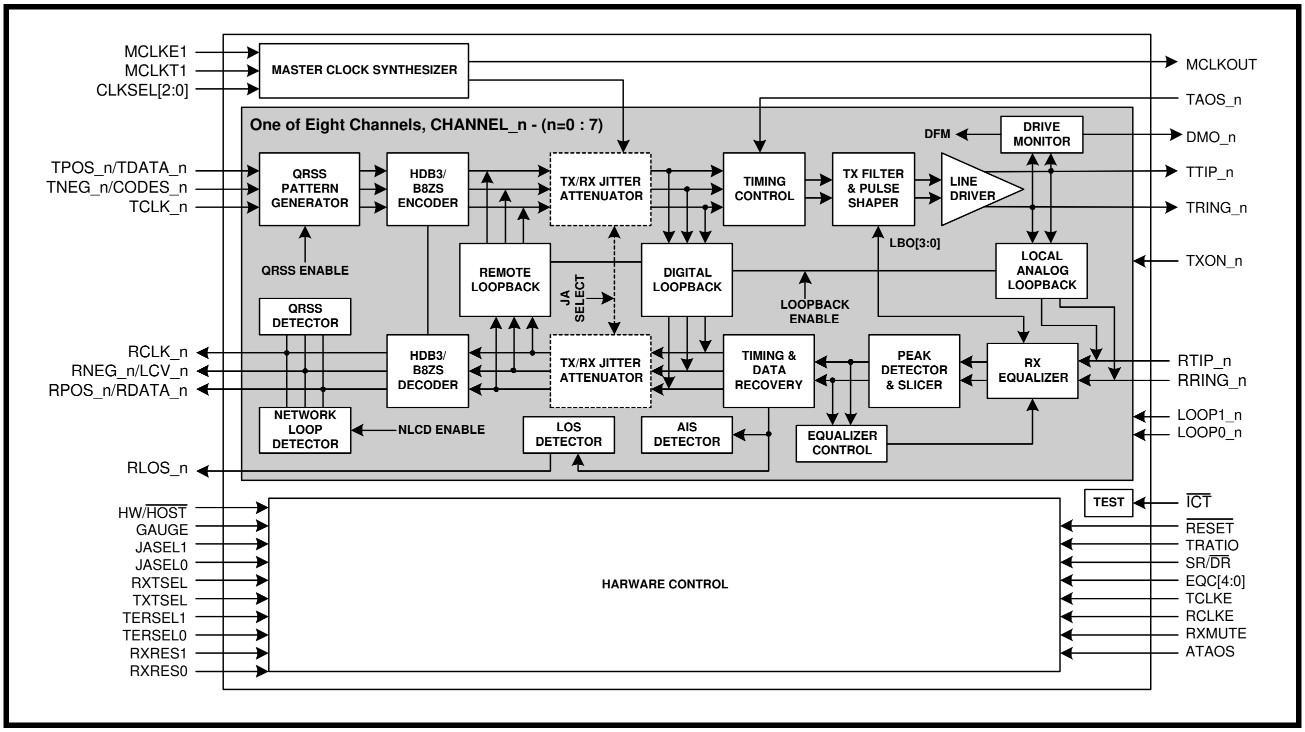


FIGURE 2. BLOCK DIAGRAM OF THE XRT83VL38 T1/E1/J1 LIU (HARDWARE MODE)



FEATURES

- Supports Section 13 - Synchronization Interface in ITU G.703 for both Transmit and Receive Paths
- Fully integrated eight channel long-haul or short-haul transceivers for E1,T1 or J1 applications
- Adaptive Receive Equalizer for up to 36dB cable attenuation
- Programable Transmit Pulse Shaper for E1,T1 or J1 short-haul interfaces
- Five fixed transmit pulse settings for T1 short-haul applications plus a fully programmable waveform generator for transmit output pulse shaping available for both T1 and E1 modes
- Transmit Line Build-Outs (LBO) for T1 long-haul application from 0dB to -22.5dB in three 7.5dB steps
- Selectable receiver sensitivity from 0 to 36dB cable loss for T1 @772kHz and 0 to 43dB for E1 @1024kHz
- Receive monitor mode handles 0 to 29dB resistive attenuation along with 0 to 6dB of cable attenuation for E1 and 0 to 3dB of cable attenuation for T1 modes
- Supports 75Ω and 120Ω (E1), 100Ω (T1) and 110Ω (J1) applications
- Internal and/or external impedance matching for 75Ω, 100Ω, 110Ω and 120Ω
- Tri-State transmit output and receive input capability for redundancy applications
- Provides High Impedance for Tx and Rx during power off
- Transmit return loss meets or exceeds ETSI 300-166 standard
- On-chip digital clock recovery circuit for high input jitter tolerance
- Crystal-less digital jitter attenuator with 32-bit or 64-bit FIFO selectable in transmit or receive paths
- On-chip frequency multiplier generates T1 or E1 Master clocks
- High receiver interference immunity
- On-chip transmit short-circuit protection and limiting, and driver fail monitor output (DMO)

- Receive loss of signal (RLOS) output
- On-chip HDB3/B8ZS/AMI encoder/decoder functions
- QRSS pattern generator and detection for testing and monitoring
- Error and Bipolar Violation Insertion and Detection
- Receiver Line Attenuation Indication Output in 1dB steps
- Network Loop-Code Detection for automatic Loop-Back Activation/Deactivation
- Transmit All Ones (TAOS) and In-Band Network Loop Up and Down code generators
- Supports Local Analog, Remote, Digital and Dual Loop-Back Modes
- Meets or exceeds T1 and E1 short-haul and long-haul network access specifications in ITU G.703, G.775, G.736 and G.823; TR-TSY-000499; ANSI T1.403 and T1.408; ETSI 300-166 and AT&T Pub 62411
- Supports both **Hardware** and **Host** (parallel or serial) Microprocessor interface for programming
- Programmable Interrupt
- Low power dissipation
- Logic inputs accept either 3.3V or 5V levels
- Dual 3.3V and 1.8V Supply Operation
- 225 ball BGA package
- -40°C to +85°C Temperature Range

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83VL38IB	225 Ball BGA	-40°C to +85°C

FIGURE 3. PACKAGE PIN OUT

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	DGND	RNEG_0	TCLK_1	TPOS_1	TAOS_2	RDY_$\overline{DTACK}$	ALE_$\overline{AS}$	CLKSEL0	DVDD	A[1]	A[3]	A[7]	TXON_0	JASEL0	TCLK_2	RLOS_3	RCLK_3	DVDD_DR
B	TDO	RPOS_0	RCLK_0	TCLK_0	TNEG_1	TAOS_1	$\overline{CS}$	CLKSEL1	DGND	A[2]	A[6]	TX0N_3	JASEL1	TPOS_2	TNEG_3	RNEG_3	RPOS_3	NC12
C	RTIP_0	RVDD_0	RLOS_0	TNEG_0	TPOS_0	TAOS_3	$\overline{RD}$_$\overline{DS}$	CLKSEL2	DGND	A[0]	A[5]	TXON_2	DMO_3	TCLK_3	DMO_2	TTIP_3	TGND_3	RTIP_3
D	RRING_0	RGND_0	TGND_0	DMO_1	DMO_0	TAOS_0	$\overline{WR}$_R/$\overline{W}$	DGND	DVDD_DR	DVDD_PDR	A[4]	TXON_1	TNEG_2	TPOS_3	RPOS_2	RVDDD_3	RGND_3	RRING_3
E	TMS	TRING_O	TTIP_0	TVDD_0	RVDD_1										TGND_2	TRING_3	TVDD_3	NC11
F	RRING_1	TGND_1	TRING_1	TVDD_1											TRING_2	TVDD_2	TTIP_2	RRING_2
G	RTIP_1	RPOS_1	RGND_1	TTIP_1											DGND	RVDD_2	RGND_2	RTIP_2
H	MCLKOUT	RNEG_1	RCLK_1	RLOS_1											RLOS_2	RCLK_2	DGND	RNEG_2
J	MCLKE1	VDDPLL_2	VDDPLL_1	DVDD_DR											RLOS_6	PTS1	AGND_BIAS	GAUGE
K	MCLKT1	DGND	GNDPLL_1	SR_$\overline{DR}$											DVDD_DR	RXON	AVDD_BIAS	DVDDD_µP
L	RTIP_5	RLOS_5	RCLK_5	GNDPLL_2											PTS2	$\overline{INT}$	RPOS_6	RTIP_6
M	RRING_5	RGND_5	RPOS_5	RNEG_5											RCLK_6	RNEG_6	RGND_6	RRING_6
N	TCK	TTIP_5	RVDD_5	TRING_5											TVDD_6	TTIP_6	RVDD_6	SENSE
P	TVDD_5	TRING_4	TGND_5	DMO_5											TVDD_7	TTIP_7	TRING_7	SER_$\overline{PAR}$
R	TDI	TTIP_4	TGND_4	TVDD_4	DMO_4	TAOS_7	D[0]	DGND	DVDD_DR	RXRES1	TERSEL0	TXON_6	TXON_7	TNEG_7	TRING_6	TGND_7	RGND_7	RRING_7
T	RRING_4	RGND_4	TCLK_4	RNEG_4	TCLK_5	TAOS_4	D[7]	$\overline{RESET}$	DGND	HW_$\overline{HOST}$	TERSEL1	RXMUTE	µPCLK	TPOS_7	RLOS_7	TGND_6	RPOS_7	RTIP_7
U	RTIP_4	RPOS_4	RCLK_4	TNEG_4	TPOS_5	TAOS_5	D[6]	D[2]	D[1]	DVDD_PDR	RXTSEL	TEST	TXON_5	TNEG_6	TCLK_7	RCLK_7	DMO_6	RVDD_7
V	DVDD_PDR	RVDD_4	RLOS_4	TPOS_4	TNEG_5	TAOS_6	D[5]	D[4]	D[3]	RXRES0	TXTSEL	$\overline{ICT}$	TXON_4	DMO_7	TPOS_6	TCLK_6	RNEG_7	DGND

XRT83VL38
(Top View)

225 Ball BGA

PIN DESCRIPTION BY FUNCTION

RECEIVE SECTIONS

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RxON	K16	**I**	**Receiver On - Harware Mode** Writing a "1" to this pin in **Hardware** mode turns on the Receive Sections of all channels. Writing a "0" shuts off the Receiver Sections of all channels.
RLOS_0	C3	**O**	**Receiver Loss of Signal for Channel_ 0:** This output signal goes "High" for at least one RCLK_0 cycle to indicate loss of signal at the receive 0 input. RLOS will remain "High" for the entire duration of the Loss of Signal detected by the receiver logic. **SEE"RECEIVER LOSS OF SIGNAL (RLOS)" ON PAGE 25.**
RLOS_1	H4		**Receiver Loss of Signal for Channel _1**
RLOS_2	H15		**Receiver Loss of Signal for Channel _2**
RLOS_3	A16		**Receiver Loss of Signal for Channel _3**
RLOS_4	V3		**Receiver Loss of Signal for Channel _4**
RLOS_5	L2		**Receiver Loss of Signal for Channel_ 5**
RLOS_6	J15		**Receiver Loss of Signal for Channel _6**
RLOS_7	T15		**Receiver Loss of Signal for Channel _7**
RCLK_0	B3	**O**	**Receiver Clock Output for Channel _0**
RCLK_1	H3		**Receiver Clock Output for Channel _1**
RCLK_2	H16		**Receiver Clock Output for Channel _2**
RCLK_3	A17		**Receiver Clock Output for Channel _3**
RCLK_4	U3		**Receiver Clock Output for Channel _4**
RCLK_5	L3		**Receiver Clock Output for Channel _5**
RCLK_6	M15		**Receiver Clock Output for Channel _6**
RCLK_7	U16		**Receiver Clock Output for Channel _7**
RNEG_0	A2	**O**	**Receiver Negative Data Output for Channel_0 - Dual-Rail mode** This signal is the receive negative-rail output data.
LCV_0	A2		**Line Code Violation Output for Channel_0 - Single-Rail mode** This signal goes "High" for one RCLK_0 cycle to indicate a code violation is detected in the received data of Channel _0. If AMI coding is selected, every bipolar violation received will cause this pin to go "High".
RNEG_1	H2		**Receiver Negative Data Output for Channel _1**
LCV_1			**Line Code Violation Output for Channel _1**
RNEG_2	H18		**Receiver Negative Data Output for Channel _2**
LCV_2			**Line Code Violation Output for Channel _2**
RNEG_3	B16		**Receiver Negative Data Output for Channel _3**
LCV_3			**Line Code Violation Output for Channel _3**
RNEG_4	T4		**Receiver Negative Data Output for Channel _4**
LCV_4			**Line Code Violation Output for Channel _4**
RNEG_5	M4		**Receiver Negative Data Output for Channel _5**
LCV_5			**Line Code Violation Output for Channel _5**
RNEG_6	M16		**Receiver Negative Data Output for Channel _6**
LCV_6			**Line Code Violation Output for Channel _6**
RNEG_7	V17		**Receiver Negative Data Output for Channel _7**
LCV_7			**Line Code Violation Output for Channel _7**

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RPOS_0	B2	**O**	**Receiver Positive Data Output for Channel _0 - Dual-Rail mode**
			This signal is the receive positive-rail output data sent to the Framer.
			Receiver NRZ Data Output for Channel _0 - Single-Rail mode
RDATA_0	B2		This signal is the receive output data.
			Receiver Positive Data Output for Channel _1
RPOS_1	G2		**Receiver NRZ Data Output for Channel _1**
RDATA_1			**Receiver Positive Data Output for Channel _2**
RPOS_2	D15		**Receiver NRZ Data Output for Channel _2**
RDATA_2			**Receiver Positive Data Output for Channel _3**
RPOS_3	B17		**Receiver NRZ Data Output for Channel _3**
RDATA_3			**Receiver Positive Data Output for Channel _4**
RPOS_4	U2		**Receiver NRZ Data Output for Channel _4**
RDATA_4			**Receiver Positive Data Output for Channel _5**
RPOS_5	M3		**Receiver NRZ Data Output for Channel _5**
RDATA_5			**Receiver Positive Data Output for Channel _6**
RPOS_6	L17		**Receiver NRZ Data Output for Channel 6**
RDATA_6			**Receiver Positive Data Output for Channel _7**
RPOS_7	T17		**Receiver NRZ Data Output for Channel _7**
RDATA_7			
RTIP_0	C1	**I**	**Receiver Differential Tip Input for Channel _0**
			Positive differential receive input from the line
RTIP_1	G1		**Receiver Differential Tip Input for Channel _1**
RTIP_2	G18		**Receiver Differential Tip Input for Channel _2**
RTIP_3	C18		**Receiver Differential Tip Input for Channel _3**
RTIP_4	U1		**Receiver Differential Tip Input for Channel _4**
RTIP_5	L1		**Receiver Differential Tip Input for Channel _5**
RTIP_6	L18		**Receiver Differential Tip Input for Channel _6**
RTIP_7	T18		**Receiver Differential Tip Input for Channel _7**
RRING_0	D1	**I**	**Receiver Differential Ring Input for Channel _0**
			Negative differential receive input from the line
RRING_1	F1		**Receiver Differential Ring Input for Channel _1**
RRING_2	F18		**Receiver Differential Ring Input for Channel _2**
RRING_3	D18		**Receiver Differential Ring Input for Channel _3**
RRING_4	T1		**Receiver Differential Ring Input for Channel _4**
RRING_5	M1		**Receiver Differential Ring Input for Channel _5**
RRING_6	M18		**Receiver Differential Ring Input for Channel _6**
RRING_7	R18		**Receiver Differential Ring Input for Channel _7**
RXMUTE	T12	**I**	**Receive Data Muting** When a LOS condition occurs, the outputs RPOS_n/RNEG_n will be muted, (forced to ground) to prevent data chattering. Tie this pin "Low" to disable the muting function. ***NOTES:*** 1. *This pin is internally pulled "High" with a 50kΩ resistor.* 2. *In **Hardware mode**, all receive channels share the same RXMUTE control function.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RXRES1 RXRES0	R10 V10	I	**Receive External Resistor Control Pins - Hardware mode** **Receive External Resistor Control Pin 1:** **Receive External Resistor Control Pin 0:** These pins determine the value of the external Receive fixed resistor according to the following table: *(see table below)* **NOTE:** *These pins are internally pulled "Low" with a 50kΩ resistor.*
RCLKE µPTS1	J16 J16	I	**Receive Clock Edge - Hardware mode** Set this pin "High" to sample RPOS_N/RNEG_n on the falling edge of RCLK_n. With this pin tied "Low", output data are updated on the rising edge of RCLK_n. **Microprocessor Type Select Input pin 1 - Host mode** This pin along with µPTS2 (pin 128) is used to select the microprocessor type. **SEE"MICROPROCESSOR TYPE SELECT INPUT PINS - HOST MODE:" ON PAGE 12.** **NOTE:** *This pin is internally pulled "Low" with a 50kΩ resistor.*

RXRES1	RXRES0	Required Fixed External RX Resistor
0	0	No External Fixed Resistor
0	1	240Ω
1	0	210Ω
1	1	150Ω

TRANSMITTER SECTIONS

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
E µPTS2	L15 L15	I	**Transmit Clock Edge - Hardware mode** Set this pin "High" to sample transmit input data on the rising edge of TCLK_n. With this pin tied "Low", input data are sampled on the falling edge of TCLK_n. **Microprocessor Type Select Input pin 2 - Host mode** This pin along with µPTS1 (pin 133) selects the microprocessor type. **SEE"MICROPROCESSOR TYPE SELECT INPUT PINS - HOST MODE:" ON PAGE 12.** **NOTE:** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TTIP_0	E3	O	**Transmitter Tip Output for Channel _0** Positive differential transmit output to the line.
TTIP_1	G4		**Transmitter Tip Output for Channel _1**
TTIP_2	F17		**Transmitter Tip Output for Channel _2**
TTIP_3	C16		**Transmitter Tip Output for Channel _3**
TTIP_4	R2		**Transmitter Tip Output for Channel _4**
TTIP_5	N2		**Transmitter Tip Output for Channel _5**
TTIP_6	N16		**Transmitter Tip Output for Channel _6**
TTIP_7	P16		**Transmitter Tip Output for Channel _7**

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TRING_0	E2	O	**Transmitter Ring Output for Channel _0** Negative differential transmit output to the line.
TRING_1	F3		**Transmitter Ring Output for Channel _1**
TRING_2	F15		**Transmitter Ring Output for Channel _2**
TRING_3	E16		**Transmitter Ring Output for Channel _3**
TRING_4	P2		**Transmitter Ring Output for Channel _4**
TRING_5	N4		**Transmitter Ring Output for Channel _5**
TRING_6	R15		**Transmitter Ring Output for Channel _6**
TRING_7	P17		**Transmitter Ring Output for Channel _7**
TPOS_0	C5	I	**Transmitter Positive Data Input for Channel _0 - Dual-Rail mode** This signal is the positive-rail input data for transmitter 0.
TDATA_0			**Transmitter 0 Data Input - Single-Rail mode** This pin is used as the NRZ input data for transmitter 0.
TPOS_1	A4		**Transmitter Positive Data Input for Channel _1**
TDATA_1			**Transmitter 1 Data Input**
TPOS_2	B14		**Transmitter Positive Data Input for Channel _2**
TDATA_2			**Transmitter 2 Data Input**
TPOS_3	D14		**Transmitter Positive Data Input for Channel _3**
TDATA_3			**Transmitter 3 Data Input**
TPOS_4	V4		**Transmitter Positive Data Input for Channel _4**
TDATA_4			**Transmitter 4 Data Input**
TPOS_5	U5		**Transmitter Positive Data Input for Channel _5**
TDATA_5			**Transmitter 5 Data Input**
TPOS_6	V15		**Transmitter Positive Data Input for Channel _6**
TDATA_6			**Transmitter 6 Data Input**
TPOS_7	T14		**Transmitter Positive Data Input for Channel _7**
TDATA_7			**Transmitter 7 Data Input** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for each channel.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TNEG_0	C4	**I**	**Transmitter Negative NRZ Data Input for Channel _0** **Dual-Rail mode** This signal is the negative-rail input data for transmitter 0. **Single-Rail mode** This pin can be left unconnected.
CODES_0	C4		**Coding Select for Channel _0 - Hardware mode and Single-Rail mode** Connecting this pin “Low” enables HDB3 in E1 or B8ZS in T1 encoding and decoding for Channel _0. Connecting this pin “High” selects AMI data format.
TNEG_1	B5		**Transmitter Negative NRZ Data Input for Channel _1**
CODES_1			**Coding Select for Channel _1**
TNEG_2	D13		**Transmitter Negative NRZ Data Input for Channel _2**
CODES_2			**Coding Select for Channel _2**
TNEG_3	B15		**Transmitter Negative NRZ Data Input for Channel _3**
CODES_3			**Coding Select for Channel _3**
TNEG_4	U4		**Transmitter Negative NRZ Data Input for Channel _4**
CODES_4			**Coding Select for Channel _4**
TNEG_5	V5		**Transmitter Negative NRZ Data Input for Channel _5**
CODES_5			**Coding Select for Channel _5**
TNEG_6	U14		**Transmitter Negative NRZ Data Input for Channel _6**
CODES_6			**Coding Select for Channel _6**
TNEG_7	R14		**Transmitter Negative NRZ Data Input for Channel _7**
CODES_7			**Coding Select for Channel _7** **NOTE:** *Internally pulled “Low” with a 50kΩ resistor for each channel.*
TCLK_0	B4	**I**	**Transmitter Clock Input for Channel _0 - Host mode and Hardware mode** **E1** rate at 2.048MHz ± 50ppm. **T1** rate at 1.544MHz ± 32ppm. During normal operation TCLK_0 is used for sampling input data at TPOS_0/ TDATA_0 and TNEG_0/CODES_0 while MCLK is used as the timing reference for the transmit pulse shaping circuit.
TCLK_1	A3		**Transmitter Clock Input for Channel _1**
TCLK_2	A15		**Transmitter Clock Input for Channel _2**
TCLK_3	C14		**Transmitter Clock Input for Channel _3**
TCLK_4	T3		**Transmitter Clock Input for Channel _4**
TCLK_5	T5		**Transmitter Clock Input for Channel _5**
TCLK_6	V16		**Transmitter Clock Input for Channel _6**
TCLK_7	U15		**Transmitter Clock Input for Channel _7** **NOTE:** *Internally pulled “Low” with a 50kΩ resistor for all channels.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TAOS_0	D6	**I**	**Transmit All Ones for Channel _0 - Hardware mode** Setting this pin "High" enables the transmission of an "All Ones" Pattern from Channel _0. A "Low" level stops the transmission of the "All Ones" Pattern.
TAOS_1	B6		**Transmit All Ones for Channel _1**
TAOS_2	A5		**Transmit All Ones for Channel _2**
TAOS_3	C6		**Transmit All Ones for Channel _3**
TAOS_4	T6		**Transmit All Ones for Channel _4**
TAOS_5	U6		**Transmit All Ones for Channel _5**
TAOS_6	V6		**Transmit All Ones for Channel _6**
TAOS_7	R6		**Transmit All Ones for Channel _7** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*
TXON_0	A13	**I**	**Transmitter Turn On for Channel _0** **Hardware mode** Setting this pin "High" turns on the Transmit and Receive Sections of Channel _0. When TXON_0 = "0" then TTIP_0 and TRING_0 driver outputs will be tri-stated. **In Host mode** The TXON_n bits in the channel control registers turn each channel Transmit and Receive section ON or OFF. However, control of the on/off function can be transferred to the **Hardware** pins by setting the TXONCNTL bit (bit 7) to "1" in the register at address hex 0x82.
TXON_1	D12		**Transmitter Turn On for Channel _1**
TXON_2	C12		**Transmitter Turn On for Channel _2**
TXON_3	B12		**Transmitter Turn On for Channel _3**
TXON_4	V13		**Transmitter Turn On for Channel _4**
TXON_5	U13		**Transmitter Turn On for Channel _5**
TXON_6	R12		**Transmitter Turn On for Channel _6**
TXON_7	R13		**Transmitter Turn On for Channel _7** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor for all channels.*

MICROPROCESSOR INTERFACE

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
HW_$\overline{\text{HOST}}$	T10	I	**Mode Control Input** This pin selects **Hardware** or **Host mode**. Leave this pin unconnected or tie "High" to select **Hardware mode**. For **Host mode**, this pin must be tied "Low". *NOTE: Internally pulled "High" with a 50kΩ resistor.*
$\overline{\text{WR}}$_R/$\overline{\text{W}}$	D7	I	**Write Input (Read/Write) - Host mode:** **Intel bus timing**: A "Low" pulse on $\overline{\text{WR}}$ selects a write operation when $\overline{\text{CS}}$ pin is "Low". **Motorola bus timing:** A "High" pulse on R/$\overline{\text{W}}$ selects a read operation and a "Low" pulse on R/$\overline{\text{W}}$ selects a write operation when $\overline{\text{CS}}$ is "Low".
EQC0	D7		**Equalizer Control Input pin 0 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31. *NOTE: Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{RD}}$_$\overline{\text{DS}}$	C7	I	**Read Input (Data Strobe) - Host mode** **Intel bus timing:** A "Low" pulse on $\overline{\text{RD}}$ selects a read operation when the $\overline{\text{CS}}$ pin is "Low". **Motorola bus timing:** A "Low" pulse on $\overline{\text{DS}}$ indicates a read or write operation when the $\overline{\text{CS}}$ pin is "Low".
EQC1	C7		**Equalizer Control Input pin 1 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31. *NOTE: Internally pulled "Low" with a 50kΩ resistor.*
ALE_$\overline{\text{AS}}$	A7	I	**Address Latch Input (Address Strobe) - Host mode** **Intel bus timing:** The address inputs are latched into the internal register on the falling edge of ALE. **Motorola bus timing:** The address inputs are latched into the internal register on the falling edge of $\overline{\text{AS}}$.
EQC2	A7		**Equalizer Control Input pin 2 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31. *NOTE: Internally pulled "Low" with a 50kΩ resistor.*
$\overline{\text{CS}}$	B7	I	**Chip Select Input - Host mode:** This signal must be "Low" in order to access the parallel port.
EQC3	B7		**Equalizer Control Input pin 3 - Hardware mode:** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31. *NOTE: Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RDY_DTACK	A6	O	**Ready Output (Data Transfer Acknowledge Output) - Host mode** **Intel bus timing**: RDY is asserted "High" to indicate the device has completed a read or write operation. **Motorola bus timing**: DTACK is asserted "Low" to indicate the device has completed a read or write cycle.
EQC4	A6	I	**Equalizer Control Input pin 4 - Hardware mode** Pins EQC0, EQC1, EQC2, EQC3 and EQC4 select the Receive Equalizer and Transmitter Line Build Out. SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31. *NOTE: Internally pulled "Low" with a 50kΩ resistor.*
			Microprocessor Type Select Input Pins - Host Mode:
µPTS1	J16	I	**Microprocessor Type Select Input Bit 1**
µPTS2	L15		**Microprocessor Type Select Input Bit 2**

µPTS2	µPTS1	µP Type
0	0	Intel 8051 Asynchronous
0	1	Motorola Asynchronous
1	0	Power PC Synchronous
1	1	MPC8xx Motorola Synchronous

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
RCLKE	J16		**Receive Clock Edge - Hardware mode** SEE"RECEIVE CLOCK EDGE - HARDWARE MODE" ON PAGE 7.
TCLKE	L15		**Transmit Clock Edge - Hardware mode** SEE"TRANSMIT CLOCK EDGE - HARDWARE MODE" ON PAGE 7. *NOTE: These pins are internally pulled "Low" with a 50kΩ resistor.*
			Microprocessor Read/Write Data Bus Pins - Host mode
D[7]	T7	I/O	**Data Bus[7]**
D[6]	U7		**Data Bus[6]**
D[5]	V7		**Data Bus[5]**
D[4]	V8		**Data Bus[4]**
D[3]	V9		**Data Bus[3]**
D[2]	U8		**Data Bus[2]**
D[1]	U9		**Data Bus[1]**
D[0]/SDO	R7		**Data Bus[0]** if SER_PAR = 0 **or Serial Data Input** if SER_PAR = 1
			Loop-back Control Pins, Bits [1:0] Channel_[7:4] - Hardware Mode Pins 67-74 and 173-180 control which Loop-Back mode is selected per channel. SEE"LOOP-BACK CONTROL PINS, BITS [1:0] CHANNEL_[7:0]" ON PAGE 17. *NOTE: Internally pulled "Low" with a 50kΩ resistor for all channels.*
LOOP1_4	T7		
LOOP0_4	U7		
LOOP1_5	V7		
LOOP0_5	V8		
LOOP1_6	V9		
LOOP0_6	U8		
LOOP1_7	U9		
LOOP0_7	R7		

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
 A[7] A[6] A[5] A[4] A[3] A[2] A[1] A[0]/SDI	 A12 B11 C11 D11 A11 B10 A10 C10	 I	**Microprocessor Interface Address Bus Pins** - **Host mode:** **Microprocessor Interface Address Bus[7]** **Microprocessor Interface Address Bus[6]** **Microprocessor Interface Address Bus[5]** **Microprocessor Interface Address Bus[4]** **Microprocessor Interface Address Bus[3]** **Microprocessor Interface Address Bus[2]** **Microprocessor Interface Address Bus[1]** **Microprocessor Interface Address Bus[0]** if SER_$\overline{\text{PAR}}$ = 0 **or Serial Data Input** if SER_$\overline{\text{PAR}}$ = 1
 LOOP1_3 LOOP0_3 LOOP1_2 LOOP0_2 LOOP1_1 LOOP0_1 LOOP1_0 LOOP0_0	 A12 B11 C11 D11 A11 B10 A10 C10		**Loop-back Control Pins, Bits [1:0] Channel_[3:0]** In **Hardware mode**, pins 67-74 and 173-180 control which Loop-Back mode is selected per channel. **SEE"LOOP-BACK CONTROL PINS, BITS [1:0] CHANNEL_[7:0]" ON PAGE 17.** **NOTE:** *These pins are internally pulled "Low" with a 50kΩ resistor.*
µPCLK/SCLK	T13	I	**Microprocessor Clock Input - Host Mode:** **µPCLK -** Input clock for synchronous parrallel microprocessor operation. Maximum clock rate is 54 MHz, SER_$\overline{\text{PAR}}$ = 0 **SCLK** - Input serial clock for SPI interface, SER_$\overline{\text{PAR}}$ = 1 **NOTE:** *This pin is internally pulled "Low" with a 50kΩ resistor for asynchronous microprocessor interface when no clock is present.*
ATAOS	T13		**Automatic Transmit "All Ones" - Hardware mode** This pin functions as an Automatic Transmit "All Ones". **SEE"AUTOMATIC TRANSMIT "ALL ONES" PATTERN - HARDWARE MODE" ON PAGE 16.**
$\overline{\text{INT}}$	L16	O	**Interrupt Output - Host mode** This pin goes "Low" to indicate an alarm condition has occurred within the device. Interrupt generation can be globally disabled by setting the GIE bit to a "0" in the command control register.
TRATIO	L16	I	**Transmitter Transformer Ratio Select - Hardware mode** TRATIO is Not Supported in the 83VL38. This pin is for $\overline{\text{INT}}$ only. **NOTE:** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*

JITTER ATTENUATOR

Signal Name	Lead #	Type	Description
JASEL0 JASEL1	A14 B13	I	**Jitter Attenuator Select Pins Hardware Mode** **Jitter Attenuator select Bit 0** **Jitter Attenuator select Bit 1** JASEL[1:0] pins are used to place the jitter attenuator in the transmit path, the receive path or to disable it. <table><tr><th>JASEL1</th><th>JASEL0</th><th>JA PATH</th></tr><tr><td>0</td><td>0</td><td>Disabled</td></tr><tr><td>0</td><td>1</td><td>Transmit Path</td></tr><tr><td>1</td><td>0</td><td>Receive Path</td></tr><tr><td>1</td><td>1</td><td>Rx & Tx Paths</td></tr></table>**Note:** *These pins are internally pulled “Low” with 50kΩ resistors.*

CLOCK SYNTHESIZER

Signal Name	Lead #	Type	Description
MCLKOUT	H1	O	**Synthesized Master Clock Output** This signal is the output of the Master Clock Synthesizer PLL which is at T1 or E1 rate based upon the mode of operation.
MCLKT1	K1	I	**T1 Master Clock Input** This signal is an independent 1.544MHz clock for T1 systems with accuracy better than ±50ppm and duty cycle within 40% to 60%. MCLKT1 is used in the T1 mode. **Notes:** 1. *All channels of the XRT83VL38 must be operated at the same clock rate, either T1, E1 or J1.* 2. *See pin 26 description for further explanation for the usage of this pin.* 3. *Internally pulled “Low” with a 50kΩ resistor.*
MCLKE1	J1	I	**E1 Master Clock Input** A 2.048MHz clock for with an accuracy of better than ±50ppm and a duty cycle of 40% to 60% can be provided at this pin. In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. **Notes:** 1. *All channels of the XRT83VL38 must be operated at the same clock rate, either T1, E1 or J1.* 2. *Internally pulled “Low” with a 50kΩ resistor.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
CLKSEL0 **CLKSEL1** **CLKSEL2**	A8 B8 C8	**I**	**Clock Select inputs for Master Clock Synthesizer - Hardware mode** CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an external accurate clock source according to the table below. In **Hardware mode,** the MCLKRATE control signal is generated from the state of EQC[4:0] inputs. In **Host mode,** the state of these pins are ignored and the master frequency PLL is controlled by the corresponding interface bits. See **Table 40** register address 10000001

MCLKE1 kHz	MCLKT1 kHz	CLKSEL 2	CLKSEL1	CLKSEL0	MCLKRATE	CLKOUT kHz
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544

NOTE: *These pins are internally pulled "Low" with a 50kΩ resistor.*

ALARM FUNCTIONS/REDUNDANCY SUPPORT

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
GAUGE	J18	**I**	**Twisted Pair Cable Wire Gauge Select - Hardware Mode** Connect this pin "High" to select 26 Gauge wire. Connect this pin "Low" to select 22 and 24 gauge wire for all channels. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
DMO_0	D5	**O**	**Driver Failure Monitor Channel _0:** This pin transitions "High" if a short circuit condition is detected in the transmit driver of Channel _0, or no transmit output pulse is detected for more than 128 TCLK_0 cycles.
DMO_1	D4		**Driver Failure Monitor Channel _1**
DMO_2	C15		**Driver Failure Monitor Channel _2**
DMO_3	C13		**Driver Failure Monitor Channel _3**
DMO_4	R5		**Driver Failure Monitor Channel _4**
DMO_5	P4		**Driver Failure Monitor Channel _5**
DMO_6	U17		**Driver Failure Monitor Channel _6**
DMO_7	V14		**Driver Failure Monitor Channel _7**
ATAOS	T13	**I**	**Automatic Transmit "All Ones" Pattern - Hardware Mode** A "High" level on this pin enables the automatic transmission of an "All Ones" AMI pattern from the transmitter of any channel that the receiver of that channel has detected an LOS condition. A "Low" level on this pin disables this function. *Note: All channels share the same ATAOS control function.*
µPCLK/SCLK	T13		**Microprocessor Clock Input - Host mode** **SEE"MICROPROCESSOR CLOCK INPUT - HOST MODE:" ON PAGE 13.** ***NOTE:*** *This pin is internally pulled "Low" for asynchronous microprocessor interface when no clock is present.*
TRATIO	L16	**I**	**Transmitter Transformer Ratio Select - Hardware mode** TRATIO is Not Supported in the 83VL38. This pin is for $\overline{\text{INT}}$ only..
$\overline{\text{INT}}$	L16	**O**	**Interrupt Output - Host mode** This pin is asserted "Low" to indicate an alarm condition. **SEE"INTERRUPT OUTPUT - HOST MODE" ON PAGE 13.** ***NOTE:*** *This pin is an open drain output and requires an external 10kΩ pull-up resistor.*
$\overline{\text{RESET}}$	T8	**I**	**Hardware Reset (Active "Low"):** When this pin is tied "Low" for more than 10µs, the device is put in the reset state. **Exar recommends initiating a Harware reset upon power up.** ***NOTE:*** *This pin is internally pulled "High" with a 50kΩ resistor.*
SR/$\overline{\text{DR}}$	K4	**I**	**Single-Rail/Dual-Rail Data Format:** Connect this pin "Low" to select transmit and receive data format in **Dual-Rail mode**. In this mode, HDB3 or B8ZS encoder and decoder are not available. Connect this pin "High" to select **single-rail data format**. ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
			Loop-back Control Pins, Bits [1:0] Channel_[7:0]
LOOP1_0	A10	**I**	**Loop-back Control bit 1, Channel _0**
LOOP0_0	C10		**Loop-back Control bit 0, Channel _0**
LOOP1_1	A11		**Loop-back Control bit 1, Channel _1**
LOOP0_1	B10		**Loop-back Control bit 0, Channel _1**
LOOP1_2	C11		**Loop-back Control bit 1, Channel _2**
LOOP0_2	D11		**Loop-back Control bit 0, Channel _2**
LOOP1_3	A12		**Loop-back Control bit 1, Channel _3**
LOOP0_3	B11		**Loop-back Control bit 0, Channel _3**
LOOP1_4	T7		**Loop-back Control bit 1, Channel _4**
LOOP0_4	U7		**Loop-back Control bit 0, Channel _4**
LOOP1_5	V7		**Loop-back Control bit 1, Channel _5**
LOOP0_5	V8		**Loop-back Control bit 0, Channel _5**
LOOP1_6	V9		**Loop-back Control bit 1, Channel _6**
LOOP0_6	U8		**Loop-back Control bit 0, Channel _6**
LOOP1_7	U9		**Loop-back Control bit 1, Channel _7**
LOOP0_7	R7		**Loop-back Control bit 0, Channel _7**
			In Hardware mode, these pins control the Loop-Back mode for each channel_n per the following table.

LOOP1_n	LOOP0_n	MODE
0	0	Normal Mode No Loop-Back Channel_n
0	1	Local Loop-Back Channel_n
1	0	Remote Loop-Back Channel_n
1	1	Digital Loop-Back Channel_n

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
A[1]	A10		**Microprocessor Address A[7:0] and Data Bus Pins D[7:0] - Host mode**
A[0]/SDI	C10		These pins are microprocessor address and data bus pins. **SEE"MICROPROCESSOR INTERFACE ADDRESS BUS PINS - HOST MODE:" ON PAGE 13.** and **see "Microprocessor Read/Write Data Bus Pins - Host mode" on page 12.**
A[3]	A11		**NOTE:** *These pins are internally pulled "Low" with a 50kΩ resistor.*
A[2]	B10		
A[5]	C11		
A[4]	D11		
A[7]	A12		
A[6]	B11		
D[7]	T7		
D[6]	U7		
D[5]	V7		
D[4]	V8		
D[3]	V9		
D[2]	U8		
D[1]	U9		
D[0]/SDO	R7		

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
EQC4	A6	I	**Equalizer Control Input 4 - Hardware mode** This pin together with pins EQC[3:0] is used to control the transmit pulse shaping, transmit line build-out (LBO) and receive monitoring while operating at one of either the T1, E1 or J1 clock rates/modes. **SEE"RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS" ON PAGE 31.** for description of Transmit Equalizer Control bits.
EQC3	B7	I	**Equalizer Control Input 3**
EQC2	A7	I	**Equalizer Control Input 2**
EQC1	C7	I	**Equalizer Control Input 1**
EQC0	D7	I	**Equalizer Control Input 0** ***NOTES:*** 1. *In **Hardware mode** all transmit channels share the same pulse setting controls function.* 2. *All channels of an XRT83VL38 must operate at the same clock rate, either the T1, E1 or J1 modes.*
$\overline{RDY}$_$\overline{DTACK}$	A6	O	In **Host mode**, these pins perform various microprocessor functions. **SEE"MICRO-PROCESSOR INTERFACE" ON PAGE 11.** ***NOTE:*** *Internally pulled "Low" with a 50kΩ resistor.*
$\overline{CS}$	B7	I	
ALE_$\overline{AS}$	A7	I	
$\overline{RD}$_$\overline{DS}$	C7	I	
$\overline{WR}$_R/$\overline{W}$	D7	I	
RXTSEL	U11	I	**Receiver Termination Select** In **Hardware mode**, when this pin is "Low" the receive line termination is determined only by an external resistor. When "High", the receive termination is realized by the internal resistor or the combination of internal and external resistors. These conditions are described in the table below. ***NOTE:*** *In **Hardware mode** all channels share the same RXTSEL control function.* **RXTSEL** / **RX Termination**: **0** = **External**; **1** = **Internal** In **Host mode**, the RXTSEL_n bits in the channel control registers determine if the receiver termination is external or internal. However, the function of RXTSEL can be transferred to the **Hardware** pin by setting the TERCNTL bit (bit 6) to "1" in the register address hex 0x82. ***NOTE:*** *This pin is internally pulled "Low" with a 50kΩ resistor.*
TXTSEL	V11	I	**Transmit Termination Select - Hardware Mode** When this pin is "Low" the transmit line termination is determined only by an external resistor. When "High", the transmit termination is realized only by the internal resistor. **TXTSEL** / **TX Termination**: **0** = **External**; **1** = **Internal** ***NOTES:*** 1. *This part does not support external termination in E1 operation.* 2. *This pin is internally pulled "Low" with a 50kΩ resistor.* 3. *In **Hardware mode** all channels share the same **TXTSEL** control function.*

RXTSEL	RX Termination
0	External
1	Internal

TXTSEL	TX Termination
0	External
1	Internal

<table>
<tr><th>SIGNAL NAME</th><th>LEAD #</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>TERSEL1
TERSEL0</td><td>T11
R11</td><td>I</td><td>Termination Impedance Select bit 1:
Termination Impedance Select bit 0:
In the Hardware mode and in the internal termination mode (TXTSEL="1" and RXTSEL="1") TERSEL[1:0] control the transmit and receive termination impedance according to the following table.
<table>
<tr><th>TERSEL1</th><th>TERSEL0</th><th>Termination</th></tr>
<tr><td>0</td><td>0</td><td>100Ω</td></tr>
<tr><td>0</td><td>1</td><td>110Ω</td></tr>
<tr><td>1</td><td>0</td><td>75Ω</td></tr>
<tr><td>1</td><td>1</td><td>120Ω</td></tr>
</table>
In the internal termination mode the receiver termination of each receiver is realized completely by internal resistors or by the combination of internal and one fixed external resistor (see description of RXRES[1:0] pins).
In the internal termination mode the transformer ratio of 1:2 and 1:1 is required for transmitter and receiver respectively with the transmitter output AC coupled to the transformer.
NOTES:
1. This pin is internally pulled "Low" with a 50kΩ resistor.
2. In Hardware mode, all channels share the same TERSEL control function.
3. In the external termination mode a 1:2 transformer ratio must be used for the transmitter.</td></tr>
<tr><td>TEST</td><td>U12</td><td>I</td><td>Manufacturing Test:
NOTE: For normal operation this pin must be tied to ground.</td></tr>
<tr><td>$\overline{\text{ICT}}$</td><td>V12</td><td>I</td><td>In-Circuit Testing (Active "Low"):
When this pin is tied "Low", all output pins are forced to a high impedance state for in-circuit testing.
Pulling $\overline{\text{RESET}}$ and $\overline{\text{ICT}}$ pins "Low" simultaneously will put the chip in factory test mode. This condition should not be permitted during normal operation.
NOTE: This pin is internally pulled "High" with a 50kΩ resistor.</td></tr>
</table>

SERIAL MICROPROCESSOR INTERFACE

SIGNAL NAME	BGA LEAD #	TYPE	DESCRIPTION
SER_$\overline{\text{PAR}}$	P18	**I**	**Serial/Parallel Select Input (Host Mode Only)** This pin is used in the Host mode to select between the parallel microprocessor or serial interface. By default, the Host mode operates in the parallel microprocessor mode. To configure the device for a serial interface, this pin must be pulled "HIgh". ***NOTE:** Internally pulled "Low" with a 50kΩ resistor.*
SCLK	T13	**I**	**Serial Clock Input (Host Mode Only)** If Pin SER_$\overline{\text{PAR}}$ is pulled "High", this input pin is used the timing reference for the serial microprocessor interface. See the Microprocessor Section of this datasheet for details.
SDI	C10	**I**	**Serial Data Input (Host Mode Only)** If Pin SER_$\overline{\text{PAR}}$ is pulled "High", this input pin from the serial interface is used to input the serial data for Read and Write operations. See the Microprocessor Section of this datasheet for details.
SDO	R7	**O**	**Serial Data Output (Host Mode Only)** If Pin SER_$\overline{\text{PAR}}$ is pulled "High", this output pin from the serial interface is used to read back the regsiter contents. See the Microprocessor Section of this datasheet for details.
TDO	B1		**Test Data Out** This pin is used as the output data pin for the boundary scan chain.
TDI	R1		**Test Data In** This pin is used as the input data pin for the boundary scan chain. For normal operation, this pin should be pulled "High". ***NOTE:** Internally pulled "High" with a 50kΩ resistor.*
TCK	N1		**Test Clock Input** This pin is used as the input clock source for the boundary scan chain. For normal operation, this pin should be pulled "High". ***NOTE:** Internally pulled "High" with a 50kΩ resistor.*
TMS	E1		**Test Mode Select** This pin is used as the input mode select for the boundary scan chain. For normal operation, this pin should be pulled "High". ***NOTE:** Internally pulled "High" with a 50kΩ resistor.*
SENSE	N18	**O**	**Factory Test Pin** This pin shpould be left floating.

POWER AND GROUND

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
TGND_0 **TGND_1** **TGND_2** **TGND_3** **TGND_4** **TGND_5** **TGND_6** **TGND_7**	D3 F2 E15 C17 R3 P3 T16 R16	****	**Transmitter Analog Ground for Channel _0** It is recomended that all ground pins form this device be tied together.
TVDD_0 **TVDD_1** **TVDD_2** **TVDD_3** **TVDD_4** **TVDD_5** **TVDD_6** **TVDD_7**	E4 F4 F16 E17 R4 P1 N15 P15	****	**Transmitter Analog Power Supply (3.3V ± 5%)** TVDD can be shared with DVDD. However, it is recommended that TVDD be isolated from the analog supply RVDD. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Each power supply pin should be bypassed to ground with an external 0.1uf capcitor.
RVDD_0 **RVDD_1** **RVDD_2** **RVDD_3** **RVDD_4** **RVDD_5** **RVDD_6** **RVDD_7**	C2 E5 G16 D16 V2 N3 N17 U18	****	**Receiver Analog Positive Supply (3.3V± 5%)** RVDD should not be shared with any other supply. It is recommended that RVDD be isolated from the digital supply DVDD and the analog power supply TVDD. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Each power supply pin should be bypassed to ground with an external 0.1uf capcitor.
RGND_0 **RGND_1** **RGND_2** **RGND_3** **RGND_4** **RGND_5** **RGND_6** **RGND_7**	D2 G3 G17 D17 T2 M2 M17 R17	****	**Receiver Analog Ground for Channel_0** It is recomended that all ground pins form this device be tied together.
AVDD	K17 J3 J2	****	**Analog Positive Supply (1.8V± 5%)** AVDD should be isolated from other supplies. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Each power supply pin should be bypassed to ground with at least one 0.1uf capcitor
AGND	J17 K3 L4	****	**Analog Ground** It is recomended that all ground pins form this device be tied together.
DVDD1v8	U10 K18 D10 A9 V1		**Digital Positive Supply (1.8V± 5%)** DVDD1v8 should be isolated from other analog supplies. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Every two DVDD1v8 power supply pins should be bypassed to ground with at least one 0.1uf capcitor

SIGNAL NAME	LEAD #	TYPE	DESCRIPTION
DVDD3v3	R9 K15 J4 D9 A18	****	**Digital Positive Supply (3.3V± 5%)** DVDD3v3 should be isolated from other analog supplies. For best results use an internal power plane for isolation. If an internal power plane is not available, a ferite bead can be used. Every two DVDD3v3 power supply pins should be bypassed to ground with at least one 0.1uf capcitor
DGND	A1 R8 T9 H17 B9 D8 C9 G15 K2 V18	****	**Digital Ground** It is recomended that all ground pins form this device be tied together.
NC11 **NC12**	E18 B18		**No Connect Pin**

FUNCTIONAL DESCRIPTION

The XRT83VL38 is a fully integrated long-haul and short-haul transceiver intended for T1, J1 or E1 systems. Simplified block diagrams of the chip are shown in Figure 1, **Host** mode and Figure 2, **Hardware** mode. The XRT83VL38 can receive signals that have been attenuated from 0 to 36dB at 772kHz (0 to 6000 feet cable loss) for T1 and from 0 to 43dB at 1024kHz for E1 systems.

In T1 applications, the XRT83VL38 can generate five transmit pulse shapes to meet the short-haul Digital Cross-connect (DSX-1) template requirement as well as four CSU Line Build-Out (LBO) filters of 0dB, -7.5dB, -15dB and -22.5dB as required by FCC rules. It also provides programmable transmit output pulse generators for each channel that can be used for output pulse shaping allowing performance improvement over a wide variety of conditions (The arbitrary pulse generators are available for both T1 and E1, in short-haul configuration). The operation and configuration of the XRT83VL38 can be controlled through a microprocessor **Host** interface (parallel or serial) or **Hardware** control.

MASTER CLOCK GENERATOR

Using a variety of external clock sources, the on-chip frequency synthesizer generates the T1 (1.544MHz) or E1 (2.048MHz) master clocks necessary for the transmit pulse shaping and receive clock recovery circuit.

There are two master clock inputs MCLKE1 and MCLKT1. In systems where both T1 and E1 master clocks are available these clocks can be connected to the respective pins. All channels of a given XRT83VL38 must be operated at the same clock rate, either T1, E1 or J1 modes.

In systems that have only one master clock source available (E1 or T1), that clock should be connected to both MCLKE1 and MCLKT1 inputs for proper operation. T1 or E1 master clocks can be generated from a single 1.544MHz or 2.048MHz external clock under the control of CLKSEL[2:0] inputs according to Table 1.

NOTE: EQC[4:0] determine the T1/E1 operating mode. See Table 5 for details.

FIGURE 4. TWO INPUT CLOCK SOURCE

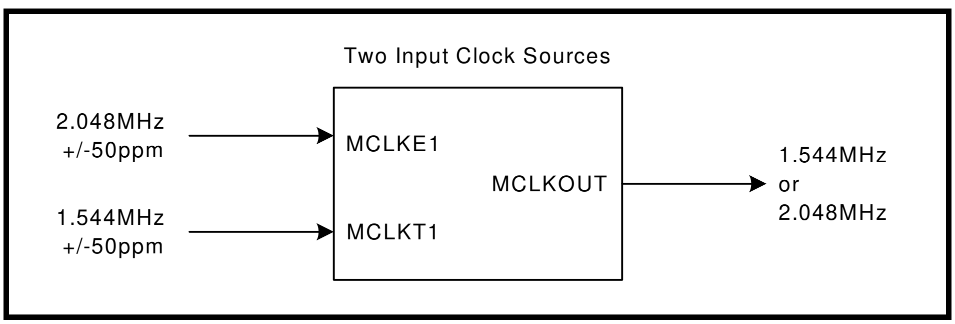


FIGURE 5. ONE INPUT CLOCK SOURCE

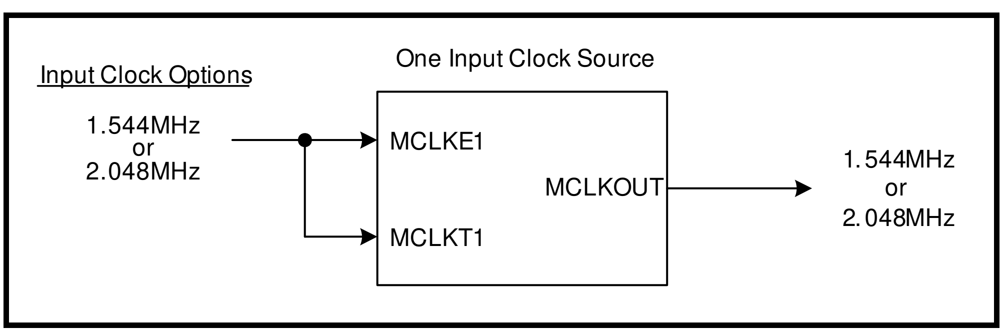


TABLE 1: MASTER CLOCK GENERATOR

MCLKE1 KHZ	MCLKT1 KHZ	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	MASTER CLOCK KHZ
2048	2048	0	0	0	0	2048
2048	2048	0	0	0	1	1544
2048	1544	0	0	0	0	2048
1544	1544	0	0	1	1	1544
1544	1544	0	0	1	0	2048
2048	1544	0	0	1	1	1544

In **Host** mode the programming is achieved through the corresponding interface control bits, the state of the CLKSEL[2:0] control bits and the state of the MCLKRATE interface control bit.

RECEIVER

RECEIVER INPUT

At the receiver input, a cable attenuated AMI signal can be coupled to the receiver through a capacitor or a 1:1 transformer. The input signal is first applied to a selective equalizer for signal conditioning. The maximum equalizer gain is up to 36dB for T1 and 43dB for E1 modes. The equalized signal is subsequently applied to a peak detector which in turn controls the equalizer settings and the data slicer. The slicer threshold for both E1 and T1 is typically set at 50% of the peak amplitude at the equalizer output. After the slicers, the digital representation of the AMI signals are applied to the clock and data recovery circuit. The recovered data subsequently goes through the jitter attenuator and decoder (if selected) for HDB3 or B8ZS decoding before being applied to the RPOS_n/RDATA_n and RNEG_n/LCV_n pins. Clock recovery is accomplished by a digital phase-locked loop (DPLL) which does not require any external components and can tolerate high levels of input jitter that meets or exceeds the ITU-G.823 and TR-TSY000499 standards.

RECEIVE MONITOR MODE

In applications where Monitor mode is desired, the equalizer can be configured in a gain mode which handles input signals attenuated resistively up to 29dB, along with 0 to 6dB cable attenuation for both T1 and E1 applications, refer to Table 5 for details. This feature is available in both **Hardware** and **Host** modes.

RECEIVER LOSS OF SIGNAL (RLOS)

For compatibility with ITU G.775 requirements, the RLOS monitoring function is implemented using both analog and digital detection schemes. If the analog RLOS condition occurs, a digital detector is activated to count for 32 consecutive zeros in E1 (4096 bits in Extended Los mode, EXLOS = "1") or 175 consecutive zeros in T1 before RLOS is asserted. RLOS is cleared when the input signal rises +3dB (built in hysteresis) above the point at which it was declared and meets 12.5% ones density of 4 ones in a 32 bit window, with no more than 16 consecutive zeros for E1. In T1 mode, RLOS is cleared when the input signal rises +3dB (built in hysteresis) above the point at which it was declared and contains 16 ones in a 128 bit window with no more than 100 consecutive zeros in the data stream. When loss of signal occurs, RLOS register indication and register status will change. If the RLOS register enable is set high (enabled), the alarm will trigger an interrupt causing the interrupt pin ($\overline{INT}$) to go low. Once the alarm status register has been read, it will automatically reset upon read (RUR), and the $\overline{INT}$ pin will return high.

Analog RLOS

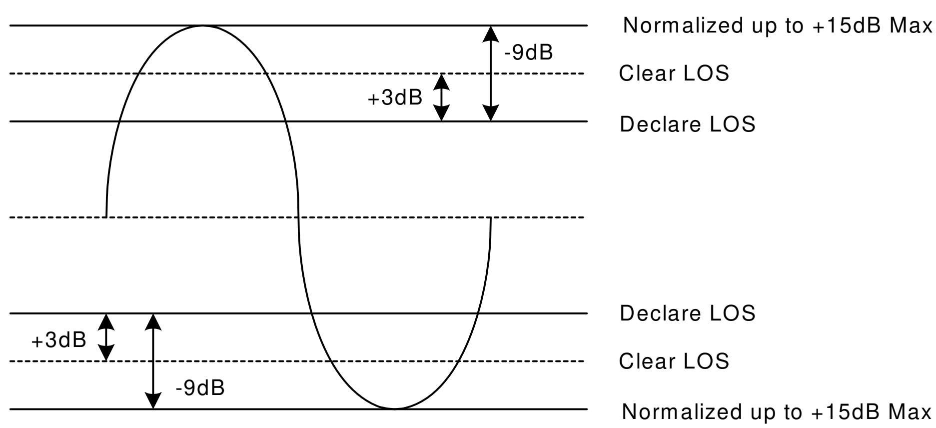
Setting the Receiver Inputs to -15dB T1/E1 Short Haul Mode

By setting the receiver inputs to -15dB T1/E1 short haul mode, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +15dB normalizing the T1/E1 input signal.

NOTE: *This is the only setting that refers to cable loss (frequency), not flat loss (resistive).*

Once the T1/E1 input signal has been normalized to 0dB by adding the maximum gain (+15dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -24dB (-15dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total cable attenuation of -21dB. See Figure 6 for a simplified diagram.

FIGURE 6. SIMPLIFIED DIAGRAM OF -15dB T1/E1 SHORT HAUL MODE AND RLOS CONDITION



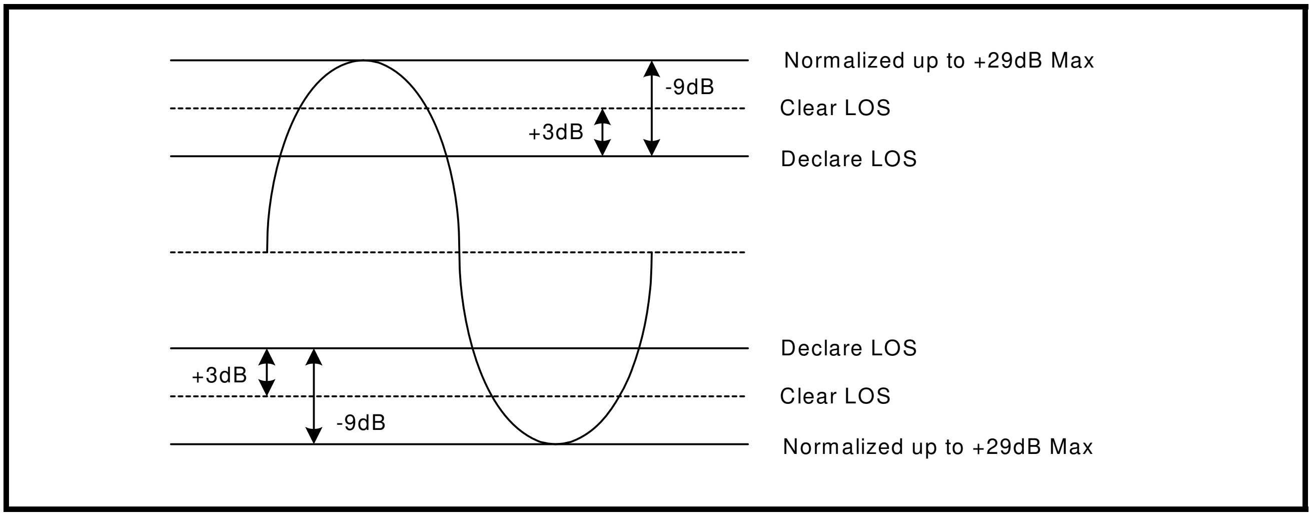
Setting the Receiver Inputs to -29dB T1/E1 Gain Mode

By setting the receiver inputs to -29dB T1/E1 gain mode, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +29dB normalizing the T1/E1 input signal.

NOTE: *This is the only setting that refers to flat loss (resistive). All other modes refer to cable loss (frequency).*

Once the T1/E1 input signal has been normalized to 0dB by adding the maximum gain (+29dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -38dB (-29dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total flat loss of -35dB. See **Figure 7** for a simplified diagram.

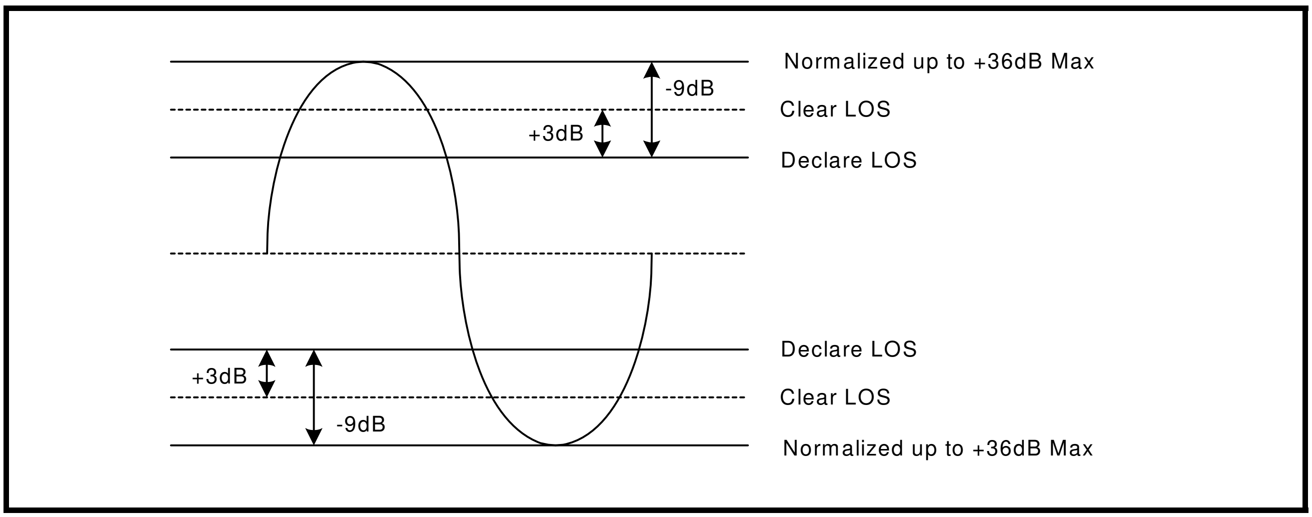
FIGURE 7. SIMPLIFIED DIAGRAM OF -29dB T1/E1 GAIN MODE AND RLOS CONDITION



Setting the Receiver Inputs to -36dB T1/E1 Long Haul Mode

By setting the receiver inputs to -36dB T1/E1 long haul mode, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +36dB normalizing the T1 input signal. This setting refers to cable loss (frequency), not flat loss (resistive). Once the T1/E1 input signal has been normalized to 0dB by adding the maximum gain (+36dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -45dB (-36dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total cable attenuation of -42dB. See **Figure 8** for a simplified diagram.

FIGURE 8. SIMPLIFIED DIAGRAM OF -36dB T1/E1 LONG HAUL MODE AND RLOS CONDITION

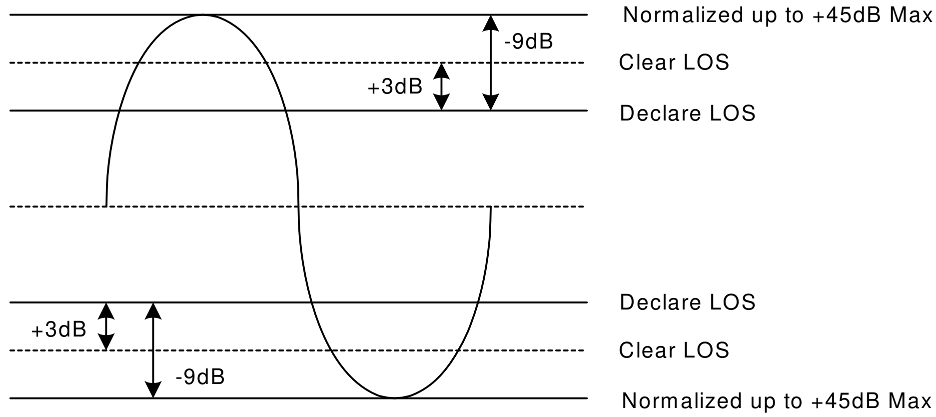


E1 Extended RLOS

E1: Setting the Receiver Inputs to Extended RLOS

By setting the receiver inputs to extended RLOS, the equalizer will detect the incoming amplitude and make adjustments by adding gain up to a maximum of +43dB normalizing the E1 input signal. This setting refers to cable loss (frequency), not flat loss (resistive). Once the E1 input signal has been normalized to 0dB by adding the maximum gain (+43dB), the receiver will declare RLOS if the signal is attenuated by an additional -9dB. The total cable loss at RLOS declaration is typically -52dB (-43dB + -9dB). A 3dB hysteresis was designed so that transients will not trigger the RLOS to clear. Therefore, the RLOS will typically clear at a total cable attenuation of -49dB. See Figure 9 for a simplified diagram.

FIGURE 9. SIMPLIFIED DIAGRAM OF EXTENDED RLOS MODE (E1 ONLY)



RECEIVE HDB3/B8ZS DECODER

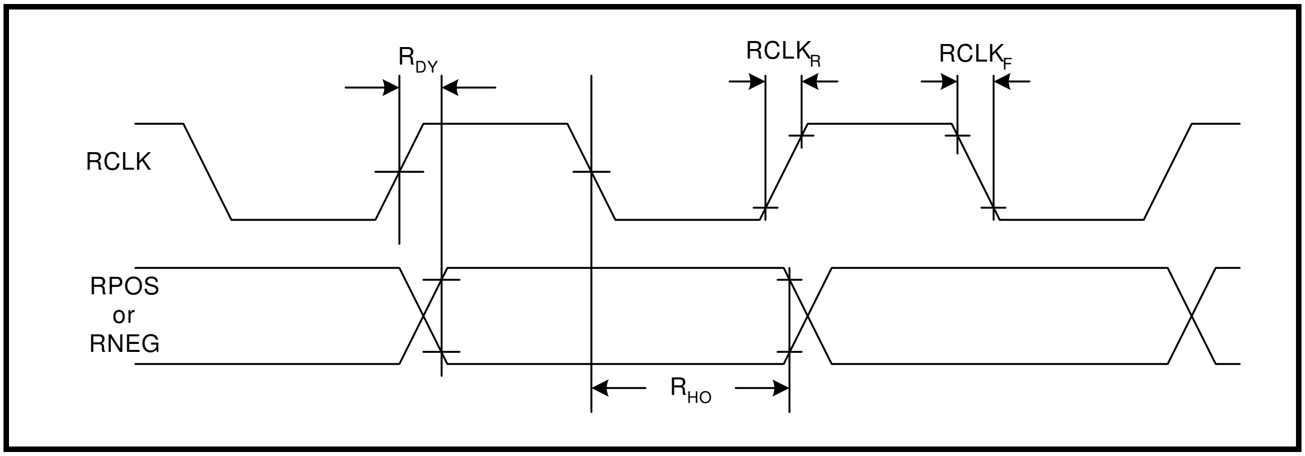
The Decoder function is available in both **Hardware** and **Host** modes on a per channel basis by controlling the TNEG_n/CODES_n pin or the CODES_n interface bit. The decoder function is only active in single-rail Mode. When selected, receive data in this mode will be decoded according to HDB3 rules for E1 and B8ZS for T1 systems. Bipolar violations that do not conform to the coding scheme will be reported as Line Code Violation at the RNEG_n/LCV_n pin of each channel. The length of the LCV pulse is one RCLK cycle for each code violation. In E1mode only, an excessive number of zeros in the receive data stream is also reported as an error at the same output pin. If AMI decoding is selected in single rail mode, every bipolar violation in the receive data stream will be reported as an error at the RNEG_n/LCV_n pin.

RECOVERED CLOCK (RCLK) SAMPLING EDGE

This feature is available in both **Hardware** and **Host** modes on a global basis. In **Host** mode, the sampling edge of RCLK output can be changed through the interface control bit RCLKE. If a “1” is written in the RCLKE interface bit, receive data output at RPOS_n/RDATA_n and RNEG_n/LCV_n are updated on the falling edge of

RCLK for all eight channels. Writing a “0” to the RCLKE register, updates the receive data on the rising edge of RCLK. In **Hardware** mode the same feature is available under the control of the RCLKE pin.

FIGURE 10. RECEIVE CLOCK AND OUTPUT DATA TIMING



JITTER ATTENUATOR

To reduce phase and frequency jitter in the recovered clock, the jitter attenuator can be placed in the receive signal path. The jitter attenuator uses a data FIFO (First In First Out) with a programmable depth that can vary between 2x32 and 2x64. The jitter attenuator can also be placed in the transmit signal path or disabled altogether depending upon system requirements. The jitter attenuator, other than using the master clock as reference, requires no external components. With the jitter attenuator selected, the typical throughput delay from input to output is 16 bits for 32 bit FIFO size or 32 bits for 64 bit FIFO size. When the read and write pointers of the FIFO in the jitter attenuator are within two bits of over-flowing or under-flowing, the bandwidth of the jitter attenuator is widened to track the short term input jitter, thereby avoiding data corruption. When this situation occurs, the jitter attenuator will not attenuate input jitter until the read/write pointer's position is outside the two bits window. Under normal condition, the jitter transfer characteristic meets the narrow bandwidth requirement as specified in ITU- G.736, ITU- I.431 and AT&T Pub 62411 standards.

In T1 mode the Jitter Attenuator Bandwidth is always set to 3Hz. In E1 mode, the bandwidth can be reduced through the JABW control signal. When JABW is set “High” the bandwidth of the jitter attenuator is reduced from 10Hz to 1.5Hz. Under this condition the FIFO length is automatically set to 64 bits and the 32 bits FIFO length will not be available in this mode. Jitter attenuator controls are available on a per channel basis in the **Host** mode and on a global basis in the **Hardware** mode.

GAPPED CLOCK (JA MUST BE ENABLED IN THE TRANSMIT PATH)

The XRT83VL38 LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to T1 or E1 data, stuffing bits are removed which can leave gaps in the incoming data stream. If the jitter attenuator is enabled in the transmit path, the 32-Bit or 64-Bit FIFO is used to smooth the gapped clock into a steady T1 or E1 output. The maximum gap width of the 8-Channel LIU is shown in Table 2.

TABLE 2: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

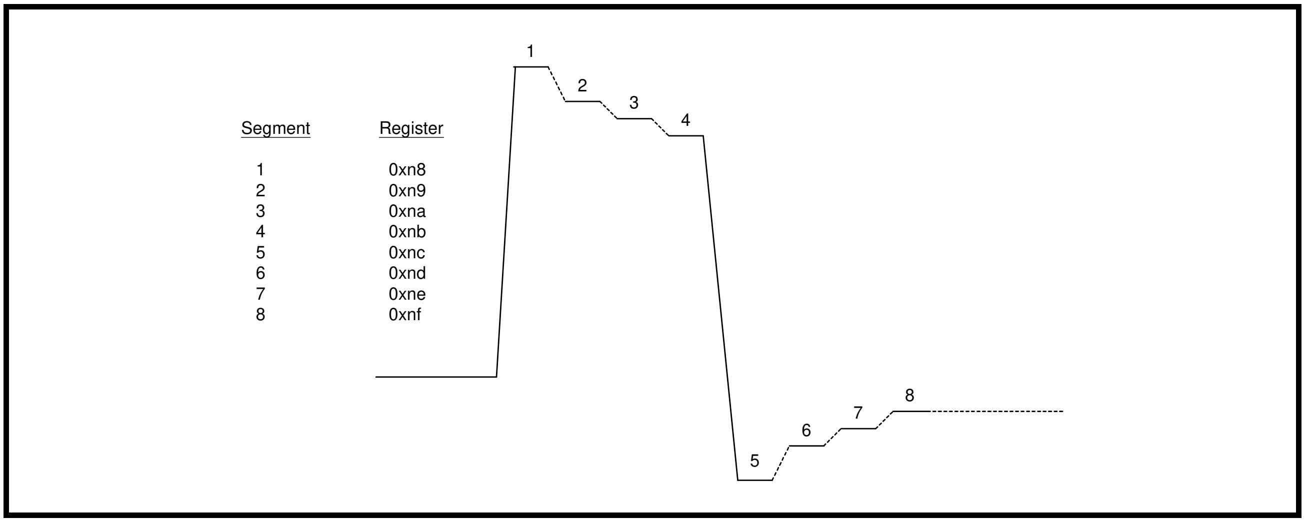
FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the jitter attenuator should be enabled in the receive path.*

ARBITRARY PULSE GENERATOR FOR T1 AND E1

The arbitrary pulse generator divides the pulse into eight individual segments. Each segment is set by a 7-Bit binary word by programming the appropriate channel register. This allows the system designer to set the overshoot, amplitude, and undershoot for a unique line build out. The MSB (bit 7) is a sign-bit. If the sign-bit is set to “1”, the segment will move in a positive direction relative to a flat line (zero) condition. If this sign-bit is set to “0”, the segment will move in a negative direction relative to a flat line condition. A pulse with numbered segments is shown in **Figure 11**.

FIGURE 11. ARBITRARY PULSE SEGMENT ASSIGNMENT



***NOTE:** By default, the arbitrary segments are programmed to 0x00h. The transmitter outputs will result in an all zero pattern to the line. For E1 arbitrary mode, see global register 0xC0h.*

TRANSMITTER

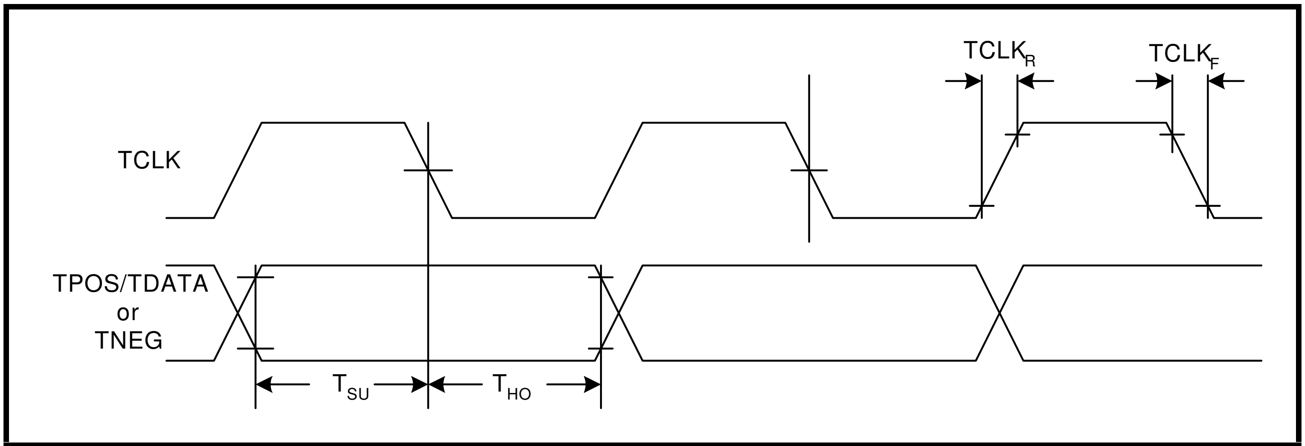
DIGITAL DATA FORMAT

Both the transmitter and receiver can be configured to operate in dual or single-rail data formats. This feature is available under both **Hardware** and **Host** control modes, on a global basis. The dual or single-rail data format is determined by the state of the SR/$\overline{\text{DR}}$ pin in **Hardware** mode or SR/$\overline{\text{DR}}$ interface bit in the **Host** mode. In single-rail mode, transmit clock and NRZ data are applied to TCLK_n and TPOS_n/TDATA_n pins respectively. In single-rail and **Hardware** mode the TNEG_n/CODES_n input can be used as the CODES function. With TNEG_n/CODES_n tied “Low”, HDB3 or B8ZS encoding and decoding are enabled for E1 and T1 modes respectively. With TNEG_n/CODES_n tied “High”, the AMI coding scheme is selected. In both dual or single-rail modes of operations, the transmitter converts digital input data to a bipolar format before being transmitted to the line.

TRANSMIT CLOCK (TCLK) SAMPLING EDGE

Serial transmit data at TPOS_n/TDATA_n and TNEG_n/CODES_n are clocked into the XRT83VL38 under the synchronization of TCLK_n. With a “0” written to the TCLKE interface bit, or by pulling the TCLKE pin “Low”, input data is sampled on the falling edge of TCLK_n. The sampling edge is inverted with a “1” written to TCLKE interface bit, or by connecting the TCLKE pin “High”.

FIGURE 12. TRANSMIT CLOCK AND INPUT DATA TIMING



TRANSMIT HDB3/B8ZS ENCODER

The Encoder function is available in both **Hardware** and **Host** modes on a per channel basis by controlling the TNEG_n/CODES_n pin or CODES interface bit. The encoder is only available in single-rail mode. In E1 mode and with HDB3 encoding selected, any sequence with four or more consecutive zeros in the input serial data from TPOS_n/TDATA_n, will be removed and replaced with 000V or B00V, where "B" indicates a pulse conforming with the bipolar rule and "V" representing a pulse violating the rule. An example of HDB3 Encoding is shown in Table 3. In a T1 system, an input data sequence with eight or more consecutive zeros will be removed and replaced using the B8ZS encoding rule. An example of Bipolar with 8 Zero Substitution (B8ZS) encoding scheme is shown in Table 4. Writing a "1" into the CODES_n interface bit or connecting the TNEG_n/CODES_n pin to a "High" level selects the AMI coding for both E1 or T1 systems.

TABLE 3: EXAMPLES OF HDB3 ENCODING

	NUMBER OF PULSE BEFORE NEXT 4 ZEROS	NEXT 4 BITS
Input		0000
HDB3 (case1)	odd	000V
HDB3 (case2)	even	B00V

TABLE 4: EXAMPLES OF B8ZS ENCODING

CASE 1	PRECEDING PULSE	NEXT 8 BITS
Input	+	00000000
B8ZS		000VB0VB
AMI Output	+	000+ -0- +
CASE 2		
Input	-	00000000
B8ZS		000VB0VB
AMI Output	-	000- +0+ -

DRIVER FAILURE MONITOR (DMO)

The driver monitor circuit is used to detect transmit driver failure by monitoring the activities at TTIP and TRING outputs. Driver failure may be caused by a short circuit in the primary transformer or system problems at the transmit input. If the transmitter of a channel has no output for more than 128 clock cycles, the corresponding DMO pin goes “High” and remains “High” until a valid transmit pulse is detected. In **Host** mode, the failure of the transmit channel is reported in the corresponding interface bit. If the DMOIE bit is also enabled, any transition on the DMO interface bit will generate an interrupt. The driver failure monitor is supported in both **Hardware** and **Host** modes on a per channel basis.

TRANSMIT PULSE SHAPER & LINE BUILD OUT (LBO) CIRCUIT

The transmit pulse shaper circuit uses the high speed clock from the Master timing generator to control the shape and width of the transmitted pulse. The internal high-speed timing generator eliminates the need for a tightly controlled transmit clock (TCLK) duty cycle. With the jitter attenuator not in the transmit path, the transmit output will generate no more than 0.025Unit Interval (UI) peak-to-peak jitter. In **Hardware** mode, the state of the A[4:0]/EQC[4:0] pins determine the transmit pulse shape for all eight channels. In **Host** mode transmit pulse shape can be controlled on a per channel basis using the interface bits EQC[4:0]. The chip supports five fixed transmit pulse settings for T1 Short-haul applications plus a fully programmable waveform generator for arbitrary transmit output pulse shapes (The arbitrary pulse generators are available for both T1 and E1). Transmit Line Build-Outs for T1 long-haul application are supported from 0dB to -22.5dB in three 7.5dB steps. The choice of the transmit pulse shape and LBO under the control of the interface bits are summarized in Table 5. For CSU LBO transmit pulse design information, refer to ANSI T1.403-1993 Network-to-Customer Installation specification, Annex-E.

NOTE: *EQC[4:0] determine the T1/E1 operating mode of the XRT83VL38. When EQC4 = “1” and EQC3 = “1”, the XRT83VL38 is in the E1 mode, otherwise it is in the T1/J1 mode. For details on how to enable the E1 arbitrary mode, see global register 0xC0h.*

TABLE 5: RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS

EQC4	EQC3	EQC2	EQC1	EQC0	E1/T1 MODE & RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE	CODING
0	0	0	0	0	T1 Long Haul/36dB	0dB	100Ω/ TP	B8ZS
0	0	0	0	1	T1 Long Haul/36dB	-7.5dB	100Ω/ TP	B8ZS
0	0	0	1	0	T1 Long Haul/36dB	-15dB	100Ω/ TP	B8ZS
0	0	0	1	1	T1 Long Haul/36dB	-22.5dB	100Ω/ TP	B8ZS
0	0	1	0	0	T1 Long Haul/45dB	0dB	100Ω/ TP	B8ZS
0	0	1	0	1	T1 Long Haul/45dB	-7.5dB	100Ω/ TP	B8ZS
0	0	1	1	0	T1 Long Haul/45dB	-15dB	100Ω/ TP	B8ZS
0	0	1	1	1	T1 Long Haul/45dB	-22.5dB	100Ω/ TP	B8ZS
0	1	0	0	0	T1 Short Haul/15dB	0-133 ft./ 0.6dB	100Ω/ TP	B8ZS
0	1	0	0	1	T1 Short Haul/15dB	133-266 ft./ 1.2dB	100Ω/ TP	B8ZS
0	1	0	1	0	T1 Short Haul/15dB	266-399 ft./ 1.8dB	100Ω/ TP	B8ZS
0	1	0	1	1	T1 Short Haul/15dB	399-533 ft./ 2.4dB	100Ω/ TP	B8ZS
0	1	1	0	0	T1 Short Haul/15dB	533-655 ft./ 3.0dB	100Ω/ TP	B8ZS

TABLE 5: RECEIVE EQUALIZER CONTROL AND TRANSMIT LINE BUILD-OUT SETTINGS

EQC4	EQC3	EQC2	EQC1	EQC0	E1/T1 MODE & RECEIVE SENSITIVITY	TRANSMIT LBO	CABLE	CODING
0	1	1	0	1	T1 Short Haul/15dB	Arbitrary Pulse	100Ω/ TP	B8ZS
0	1	1	1	0	T1 Gain Mode/29dB	0-133 ft./ 0.6dB	100Ω/ TP	B8ZS
0	1	1	1	1	T1 Gain Mode/29dB	133-266 ft./ 1.2dB	100Ω/ TP	B8ZS
1	0	0	0	0	T1 Gain Mode/29dB	266-399 ft./ 1.8dB	100Ω/ TP	B8ZS
1	0	0	0	1	T1 Gain Mode/29dB	399-533 ft./ 2.4dB	100Ω/ TP	B8ZS
1	0	0	1	0	T1 Gain Mode/29dB	533-655 ft./ 3.0dB	100Ω/ TP	B8ZS
1	0	0	1	1	T1 Gain Mode/29dB	Arbitrary Pulse	100Ω/ TP	B8ZS
1	0	1	0	0	T1 Gain Mode/29dB	0dB	100Ω/ TP	B8ZS
1	0	1	0	1	T1 Gain Mode/29dB	-7.5dB	100Ω/ TP	B8ZS
1	0	1	1	0	T1 Gain Mode/29dB	-15dB	100Ω/ TP	B8ZS
1	0	1	1	1	T1 Gain Mode/29dB	-22.5dB	100Ω/ TP	B8ZS
1	1	0	0	0	E1 Long Haul/36dB	ITU G.703/Arbitrary	75Ω Coax	HDB3
1	1	0	0	1	E1 Long Haul/36dB	ITU G.703/Arbitrary	120Ω TP	HDB3
1	1	0	1	0	E1 Long Haul/43dB	ITU G.703/Arbitrary	75Ω Coax	HDB3
1	1	0	1	1	E1 Long Haul/43dB	ITU G.703/Arbitrary	120Ω TP	HDB3
1	1	1	0	0	E1 Short Haul	ITU G.703/Arbitrary	75Ω Coax	HDB3
1	1	1	0	1	E1 Short Haul	ITU G.703/Arbitrary	120Ω TP	HDB3
1	1	1	1	0	E1 Gain Mode	ITU G.703/Arbitrary	75Ω Coax	HDB3
1	1	1	1	1	E1 Gain Mode	ITU G.703/Arbitrary	120Ω TP	HDB3

TRANSMIT AND RECEIVE TERMINATIONS

The XRT83VL38 is a versatile LIU that can be programmed to use one Bill of Materials (BOM) for worldwide applications for T1, J1 and E1. For specific applications the internal terminations can be disabled to allow the use of existing components and/or designs.

RECEIVER (CHANNELS 0 - 7)

INTERNAL RECEIVE TERMINATION MODE

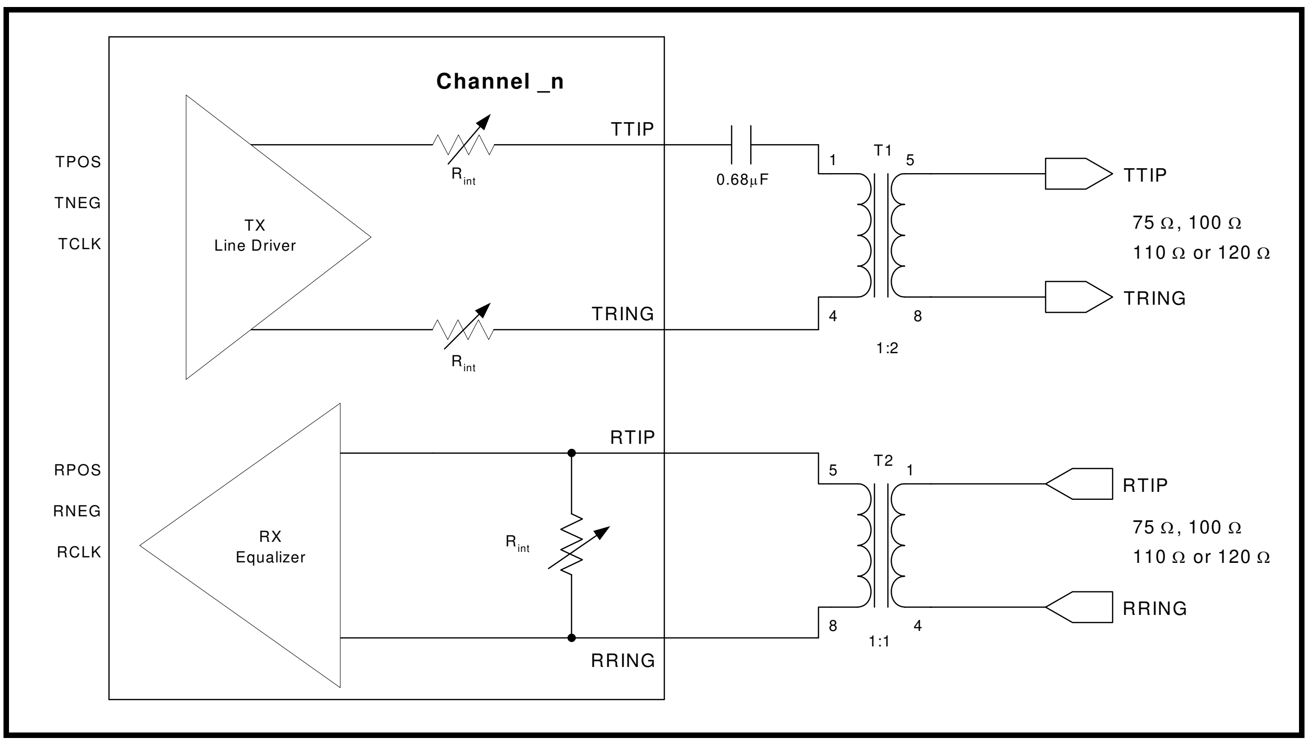
In **Hardware** mode, RXTSEL (Pin 83) can be tied “High” to select internal termination mode for all receive channels or tied “Low” to select external termination mode. Individual channel control can only be done in **Host** mode. By default the XRT83VL38 is set for external termination mode at power up or at **Hardware** reset.

TABLE 6: RECEIVE TERMINATION CONTROL

RXTSEL	RX TERMINATION
0	EXTERNAL
1	INTERNAL

In **Host** mode, bit 7 in the appropriate channel register, (Table 24, “Microprocessor Register #1, Bit Description,” on page 59), is set “High” to select the internal termination mode for that specific receive channel.

FIGURE 13. SIMPLIFIED DIAGRAM FOR THE INTERNAL RECEIVE AND TRANSMIT TERMINATION MODE



If the internal termination mode (RXTSEL = “1”) is selected, the effective impedance for E1, T1 or J1 can be achieved either with an internal resistor or a combination of internal and external resistors as shown in Table 7.

***NOTE:** In **Hardware** mode, pins RXRES[1:0] control all channels.*

TABLE 7: RECEIVE TERMINATIONS

RXTSEL	TERSEL1	TERSEL0	RXRES1	RXRES0	R_{ext}	R_{int}	MODE
0	x	x	x	x	R_{ext}	∞	T1/E1/J1
1	0	0	0	0	∞	100Ω	T1
1	0	1	0	0	∞	110Ω	J1
1	1	0	0	0	∞	75Ω	E1
1	1	1	0	0	∞	120Ω	E1
1	0	0	0	1	240Ω	172Ω	T1
1	0	1	0	1	240Ω	204Ω	J1
1	1	0	0	1	240Ω	108Ω	E1
1	1	1	0	1	240Ω	240Ω	E1
1	0	0	1	0	210Ω	192Ω	T1
1	0	1	1	0	210Ω	232Ω	J1
1	1	0	1	0	210Ω	116Ω	E1
1	1	1	1	0	210Ω	280Ω	E1
1	0	0	1	1	150Ω	300Ω	T1
1	0	1	1	1	150Ω	412Ω	J1
1	1	0	1	1	150Ω	150Ω	E1
1	1	1	1	1	150Ω	600Ω	E1

Figure 14 is a simplified diagram for T1 (100Ω) in the external receive and transmit termination mode. Figure 15 is a simplified diagram for E1 (75Ω) in the external receive and internal transmit termination mode.

FIGURE 14. SIMPLIFIED DIAGRAM FOR T1 IN THE EXTERNAL TERMINATION MODE (RXTSEL= 0 & TXTSEL= 0)

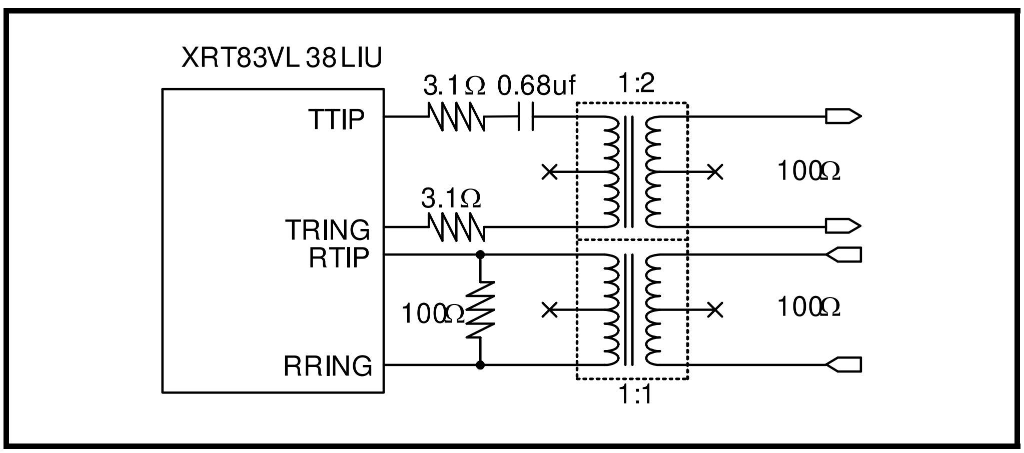
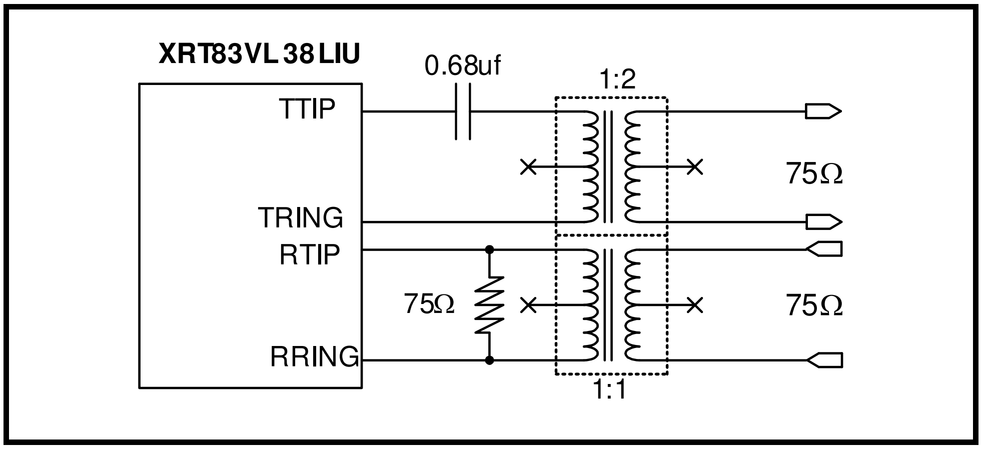


FIGURE 15. SIMPLIFIED DIAGRAM FOR E1 IN EXTERNAL RECEIVE TERMINATION MODE (RXTSEL= 0) AND INTERNAL TRANSMIT TERMINATION MODE (TXTEL= 1)



TRANSMITTER (CHANNELS 0 - 7)

TRANSMIT TERMINATION MODE

In **Hardware** mode, TXTSEL (Pin 84) can be tied "High" to select internal termination mode for all transmit channels or tied "Low" for external termination. Individual channel control can be done only in **Host** mode. In **Host** mode, bit 6 in the appropriate register for a given channel is set "High" to select the internal termination mode for that specific transmit channel, see **Table 24, "Microprocessor Register #1, Bit Description," on page 59**.

In internal mode, no external resistors are used. An external capacitor of 0.68μF is used for proper operation of the internal termination circuitry, see **Figure 13**.

TABLE 8: TERMINATION SELECT CONTROL

TERSEL1	TERSEL0	TERMINATION
0	0	100Ω
0	1	110Ω
1	0	75Ω
1	1	120Ω

EXTERNAL TRANSMIT TERMINATION MODE

By default the XRT83VL38 is set for external termination mode at power up or at **Hardware** reset.

When external transmit termination mode is selected, the internal termination circuitry is disabled. The value of the external resistors is chosen for a specific application. **Figure 14** is a simplified block diagram for T1 (100Ω) in the external receive and transmit termination mode. **Figure 15** is a simplified block diagram for E1 (75Ω) in the external receive termination and internal transmit termination mode.

Table 9 summarizes the transmit terminations.

TABLE 9: TRANSMIT TERMINATIONS

	TERSEL1	TERSEL0	TXTSEL	R_{int} Ω	n (turns Ratio)	R_{ext} Ω	C_{ext}
			0=EXTERNAL 1=INTERNAL	SET BY CONTROL BITS	n, R_{ext}, AND C_{ext} ARE SUGGESTED SETTINGS		
T1 100 Ω	0	0	0	0Ω	2	3.1Ω	0
	0	0	1	12.5Ω	2	0Ω	0.68µF
J1 110 Ω	0	1	0	0Ω	2	3.1Ω	0
	0	1	1	13.75Ω	2	0Ω	0.68µF
E1 75 Ω	1	0	0	E1 external Transmit termination not supported			
	1	0	1	9.4Ω	2	0Ω	0.68µF
E1 120 Ω	1	1	0	E1 external Transmit termination not supported			
	1	1	1	15Ω	2	0Ω	0.68µF

REDUNDANCY APPLICATIONS

Telecommunication system design requires signal integrity and reliability. When a T1/E1 primary line card has a failure, it must be swapped with a backup line card while maintaining connectivity to a backplane without losing data. System designers can achieve this by implementing common redundancy schemes with the XRT83VL38 Line Interface Unit (LIU). The XRT83VL38 offers features that are tailored to redundancy applications while reducing the number of components and providing system designers with solid reference designs. These features allow system designers to implement redundancy applications that ensure reliability. The Internal Impedance mode eliminates the need for external relays when using the 1:1 and 1+1 redundancy schemes.

PROGRAMMING CONSIDERATIONS

In many applications switching the control of the transmitter outputs and the receiver line impedance to **hardware** control will provide faster transmitter ON/OFF switching.

In **Host** Mode, there are two bits in register 130 (82H) that control the transmitter outputs and the Rx line impedance select, TXONCNTL (Bit 7) and TERCNTL (Bit 6).

Setting bit-7 (TXONCNTL) to a “1” transfers the control of the Transmit On/Off function to the TXON_n **Hardware** control pins. (Pins 90 through 93 and pins 169 through 172). The TXON is used to tri-state the transmit outputs when used in a redundancy application.

Setting bit-6 (TERCNTL) to a “1” transfers the control of the Rx line impedance select (RXTSEL) to the RXTSEL **Hardware** control pin (pin 83).

Either mode works well with redundancy applications. The user can determine which mode has the fastest switching time for a unique application.

TYPICAL REDUNDANCY SCHEMES

- ·1:1 One backup card for every primary card (Facility Protection)
- ·1+1 One backup card for every primary card (Line Protection)
- ·N+1One backup card for N primary cards

1:1 REDUNDANCY

A 1:1 facility protection redundancy scheme has one backup card for every primary card. When using 1:1 redundancy, the backup card has its transmitters tri-stated and its receivers in high impedance. This eliminates the need for external relays and provides one bill of materials for all interface modes of operation. The transmit and receive sections of the LIU device are described separately.

1+1 REDUNDANCY

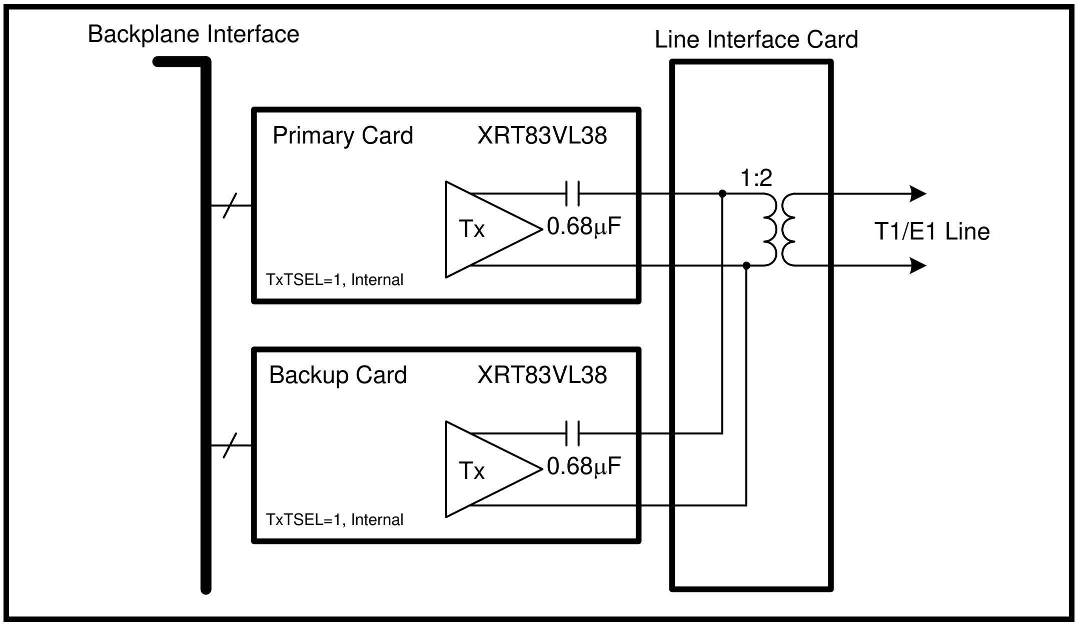
A 1+1 line protection redundancy scheme has one backup card for every primary card, and the receivers on the backup card are monitoring the receiver inputs. Therefore, the receivers on both cards need to be active. The transmit outputs require no external resistors. The transmit and receive sections of the LIU device are described separately.

TRANSMIT 1:1 & 1+1 REDUNDANCY

For 1:1 and 1+1 redundancy, the transmitters on the primary and backup card should be programmed for Internal Impedance mode. The transmitters on the backup card should be tri-stated. Select the appropriate impedance for the desired mode of operation, T1/E1/J1. A 0.68uF capacitor is used in series with TTIP for blocking DC bias. See Figure 16 for a simplified block diagram of the transmit section for 1:1 and 1+1 redundancy scheme.

NOTE: *For simplification, the over voltage protection circuitry was omitted.*

FIGURE 16. SIMPLIFIED BLOCK DIAGRAM OF THE TRANSMIT SECTION FOR 1:1 & 1+1 REDUNDANCY

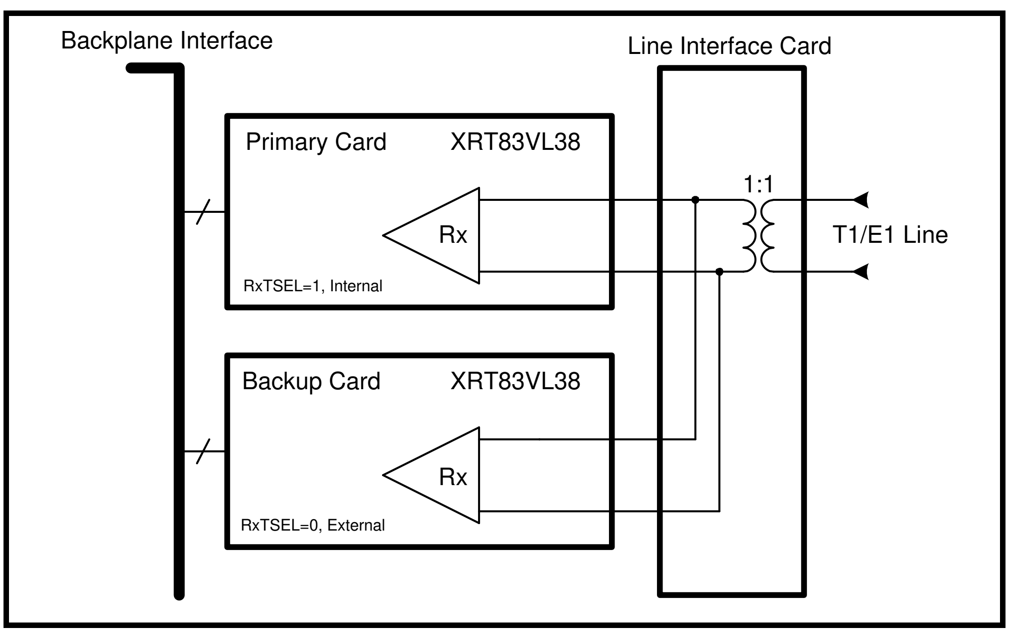


RECEIVE 1:1 & 1+1 REDUNDANCY

For 1:1 and 1+1 redundancy, the receivers on the primary card should be programmed for Internal Impedance mode. The receivers on the backup card should be programmed for External Impedance mode. Since there is no external resistor in the circuit, the receivers on the backup card will be high impedance. This key design feature eliminates the need for relays and provides one bill of materials for all interface modes of operation. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to Internal Impedance mode, then the primary card to External Impedance mode. See Figure 17 for a simplified block diagram of the receive section for a 1:1 and 1+1 redundancy scheme.

NOTE: *For simplification, the over voltage protection circuitry was omitted.*

FIGURE 17. SIMPLIFIED BLOCK DIAGRAM - RECEIVE SECTION FOR 1:1 AND 1+1 REDUNDANCY



N+1 REDUNDANCY

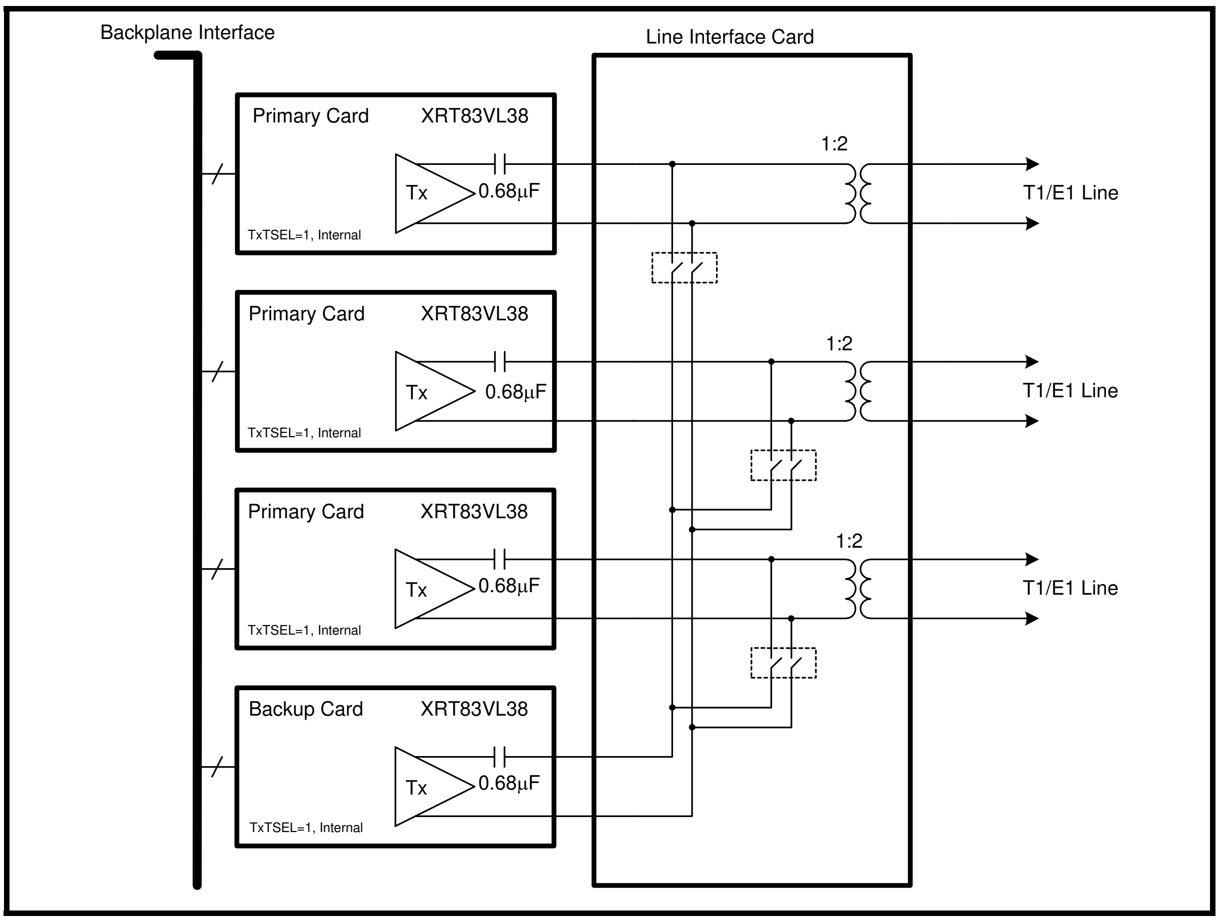
N+1 redundancy has one backup card for N primary cards. Due to impedance mismatch and signal contention, external relays are necessary when using this redundancy scheme. The advantage of relays is that they create complete isolation between the primary cards and the backup card. This allows all transmitters and receivers on the primary cards to be configured in internal impedance mode, providing one bill of materials for all interface modes of operation. The transmit and receive sections of the XRT83VL38 are described separately.

TRANSMIT

For N+1 redundancy, the transmitters on all cards should be programmed for internal impedance mode providing one bill of materials for T1/E1/J1. The transmitters on the backup card do not have to be tri-stated. To swap the primary card, close the desired relays, and tri-state the transmitters on the failed primary card. A 0.68μF capacitor is used in series with TTIP for blocking DC bias. See **Figure 18** for a simplified block diagram of the transmit section for an N+1 redundancy scheme.

NOTE: *For simplification, the over voltage protection circuitry was omitted.*

FIGURE 18. SIMPLIFIED BLOCK DIAGRAM - TRANSMIT SECTION FOR N+1 REDUNDANCY

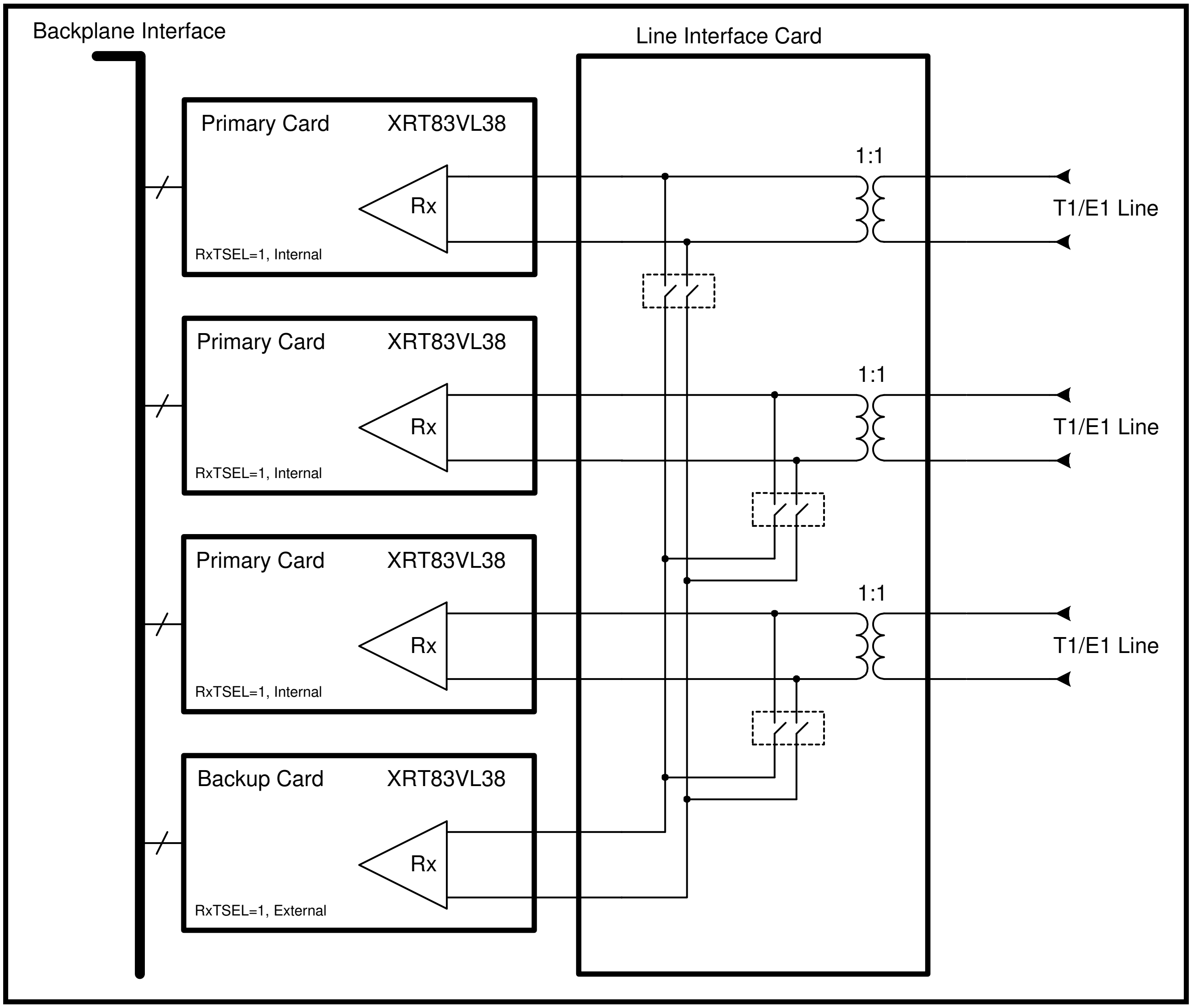


RECEIVE

For N+1 redundancy, the receivers on the primary cards should be programmed for internal impedance mode. The receivers on the backup card should be programmed for external impedance mode. Since there is no external resistor in the circuit, the receivers on the backup card will be high impedance. Select the impedance for the desired mode of operation, T1/E1/J1. To swap the primary card, set the backup card to internal impedance mode, then the primary card to external impedance mode. See **Figure 19**. for a simplified block diagram of the receive section for a N+1 redundancy scheme.

NOTE: *For simplification, the over voltage protection circuitry was omitted.*

FIGURE 19. SIMPLIFIED BLOCK DIAGRAM - RECEIVE SECTION FOR N+1 REDUNDANCY



PATTERN TRANSMIT AND DETECT FUNCTION

Several test and diagnostic patterns can be generated and detected by the chip. In **Hardware** mode each channel can be independently programmed to transmit an All Ones pattern by applying a “High” level to the corresponding TAOS_n pin. In **Host** mode, the three interface bits TXTEST[2:0] control the pattern generation and detection independently for each channel according to **Table 10**.

TABLE 10: PATTERN TRANSMISSION CONTROL

TXTEST2	TXTEST1	TXTEST0	TEST PATTERN
0	x	x	None
1	0	0	TDQRSS
1	0	1	TAOS
1	1	0	TLUC
1	1	1	TLDC

TRANSMIT ALL ONES (TAOS)

This feature is available in both **Hardware** and **Host** modes. With the TAOS_n pin connected to a “High” level or when interface bits TXTEST2=“1”, TXTEST1=“0” and TXTEST0=“1” the transmitter ignores input from TPOS_n/TDATA_n and TNEG_n/CODES_n pins and sends a continuous AMI encoded all “Ones” signal to the line, using TCLK_n clock as the reference. In addition, when the **Hardware** pin and interface bit ATAOS is activated, the chip will automatically transmit the All “Ones” data from any channel that detects an RLOS condition. This feature is not available on a per channel basis. TCLK_n must NOT be tied “Low”.

NETWORK LOOP CODE DETECTION AND TRANSMISSION

This feature is available in **Host** mode only. When the interface bits TXTEST2=”1”, TXTEST1=”1” and TXTEST0=”0” the chip is enabled to transmit the “00001” Network Loop-Up Code from the selected channel requesting a Loop-Back condition from the remote terminal. Simultaneously setting the interface bits NLCDE1=”0” and NLCDE0=”1” enables the Network Loop-Up code detection in the receiver. If the “00001” Network Loop-Up code is detected in the receive data for longer than 5 seconds, the NLCD bit in the interface register is set indicating that the remote terminal has activated remote Loop-Back and the chip is receiving its own transmitted data. When the interface bits TXTEST2=”1”, TXTEST1=”1” and TXTEST0=”1” the chip is enabled to transmit the Network Loop-Down Code (TLDC) “001” from the selected channel requesting the remote terminal the removal of the Loop-Back condition.

In the **Host** mode each channel is capable of monitoring the contents of the receive data for the presence of Loop-Up or Loop-Down code from the remote terminal. In the **Host** mode the two interface bits NLCDE[1:0] control the Loop-Code detection independently for each channel according to **Table 11**.

TABLE 11: LOOP-CODE DETECTION CONTROL

NLCDE1	NLCDE0	CONDITION
0	0	Disable Loop-Code Detection
0	1	Detect Loop-Up Code in Receive Data
1	0	Detect Loop-Down Code in Receive Data
1	1	Automatic Loop-Code detection and Remote Loop-Back Activation

Setting the interface bits to NLCDE1=”0” and NLCDE0=”1” activates the detection of the Loop-Up code in the receive data. If the “00001” Network Loop-Up code is detected in the receive data for longer than 5 seconds, the NLCD interface bit is set to “1” and stays in this state for as long as the receiver continues to receive the

Network Loop-Up Code. In this mode if the NLCD interrupt is enabled, the chip will initiate an interrupt on every transition of NLCD. The host has the option to ignore the request from the remote terminal, or to respond to the request and manually activate Remote Loop-Back. The host can subsequently activate the detection of the Loop-Down Code by setting NLCDE1="1" and NLCDE0="0". In this case, receiving the "001" Loop-Down Code for longer than 5 seconds will set the NLCD bit to "1" and if the NLCD interrupt is enabled, the chip will initiate an interrupt on every transition of NLCD. The host can respond to the request from the remote terminal and remove Loop-Back condition. In the manual Network Loop-Up (NLCDE1="0" and NLCDE0="1") and Loop-Down (NLCDE1="1" and NLCDE0="0") Code detection modes, the NLCD interface bit will be set to "1" upon receiving the corresponding code in excess of 5 seconds in the receive data. The chip will initiate an interrupt any time the status of the NLCD bit changes and the Network Loop-code interrupt is enabled.

In the **Host** mode, setting the interface bits NLCDE1="1" and NLCDE0="1" enables the automatic Loop-Code detection and Remote Loop-Back activation mode if, TXTEST[2:0] is NOT equal to "110". As this mode is initiated, the state of the NLCD interface bit is reset to "0" and the chip is programmed to monitor the receive input data for the Loop-Up Code. If the "00001" Network Loop-Up Code is detected in the receive data for longer than 5 seconds in addition to the NLCD bit in the interface register being set, Remote Loop-Back is automatically activated. The chip stays in remote Loop-Back even if it stops receiving the "00001" pattern. After the chip detects the Loop-Up code, sets the NLCD bit and enters Remote Loop-Back, it automatically starts monitoring the receive data for the Loop-Down code. In this mode however, the NLCD bit stays set even if the receiver stops receiving the Loop-Up code, which is an indication to the host that the Remote Loop-Back is still in effect. Remote Loop-Back is removed if the chip detects the "001" Loop-Down code for longer than 5 seconds. Detecting the "001" code also results in resetting the NLCD interface bit and initiating an interrupt. The Remote Loop-Back can also be removed by taking the chip out of the Automatic detection mode by programming it to operate in a different state. The chip will not respond to remote Loop-Back request if Local Analog Loop-Back is activated locally. When programmed in Automatic detection mode the NLCD interface bit stays "High" for the whole time the Remote Loop-Back is activated and initiates an interrupt any time the status of the NLCD bit changes provided the Network Loop-code interrupt is enabled.

TRANSMIT AND DETECT QUASI-RANDOM SIGNAL SOURCE (TDQRSS)

Each channel of XRT83VL38 includes a QRSS pattern generation and detection block for diagnostic purposes that can be activated only in the **Host** mode by setting the interface bits TXTEST2="1", TXTEST1="0" and TXTEST0="0". For T1 systems, the QRSS pattern is a 2^{20}-1pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros. For E1 systems, the QRSS pattern is 2^{15} -1 PRBS with an inverted output. With QRSS and Analog Local Loop-Back enabled simultaneously, and by monitoring the status of the QRPD interface bit, all main functional blocks within the transceiver can be verified.

When the receiver achieves QRSS synchronization with fewer than 4 errors in a 128 bits window, QRPD changes from "Low" to "High". After pattern synchronization, any bit error will cause QRPD to go "Low" for one clock cycle. If the QRPDIE bit is enabled, any transition on the QRPD bit will generate an interrupt.

With TDQRSS activated, a bit error can be inserted in the transmitted QRSS pattern by transitioning the INSBER interface bit from "0" to "1". Bipolar violation can also be inserted either in the QRSS pattern, or input data when operating in the single-rail mode by transitioning the INSBPV interface bit from "0" to "1". The state of INSBER and INSBPV bits are sampled on the rising edge of the TCLK_n. To insure the insertion of the bit error or bipolar violation, a "0" should be written in these bit locations before writing a "1".

LOOP-BACK MODES

The XRT83VL38 supports several Loop-Back modes under both **Hardware** and **Host** control. In **Hardware** mode the two LOOP[1:0] pins control the Loop-Back functions for each channel independently according to **Table 12**.

TABLE 12: LOOP-BACK CONTROL IN HARDWARE MODE

LOOP1	LOOP0	LOOP-BACK MODE
0	0	None
0	1	Analog
1	0	Remote
1	1	Digital

In **Host** mode the Loop-Back functions are controlled by the three LOOP[2:0] interface bits. Each channel can be programmed independently according to **Table 13**.

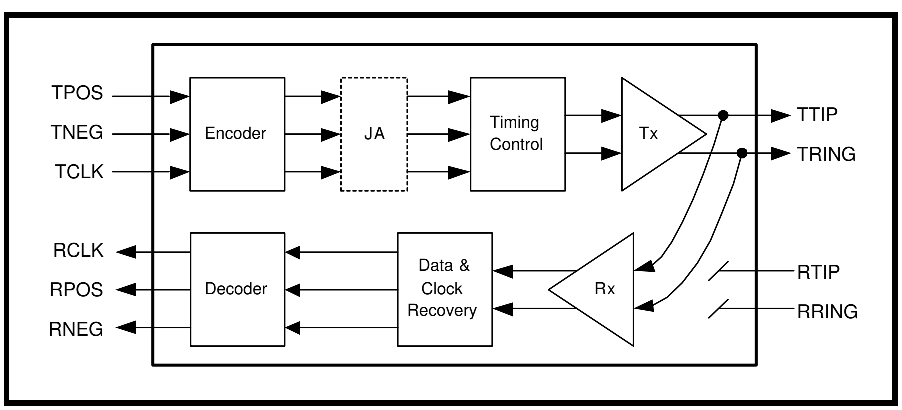
TABLE 13: LOOP-BACK CONTROL IN HOST MODE

LOOP2	LOOP1	LOOP0	LOOP-BACK MODE
0	X	X	None
1	0	0	Dual
1	0	1	Analog
1	1	0	Remote
1	1	1	Digital

LOCAL ANALOG LOOP-BACK (ALOOP)

With Local Analog Loop-Back activated, the transmit data at TTIP and TRING are looped-back to the analog input of the receiver. External inputs at RTIP/RRING in this mode are ignored while valid transmit data continues to be sent to the line. Local Analog Loop-Back exercises most of the functional blocks of the XRT83VL38 including the jitter attenuator which can be selected in either the transmit or receive paths. Local Analog Loop-Back is shown in **Figure 20**.

FIGURE 20. LOCAL ANALOG LOOP-BACK SIGNAL FLOW

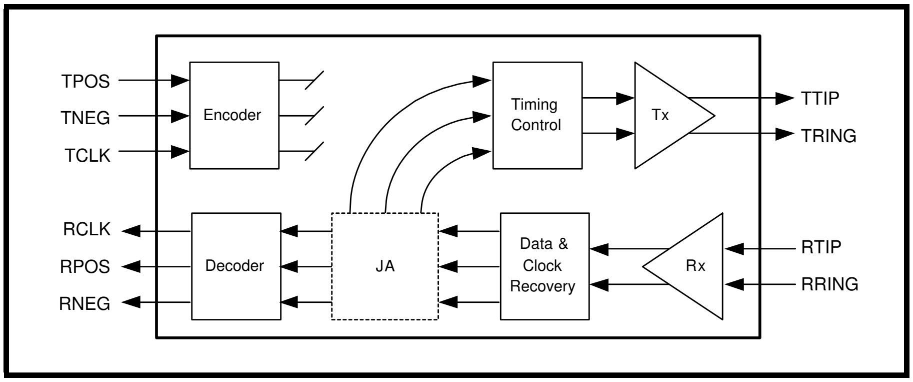


In this mode, the jitter attenuator (if selected) can be placed in the transmit or receive path.

REMOTE LOOP-BACK (RLOOP)

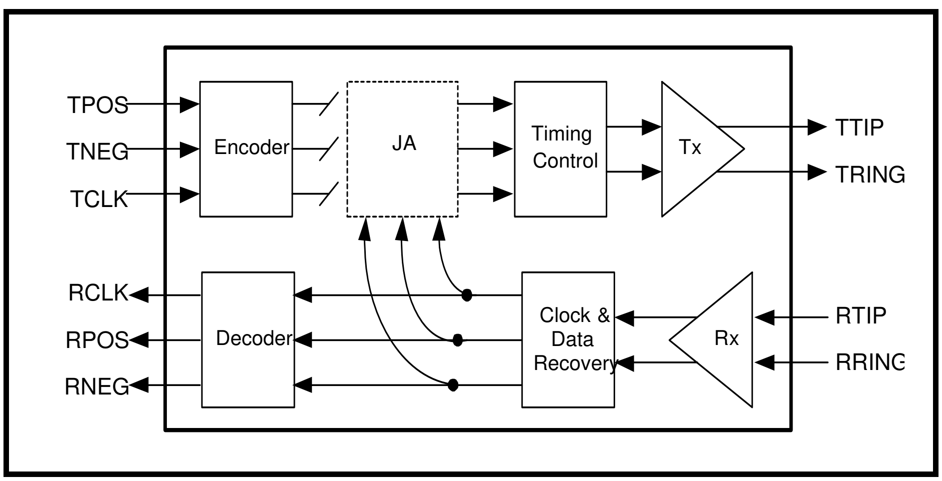
With Remote Loop-Back activated, receive data after the jitter attenuator (if selected in the receive path) is looped back to the transmit path using RCLK as transmit timing. In this mode transmit clock and data are ignored, while RCLK and receive data will continue to be available at their respective output pins. Remote Loop-Back with jitter attenuator selected in the receive path is shown in **Figure 21**.

FIGURE 21. REMOTE LOOP-BACK MODE WITH JITTER ATTENUATOR SELECTED IN RECEIVE PATH



In the Remote Loop-Back mode if the jitter attenuator is selected in the transmit path, the receive data from the Clock and Data Recovery block is looped back to the transmit path and is applied to the jitter attenuator using RCLK as transmit timing. In this mode the transmit clock and data are also ignored, while RCLK and received data will continue to be available at their respective output pins. Remote Loop-Back with the jitter attenuator selected in the transmit path is shown in **Figure 22**.

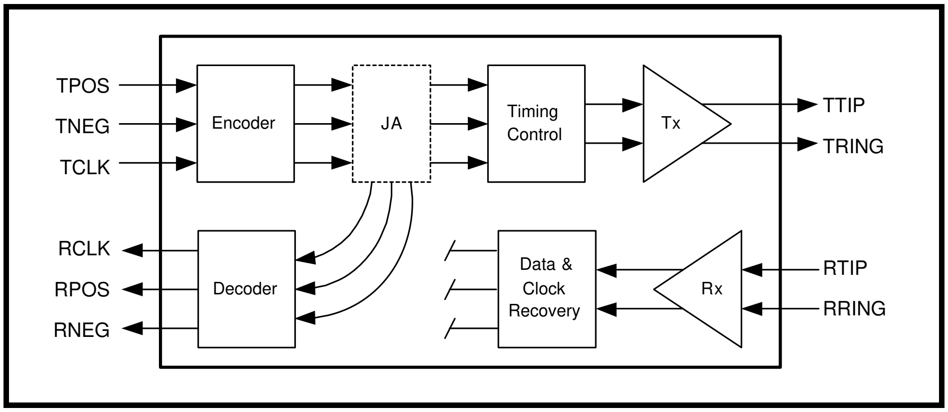
FIGURE 22. REMOTE LOOP-BACK MODE WITH JITTER ATTENUATOR SELECTED IN TRANSMIT PATH



DIGITAL LOOP-BACK (DLOOP)

Digital Loop-Back or Local Loop-Back allows the transmit clock and data to be looped back to the corresponding receiver output pins through the encoder/decoder and jitter attenuator. In this mode, receive data and clock are ignored, but the transmit data will be sent to the line uninterrupted. This loop back feature allows users to configure the line interface as a pure jitter attenuator. The Digital Loop-Back signal flow is shown in Figure 23.

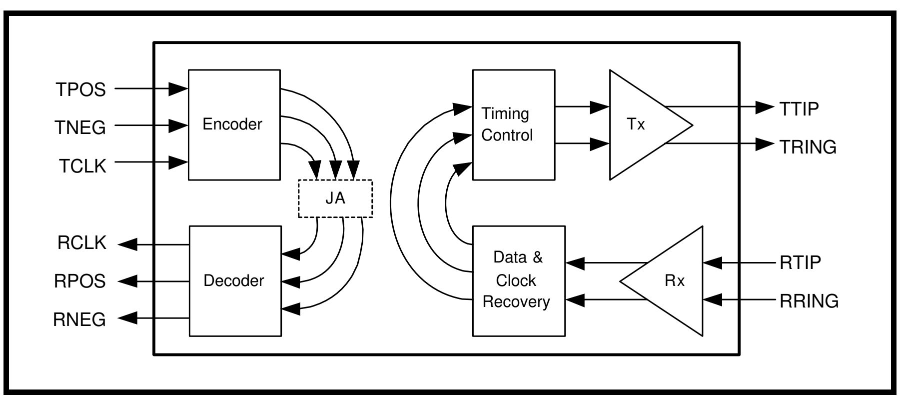
FIGURE 23. DIGITAL LOOP-BACK MODE WITH JITTER ATTENUATOR SELECTED IN TRANSMIT PATH



DUAL LOOP-BACK

Figure 24 depicts the data flow in dual-loopback. In this mode, selecting the jitter attenuator in the transmit path will have the same result as placing the jitter attenuator in the receive path. In dual Loop-Back mode the recovered clock and data from the line are looped back through the transmitter to the TTIP and TRING without passing through the jitter attenuator. The transmit clock and data are looped back through the jitter attenuator to the RCLK and RPOS/RDATA and RNEG pins. For proper operation of Dual Loop-Back mode, TCLK must be present.

FIGURE 24. SIGNAL FLOW IN DUAL LOOP-BACK MODE



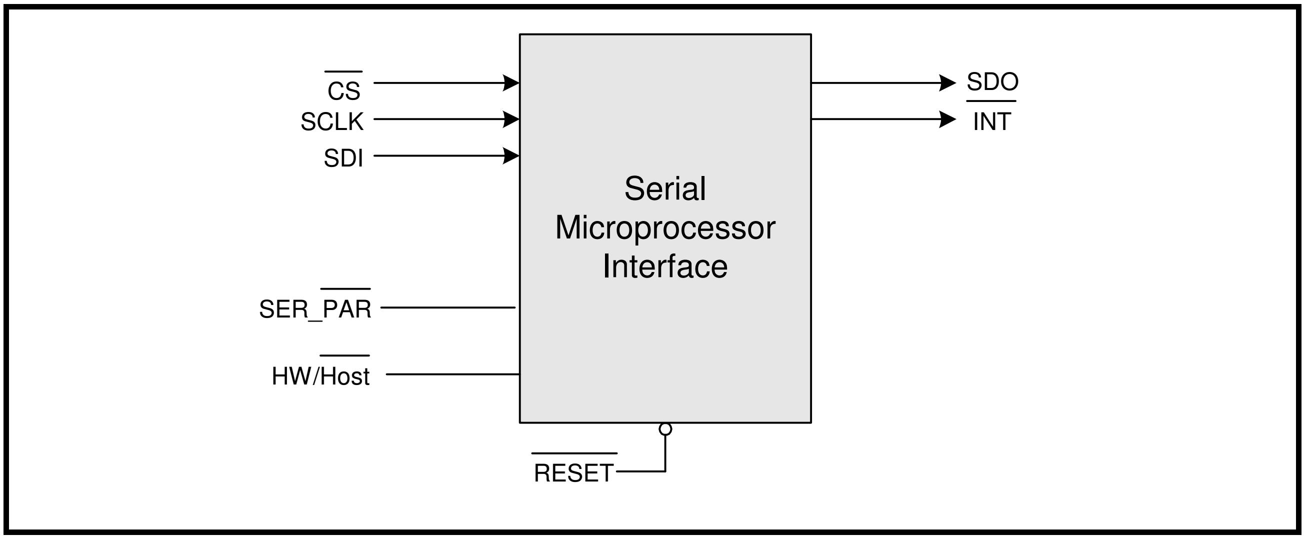
MICROPROCESSOR INTERFACE

The microprocessor interface can be accessed through a standard serial interface or a standard parallel microprocessor interface. The SER_PAR pin is used to select between the two. By default, the chip is configured in the Parallel Microprocessor interace. For Serial communication, this pin must be pulled “High”.

SERIAL MICROPROCESSOR INTERFACE BLOCK

The serial microprocessor uses a standard 3-pin serial port with CS, SCLK, and SDI for programming the LIU. Optional pins such as SDO, INT, and RESET allow the ability to read back contents of the registers, monitor the LIU via an interrupt pin, and reset the LIU to its default configuration by pulling reset "Low" for more than 10µS. A simplified block diagram of the Serial Microprocessor is shown in **Figure 25**.

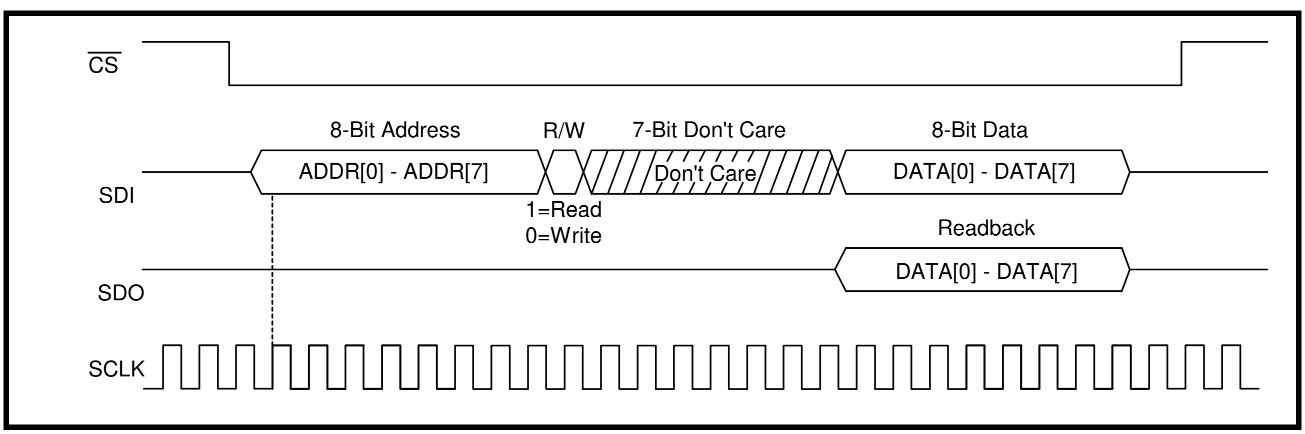
FIGURE 25. SIMPLIFIED BLOCK DIAGRAM OF THE SERIAL MICROPROCESSOR INTERFACE



SERIAL TIMING INFORMATION

The serial port requires 24 bits of data applied to the SDI (Serial Data Input) pin. The Serial Microprocessor samples SDI on the rising edge of SCLK (Serial Clock Input). The data is not latched into the device until all 24 bits of serial data have been sampled. A timing diagram of the Serial Microprocessor is shown in **Figure 26**.

FIGURE 26. TIMING DIAGRAM FOR THE SERIAL MICROPROCESSOR INTERFACE



NOTE: *For applications without a free running SCLK, a minimum of 1 SCLK pulse must be applied when CS is “High”, befrore pulling CS “Low”.*

24-BIT SERIAL DATA INPUT DESCRITPTION

The serial data input is sampled on the rising edge of SCLK. In readback mode, the serial data output is updated on the falling edge of SCLK. The serial data must be applied to the LIU LSB first. The 24 bits of serial data are described below.

ADDR[7:0] (SCLK1 - SCLK8)

The first 8 SCLK cycles are used to provide the address to which a Read or Write operation will occur. ADDR[0] (LSB) must be sent to the LIU first followed by ADDR[1] and so forth until all 8 address bits have been sampled by SCLK.

R/W (SCLK9)

The next serial bit applied to the LIU informs the microprocessor that a Read or Write operation is desired. If the R/W bit is set to "0", the microprocessor is configured for a Write operation. If the R/W bit is set to "1", the microprocessor is configured for a Read operation.

DUMMY BITS (SCLK10 - SCLK16)

The next 7 SCLK cycles are used as dummy bits. Seven bits were chosen so that the serial interface can easily be divided into three 8-bit words to be compliant with standard serial interface devices. The state of these bits are ignored and can hold either "0" or "1" during both Read and Write operations.

DATA[7:0] (SCLK17 - SCLK24)

The next 8 SCLK cycles are used to provide the data to be written into the internal register chosen by the address bits. DATA[0] (LSB) must be sent to the LIU first followed by DATA[1] and so forth until all 8 data bits have been sampled by SCLK. Once 24 SCLK cycles have been completed, the LIU holds the data until $\overline{CS}$ is pulled "High" whereby, the serial microprocessor latches the data into the selected internal register.

8-BIT SERIAL DATA OUTPUT DESCRIPTION

The serial data output is updated on the falling edge of SCLK17 - SCLK24 if R/W is set to "1". DATA[0] (LSB) is provided on SCLK17 to the SDO pin first followed by DATA[1] and so forth until all 8 data bits have been updated. The SDO pin allows the user to read the contents stored in individual registers by providing the desired address on the SDI pin during the Read cycle.

FIGURE 27. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

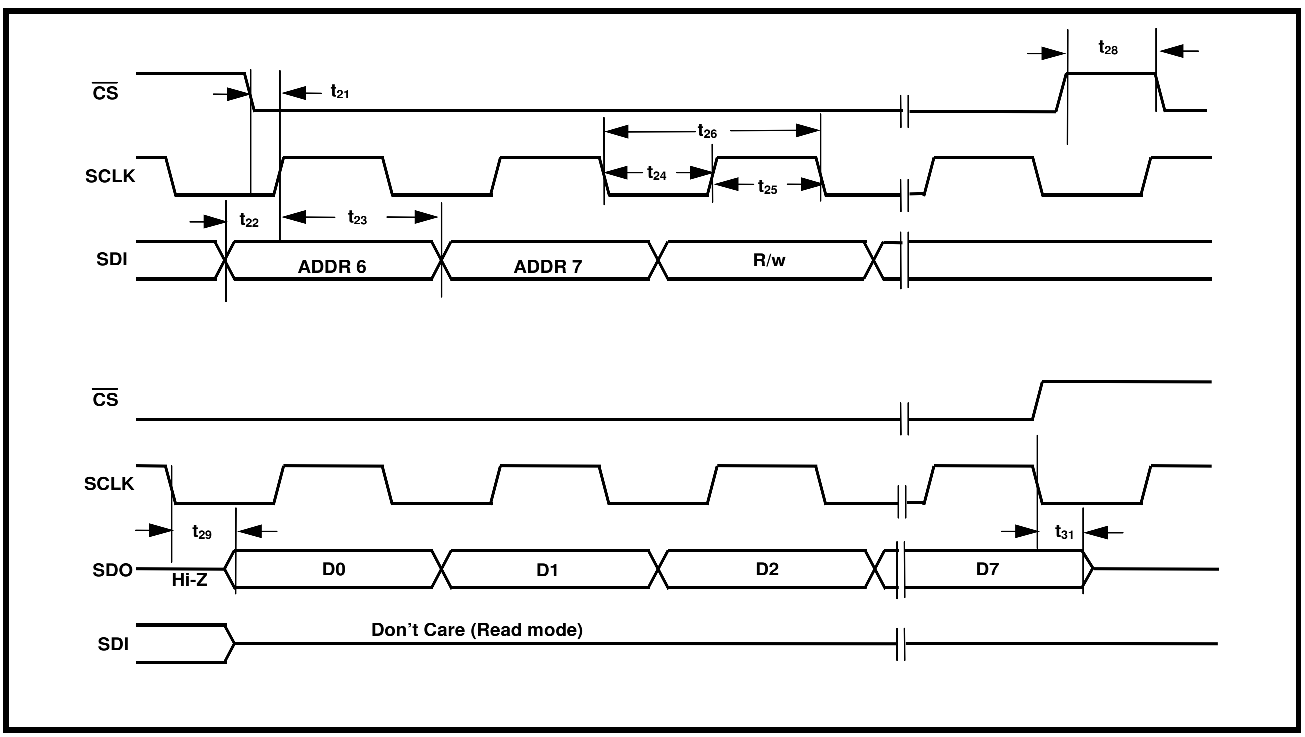


TABLE 14: MICROPROCESSOR SERIAL INTERFACE TIMINGS ($T_A = 25^0C$, V_{DD}=3.3V± 5% AND LOAD = 10PF)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk	5			ns
t_{22}	SDI to Rising Edge of SClk	5			ns
t_{23}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{24}	SClk "Low" Time	20			ns
t_{25}	SClk "High" Time	20			ns
t_{26}	SClk Period	40			ns
t_{28}	$\overline{CS}$ Inactive Time	40			ns
t_{29}	Falling Edge of SClk to SDO Valid Time			5	ns
t_{31}	Rising edge of $\overline{CS}$ to High Z			5	ns

PARALLEL MICROPROCESSOR INTERFACE BLOCK

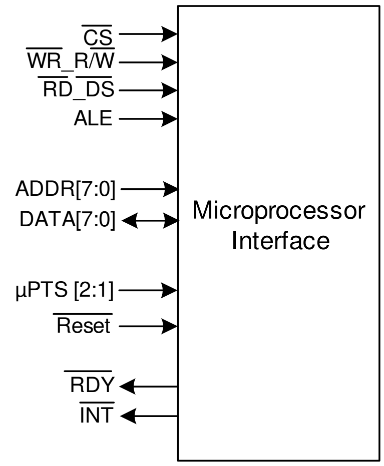
The Parallel Microprocessor Interface section supports communication between the local microprocessor (µP) and the LIU. The XRT83VL38 supports an Intel asynchronous interface and Motorola 68K asynchronous interface. The microprocessor interface is selected by the state of the µPTS[2:1] input pins. Selecting the microprocessor interface is shown in Table 15.

TABLE 15: SELECTING THE MICROPROCESSOR INTERFACE MODE

µPTS[2:1]	MICROPROCESSOR MODE
0h (00)	Intel 68HC11, 8051, 80C188 (Asynchronous)
1h (01)	Motorola 68K (Asynchronous)

The XRT83VL38 uses multipurpose pins to configure the device appropriately. The local µP configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The microprocessor interface also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in Figure 28.

FIGURE 28. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



THE MICROPROCESSOR INTERFACE BLOCK SIGNALS

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in Table 16, Table 17, and Table 18. The microprocessor interface can be configured to operate in Intel mode or Motorola mode. When the microprocessor interface is operating in Intel mode, some of the control signals function in a manner required by the Intel 80xx family of microprocessors. Likewise, when the microprocessor interface is operating in Motorola mode, then these control signals function in a manner as required by the Motorola microprocessors. (For using a Motorola 68K asynchronous processor, see Figure 30 and Table 20) Table 16 lists and describes those microprocessor interface signals whose role is constant across the two modes. Table 17 describes the role of some of these signals when the microprocessor interface is operating in the Intel mode. Likewise, Table 18 describes the role of these signals when the microprocessor interface is operating in the Motorola Power PC mode.

TABLE 16: XRT83VL38 MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH INTEL AND MOTOROLA MODES

PIN NAME	TYPE	DESCRIPTION
µPTS[2:1]	I	**Microprocessor Interface Mode Select Input pins** These two pins are used to specify the microprocessor interface mode. The relationship between the state of these two input pins, and the corresponding microprocessor mode is presented in Table 15.
DATA[7:0]	I/O	**Bi-Directional Data Bus for register "Read" or "Write" Operations.**
ADDR[7:0]	I	**Eight-Bit Address Bus Inputs** The XRT83VL38 LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access.
CS	I	**Chip Select Input** This active low signal selects the microprocessor interface of the XRT83VL38 LIU and enables Read/Write operations with the on-chip register locations.

TABLE 17: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT83VL38 PIN NAME	INTEL EQUIVALENT PIN	TYPE	DESCRIPTION
ALE	ALE	I	**Address-Latch Enable:** This active high signal is used to latch the contents on the address bus ADDR[7:0]. The contents of the address bus are latched into the ADDR[7:0] inputs on the falling edge of ALE.
RD_DS	RD	I	**Read Signal:** This active low input functions as the read signal from the local µP. When this pin is pulled “Low” (if CS is “Low”) the LIU is informed that a read operation has been requested and begins the process of the read cycle.
WR_R/W	WR	I	**Write Signal:** This active low input functions as the write signal from the local µP. When this pin is pulled “Low” (if CS is “Low”) the LIU is informed that a write operation has been requested and begins the process of the write cycle.
RDY	RDY	O	**Ready Output:** This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.

TABLE 18: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT83VL38 PIN NAME	MOTOROLA EQUIVALENT PIN	TYPE	DESCRIPTION
ALE	AS	I	**Address Strobe:** This active high signal is used to latch the contents on the address bus ADDR[7:0]. The contents of the address bus are latched into the ADDR[7:0] inputs on the falling edge of AS.
WR_R/W	R/W	I	**Read/Write:** This input pin from the local µP is used to inform the LIU whether a Read or Write operation has been requested. When this pin is pulled “High”, DS will initiate a read operation. When this pin is pulled “Low”, DS will initiate a write operation.
RD_DS	DS	I	**Data Strobe:** This active low input functions as the read or write signal from the local µP dependent on the state of R/W. When DS is pulled “Low” (If CS is “Low”) the LIU begins the read or write operation.
RDY	DTACK	O	**Data Transfer Acknowledge:** This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.

INTEL MODE PROGRAMMED I/O ACCESS (ASYNCHRONOUS)

If the LIU is interfaced to an Intel type µP, then it should be configured to operate in the Intel mode. Intel type Read and Write operations are described below.

Intel Mode Read Cycle

Whenever an Intel-type µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the CS pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The µP should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.

5. Next, the µP should indicate that this current bus cycle is a Read operation by toggling the RD input pin "Low". This action also enables the bi-directional data bus output drivers of the LIU.
6. After the µP toggles the Read signal "Low", the LIU will toggle the RDY output pin "Low". The LIU does this in order to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
7. After the µP detects the RDY signal and has read the data, it can terminate the Read Cycle by toggling the RD input pin "High".

NOTE: ALE can be tied "High" if this signal is not available.

The Intel Mode Write Cycle

Whenever an Intel type µP wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the CS pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. Toggle the ALE input pin "High". This step enables the address bus input drivers, within the microprocessor interface block of the LIU.
4. The µP should then toggle the ALE pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
5. The µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus DATA[7:0].
6. Next, the µP should indicate that this current bus cycle is a Write operation by toggling the WR input pin "Low". This action also enables the bi-directional data bus input drivers of the LIU.
7. After the µP toggles the Write signal "Low", the LIU will toggle the RDY output pin "Low". The LIU does this in order to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.

NOTE: ALE can be tied "High" if this signal is not available.

The Intel Read and Write timing diagram is shown in **Figure 29**. The timing specifications are shown in **Table 19**.

FIGURE 29. INTEL µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

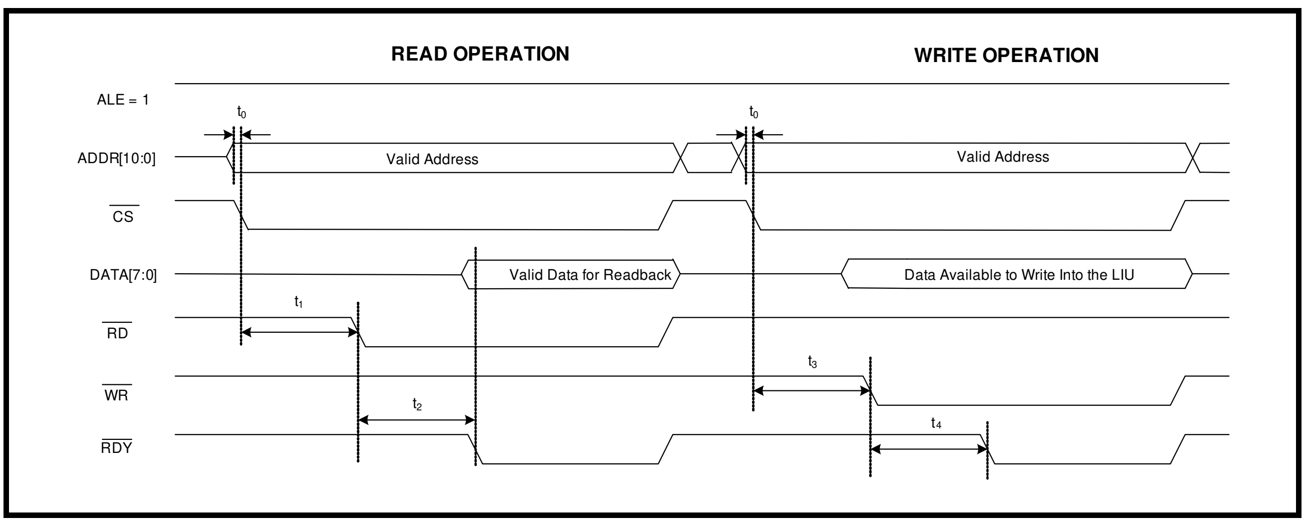


TABLE 19: INTEL MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	65	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{RD}$ Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	65	-	ns
t_4	$\overline{WR}$ Assert to $\overline{RDY}$ Assert	-	90	ns
NA	$\overline{WR}$ Pulse Width (t_4)	90	-	ns

MOTOROLA MODE PROGRAMMED I/O ACCESS (ASYNCHRONOUS)

If the LIU is interfaced to a Motorola type µP, it should be configured to operate in the Motorola mode. Motorola type programmed I/O Read and Write operations are described below.

Motorola Mode Read Cycle

Whenever a Motorola type µP wishes to read the contents of a register, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. The µP should then toggle the AS pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the µP should indicate that this current bus cycle is a Read operation by pulling the R/$\overline{W}$ input pin "High".
5. Toggle the DS input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
6. After the µP toggles the DS signal "Low", the LIU will toggle the $\overline{DTACK}$ output pin "Low". The LIU does this in order to inform the µP that the data is available to be read by the µP, and that it is ready for the next command.
7. After the µP detects the $\overline{DTACK}$ signal and has read the data, it can terminate the Read Cycle by toggling the DS input pin "High".

Motorola Mode Write Cycle

Whenever a motorola type µP wishes to write a byte or word of data into a register within the LIU, it should do the following.

1. Place the address of the target register on the address bus input pins ADDR[7:0].
2. While the µP is placing this address value on the address bus, the address decoding circuitry should assert the $\overline{CS}$ pin of the LIU, by toggling it "Low". This action enables further communication between the µP and the LIU microprocessor interface block.
3. The µP should then toggle the AS pin "Low". This step causes the LIU to latch the contents of the address bus into its internal circuitry. At this point, the address of the register has now been selected.
4. Next, the µP should indicate that this current bus cycle is a Write operation by pulling the R/$\overline{W}$ input pin "Low".
5. Toggle the DS input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
6. After the µP toggles the DS signal "Low", the LIU will toggle the $\overline{DTACK}$ output pin "Low". The LIU does this in order to inform the µP that the data has been written into the internal register location, and that it is ready for the next command.

7. After the µP detects the $\overline{DTACK}$ signal and has read the data, it can terminate the Read Cycle by toggling the DS input pin "High".

The Motorola Read and Write timing diagram is shown in **Figure 30**. The timing specifications are shown in **Table 20**.

FIGURE 30. MOTOROLA 68K µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

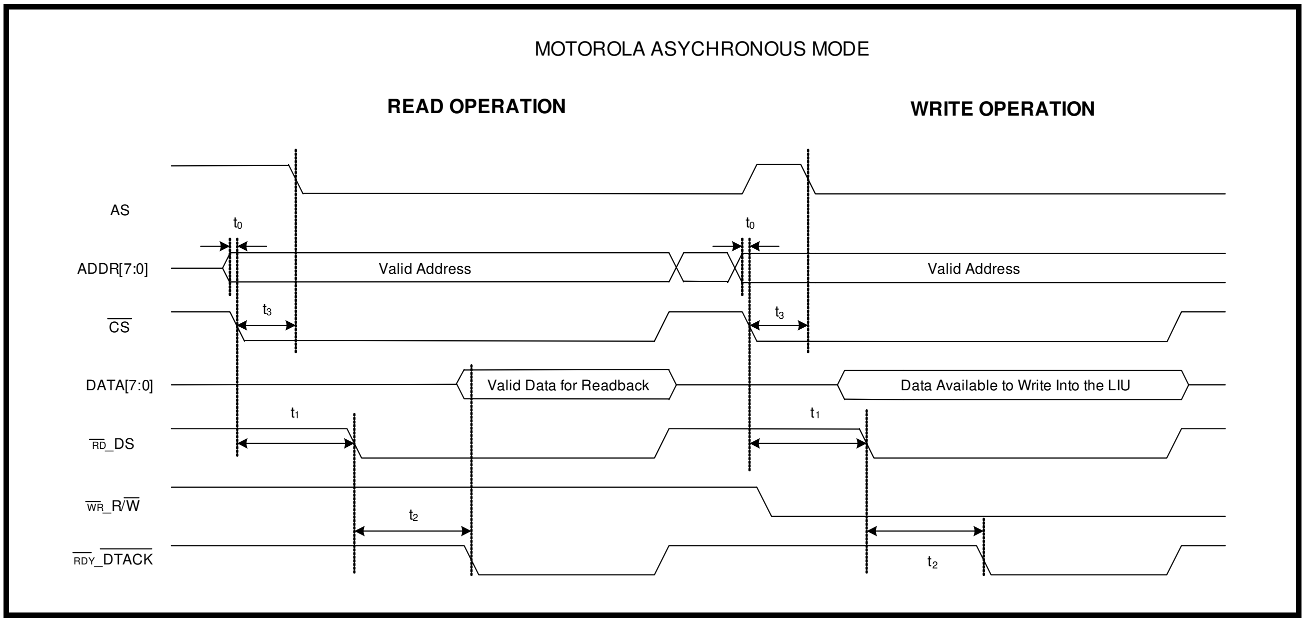


TABLE 20: MOTOROLA 68K MICROPROCESSOR INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{DS}$ (Pin $\overline{RD}$_DS) Assert	65	-	ns
t_2	DS Assert to $\overline{DTACK}$ Assert	-	90	ns
NA	DS Pulse Width (t_2)	90	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{AS}$ (Pin ALE) Falling Edge	0	-	ns

MICROPROCESSOR REGISTER TABLES

The microprocessor interface consists of 256 addressable locations. Each channel uses 16 dedicated 8 byte registers for independent programming and control. There are four additional registers for global control of all channels and two registers for device identification and revision numbers. The remaining registers are for factory test and future expansion. The control register map and the function of the individual bits are summarized in **Table 21** and **Table 22** respectively.

TABLE 21: MICROPROCESSOR REGISTER ADDRESS

REGISTER NUMBER	REGISTER ADDRESS		FUNCTION
	HEX	BINARY	
0 - 15	0x00 - 0x0F	00000000 - 00001111	Channel 0 Control Registers
16 - 31	0x10 -0x1F	00010000 - 00011111	Channel 1 Control Registers
32 - 47	0x20 - 0x2F	00100000 - 00101111	Channel 2 Control Registers
48 - 63	0x30 - 0x3F	00110000 - 00111111	Channel 3 Control Registers
64 - 79	0x40 - 0x4F	01000000 - 01001111	Channel 4 Control Registers
80 - 95	0x50 - 0x5F	01010000 - 01011111	Channel 5 Control Registers
96-111	0x60 - 0x6F	01100000 - 01101111	Channel 6 Control Registers
112 - 127	0x70 - 0x7F	01110000 - 01111111	Channel 7 Control Registers
128 - 131	0x80 - 0x83	10000000 - 10000011	Command Control registers for all 8 channels
132 -139	0x84 - 0x8B	10000100 - 10001011	R/W registers reserved for testing channels 0-3
140 - 191	0x8C - 0xBF	10001100 - 10111111	Reserved
192	0xC0	11000000	Command Control register for all 8 channels
193 - 195	0xC1 - 0xC3	11000001 - 11000011	Reserved
196 - 203	0xC4 - 0xCB	11000100 - 11001011	R/W registers reserved for testing channels 4-7
204 - 253	0xCC - 0xFD	11001100 - 11111101	Reserved
254	0xFE	11111110	Device “ID”
255	0xFF	11111111	Device “Revision ID”

TABLE 22: MICROPROCESSOR REGISTER BIT DESCRIPTION

REG. #	ADDRESS	REG. TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Channel 0 Control Registers										
0	00000000 Hex 0x00	R/W	QRSS/PRBS	PRBS_Rx/$\overline{\text{Tx}}$	RXON_n	EQC4_n	EQC3_n	EQC2_n	EQC1_n	EQC0_n
1	00000001 Hex 0x01	R/W	RXTSEL_n	TXTSEL_n	TERSEL1_n	TERSEL0_n	JASEL1_n	JASEL0_n	JABW_n	FIFOS_n
2	00000010 Hex 0x02	R/W	INVQRSS_n	TXTEST2_n	TXTEST1_n	TXTEST0_n	TXON_n	LOOP2_n	LOOP1_n	LOOP0_n
3	00000011 Hex 0x03	R/W	NLCDE1_n	NLCDE0_n	CODES_n	RXRES1_n	RXRES0_n	INSBPV_n	INSBER_n	Reserved
4	00000100 Hex 0x04	R/W	Reserved	DMOIE_n	FLSIE_n	LCVIE_n	NLCDIE_n	AISDIE_n	RLOSIE_n	QRPDIE_n
5	00000101 Hex 0x05	RO	Reserved	DMO_n	FLS_n	LCV_n	NLCD_n	AISD_n	RLOS_n	QRPD_n
6	00000110 Hex 0x06	RUR	Reserved	DMOIS_n	FLSIS_n	LCVIS_n	NLCDIS_n	AISDIS_n	RLOSIS_n	QRPDIS_n

TABLE 22: MICROPROCESSOR REGISTER BIT DESCRIPTION

REG. #	ADDRESS	REG. TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
7	00000111 Hex 0x07	RO	Reserved	Reserved	CLOS5_n	CLOS4_n	CLOS3_n	CLOS2_n	CLOS1_n	CLOS0_n
8	00001000 Hex 0x08	R/W	X	B6S1_n	B5S1_n	B4S1_n	B3S1_n	B2S1_n	B1S1_n	B0S1_n
9	00001001 Hex 0x09	R/W	X	B6S2_n	B5S2_n	B4S2_n	B3S2_n	B2S2_n	B1S2_n	B0S2_n
10	00001010 Hex 0x0A	R/W	X	B6S3_n	B5S3_n	B4S3_n	B3S3_n	B2S3_n	B1S3_n	B0S3_n
11	00001011 Hex 0x0B	R/W	X	B6S4_n	B5S4_n	B4S4_n	B3S4_n	B2S4_n	B1S4_n	B0S4_n
12	00001100 Hex 0x0C	R/W	X	B6S5_n	B5S5_n	B4S5_n	B3S5_n	B2S5_n	B1S5_n	B0S5_n
13	00001101 Hex 0x0D	R/W	X	B6S6_n	B5S6_n	B4S6_n	B3S6_n	B2S6_n	B1S6_n	B0S6_n
14	00001110 Hex 0x0E	R/W	X	B6S7_n	B5S7_n	B4S7_n	B3S7_n	B2S7_n	B1S7_n	B0S7_n
15	00001111 Hex 0x0F	R/W	X	B6S8_n	B5S8_n	B4S8_n	B3S8_n	B2S8_n	B1S8_n	B0S8_n
			Reset = 0	Reset = 0	Reset = 0	Reset = 0	Reset = 0	Reset = 0	Reset = 0	Reset = 0
Command Control Global Registers for all 8 channels										
16-31	0001xxxx Hex 0x10-0x1F	R/W	Channel 1Control Register (see Registers 0-15 for description)							
32-47	0010xxxx Hex 0x20-ox2F	R/W	Channel 2 Control Register (see Registers 0-15 for description)							
48-63	0011xxxx Hex 0x30-0x3F	R/W	Channel 3 Control Register (see Registers 0-15 for description)							
64-79	0100xxxx Hex 0x40-0x4F	R/W	Channel 4 Control Register (see Registers 0-15 for description)							
80-95	0101xxxx Hex 0x50-0x5F	R/W	Channel 5 Control Register (see Registers 0-15 for description)							
96-111	0110xxxx Hex 0x60-0x6F	R/W	Channel 6 Control Register (see Registers 0-15 for description)							
112-127	0111xxxx Hex 0x70-0x7F	R/W	Channel 7 Control Register (see Registers 0-15 for description)							
Command Control Registers for All 8 Channels										
128	10000000 Hex 0x80	R/W	SR/$\overline{DR}$	ATAOS	RCLKE	TCLKE	DATAP	Reserved	GIE	SRESET
129	10000001 Hex 0x81	R/W	Reserved	CLKSEL2	CLKSEL1	CLKSEL0	MCLKRATE	RXMUTE	EXLOS	ICT
130	10000010 Hex 0x82	R/W	TXONCNTL	TERCNTL	Reserved	Reserved	Reserved			

TABLE 22: MICROPROCESSOR REGISTER BIT DESCRIPTION

REG. #	ADDRESS	REG. TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
131	10000011 Hex 0x83	R/W	GAUGE1	GAUGE0	Reserved	Reserved	SL_1	SL_0	EQG_1	EQG_0
Test Registers for channels 0 - 3										
132	10000100	R/W	Test byte 0							
133	10000101	R/W	Test byte 1							
134	10000110	R/W	Test byte 2							
135	10000111	R/W	Test byte 3							
136	10001000	R/W	Test byte 4							
137	10001001	R/W	Test byte 5							
138	10001010	R/W	Test byte 6							
139	10001011	R/W	Test byte 7							
Unused Registers										
140-191	100011xx									
Command Control Register for All 8 Channels										
192	11000000 Hex 0xC0	R/W	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	E1Arben
Unused Registers										
193-195	110000xx									
Test Registers for channels 4 - 7										
196	11000100	R/W	Test byte 0							
197	11000101	R/W	Test byte 0							
198	11000110	R/W	Test byte 0							
199	11000111	R/W	Test byte 0							
200	11001000	R/W	Test byte 0							
201	11001001	R/W	Test byte 0							
202	11001010	R/W	Test byte 0							
203	11001011	R/W	Test byte 0							
Unused Registers										
204	11001100									
….										
253	11111101									
ID Registers										
254	11111110 Hex 0xFE	RO	DEVICE ID hex: FD - Binary 11101010 (0xEA)							
255	11111111 Hex 0xFF	RO	DEVICE “Revision ID”							

MICROPROCESSOR REGISTER DESCRIPTIONS

TABLE 23: MICROPROCESSOR REGISTER #0, BIT DESCRIPTION

REGISTER ADDRESS 00000000 00010000 00100000 00110000 01000000 01010000 01100000 01110000 BIT #	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7 NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7	QRSS/PRBS	QRSS/PRBS Select Bit This bit selects between QRSS and PRBS. 1 = QRSS 0 = PRBS	R/W	0
D6	PRBS_Rx/$\overline{\text{Tx}}$	**PRBS Receive/Transmit Select:** This bit is used to select where the output of the PRBS Generator is directed if PRBS generation is enabled. 0 = Normal Operation - PRBS generator is output on TTIP and TRING if PRBS generation is enabled. 1 = PRBS Generator is output on RPOS; RNEG is internally grounded, if PRBS generation is enabled. ***NOTE:*** *If PRBS generation is disabled (see TxTEST[2:0]), user should set this bit to '0' for normal operation.*	R/W	
D5	RXON_n	**Receiver ON:** Writing a "1" into this bit location turns on the Receive Section of channel n. Writing a "0" shuts off the Receiver Section of channel n. ***NOTES:*** *1. This bit provides independent turn-off or turn-on control of each receiver channel.* *2. In **Hardware** mode all receiver channels are always on in the TQFP package. In the BGA package all receiver channels can be turned on or off together by applying the appropriate signal to the RXON pin (# K16).*	R/W	0
D4	EQC4_n	**Equalizer Control bit 4:** This bit together with EQC[3:0] are used for controlling transmit pulse shaping, transmit line build-out (LBO) and receive monitoring for either T1 or E1 Modes of operation. See Table 5 for description of Equalizer Control bits.	R/W	0
D3	EQC3_n	**Equalizer Control bit 3:** See bit D4 description for function of this bit	R/W	0
D2	EQC2_n	**Equalizer Control bit 2:** See bit D4 description for function of this bit	R/W	0

TABLE 23: MICROPROCESSOR REGISTER #0, BIT DESCRIPTION

D1	EQC1_n	**Equalizer Control bit 1:** See bit D4 description for function of this bit	R/W	0
D0	EQC0_n	**Equalizer Control bit 0:** See bit D4 description for function of this bit	R/W	0

TABLE 24: MICROPROCESSOR REGISTER #1, BIT DESCRIPTION

<table>
<tr><th>REGISTER ADDRESS
00000001
00010001
00100001
00110001
01000001
01010001
01100001
01110001</th><th>CHANNEL_n
CHANNEL_0
CHANNEL_1
CHANNEL_2
CHANNEL_3
CHANNEL_4
CHANNEL_5
CHANNEL_6
CHANNEL_7</th><th rowspan="2">FUNCTION</th><th rowspan="2">REGISTER TYPE</th><th rowspan="2">RESET VALUE</th></tr>
<tr><th>BIT #</th><th>NAME</th></tr>
<tr><td>D7</td><td>RXTSEL_n</td><td>Receiver Termination Select: In Host mode, this bit is used to select between the internal and external line termination modes for the receiver according to the following table;
<table><tr><th>RXTSEL</th><th>RX Termination</th></tr><tr><td>0</td><td>External</td></tr><tr><td>1</td><td>Internal</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>D6</td><td>TXTSEL_n</td><td>Transmit Termination Select: In Host mode, this bit is used to select between the internal and external line termination modes for the transmitter according to the following table;
<table><tr><th>TXTSEL</th><th>TX Termination</th></tr><tr><td>0</td><td>External</td></tr><tr><td>1</td><td>Internal</td></tr></table></td><td>R/W</td><td>0</td></tr>
<tr><td>D5</td><td>TERSEL1_n</td><td>Termination Impedance Select1:
In Host mode and in internal termination mode, (TXTSEL = “1” and RXTSEL = “1”) TERSEL[1:0] control the transmit and receive termination impedance according to the following table;
<table><tr><th>TERSEL1</th><th>TERSEL0</th><th>Termination</th></tr><tr><td>0</td><td>0</td><td>100Ω</td></tr><tr><td>0</td><td>1</td><td>110Ω</td></tr><tr><td>1</td><td>0</td><td>75Ω</td></tr><tr><td>1</td><td>1</td><td>120Ω</td></tr></table>In the internal termination mode, the receiver termination of each receiver is realized completely by internal resistors or by the combination of internal and one fixed external resistor.
In the internal termination mode, the transmitter output should be AC coupled to the transformer.</td><td>R/W</td><td>0</td></tr>
<tr><td>D4</td><td>TERSEL0_n</td><td>Termination Impedance Select bit 0:</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 24: MICROPROCESSOR REGISTER #1, BIT DESCRIPTION

D3	JASEL1_n	**Jitter Attenuator select bit 1:** The JASEL1 and JASEL0 bits are used to disable or place the jitter attenuator of each channel independently in the transmit or receive path.	R/W	0

JASEL1 bit D3	JASEL0 bit D2	JA Path
0	0	JA Disabled
0	1	JA in Transmit Path
1	0	JA in Receive Path
1	1	JA in Receive Path

D2	JASEL0_n	**Jitter Attenuator select bit 0:** See description of bit D3 for the function of this bit.	R/W	0
D1	JABW_n	**Jitter Attenuator Bandwidth Select:** In E1 mode, set this bit to "1" to select a 1.5Hz Bandwidth for the Jitter Attenuator. The FIFO length will be automatically set to 64 bits. Set this bit to "0" to select 10Hz Bandwidth for the Jitter Attenuator in E1 mode. In T1 mode the Jitter Attenuator Bandwidth is permanently set to 3Hz, and the state of this bit has no effect on the Bandwidth.	R/W	0

Mode	JABW bit D1	FIFOS_n bit D0	JA B-W Hz	FIFO Size
T1	0	0	3	32
T1	0	1	3	64
T1	1	0	3	32
T1	1	1	3	64
E1	0	0	10	32
E1	0	1	10	64
E1	1	0	1.5	64
E1	1	1	1.5	64

D0	FIFOS_n	**FIFO Size Select:** See table of bit D1 above for the function of this bit.	R/W	0

TABLE 25: MICROPROCESSOR REGISTER #2, BIT DESCRIPTION

REGISTER ADDRESS 00000010 00010010 00100010 00110010 01000010 01010010 01100010 01110010	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	INVQRSS_n	**Invert QRSS Pattern:** When TQRSS is active, Writing a “1” to this bit inverts the polarity of transmitted QRSS pattern. Writing a “0” sends the QRSS pattern with no inversion.	R/W	0
D6	TXTEST2_n	**Transmit Test Pattern bit 2**: This bit together with TXTEST1 and TXTEST0 are used to generate and transmit test patterns according to the following table: TXTEST2 / TXTEST1 / TXTEST0 / Test Pattern: 0 / X / X / No Pattern 1 / 0 / 0 / TDQRSS 1 / 0 / 1 / TAOS 1 / 1 / 0 / TLUC 1 / 1 / 1 / TLDC **TDQRSS (Transmit/Detect Quasi-Random Signal):** This condition when activated enables Quasi-Random Signal Source generation and detection for the selected channel number n. In a T1 system QRSS pattern is a 2^{20}-1 pseudo-random bit sequence (PRBS) with no more than 14 consecutive zeros. In a E1 system, QRSS is a 2^{15}-1 PRBS pattern. **TAOS (Transmit All Ones):** Activating this condition enables the transmission of an All Ones Pattern from the selected channel number n. **TLUC (Transmit Network Loop-Up Code):** Activating this condition enables the Network Loop-Up Code of “00001” to be transmitted to the line for the selected channel number n. When Network Loop-Up code is being transmitted, the XRT83VL38 will ignore the Automatic Loop-Code detection and Remote Loop-Back activation (NLCDE1 =“1”, NLCDE0 =“1”, if activated) in order to avoid activating Remote Digital Loop-Back automatically when the remote terminal responds to the Loop-Back request. **TLDC (Transmit Network Loop-Down Code):** Activating this condition enables the network Loop-Down Code of “001” to be transmitted to the line for the selected channel number n.	R/W	0
D5	TXTEST1_n	**Transmit Test pattern bit 1:** See description of bit D6 for the function of this bit.	R/W	0

TXTEST2	TXTEST1	TXTEST0	Test Pattern
0	X	X	No Pattern
1	0	0	TDQRSS
1	0	1	TAOS
1	1	0	TLUC
1	1	1	TLDC

TABLE 25: MICROPROCESSOR REGISTER #2, BIT DESCRIPTION

<table>
<tr><td>D4</td><td>TXTEST0_n</td><td>Transmit Test Pattern bit 0: See description of bit D6 for the function of this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>D3</td><td>TXON_n</td><td>Transmitter ON: Writing a “1” into this bit location turns on the Transmit and Receive Sections of channel n. Writing a “0” shuts off the Transmit Section of channel n. In this mode, TTIP_n and TRING_n driver outputs will be tri-stated for power reduction or redundancy applications.</td><td>R/W</td><td>0</td></tr>
<tr><td>D2</td><td>LOOP2_n</td><td>Loop-Back control bit 2: This bit together with the LOOP1 and LOOP0 bits control the Loop-Back modes of the chip according to the following table:
<table>
<tr><th>LOOP2</th><th>LOOP1</th><th>LOOP0</th><th>Loop-Back Mode</th></tr>
<tr><td>0</td><td>X</td><td>X</td><td>No Loop-Back</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Dual Loop-Back</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Analog Loop-Back</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Remote Loop-Back</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Digital Loop-Back</td></tr>
</table></td><td></td><td></td></tr>
<tr><td>D1</td><td>LOOP1_n</td><td>Loop-Back control bit 1: See description of bit D2 for the function of this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>D0</td><td>LOOP0_n</td><td>Loop-Back control bit 0: See description of bit D2 for the function of this bit.</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 26: MICROPROCESSOR REGISTER #3, BIT DESCRIPTION

<table>
<tr><th>REGISTER ADDRESS
00000011
00010011
00100011
00110011
01000011
01010011
01100011
01110011</th><th>CHANNEL_n
CHANNEL_0
CHANNEL_1
CHANNEL_2
CHANNEL_3
CHANNEL_4
CHANNEL_5
CHANNEL_6
CHANNEL_7</th><th rowspan="2">FUNCTION</th><th rowspan="2">REGISTER TYPE</th><th rowspan="2">RESET VALUE</th></tr>
<tr><th>BIT #</th><th>NAME</th></tr>
<tr><td>D7</td><td>NLCDE1_n</td><td>Network Loop Code Detection Enable Bit 1:
This bit together with NLCDE0_n control the Loop-Code detection of each channel.
<table>
<tr><th>NLCDE1</th><th>NLCDE0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>Disable Loop-code detection</td></tr>
<tr><td>0</td><td>1</td><td>Detect Loop-Up code in receive data</td></tr>
<tr><td>1</td><td>0</td><td>Detect Loop-Down code in receive data</td></tr>
<tr><td>1</td><td>1</td><td>Automatic Loop-Code detection</td></tr>
</table>
When NLCDE1 =”0” and NLCDE0 = “1” or NLCDE1 = “1” and NLCDE0 = “0”, the chip is manually programmed to monitor the receive data for the Loop-Up or Loop-Down code respectively.When the presence of the “00001” or “001” pattern is detected for more than 5 seconds, the status of the NLCD bit is set to “1” and if the NLCD interrupt is enabled, an interrupt is initiated.The Host has the option to control the Loop-Back function manually.
Setting the NLCDE1 = “1” and NLCDE0 = “1” enables the Automatic Loop-Code detection and Remote Loop-Back activation mode. As this mode is initiated, the state of the NLCD interface bit is reset to “0” and the chip is programmed to monitor the receive data for the Loop-Up code. If the “00001” pattern is detected for longer than 5 seconds, the NLCD bit is set “1”, Remote Loop-Back is activated and the chip is automatically programmed to monitor the receive data for the Loop-Down code. The NLCD bit stays set even after the chip stops receiving the Loop-Up code. The Remote Loop-Back condition is removed when the chip receives the Loop-Down code for more than 5 seconds or if the Automatic Loop-Code detection mode is terminated.</td><td>R/W</td><td>0</td></tr>
<tr><td>D6</td><td>NLCDE0_n</td><td>Network Loop Code Detection Enable Bit 0:
See description of D7 for function of this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>D5</td><td>CODES_n</td><td>Encoding and Decoding Select:
Writing a “0” to this bits selects HDB3 or B8ZS encoding and decoding for channel number n. Writing “1” selects an AMI coding scheme. This bit is only active when single rail mode is selected.</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 26: MICROPROCESSOR REGISTER #3, BIT DESCRIPTION

D4	RXRES1_n	Receive External Resistor Control Pin 1: In **Host** mode, this bit along with the RXRES0_n bit selects the value of the external Receive fixed resistor according to the following table; RXRES1_n / RXRES0_n / Required Fixed External RX Resistor: 0 / 0 / No external Fixed Resistor 0 / 1 / 240Ω 1 / 0 / 210Ω 1 / 1 / 150Ω	R/W	0
D3	RXRES0_n	**Receive External Resistor Control Pin 0:** For function of this bit see description of D4 the RXRES1_n bit.	R/W	0
D2	INSBPV_n	**Insert Bipolar Violation:** When this bit transitions from "0" to "1", a bipolar violation is inserted in the transmitted data stream of the selected channel number n. Bipolar violation can be inserted either in the QRSS pattern, or input data when operating in single-rail mode. The state of this bit is sampled on the rising edge of the respective TCLK_n. **NOTE:** *To ensure the insertion of a bipolar violation, a "0" should be written in this bit location before writing a "1".*	R/W	0
D1	INSBER_n	**Insert Bit Error:** With TDQRSS enabled, when this bit transitions from "0" to "1", a bit error will be inserted in the transmitted QRSS pattern of the selected channel number n. The state of this bit is sampled on the rising edge of the respective TCLK_n. **NOTE:** *To ensure the insertion of bit error, a "0" should be written in this bit location before writing a "1".*	R/W	0
D0	Reserved	**Reserved**	R/W	0

TABLE 27: MICROPROCESSOR REGISTER #4, BIT DESCRIPTION

REGISTER ADDRESS 00000100 00010100 00100100 00110100 01000100 01010100 01100100 01110100	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	**NAME**			
D7	Reserved		RO	0
D6	DMOIE_n	**DMO Interrupt Enable:** Writing a "1" to this bit enables DMO interrupt generation, writing a "0" masks it.	R/W	0

TABLE 27: MICROPROCESSOR REGISTER #4, BIT DESCRIPTION

D5	FLSIE_n	**FIFO Limit Status Interrupt Enable:** Writing a “1” to this bit enables interrupt generation when the FIFO limit is within to 3 bits, writing a “0” to masks it.	R/W	0
D4	LCVIE_n	**Line Code Violation Interrupt Enable:** Writing a “1” to this bit enables Line Code Violation interrupt generation, writing a “0” masks it.	R/W	0
D3	NLCDIE_n	**Network Loop-Code Detection Interrupt Enable:** Writing a “1” to this bit enables Network Loop-code detection interrupt generation, writing a “0” masks it.	R/W	0
D2	AISDIE_n	**AIS Interrupt Enable:** Writing a “1” to this bit enables Alarm Indication Signal detection interrupt generation, writing a “0” masks it.	R/W	0
D1	RLOSIE_n	**Receive Loss of Signal Interrupt Enable:** Writing a “1” to this bit enables Loss of Receive Signal interrupt generation, writing a “0” masks it.	R/W	0
D0	QRPDIE_n	**QRSS Pattern Detection Interrupt Enable:** Writing a “1” to this bit enables QRSS pattern detection interrupt generation, writing a “0” masks it.	R/W	0

TABLE 28: MICROPROCESSOR REGISTER #5, BIT DESCRIPTION

REGISTER ADDRESS 00000101 00010101 00100101 00110101 01000101 01010101 01100101 01110101	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		RO	0
D6	DMO_n	**Driver Monitor Output:** This bit is set to a "1" to indicate transmit driver failure is detected. The value of this bit is based on the current status of DMO for the corresponding channel. If the DMOIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0
D5	FLS_n	**FIFO Limit Status:** This bit is set to a "1" to indicate that the jitter attenuator read/write FIFO pointers are within +/- 3 bits. If the FLSIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0
D4	LCV_n	**Line Code Violation:** This bit is set to a "1" to indicate that the receiver of channel n is currently detecting a Line Code Violation or an excessive number of zeros in the B8ZS or HDB3 modes. If the LCVIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0

TABLE 28: MICROPROCESSOR REGISTER #5, BIT DESCRIPTION

D3	NLCD_n	**Network Loop-Code Detection:** This bit operates differently in the Manual or the Automatic Network Loop-Code detection modes. **In the Manual Loop-Code detection mode**, (NLCDE1 = "0" and NLCDE0 = "1" or NLCDE1 = "1" and NLCDE0 = "0") this bit gets set to "1" as soon as the Loop-Up ("00001") or Loop-Down ("001") code is detected in the receive data for longer than 5 seconds. The NLCD bit stays in the "1" state for as long as the chip detects the presence of the Loop-code in the receive data and it is reset to "0" as soon as it stops receiving it. In this mode, if the NLCD interrupt is enabled, the chip will initiate an interrupt on every transition of the NLCD. **When the Automatic Loop-code detection mode,** (NLCDE1 = "1" and NLCDE0 ="1") is initiated, the state of the NLCD interface bit is reset to "0" and the chip is programmed to monitor the receive input data for the Loop-Up code. This bit is set to a "1" to indicate that the Network Loop Code is detected for more than 5 seconds. Simultaneously the Remote Loop-Back condition is automatically activated and the chip is programmed to monitor the receive data for the Network Loop Down code. The NLCD bit stays in the "1" state for as long as the Remote Loop-Back condition is in effect even if the chip stops receiving the Loop-Up code. Remote Loop-Back is removed if the chip detects the "001" pattern for longer than 5 seconds in the receive data.Detecting the "001" pattern also results in resetting the NLCD interface bit and initiating an interrupt provided the NLCD interrupt enable bit is active. **When programmed in Automatic detection mode,** the NLCD interface bit stays "High" for the entire time the Remote Loop-Back is active and initiate an interrupt anytime the status of the NLCD bit changes. In this mode, the **Host** can monitor the state of the NLCD bit to determine if the Remote Loop-Back is activated.	RO	0
D2	AISD_n	**Alarm Indication Signal Detect:** This bit is set to a "1" to indicate All Ones Signal is detected by the receiver. The value of this bit is based on the current status of Alarm Indication Signal detector of channel n. If the AISDIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0
D1	RLOS_n	**Receive Loss of Signal:** This bit is set to a "1" to indicate that the receive input signal is lost. The value of this bit is based on the current status of the receive input signal of channel n. If the RLOSIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0
D0	QRPD_n	**Quasi-random Pattern Detection:** This bit is set to a "1" to indicate the receiver is currently in synchronization with QRSS pattern. The value of this bit is based on the current status of Quasi-random pattern detector of channel n. If the QRPDIE bit is enabled, any transition on this bit will generate an Interrupt.	RO	0

TABLE 29: MICROPROCESSOR REGISTER #6, BIT DESCRIPTION

REGISTER ADDRESS 00000110 00010110 00100110 00110110 01000110 01010110 01100110 01110110	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		RO	0
D6	DMOIS_n	**Driver Monitor Output Interrupt Status:** This bit is set to a "1" every time the DMO status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D5	FLSIS_n	**FIFO Limit Interrupt Status:** This bit is set to a "1" every time when FIFO Limit (Read/Write pointer with +/- 3 bits apart) status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D4	LCVIS_n	**Line Code Violation Interrupt Status:** This bit is set to a "1" every time when LCV status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D3	NLCDIS_n	**Network Loop-Code Detection Interrupt Status:** This bit is set to a "1" every time when NLCD status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D2	AISDIS_n	**AIS Detection Interrupt Status:** This bit is set to a "1" every time when AISD status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D1	RLOSIS_n	**Receive Loss of Signal Interrupt Status:** This bit is set to a "1" every time RLOS status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0
D0	QRPDIS_n	**Quasi-Random Pattern Detection Interrupt Status:** This bit is set to a "1" every time when QRPD status has changed since last read. ***NOTE:*** *This bit is reset upon read.*	RUR	0

TABLE 30: MICROPROCESSOR REGISTER #7, BIT DESCRIPTION

REGISTER ADDRESS 00000111 00010111 00100111 00110111 01000111 01010111 01100111 01110111	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		RO	0
D6	Reserved		RO	0
D5	CLOS5_n	**Cable Loss bit 5:** CLOS[5:0]_n are the six bit receive selective equalizer setting which is also a binary word that represents the cable attenuation indication within ±1dB. CLOS5_n is the most significant bit (MSB) and CLOS0_n is the least significant bit (LSB).	RO	0
D4	CLOS4_n	**Cable Loss bit 4:** See description of D5 for function of this bit.	RO	0
D3	CLOS3_n	**Cable Loss bit 3:** See description of D5 for function of this bit.	RO	0
D2	CLOS2_n	**Cable Loss bit 2:** See description of D5 for function of this bit.	RO	0
D1	CLOS1_n	**Cable Loss bit 1:** See description of D5 for function of this bit.	RO	0
D0	CLOS0_n	**Cable Loss bit 0:** See description of D5 for function of this bit.	RO	0

TABLE 31: MICROPROCESSOR REGISTER #8, BIT DESCRIPTION

REGISTER ADDRESS	CHANNEL_n	FUNCTION	REGISTER TYPE	RESET VALUE
00001000	CHANNEL_0			
00011000	CHANNEL_1			
00101000	CHANNEL_2			
00111000	CHANNEL_3			
01001000	CHANNEL_4			
01011000	CHANNEL_5			
01101000	CHANNEL_6			
01111000	CHANNEL_7			
BIT #	**NAME**			
D7	Reserved		R/W	0
D6-D0	B6S1_n - B0S1_n	**Arbitrary Transmit Pulse Shape, Segment 1:**The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode in Table 5. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the first time segment. B6S1_n-B0S1_n is in signed magnitude format with B6S1_n as the sign bit and B0S1_n as the least significant bit (LSB).	R/W	0

TABLE 32: MICROPROCESSOR REGISTER #9, BIT DESCRIPTION

REGISTER ADDRESS	CHANNEL_n	FUNCTION	REGISTER TYPE	RESET VALUE
00001001	CHANNEL_0			
00011001	CHANNEL_1			
00101001	CHANNEL_2			
00111001	CHANNEL_3			
01001001	CHANNEL_4			
01011001	CHANNEL_5			
01101001	CHANNEL_6			
01111001	CHANNEL_7			
BIT #	**NAME**			
D7	Reserved		R/W	0
D6-D0	B6S2_n - B0S2_n	**Arbitrary Transmit Pulse Shape, Segment 2** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode in Table 5. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the second time segment. B6S2_n-B0S2_n is in signed magnitude format with B6S2_n as the sign bit and B0S2_n as the least significant bit (LSB).	R/W	0

TABLE 33: MICROPROCESSOR REGISTER #10, BIT DESCRIPTION

REGISTER ADDRESS 00001010 00011010 00101010 00111010 01001010 01011010 01101010 01111010	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		R/W	0
D6-D0	B6S3_n - B0S3_n	**Arbitrary Transmit Pulse Shape, Segment 3** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode in Table 5. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the third time segment. B6S3_n-B0S3_n is in signed magnitude format with B6S3_n as the sign bit and B0S3_n as the least significant bit (LSB).	R/W	0

TABLE 34: MICROPROCESSOR REGISTER #11, BIT DESCRIPTION

REGISTER ADDRESS 00001011 00011011 00101011 00111011 01001011 01011011 01101011 01111011	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		R/W	0
D6-D0	B6S4_n - B0S4_n	**Arbitrary Transmit Pulse Shape, Segment 4** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode in Table 5. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the fourth time segment. B6S4_n-B0S4_n is in signed magnitude format with B6S4_n as the sign bit and B0S4_n as the least significant bit (LSB).	R/W	0

TABLE 35: MICROPROCESSOR REGISTER #12, BIT DESCRIPTION

REGISTER ADDRESS 00001100 00011100 00101100 00111100 01001100 01011100 01101100 01111100	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		R/W	0
D6-D0	B6S5_n - B0S5_n	**Arbitrary Transmit Pulse Shape, Segment 5** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode in **Table 5**. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the fifth time segment. B6S5_n-B0S5_n is in signed magnitude format with B6S5_n as the sign bit and B0S5_n as the least significant bit (LSB).	R/W	0

TABLE 36: MICROPROCESSOR REGISTER #13, BIT DESCRIPTION

REGISTER ADDRESS 00001101 00011101 00101101 00111101 01001101 01011101 01101101 01111101	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		R/W	0
D6-D0	B6S6_n - B0S6_n	**Arbitrary Transmit Pulse Shape, Segment 6** The shape of each channel's transmitted pulse can be made independently user programmable by selecting "Arbitrary Pulse" mode in **Table 5**. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the sixth time segment. B6S6_n-B0S6_n is in signed magnitude format with B6S6_n as the sign bit and B0S6_n as the least significant bit (LSB).	R/W	0

TABLE 37: MICROPROCESSOR REGISTER #14, BIT DESCRIPTION

REGISTER ADDRESS 00001110 00011110 00101110 00111110 01001110 01011110 01101110 01111110	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		R/W	0
D6-D0	B6S7_n - B0S7_n	**Arbitrary Transmit Pulse Shape, Segment 7** The shape of each channel's transmitted pulse can be made independently user programmable by selecting “Arbitrary Pulse” mode in Table 5. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the seventh time segment. B6S7_n-B0S7_n is in signed magnitude format with B6S7_n as the sign bit and B0S7_n as the least significant bit (LSB).	R/W	0

TABLE 38: MICROPROCESSOR REGISTER #15, BIT DESCRIPTION

REGISTER ADDRESS 00001111 00011111 00101111 00111111 01001111 01011111 01101111 01111111	CHANNEL_n CHANNEL_0 CHANNEL_1 CHANNEL_2 CHANNEL_3 CHANNEL_4 CHANNEL_5 CHANNEL_6 CHANNEL_7	FUNCTION	REGISTER TYPE	RESET VALUE
BIT #	NAME			
D7	Reserved		R/W	0
D6-D0	B6S8_n - B0S8_n	**Arbitrary Transmit Pulse Shape, Segment 8** The shape of each channel's transmitted pulse can be made independently user programmable by selecting “Arbitrary Pulse” mode in Table 5. The arbitrary pulse is divided into eight time segments whose combined duration is equal to one period of MCLK. This 7 bit number represents the amplitude of the nth channel's arbitrary pulse during the eighth time segment. B6S8_n-B0S8_n is in signed magnitude format with B6S8_n as the sign bit and B0S8_n as the least significant bit (LSB).	R/W	0

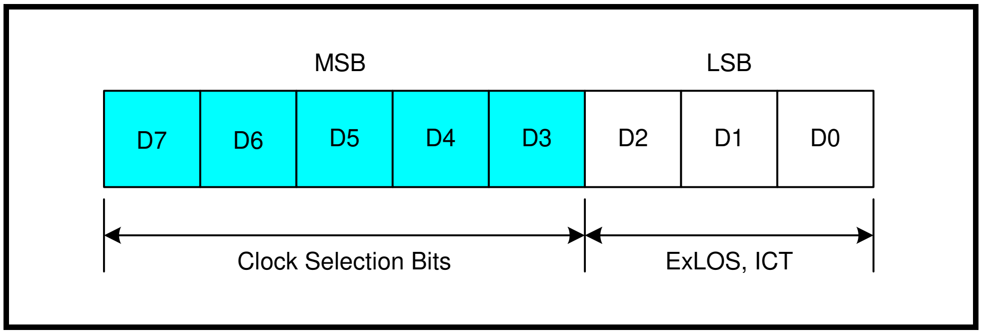
TABLE 39: MICROPROCESSOR REGISTER #128, BIT DESCRIPTION

REGISTER ADDRESS 10000000 / BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7	SR/$\overline{DR}$	**Single-rail/Dual-rail Select:** Writing a “1” to this bit configures all 8 channels in the XRT83VL38 to operate in the Single-rail mode. Writing a “0” configures the XRT83VL38 to operate in Dual-rail mode.	R/W	0
D6	ATAOS	**Automatic Transmit All Ones Upon RLOS:** Writing a “1” to this bit enables the automatic transmission of All "Ones" data to the line for the channel that detects an RLOS condition. Writing a “0” disables this feature.	R/W	0
D5	RCLKE	**Receive Clock Edge:** Writing a “1” to this bit selects receive output data of all channels to be updated on the negative edge of RCLK. Wring a “0” selects data to be updated on the positive edge of RCLK.	R/W	0
D4	TCLKE	**Transmit Clock Edge:** Writing a “0” to this bit selects transmit data at TPOS_n/TDATA_n and TNEG_n/CODES_n of all channels to be sampled on the falling edge of TCLK_n. Writing a “1” selects the rising edge of the TCLK_n for sampling.	R/W	0
D3	DATAP	**DATA Polarity:** Writing a “0” to this bit selects transmit input and receive output data of all channels to be active “High”. Writing a “1” selects an active “Low” state.	R/W	0
D2	Reserved			0
D1	GIE	**Global Interrupt Enable:** Writing a “1” to this bit globally enables interrupt generation for all channels. Writing a “0” disables interrupt generation.	R/W	0
D0	SRESET	**Software Reset µP Registers:** Writing a “1” to this bit longer than 10µs initiates a device reset through the microprocessor interface. All internal circuits are placed in the reset state with this bit set to a “1” except the microprocessor register bits.	R/W	0

CLOCK SELECT REGISTER

The input clock source is used to generate all the necessary clock references internally to the LIU. The microprocessor timing is derived from a PLL output which is chosen by programming the Clock Select Bits and the Master Clock Rate in register 0x81h. Therefore, if the clock selection bits or the MCLRATE bit are being programmed, the frequency of the PLL output will be adjusted accordingly. During this adjustment, it is important to "Not" write to any other bit location within the same register while selecting the input/output clock frequency. For best results, register 0x81h can be broken down into two sub-registers with the MSB being bits D[7:3] and the LSB being bits D[2:0] as shown in **Figure 31**. Note: Bit D[7] is a reserved bit.

FIGURE 31. REGISTER 0X81H SUB REGISTERS



Programming Examples:

Example 1: Changing bits D[7:3]

If bits D[7:3] are the only values within the register that will change in a WRITE process, the microprocessor only needs to initiate ONE write operation.

Example 2: Changing bits D[2:0]

If bits D[2:0] are the only values within the register that will change in a WRITE process, the microprocessor only needs to initiate ONE write operation.

Example 3: Changing bits within the MSB and LSB

In this scenario, one must initiate TWO write operations such that the MSB and LSB do not change within ONE write cycle. It is recommended that the MSB and LSB be treated as two independent sub-registers. One can either change the clock selection (MSB) and then change bits D[2:0] (LSB) on the SECOND write, or vice-versa. No order or sequence is necessary.

TABLE 40: MICROPROCESSOR REGISTER #129, BIT DESCRIPTION

REGISTER ADDRESS 10000001 / BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D7	Reserved		R/W	0

TABLE 40: MICROPROCESSOR REGISTER #129, BIT DESCRIPTION

<table>
<tr><td>D6</td><td>CLKSEL2</td><td>Clock Select Inputs for Master Clock Synthesizer bit 2:
In Host mode, CLKSEL[2:0] are input signals to a programmable frequency synthesizer that can be used to generate a master clock from an external accurate clock source according to the following table;
<table>
<tr><th>MCLKE1 kHz</th><th>MCLKT1 kHz</th><th>CLKSEL 2</th><th>CLKSEL1</th><th>CLKSEL0</th><th>MCLKRATE</th><th>CLKOUT kHz</th></tr>
<tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr>
<tr><td>2048</td><td>2048</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1544</td></tr>
<tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2048</td></tr>
<tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr>
<tr><td>1544</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2048</td></tr>
<tr><td>2048</td><td>1544</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1544</td></tr>
</table>
In Hardware mode, the state of these signals are ignored and the master frequency PLL is controlled by the corresponding Hardware pins.</td><td>R/W</td><td>0</td></tr>
<tr><td>D5</td><td>CLKSEL1</td><td>Clock Select inputs for Master Clock Synthesizer bit 1:
See description of bit D6 for function of this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>D4</td><td>CLKSEL0</td><td>Clock Select inputs for Master Clock Synthesizer bit 0:
See description of bit D6 for function of this bit.</td><td>R/W</td><td>0</td></tr>
<tr><td>D3</td><td>MCLKRATE</td><td>Master clock Rate Select: The state of this bit programs the Master Clock Synthesizer to generate the T1/J1 or E1 clock. The Master Clock Synthesizer will generate the E1 clock when MCLKRATE = “0”, and the T1/J1 clock when MCLKRATE = “1”.</td><td>R/W</td><td>0</td></tr>
<tr><td>D2</td><td>RXMUTE</td><td>Receive Output Mute: Writing a “1” to this bit, mutes receive outputs at RPOS/RDATA and RNEG/LCV pins to a “0” state for any channel that detects an RLOS condition.
NOTE: RCLK is not muted.</td><td>R/W</td><td>0</td></tr>
<tr><td>D1</td><td>EXLOS</td><td>Extended LOS: Writing a “1” to this bit extends the number of zeros at the receive input of each channel before RLOS is declared to 4096 bits. Writing a “0” reverts to the normal mode (175+75 bits for T1 and 32 bits for E1).</td><td>R/W</td><td>0</td></tr>
<tr><td>D0</td><td>ICT</td><td>In-Circuit-Testing: Writing a “1” to this bit configures all the output pins of the chip in high impedance mode for In-Circuit-Testing. Setting the ICT bit to “1” is equivalent to connecting the Hardware $\overline{\text{ICT}}$ pin 88 to ground.</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 41: MICROPROCESSOR REGISTER #130, BIT DESCRIPTION

<table>
<tr><th>REGISTER ADDRESS
10000010
BIT #</th><th>NAME</th><th>FUNCTION</th><th>REGISTER TYPE</th><th>RESET VALUE</th></tr>
<tr><td>D7</td><td>TXONCNTL</td><td>Transmit On Control:
In Host mode, setting this bit to “1” transfers the control of the Transmit On/Off function to the TXON_n Hardware control pins.
NOTE: This provides a faster On/Off capability for redundancy application.</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 41: MICROPROCESSOR REGISTER #130, BIT DESCRIPTION

D6	TERCNTL	**Termination Control.** In **Host** mode, setting this bit to “1” transfers the control of the RXTSEL to the RXTSEL **Hardware** control pin. ***NOTE:*** *This provides a faster On/Off capability for redundancy application.*	R/W	0
D5-D0	Reserved			

TABLE 42: MICROPROCESSOR REGISTER #131, BIT DESCRIPTION

REGISTER ADDRESS 10000011 **BIT #**	**NAME**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
D7	GAUGE1	**Wire Gauge Selector Bit 1:** This bit together with bit D6 are used to select wire gauge size as shown in the table below.	R/W	0
D6	GAUGE0	**Wire Gauge Selector Bit 0:** See bit D7.	R/W	0
D5	TxSYNC(Sect 13)	**G.703 Section 13 Transmit Pulse** When this bit is set to ’1’, the LIU transmitter will send the E1 synchrnonous waveform as described in Section 13 of ITU-T G.703. This register bit takes priority over every other LIU setting on the transmit path. 0 = Normal E1 pulse 1 = Section 13 Synchronous Pulse	R/W	0
D4	RxSYNC(Sect 13)	**G.703 Section 13 Receiver** When this bit is set to ’1’, the CDR block of the receiver is configured to accept a waveform as described in Section 13 of ITU-T G.703. 0 = Normal E1 (Equalizer Bit Settings - EQC[4:0]) 1 = Section 13 Synchronous Pulse	R/W	0

GAUGE1	**GAUGE0**	**Wire Size**
0	0	22 and 24 Gauge
0	1	22 Gauge
1	0	24 Gauge
1	1	26 Gauge

TABLE 42: MICROPROCESSOR REGISTER #131, BIT DESCRIPTION

<table>
<tr><td>D3</td><td>SL_1</td><td>Slicer Level Control bit 1: This bit and bit D2 control the slicing level for the slicer per the following table.
<table>
<tr><th>SL_1</th><th>SL_0</th><th>Slicer Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal</td></tr>
<tr><td>0</td><td>1</td><td>Decrease by 5% from Normal</td></tr>
<tr><td>1</td><td>0</td><td>Increase by 5% from Normal</td></tr>
<tr><td>1</td><td>1</td><td>Normal</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
<tr><td>D2</td><td>SL_0</td><td>Slicer Level Control bit 0: See description bit D3.</td><td>R/W</td><td>0</td></tr>
<tr><td>D1</td><td>EQG_1</td><td>Equalizer Gain Control bit 1: This bit together with bit D0 control the gain of the equalizer as shown in the table below.
<table>
<tr><th>EQG_1</th><th>EQG_0</th><th>Equalizer Gain</th></tr>
<tr><td>0</td><td>0</td><td>Normal</td></tr>
<tr><td>0</td><td>1</td><td>Reduce Gain by 1 dB</td></tr>
<tr><td>1</td><td>0</td><td>Reduce Gain by 3 dB</td></tr>
<tr><td>1</td><td>1</td><td>Normal</td></tr>
</table></td><td>R/W</td><td>0</td></tr>
<tr><td>D0</td><td>EQG_0</td><td>Equalizer Gain Control bit 0: See description of bit D1</td><td>R/W</td><td>0</td></tr>
</table>

TABLE 43: MICROPROCESSOR REGISTER #192, BIT DESCRIPTION

REGISTER ADDRESS 11000000 BIT #	NAME	FUNCTION	REGISTER TYPE	RESET VALUE
D[7:1]	Reserved	These register bits are not used.	R/W	0
D0	E1Arben	**E1 Arbitrary Pulse Enable** This bit is used to enable the Arbitrary Pulse Generators for shaping the transmit pulse shape when E1 mode is selected. If this bit is set to "1", all 8 channels will be configured for the Arbitrary Mode. However, each channel is individually controlled by programming the channel registers 0xn8 through 0xnF, where n is the number of the channel. "0" = Disabled (Normal E1 Pulse Shape ITU G.703) "1" = Arbitrary Pulse Enabled	R/W	0

ELECTRICAL CHARACTERISTICS

TABLE 44: ABSOLUTE MAXIMUM RATINGS

Storage Temperature...................-65°C to + 150°C
Operating Temperature.............-40°C to + 85°C
Supply Voltage..........................-0.5V to + 3.8V
V_{In}...-0.5V to + 5.5V
Maximum Junction Temperature.................................125ºC
Theta JA..24ºC/W
Theta JC..10ºC/W

TABLE 45: DC DIGITAL INPUT AND OUTPUT ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS
Power Supply Voltage	VDD	3.13	3.3	3.46	V
Power Supply Current	IDD	325	400	475	mA
Input High Voltage	V_{IH}	2.0	-	5.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Output High Voltage @ IOH = 2.0mA	V_{OH}	2.4	-	-	V
Output Low Voltage @IOL = 2mA.	V_{OL}	-	-	0.4	V
Input Leakage Current (except Input pins with Pull-up or Pull- down resistor).	I_L	-	-	±10	μA
Input Capacitance	C_I	-	5.0	-	pF
Output Load Capacitance	C_L	-	-	25	pF

TABLE 46: XRT83VL38 POWER CONSUMPTION

VDD=3.3V±5%, T_A=25°C, UNLESS OTHERWISE SPECIFIED

MODE	SUPPLY VOLTAGE	IMPEDANCE	TERMINATION RESISTOR	TRANSFORMER RATIO		TYP.	MAX.	UNIT	TEST CONDITIONS
				RECEIVER	TRANSMITTER				
E1	3.3V	75Ω	Internal	1:1	1:2	1.96	2.16	W	100% “1’s”
E1	3.3V	120Ω	Internal	1:1	1:2	1.85	2.04	W	100% “1’s”
T1	3.3V	100Ω	Internal	1:1	1:2	1.95	2.15	W	100% “1’s”
---	3.3V	---	External	---	---	429	472	mW	All transmitters off

TABLE 47: E1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A= -40° TO 85°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal:					Cable attenuation @1024kHz
Number of consecutive zeros before RLOS is set	10	175	255		
Input signal level at RLOS	15	20		dB	ITU-G.775, ETSI 300 233
RLOS De-asserted	12.5			dB	
Receiver Sensitivity (Short Haul with cable loss)	11			dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application. With -18dB interference signal added.
Receiver Sensitivity (Long Haul with cable loss)					With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application. With -18dB interference signal added.
Nominal	0		36	dB	
Extended	0		43	dB	
Input Impedance		13		kΩ	
Input Jitter Tolerance:					
1 Hz	37			UIpp	ITU G.823
10kHz-100kHz	0.2			UIpp	
Recovered Clock Jitter					
Transfer Corner Frequency	-	36		kHz	ITU G.736
Peaking Amplitude			-0.5	dB	
Jitter Attenuator Corner Frequency (-3dB curve) (JABW=0)	-	10	-	Hz	ITU G.736
(JABW=1)		1.5		Hz	
Return Loss:					
51kHz - 102kHz	14	-	-	dB	ITU-G.703
102kHz - 2048kHz	20			dB	
2048kHz - 3072kHz	16			dB	

TABLE 48: T1 RECEIVER ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A=-40° TO 85°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
Receiver loss of signal: Number of consecutive zeros before RLOS is set Input signal level at RLOS RLOS Clear	 100 15 12.5	 175 20 -	 250 - -	 dB % ones	 Cable attenuation @772kHz ITU-G.775, ETSI 300 233
Receiver Sensitivity (Short Haul with cable loss)	12	-		dB	With nominal pulse amplitude of 3.0V for 100Ω termination
Receiver Sensitivity (Long Haul with cable loss)	 0	-	 36	 dB	 With nominal pulse amplitude of 3.0V for 100Ω termination
Input Impedance		13	-	kΩ	
Jitter Tolerance: 1Hz 10kHz - 100kHz	 138 0.4	 - -	 - -	 UIpp	 AT&T Pub 62411
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	 - -	 9.8	 - 0.1	 KHz dB	 TR-TSY-000499
Jitter Attenuator Corner Frequency (-3dB curve)	-	6		-Hz	AT&T Pub 62411
Return Loss: 51kHz - 102kHz 102kHz - 2048kHz 2048kHz - 3072kHz	 - - -	 20 25 25	 - - -	 dB dB dB	

TABLE 49: E1 TRANSMIT RETURN LOSS REQUIREMENT

FREQUENCY	RETURN LOSS	
	G.703/CH-PTT	**ETS 300166**
51-102kHz	8dB	6dB
102-2048kHz	14dB	8dB
2048-3072kHz	10dB	8dB

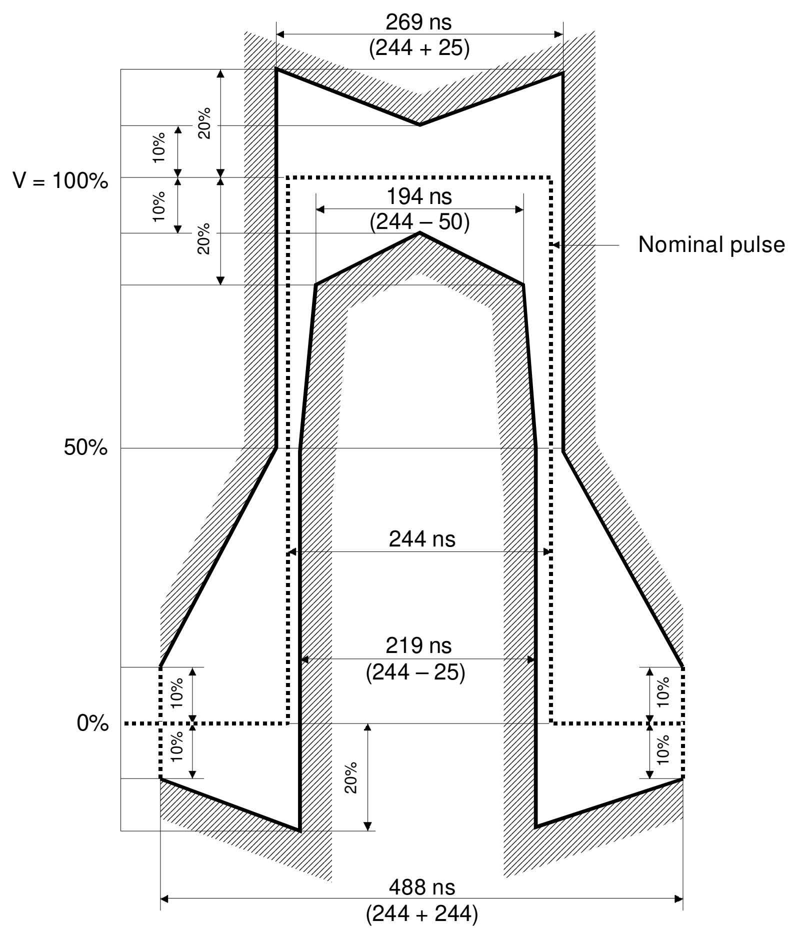
TABLE 50: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A=-40° TO 85°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude: 75Ω Application 120Ω Application	 2.185 2.76	 2.37 3.00	 2.555 3.24	 V V	Transformer with 1:2 ratio and internal termination.
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05	-	ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05	-	ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 8 14 10	 - - -	 - - -	 dB dB dB	 ETSI 300 166, CHPTT

TABLE 51: T1 TRANSMITTER ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, T_A=-40° TO 85°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**MIN.**	**TYP.**	**MAX.**	**UNIT**	**TEST CONDITIONS**
AMI Output Pulse Amplitude:	2.5	3.0	3.50	V	Transformer with 1:2 ratio and and Internal Termination.
Output Pulse Width	338	350	362	ns	ANSI T1.102
Output Pulse Width Imbalance	-	-	20	-	ANSI T1.102
Output Pulse Amplitude Imbalance	-	-	±200	mV	ANSI T1.102
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TCLK applied to the input.
Output Return Loss: 51kHz -102kHz 102kHz-2048kHz 2048kHz-3072kHz	 - - -	 15 15 15	 - - -	 dB dB dB	

FIGURE 32. ITU G.703 PULSE TEMPLATE



Note – V corresponds to the nominal peak value.

TABLE 52: TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Nominal Peak Voltage of a Mark	2.37V	3.0V
Peak voltage of a Space (no Mark)	0 ± 0.237V	0 ± 0.3V
Nominal Pulse width	244ns	244ns
Ratio of Positive and Negative Pulses Imbalance	0.95 to 1.05	0.95 to 1.05

FIGURE 33. ITU G.703 SECTION 13 SYNCHRONOUS INTERFACE PULSE TEMPLATE

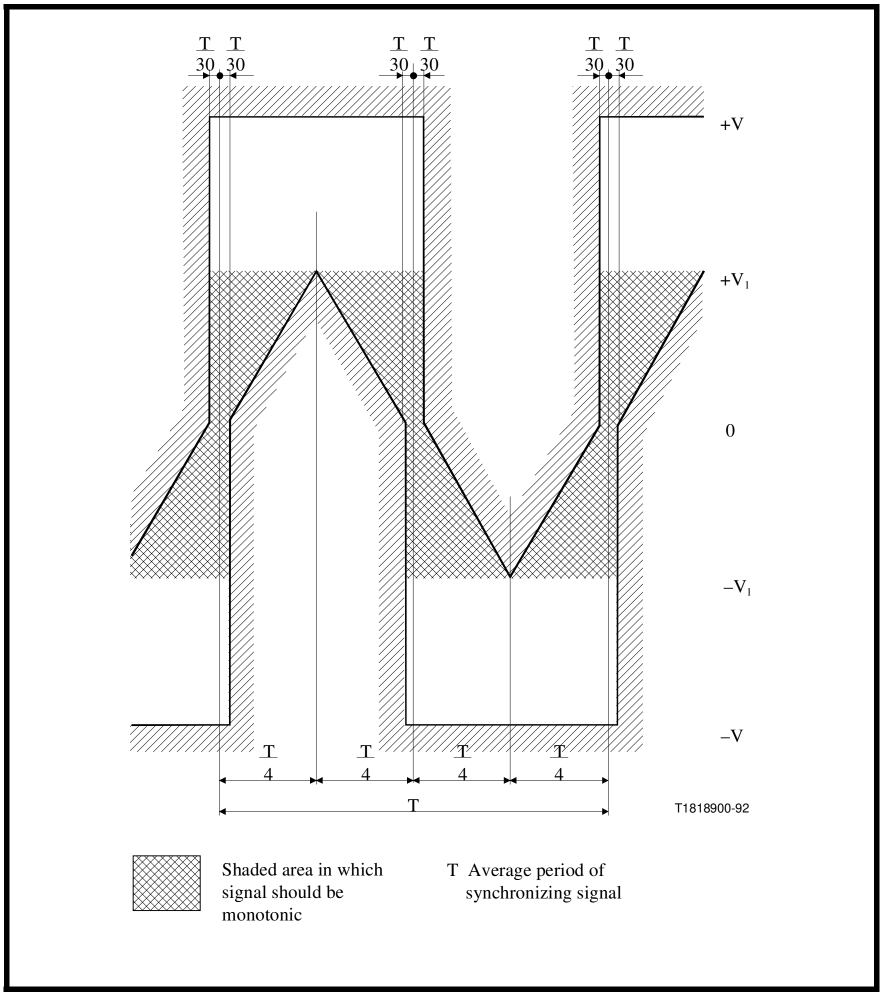


TABLE 53: E1 SYNCHRONOUS INTERFACE TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75Ω Resistive (Coax)	120Ω Resistive (twisted Pair)
Maximum Peak Voltage of a Mark	1.5V	1.9V
Minimum Peak Voltage of a Mark	0.75V	1.0V
Nominal Pulse width	244ns	244ns

FIGURE 34. DSX-1 PULSE TEMPLATE (NORMALIZED AMPLITUDE)

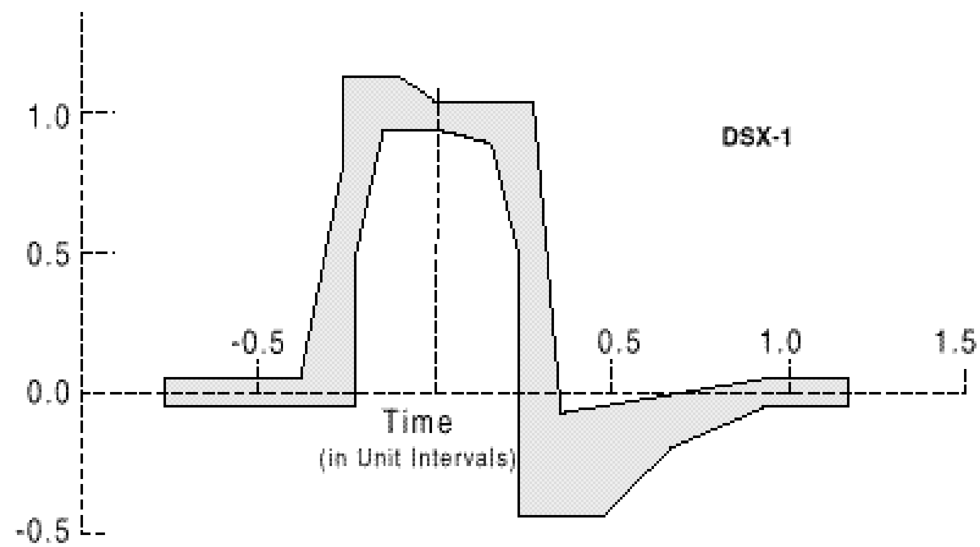


TABLE 54: DSX1 INTERFACE ISOLATED PULSE MASK AND CORNER POINTS

MINIMUM CURVE		MAXIMUM CURVE	
TIME (UI)	NORMALIZED AMPLITUDE	TIME (UI)	NORMALIZED AMPLITUDE
-0.77	-.05V	-0.77	.05V
-0.23	-.05V	-0.39	.05V
-0.23	0.5V	-0.27	.8V
-0.15	0.95V	-0.27	1.15V
0.0	0.95V	-0.12	1.15V
0.15	0.9V	0.0	1.05V
0.23	0.5V	0.27	1.05V
0.23	-0.45V	0.35	-0.07V
0.46	-0.45V	0.93	0.05V
0.66	-0.2V	1.16	0.05V
0.93	-0.05V		
1.16	-0.05V		

TABLE 55: AC ELECTRICAL CHARACTERISTICS

VDD=3.3V±5%, TA=25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
E1 MCLK Clock Frequency		-	2.048		MHz
T1 MCLK Clock Frequency		-	1.544		MHz
MCLK Clock Duty Cycle		40	-	60	%
MCLK Clock Tolerance		-	±50	-	ppm
TCLK Duty Cycle	T_{CDU}	30	50	70	%
Transmit Data Setup Time	T_{SU}	50	-	-	ns
Transmit Data Hold Time	T_{HO}	30	-	-	ns
TCLK Rise Time(10%/90%)	$TCLK_R$	-	-	40	ns
TCLK Fall Time(90%/10%)	$TCLK_F$	-	-	40	ns
RCLK Duty Cycle	R_{CDU}	45	50	55	%
Receive Data Setup Time	R_{SU}	150	-	-	ns
Receive Data Hold Time	R_{HO}	150	-	-	ns
RCLK to Data Delay	$\overline{RDY}$	-	-	40	ns
RCLK Rise Time(10% to 90%) with 25pF Loading.	$RCLK_R$	-	-	40	ns
RCLK Fall Time(90% to 10%) with 25pF Loading.	$RCLK_F$			40	ns

FIGURE 35. TRANSMIT CLOCK AND INPUT DATA TIMING

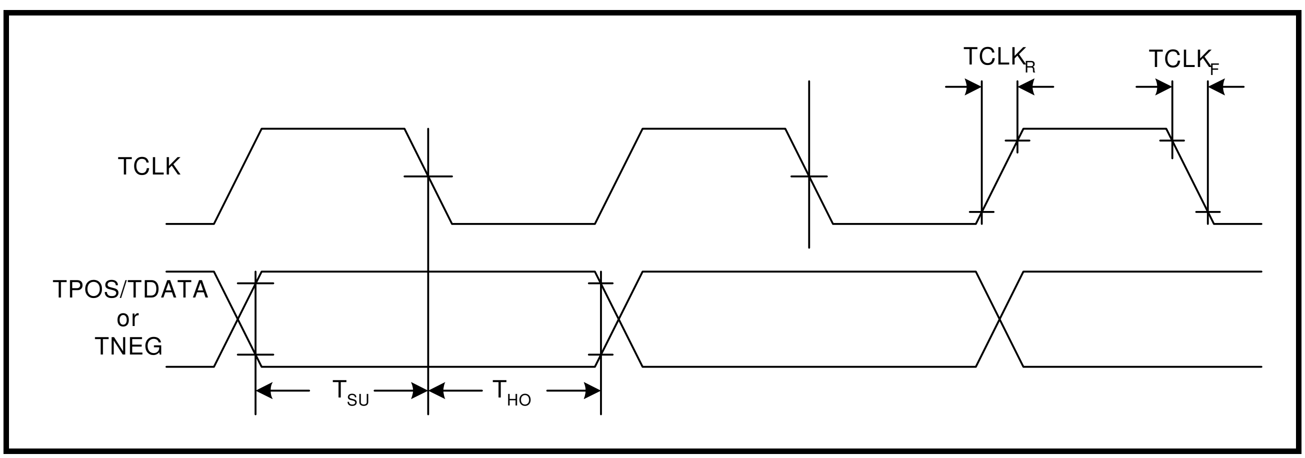
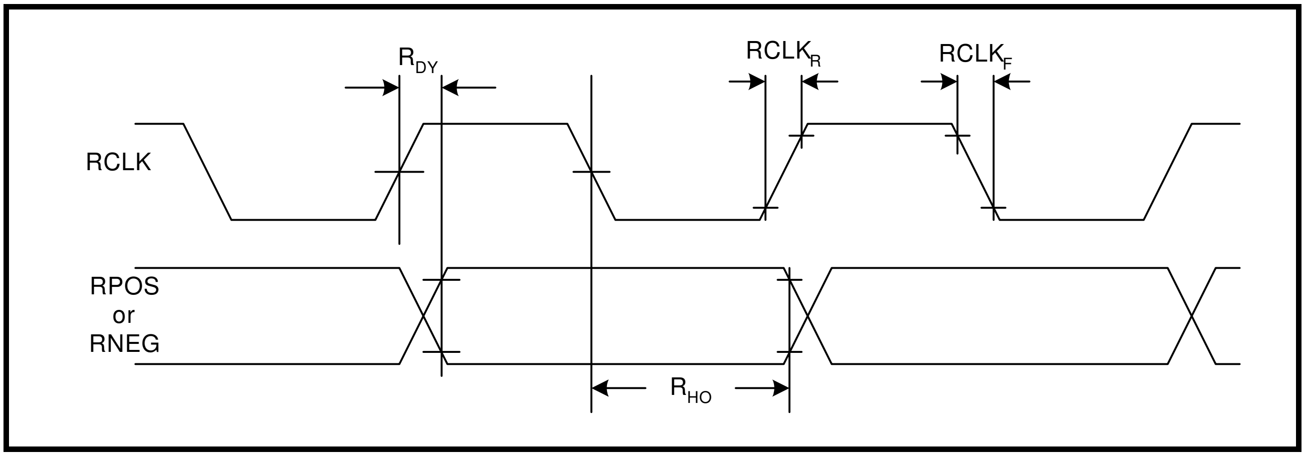


FIGURE 36. RECEIVE CLOCK AND OUTPUT DATA TIMING



MICROPROCESSOR INTERFACE I/O TIMING

INTEL INTERFACE TIMING - ASYNCHRONOUS

The signals used for the Intel microprocessor interface are: Address Latch Enable (ALE), Read Enable ($\overline{RD}$), Write Enable ($\overline{WR}$), Chip Select ($\overline{CS}$), Address and Data bits. The microprocessor interface uses minimum external glue logic and is compatible with the timings of the 8051 or 80C188 with an 8-16 MHz clock frequency, and with the timings of x86 or i960 family or microprocessors. The interface timing shown in **Figure 37** and **Figure 39** is described in **Table 56**.

FIGURE 37. INTEL ASYNCHRONOUS PROGRAMMED I/O INTERFACE TIMING

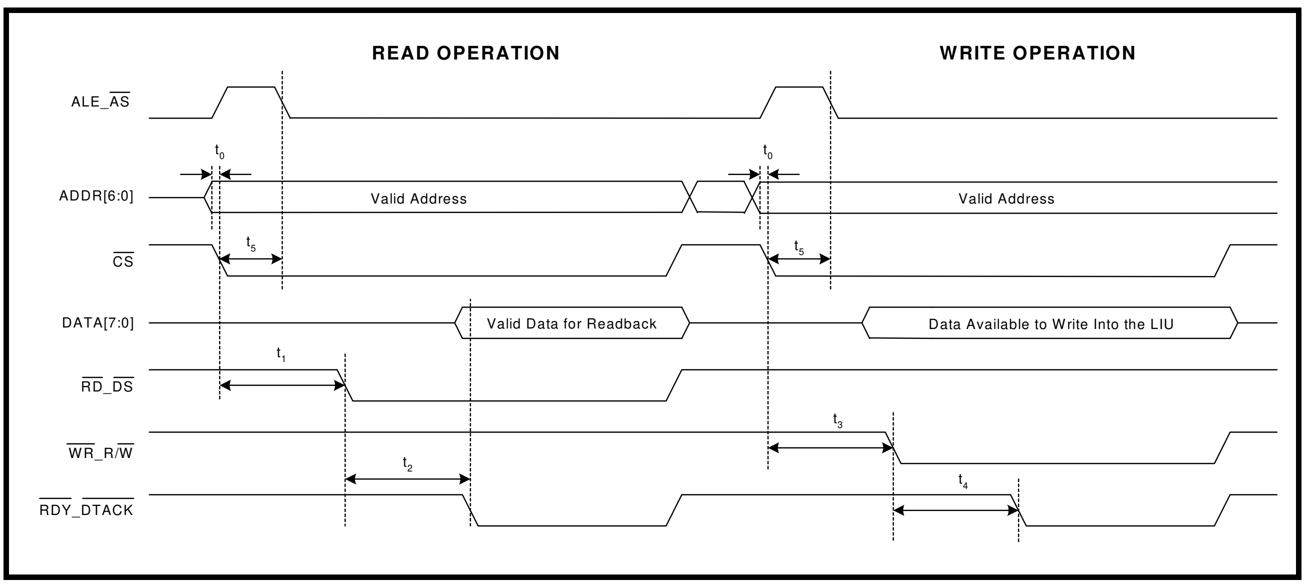


TABLE 56: ASYNCHRONOUS MODE 1 - INTEL 8051 AND 80188 INTERFACE TIMING

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to $\overline{CS}$ Falling Edge	0	-	ns
t_1	$\overline{CS}$ Falling Edge to $\overline{RD}$ Assert	20	-	ns
t_2	$\overline{RD}$ Assert to $\overline{RDY}$ Assert	-	135	ns
NA	$\overline{RD}$ Pulse Width (t2)	135	-	ns
t_3	$\overline{CS}$ Falling Edge to $\overline{WR}$ Assert	20	-	ns
t_4	$\overline{WR}$ Assert to RDY Assert	-	135	ns
NA	$\overline{WR}$ Pulse Width (t2)	135	-	ns
t_5	$\overline{CS}$ Falling Edge to AS Falling Edge	0	-	ns
Reset pulse width - both Motorola and Intel Operations (see Figure 39)				
t_9	$\overline{Reset}$ pulse width	10		µs

MOTOROLA ASYCHRONOUS INTERFACE TIMING

The signals used in the Motorola microprocessor interface mode are: Address Strobe (AS), Data Strobe (DS), Read/Write Enable (R/W), Chip Select (CS), Address and Data bits. The interface is compatible with the timing of a Motorola 68000 microprocessor family with up to 16.67 MHz clock frequency. The interface timing is shown in **Figure 38** and **Figure 39**. The I/O specifications are shown in **Table 57**.

FIGURE 38. MOTOROLA 68K ASYNCHRONOUS PROGRAMMED I/O INTERFACE TIMING

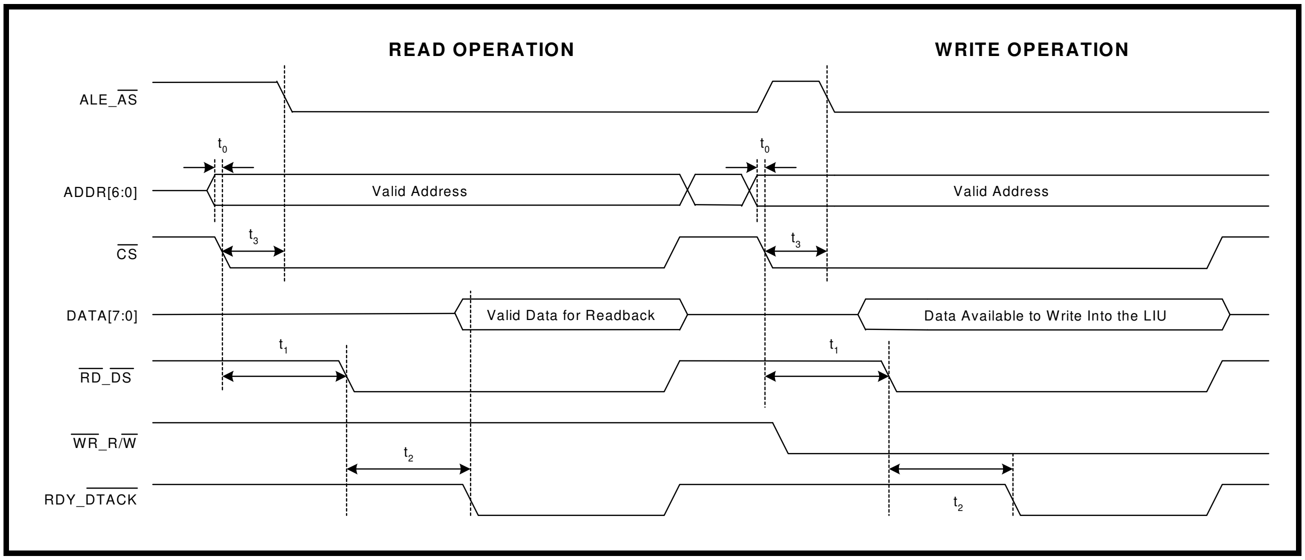
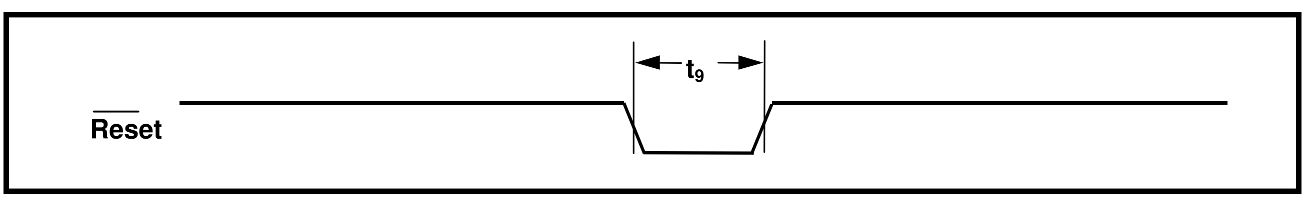


TABLE 57: ASYNCHRONOUS - MOTOROLA 68K - INTERFACE TIMING SPECIFICATION

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_0	Valid Address to CS Falling Edge	0	-	ns
t_1	CS Falling Edge to DS Assert	20	-	ns
t_2	DS Assert to DTACK Assert	-	135	ns
NA	DS Pulse Width (t2)	135	-	ns
t_3	CS Falling Edge to AS Falling Edge	0	-	ns
Reset pulse width - both Motorola and Intel Operations (see Figure 39)				
t_9	Reset pulse width	10		µs

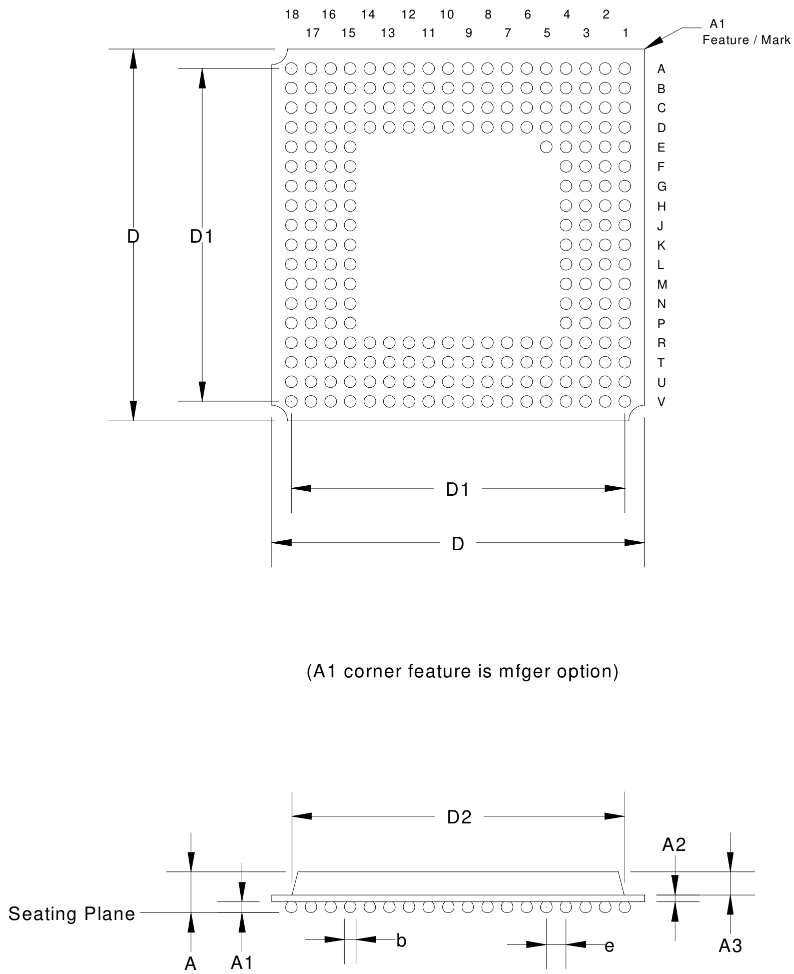
FIGURE 39. MICROPROCESSOR INTERFACE TIMING - RESET PULSE WIDTH



PACKAGE DIMENSIONS

225 BALL PLASTIC BALL GRID ARRAY (BOTTOM VIEW)

(19.0 X 19.0 X 1.0mm)



Note: The control dimension is in millimeter.

	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.049	0.096	1.24	2.45
A1	0.016	0.024	0.40	0.60
A2	0.013	0.024	0.32	0.60
A3	0.020	0.048	0.52	1.22
D	0.740	0.756	18.80	19.20
D1	0.669 BSC		17.00 BSC	
D2	0.665	0.669	16.90	17.00
b	0.020	0.028	0.50	0.70
e	0.039 BSC		1.00 BSC	

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT83VL38IB	225 Ball BGA	-40°C to +85°C

REVISIONS

REVISION #	DATE	DESCRIPTION
1.0.0	6/15/09	First Release of the Released Datasheet
1.0.1	8/27/10	Added missing pin definitions to the pin description table and updated micro-p documentation in functional desription section.