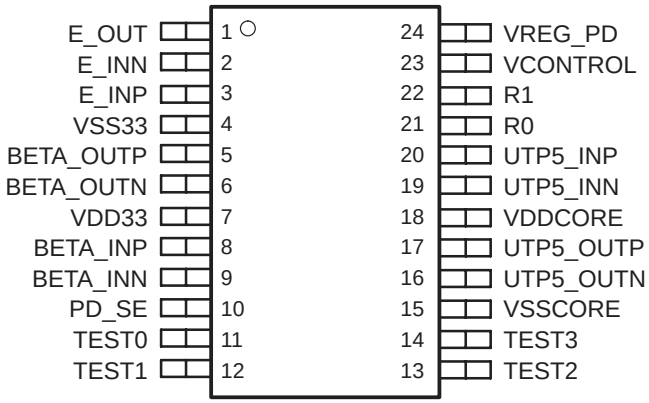
- **Fully Supports Provisions of IEEE Std 1394b-2002 at S100B Signaling Rates**
- **Provides One Transceiver to Drive IEEE Std 1394b Signaling Across Unshielded Twisted Pair Category 5 (UTP5 or CAT5) Cable or Better at 100 Megabits per Second (Mbits/s)**
- **Power-Down Features to Conserve Energy in Battery Powered Applications**
- **Single 3.3-V Supply Operation or Optional Dual 3.3-V/1.8-V Supply Operation**
- **Low-Cost High-Performance 24-Terminal TSSOP Package**
- **Low-Power Modes to Put Device Into Low Power States When Data Is Not Being Driven**

description

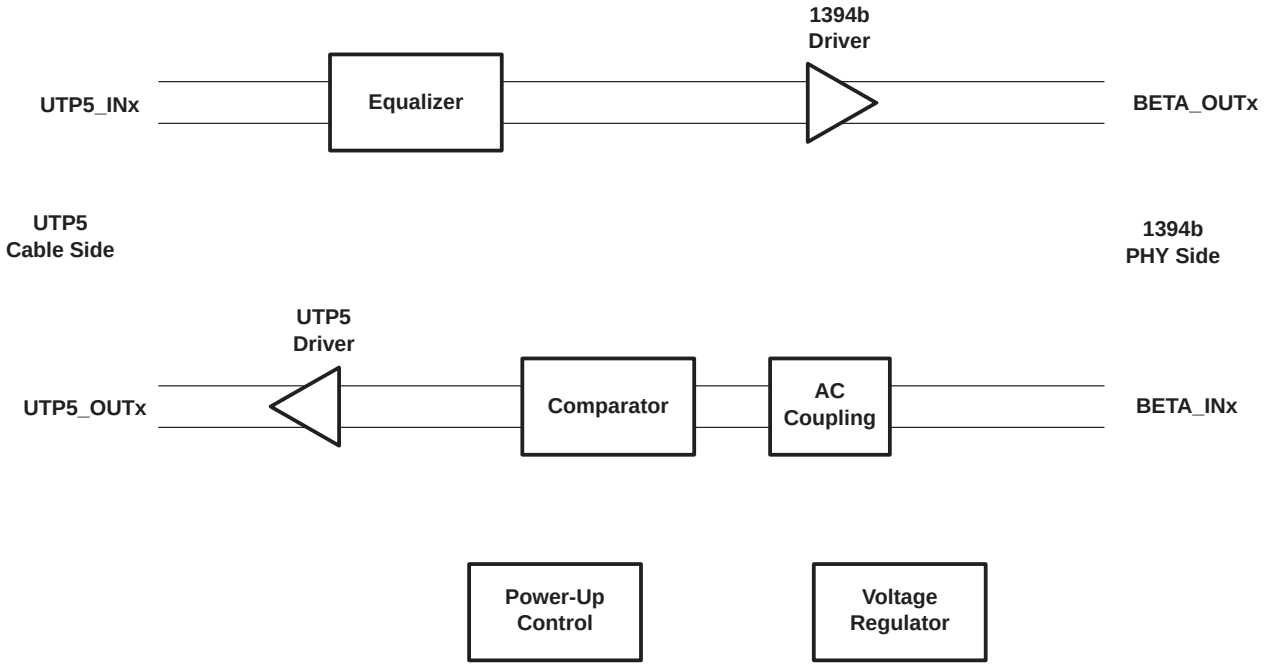
The TSB17BA1 is a single-port 100-Mbps transceiver used in transporting IEEE Std 1394b (1394b) or other coded data across CAT5 or better cabling. It is attached to a 1394b-capable port on a 1394b physical layer (PHY) to enable 1394b 100-Mbps signals to be transmitted and received across up to 100 meters of unshielded twisted-pair category 5 (UTP5) cable. Equalization is applied to the signal received from the UTP5 cable to boost signal-to-noise ratio (SNR) to allow sensing of the data. A 1394b PHY device capable of transmitting at only 100 Mbits/s in 1394b-only mode is required for correct functionality. This PHY must be connected to the TSB17BA1 at one of the twisted-pair (TP) ports, with the 110-Ω 1394b transmission line properly terminated. The TSB17BA1 must then be connected to a 100-Ω transmission line properly terminated and connected to an isolating transformer. This transformer is then connected to an RJ45 connector. All of the parameters on the UTP5 side of the TSB17BA1 are set the same as 100baseT Ethernet. This allows the mechanical and magnetic infrastructure, which is used to design a 100baseT connection, to be used when designing a 100-Mbits/s UTP5 1394b connection. This device does not implement the autocrossover functionality described in chapter 12 of IEEE Std 1394b-2002. This means the required crossover of TPA to TPB and TPB to TPA must be done in the cable or connector or PWB; in other words, a mechanical crossover must be implemented (see the Application Information section).

terminal assignments

PW PACKAGE
(TOP VIEW)



functional block diagram



equalizer

The equalizer applies equalization to the signal received from the UTP5 cable to boost SNR to allow sensing of the data.

1394b driver

This block drives the signal detected and enhanced by the equalizer from the UTP cable to a 1394b PHY port.

ac coupling

This block blocks direct current signals to the comparator. Only ac signals are propagated through this block.

comparator

This block converts 1394b signals from the 1394b PHY into levels capable of driving the UTP5 driver.

UTP5 driver

This block drives signals onto the UTP5 cable.

power-up control

This block provides a signal for the control of the device relative to the state of the supply voltage.

voltage regulator

This block regulates an externally provided 3−3.6 V down to an internally used 1.8 V.

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	TYPE	NO.		
Test Terminals				
E_INN	Test	2	I	Input reserved for future enhancement. Must be grounded for normal operation.
E_INP	Test	3	I	Input reserved for future enhancement. Must be grounded for normal operation.
E_OUT	Test	1	O	Output reserved for future enhancement. May be left unconnected for normal operation.
TEST0 TEST1 TEST2 TEST3	CMOS	11 12 13 14	I	Test control. These inputs are used in the manufacturing test of the TSB17BA1. For normal use, these terminals must be pulled low to GND.
IEEE Std 1394b PHY Terminals				
BETA_INP BETA_INN	Input from 1394b PHY	8 9	I	Input of ac-coupling block. These twisted-pair differential-signal terminals connect the TSB17BA1 BETA_INP to the 1394b PHY TPB+ and BETA_INN to the 1394b PHY TPB− terminals of the port on the 1394b PHY. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the 1394b PHY. The transmission lines between the 1394b PHY and TSB17BA1 must be terminated properly.
BETA_OUTP BETA_OUTN	Output to 1394b PHY	5 6	O	Output of 1394b driver block. These twisted-pair differential-signal terminals, connect the TSB17BA1 BETA_OUTP to the 1394b PHY TPA+ and BETA_OUTN to the 1394b PHY TPA− terminals of the port on the 1394b PHY. Board traces from each pair of positive and negative differential signal terminals must be kept matched and as short as possible to the external load resistors and to the 1394b PHY. The transmission lines between the 1394b PHY and TSB17BA1 must be terminated properly.
RJ45 Terminals				
UTP5_INN	Input from UTP5 Cable	19	I	Negative differential side of input from the UTP5 cable to the TSB17BA1 termination network. Connect to network corresponding to RJ45 pin number 6 or RJ45 pin number 8.
UTP5_INP	Input from UTP5 Cable	20	I	Positive differential side of input from the UTP5 cable to the TSB17BA1 termination network. Connect to network corresponding to RJ45 pin number 3 or RJ45 pin number 7.
UTP5_OUTN	Output to UTP5 Cable	16	O	Negative differential side of output from TSB17BA1 to the UTP5 cable termination network. Connect to network corresponding to RJ45 pin number 2.
UTP5_OUTP	Output to UTP5 Cable	17	O	Positive differential side of output from TSB17BA1 to the UTP5 cable termination network. Connect to network corresponding to RJ45 pin number 1.
Power and Ground Terminals				
PD_SE	CMOS	10	I/O	Global power down. A high on this terminal turns off all internal circuitry.
R0	Bias	21	−	Current setting resistor. This terminal is connected to a precision external resistance to set the internal operating currents and the cable-driver output currents. This terminal has a very low impedance to ground.
R1	Bias	22	I	Current setting resistor (band-gap sense voltage). This terminal is connected to a precision external resistance to set the internal operating currents and the cable-driver output currents. A resistance of 6.04 kΩ, 1% between R0 and R1, is required to meet the 1394b output-voltage limits.
VCONTROL		23	I/O	Voltage control (reserved). Nominally not connected.
VREG_PD	CMOS	24	I	Power down for voltage regulator. When driven low, the device uses an internal regulator to generate the required 1.8 V. When driven high, the internal regulator is powered down and the 1.8 V must be supplied externally to power the 1.8-V circuitry of the device. Nominally tied low to enable the internal regulator.

Terminal Functions (Continued)

TERMINAL			I/O	DESCRIPTION
NAME	TYPE	NO.		
Power and Ground Terminals (Continued)				
VDDCORE	Supply	18	−	Core power. Internal core circuit power terminal. Must be decoupled with a 1-μF capacitor in parallel with other smaller capacitors, such as 0.001-μF capacitors.
VDD33	Supply	7	−	3.3-V power. I/O 3.3-V circuit power terminals. A combination of high-frequency decoupling capacitors near each terminal are suggested, such as paralleled 0.1 μF and 0.001 μF. Lower frequency 10-μF filtering capacitors are also recommended.
VSSCORE	Supply	15	−	Core ground. Tie to the ground plane of the PWB as close as possible to the terminal.
VSS33	Supply	4	−	3.3-V ground. Tie to the ground plane of the printed wiring board (PWB) as close as possible to the terminal.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DD} (see Note 1) . . . . . −0.3 V to 4 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to V_{DD} + 0.5 V
Output voltage range at any output, V_O . . . . . −0.5 V to V_{DD} + 0.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are with respect to network ground.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$‡	$T_A = 70°C$ POWER RATING
PW§	0.93 W	10.9 mW/°C	0.44 W

‡ This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$).

§ 2-oz trace and copper pad with solder.

recommended operating conditions

		MIN	TYP†	MAX	UNIT
Supply voltage, V_{DD33}		3	3.3	3.6	V
Supply voltage, V_{DDCORE}		1.65	1.8	1.95	V
High-level input voltage, V_{IH}	TEST[0:3], PD_SE, VREG_PD	$0.7\times V_{DD}$			V
Low-level input voltage, V_{IL}	TEST[0:3], PD_SE, VREG_PD			$0.3\times V_{DD}$	V
Maximum junction temperature, T_J (see $R_{\theta JA}$ values listed in thermal characteristics table)	$R_{\theta JA}$ = 91.47°C/W, T_A = 70°C, high-K board			86.5	°C
	$R_{\theta JA}$ = 150.70°C/W, T_A = 70°C, low-K board			97.1	
1394b Differential input voltage, V_{ID}	BETA_INP−BETA_INN	200		800	mV
1394b Common-mode input voltage, V_{IC}	BETA_IN cable inputs, nonsource power node	0.4706		2.015	V
Receive input jitter	BETA_INP, BETA_INN cable inputs, S100 operation			±1.08	ns
Receive input skew	Between BETA_OUT and BETA_IN cable inputs, S100 operation			±0.8	ns

† All typical values are at V_{DD} = 3.3 V and T_A = 25°C.

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted)

driver

PARAMETER		TEST CONDITIONS	TYP	UNIT
V_{OD}	Differential output voltage (BETA)		705	mV
V_{OD}	Differential output voltage (UTP5)		500	mV
I_{BETA}	Beta drive current, BETA_OUTP, BETA_OUTN	Drivers enabled	12.5	mA
I_{UTP5}	UTP5 drive current, UTP5_OUTP, UTP5_OUTN	Drivers enabled	10	mA

receiver

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{ID}	Differential impedance	Drivers disabled	4	7		kΩ
					4	pF
Z_{IC}	Common-mode impedance	Drivers disabled	20			kΩ
					24	pF

device

PARAMETER		TEST CONDITIONS	TYP	UNIT
$I_{DDSTATIC}$	3.3-V supply current†	No signals to driver inputs	4	mA
	V_{DDCORE} supply current†		4	
	3.3-V supply current‡		7.5	
I_{DDDYN}	3.3-V supply current†	Normal operation	6	mA
	V_{DDCORE} supply current†		30	
	3.3-V supply current‡		50	

† Measured with internal regulator off, 1.8-V supply current from external source
‡ Measured with internal regulator on

thermal characteristics

PARAMETER		TEST CONDITIONS	TYP	UNIT
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, no air flow, high conductivity TI-recommended test board, chip soldered or greased to thermal land with 2-oz copper (high-K board)	91.5	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance		41.2	°C/W
$R_{\theta JA}$	Junction-to-free-air thermal resistance	Board mounted, no air flow, high conductivity JEDEC test board with 1-oz copper (low-K board)	150.7	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance		41.2	°C/W

electrical characteristics over recommended ranges of operating conditions (unless otherwise noted) (continued)

switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Jitter, transmit	Between BETA_OUT and BETA_IN		2		ns
	Skew, transmit	Between BETA_OUT and BETA_IN			0.10	ns
		Between UTP5_OUT and UTP5_IN			0.20	
t_r	TP differential rise time, transmit	10% to 90%		0.65		ns
t_f	TP differential fall time, transmit	90% to 10%		0.65		ns
t_r	UTP differential rise time, transmit	10% to 90%, at RJ45 connector		3.5		ns
t_f	UTP differential fall time, transmit	90% to 10%, at RJ45 connector		3.5		ns

PARAMETER MEASUREMENT INFORMATION

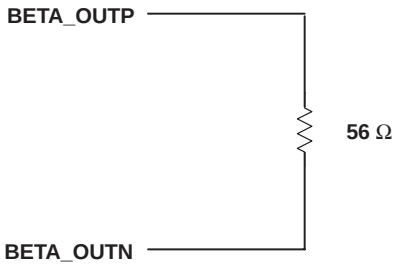


Figure 1. Test Load for Beta Connection

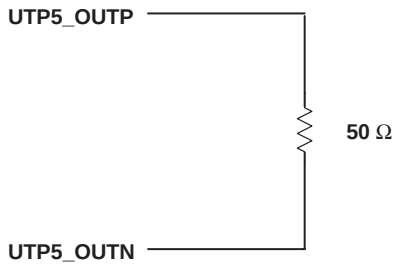


Figure 2. Test Load for UTP5 Connection

APPLICATION INFORMATION

Figure 3. 1394b Cable Termination

signal coding

The signaling generated from a 1394b PHY is 8B/10B encoded. This means to send 8 bits of data requires the transmission of 10 bits across the cable. The maximum frequency that is required to send 100 Mbits/s is a fundamental frequency of 62.5 MHz (see the IEEE Std 1394b-2002 for more explanation).

connector pins

The current IEEE Std 1394b-2002 requires that the connection from 1394b PHY signal to the RJ45 connector pin be:

- TPB+ to RJ45 pin 1
- TPB− to RJ45 pin 2
- TPA+ to RJ45 pin 7
- TPA− to RJ45 pin 8

There is a proposal to change the IEEE Std 1394b-2002 connection from 1394b PHY signal to the RJ45 connector pin to be the same as the 100baseT Ethernet. This allows use of more 100baseT Ethernet components for 1394b connections. This changes the connections to:

- TPB+ to RJ45 pin 1
- TPB− to RJ45 pin 2
- TPA+ to RJ45 pin 3
- TPA− to RJ45 pin 6

It is anticipated that the change will be implemented into IEEE Std 1394b-2002, though it has not been ratified. Therefore, it is recommended that all implementations utilize the new pinout running TPA+ to pin 3 and TPA− to pin 6. If a closed system is created, meaning the designer controls the electronics at both ends of the UTP5 cable, then using pins 7 and 8 can give as much as a 12-dB reduction in crosstalk rather than using pins 3 and 6. Please contact Texas Instruments for further details.

cable connection

The IEEE Std 1394b-2002 requires the output of a TPB port to be connected to the input of a TPA port when connecting one device to a second device. In other words, it requires a crossover somewhere between the two PHY ports. The 1394b standard further states that a UTP5 device incorporates logic that can automatically implement this crossover in the logic. The TSB17BA1 does not contain this logic, therefore, the crossover must be implemented external to the TSB17BA1.

It is recommended for users of the TSB17BA1 to:

- Design the UTP5 connection to pins 1, 2 and 3, 6 as previously detailed.
- Ship an Ethernet crossover cable with their devices.

The crossover cable connects:

- Pin 1 on the near end of the cable to pin 3 on the far end of the cable
- Pin 2 on the near end of the cable to pin 6 on the far end of the cable
- Pin 3 on the near end of the cable to pin 1 on the far end of the cable
- Pin 6 on the near end of the cable to pin 2 on the far end of the cable, thereby implementing the crossover.

APPLICATION INFORMATION

cable connection (continued)

This also works for CAT5-structured wiring cable that is typically installed in a home or office. The CAT5 cables in these structured wiring installations are wired straight through and do not crossover. It is recommended that the structured wiring hub at the center of the star-type installation contain only straight-through wiring. If the RJ45 connector is brought outside the wall, then it also is connected straight through. If all networkable devices are also created as straight-through connections, then the required crossover is implemented when the networkable device is connected to the RJ45 wall-plate connection using a crossover cable.

There is a special case for the structured wiring if the wall plate enables a 4-pin, 6-pin, or 9-pin 1394b connector. In this case, one port of the 1394b PHY is connected to the 1394b connector in the typical manner. However, the connection between the 1394b PHY and the UTP5 connection inside the wall must implement a crossover. This is true if the 1394b-structured wiring hub is wired straight through and the cable pulled is straight through. In this case, since all the electrical connections between the two 1394b ports are straight through, the crossover must be implemented on the wall-plate UTP5 connection. It is required that this crossover be completed between the RJ45 connector on the wall plate and the isolating transformer of the termination network.

Please contact Texas Instruments for further detail.

PCB layout considerations

There are certain signals that require special care in the layout of the TSB17BA1. The UTP5_INP and UTP5_INN signals are the inputs from what might be a 100-m cable. After propagating through a cable this long the signal amplitudes could be small and more easily affected by board noise. The routing for these signals from the RJ45 connector through the termination network to the PHY must be short and, if possible, a ground guard etch must be implemented to protect them from board noise. This etch must extend the length of the traces, be far enough away from the signal traces not to significantly affect the trace impedance, and be connected to the ground plane every 2 cm or less.

The precision resistor between the R1 and R0 terminals sets the internal currents and voltages of the TSB17BA1. Any noise that couples onto the R1 terminal can affect the entire device. Therefore, this connection must be kept short and as close to the TSB17BA1 as possible. This connection can also benefit from a ground guard etch around the R1 and R0 terminal connections.

To keep the noise introduced to these signals to a minimum it is recommended that no digital signals or large amplitude analog signals (like switching regulators) be routed in the vicinity of terminals 19−22 on the TSB17BA1. The output signals of the TSB17BA1 (UTP5_OUTP, UTP5_OUTN, BETA_OUTP, and BETA_OUTN) must also be routed away from these sensitive input pins.

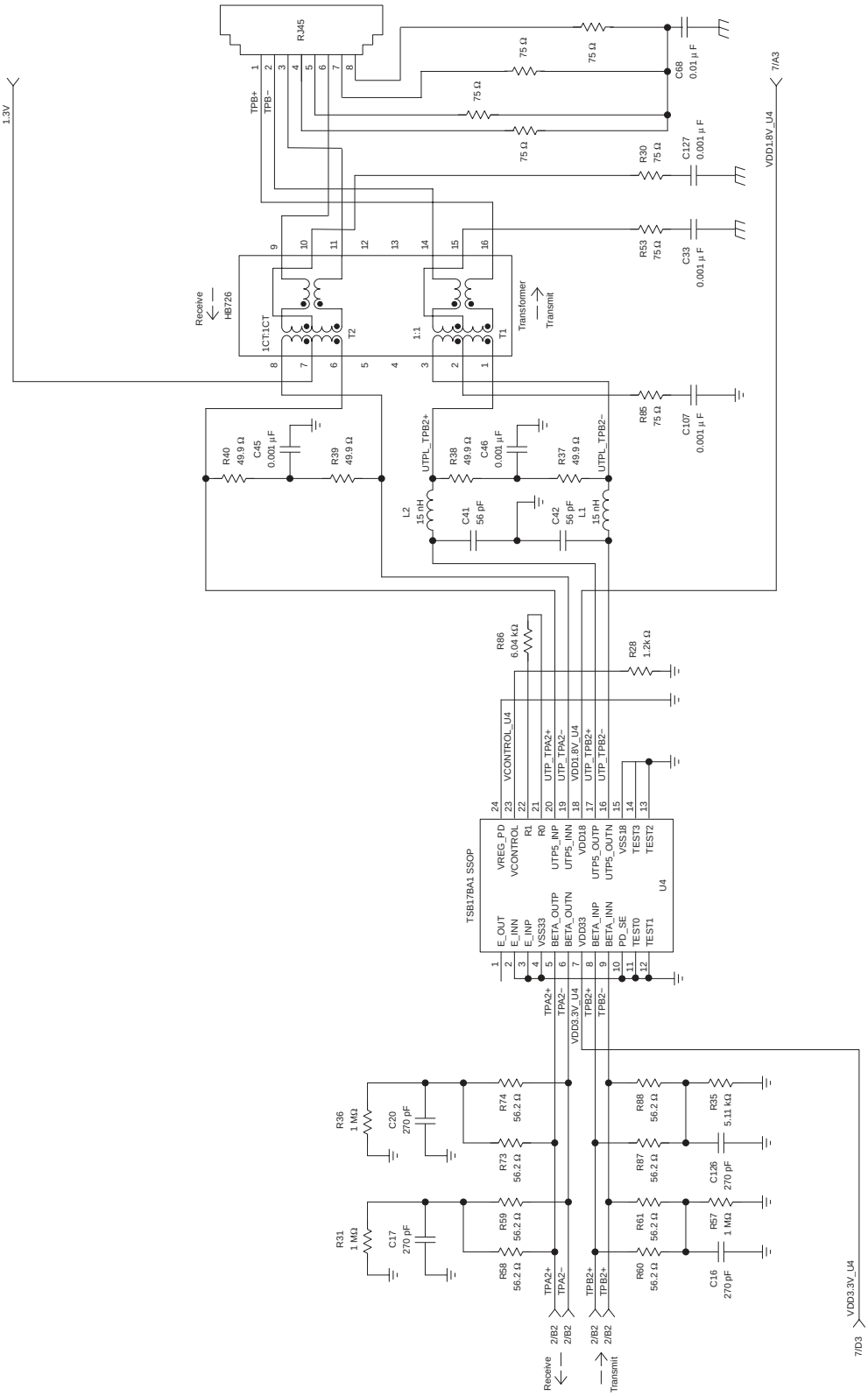


Figure 4. Example Schematic Implementation

APPENDIX A. ERRATA

UTP signal level detection issue

problem description

In some application environments, the TSB17BA1 may respond to input noise that exceeds the internal noise rejection threshold. Excessive cable length and poor quality components can contribute to the problem. Due to process variations during manufacture, the sensitivity and threshold levels may vary from device to device. One or more of the following issues may occur:

1. Some devices may be sensitive to PCB supply and input signal noise, driving the BETA_OUT pins continuously. In turn, this may cause the 1394b PHY port connected to the TSB17BA1 to enter a blocked state, preventing connection when a node is attached to the UTP port.
2. Some devices may be sensitive to PCB and cable crosstalk from the transmit data path. This crosstalk may couple into the receive data path during the toning and training process and the 1394b PHY may then attempt to negotiate with the false crosstalk signal. The 1394b PHY port may enter a blocked state prior to UTP cable attachment at one or both cable ends.
3. System or cable noise within the signal bandwidth may translate into a differential signal input to the TSB17BA1 and falsely generate BETA_OUT signaling. As a result, the 1394b PHY port attached to the TSB17BA1 may enter a blocked state before connection.

workarounds

The best problem mitigation is to avoid the circumstances that contribute to noise. The phenomenon is highly dependent on the system and the network environment, so good quality cable, good installation, and good design practice are critical. Excessively long cable runs must be avoided. Proper connector termination, high quality components (e.g., low crosstalk transformer), and good PCB layout are important. Please refer to *PCB Layout Considerations* of this data sheet for more information.

The required workaround is to provide an approximately 51-mV dc offset externally to the UTP input of the TSB17BA1 device. This may be accomplished by connecting a 1.21-kΩ, 1% resistor from the UTP5_INN terminal to signal ground, isolating the transformer from the TSB17BA1 with 0.1-µF capacitors and providing a 1.3-V common mode voltage. This circuit is shown in Figure 5.

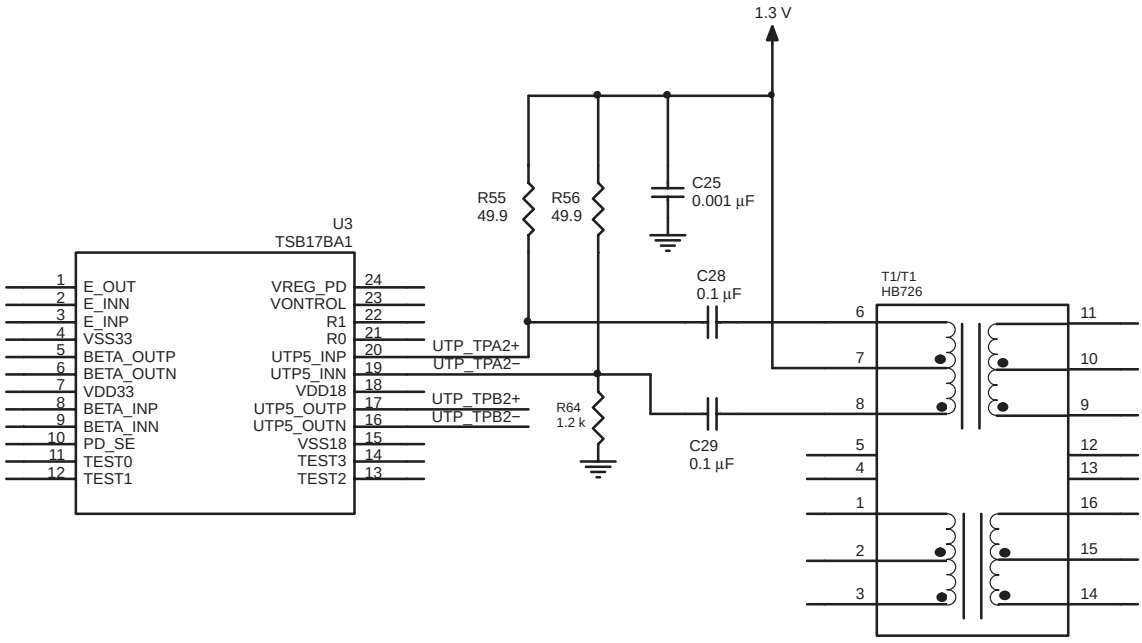


Figure 5. Workaround Circuit

This circuit, when used with parts received from Texas Instruments after 2003, should allow the device to reject in-band noise and crosstalk of at least 20 mVp-p. Alternate connection of the transformer center tap (pin 7) may provide noise immunity advantages.

The dc offset provided by the workaround circuit reduces the sensitivity of the device to both desired and undesired signals. This offset method proved successful with a sampling of TSB17BA1 devices (under nominal conditions) connected by 100m of CAT 5e cable in three segments with jack-to-jack adapter boards.

In some cases it may be possible to cycle system power to all nodes simultaneously after all UTP cables are connected (that is, terminated) and have ports connect normally. In this configuration the noise levels from issues 2 and 3 may be reduced by the cable termination. This noise reduction combined with the presence of a real signal may have enough signal-to-noise difference to allow the system to connect and operate. This solution may not work for issues 1 and 3 with large amplitude noise environments.

UTP output level issue

problem description

The TSB17BA1 UTP5_OUT output drive level is designed and tested to the same limits that the IEEE Std 1394b-2002 specification table 12−2 provides for the transmit system. Losses in the transformer, PCB, connector, etc., of a product using the TSB17BA1 may result in degraded UTP transmit levels. These reduced output levels may not meet the 1394b specification but may still operate satisfactorily.

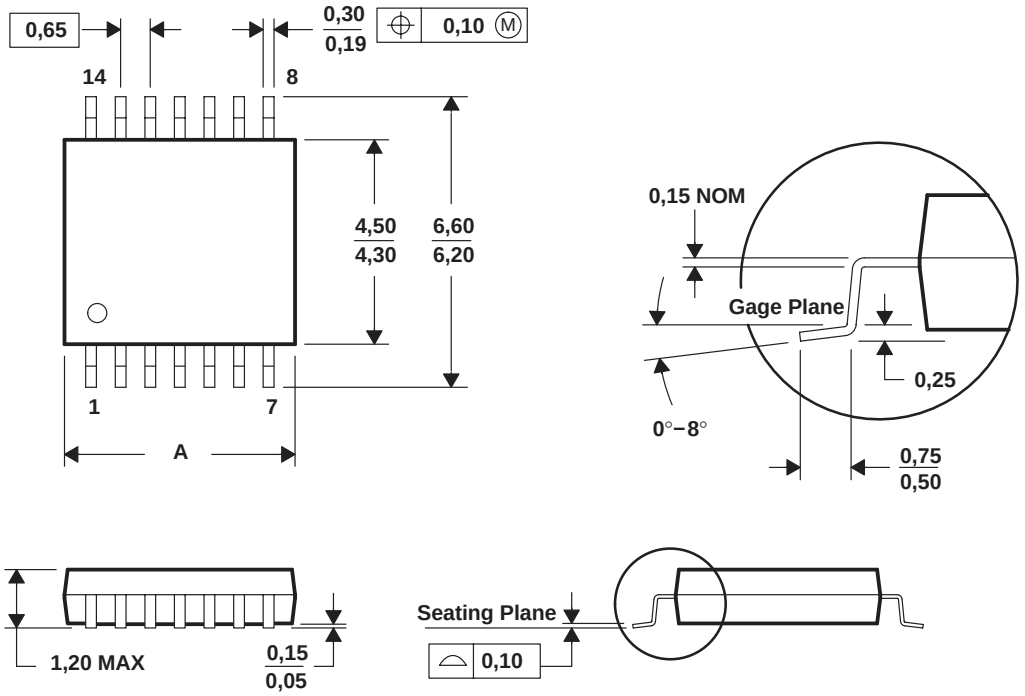
workaround

None

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265