

RF Power Field Effect Transistor

N-Channel Enhancement-Mode Lateral MOSFET

Designed for CDMA base station applications with frequencies from 920 to 960 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

- Typical Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 1400$ mA, $P_{out} = 58$ Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
920 MHz	19.9	37.7	6.1	-36.2
940 MHz	19.9	37.1	6.1	-36.6
960 MHz	19.5	36.8	6.0	-36.0

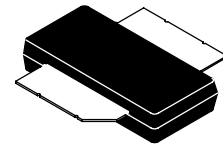
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 940 MHz, 300 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Typical P_{out} @ 1 dB Compression Point ≈ 200 Watts CW

Features

- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- 225°C Capable Plastic Package
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 inch Reel.

MRF8S9200NR3

**920-960 MHz, 58 W AVG., 28 V
 SINGLE W-CDMA
 LATERAL N-CHANNEL
 RF POWER MOSFET**



**CASE 2021-03, STYLE 1
 OM-780-2
 PLASTIC**

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +70	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 58 W CW, 28 Vdc, $I_{DQ} = 1400$ mA Case Temperature 80°C, 200 W CW, 28 Vdc, $I_{DQ} = 1400$ mA	$R_{\theta JC}$	0.30 0.25	°C/W

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 70\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 400\ \mu\text{Adc}$)	$V_{GS(th)}$	1.5	2.3	3	Vdc
Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_D = 1400\ \text{mAdc}$, Measured in Functional Test)	$V_{GS(Q)}$	2.3	3	3.8	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3.3\ \text{Adc}$)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

Functional Tests ⁽¹⁾ (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1400\ \text{mA}$, $P_{out} = 58\ \text{W Avg.}$, $f = 940\ \text{MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\ \text{MHz}$ Offset.

Power Gain	G_{ps}	18	19.9	21	dB
Drain Efficiency	η_D	34	37.1	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.8	6.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-36.6	-35	dBc
Input Return Loss	IRL	—	-22	-9	dB

Typical Broadband Performance (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1400\ \text{mA}$, $P_{out} = 58\ \text{W Avg.}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\ \text{MHz}$ Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
920 MHz	19.9	37.7	6.1	-36.2	-14
940 MHz	19.9	37.1	6.1	-36.6	-22
960 MHz	19.5	36.8	6.0	-36.0	-15

1. Part internally matched both on input and output.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 1400\text{ mA}$, 920–960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P_{1dB}	—	200	—	W
IMD Symmetry @ 160 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands $> 2\text{ dB}$)	IMD_{sym}	—	15	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	45	—	MHz
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 58\text{ W Avg.}$	G_F	—	0.7	—	dB
Gain Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔG	—	0.012	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30°C to $+85^\circ\text{C}$)	ΔP_{1dB}	—	0.001	—	dBm/ $^\circ\text{C}$

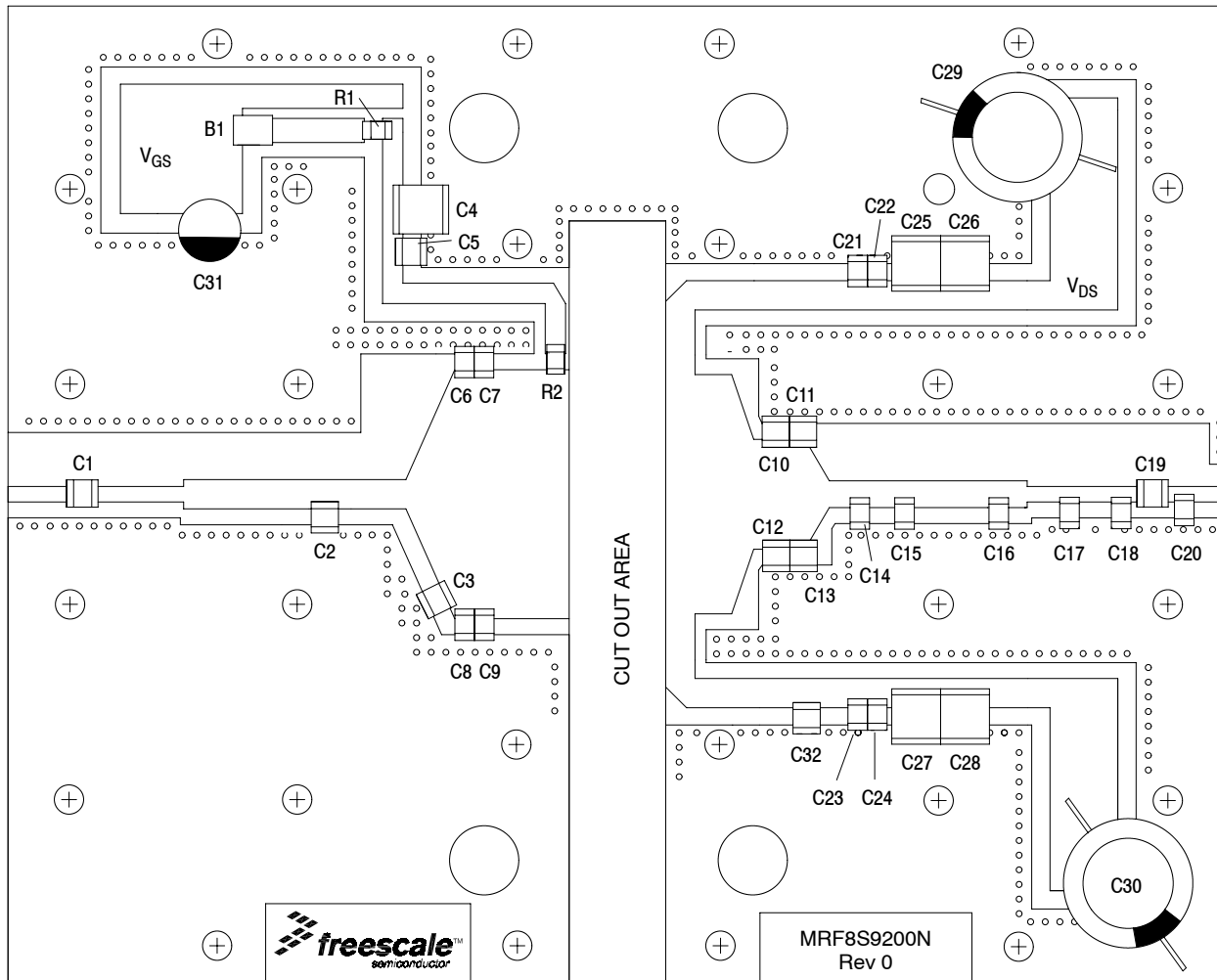


Figure 1. MRF8S9200NR3 Test Circuit Component Layout

Table 6. MRF8S9200NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Ferrite Beads, Short	2743019447	Fair-Rite
C1, C5, C19, C21, C22, C23, C24	39 pF Chip Capacitors	ATC100B390JT500XT	ATC
C2	2 pF Chip Capacitor	ATC100B2R0BT500XT	ATC
C3	6.2 pF Chip Capacitor	ATC100B6R2BT500XT	ATC
C4	2.2 μ F Chip Capacitor	C1825C225J5RAC-TU	Kemet
C6, C7, C8, C9	3.3 pF Chip Capacitors	ATC100B3R3CT500XT	ATC
C10, C12	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C11, C13	5.1 pF Chip Capacitors	ATC100B5R1CT500XT	ATC
C14, C20	0.8 pF Chip Capacitors	ATC100B0R8BT500XT	ATC
C15, C17	0.5 pF Chip Capacitors	ATC100B0R5BT500XT	ATC
C16	1.5 pF Chip Capacitor	ATC100B1R5BT500XT	ATC
C18	1.2 pF Chip Capacitor	ATC100B1R2BT500XT	ATC
C25, C26, C27, C28	10 μ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C29, C30	470 μ F, Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C31	47 μ F, 50 V Electrolytic Capacitor	476KXM050M	Illinois Cap.
C32	10 pF Chip Capacitor	ATC100B100JT500XT	ATC
R1	3.3 Ω , 1/2 W Chip Resistor	P3.3VCT-ND	Panasonic
R2	0 Ω , 3.5 A Chip Resistor	CRCW12060000Z0EA	Vishay
PCB	0.030", $\epsilon_r = 3.5$	RF-35	Taconic

TYPICAL CHARACTERISTICS

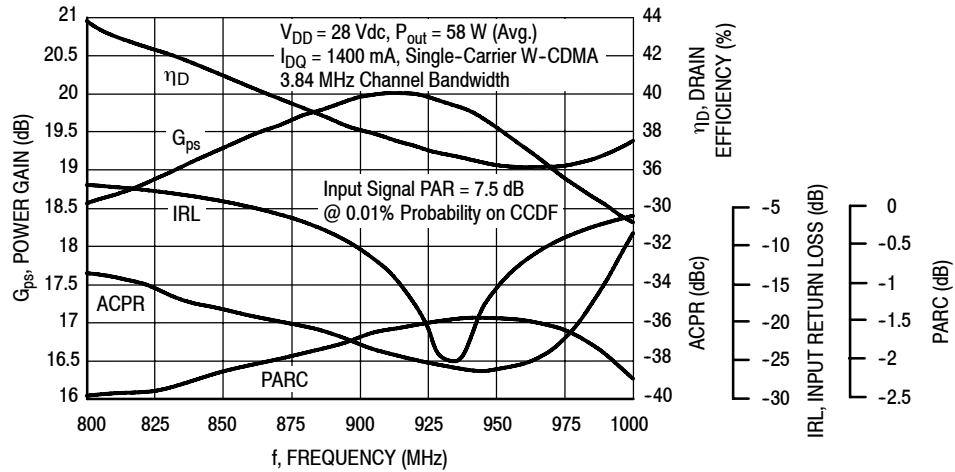


Figure 2. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 58$ Watts Avg.

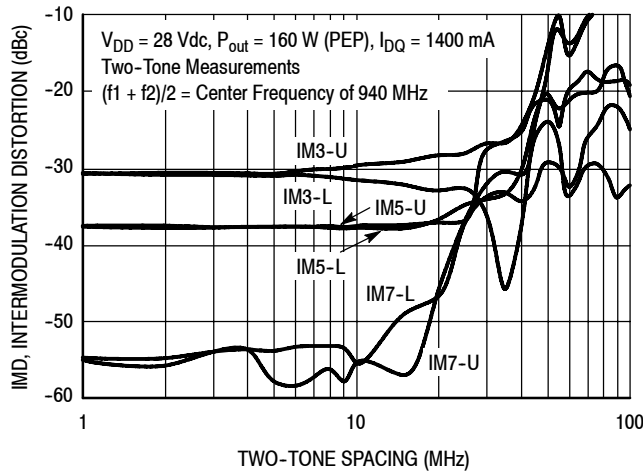


Figure 3. Intermodulation Distortion Products versus Two-Tone Spacing

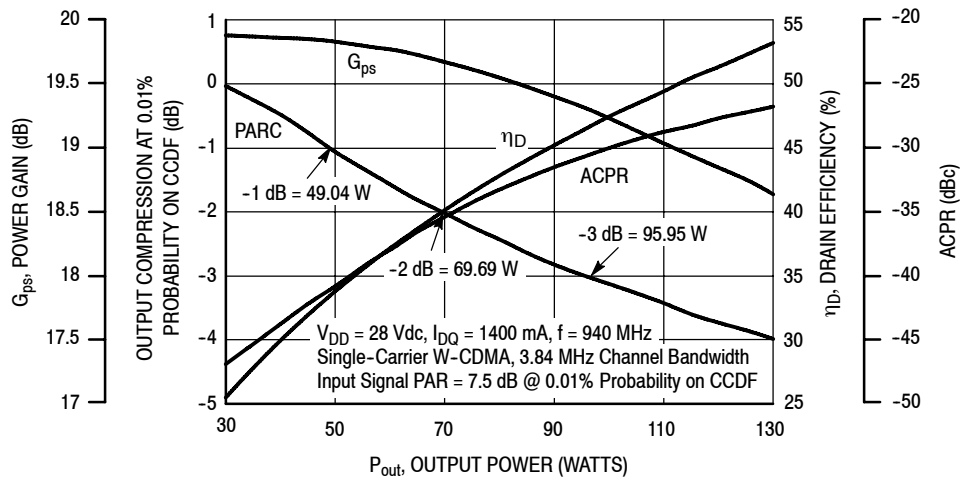


Figure 4. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

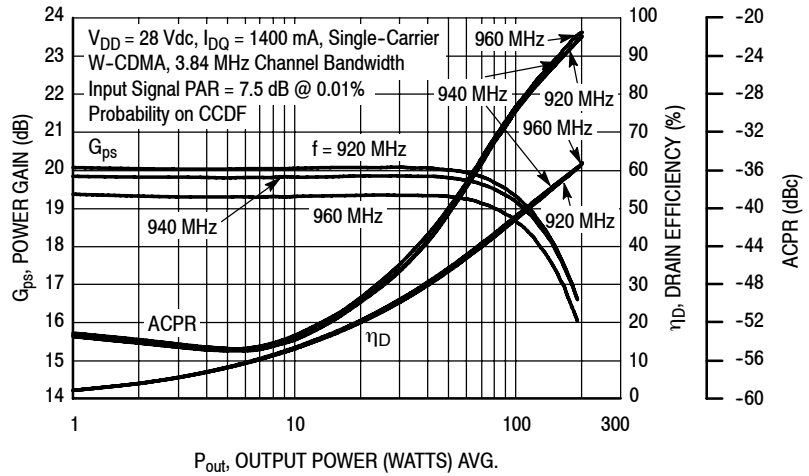


Figure 5. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

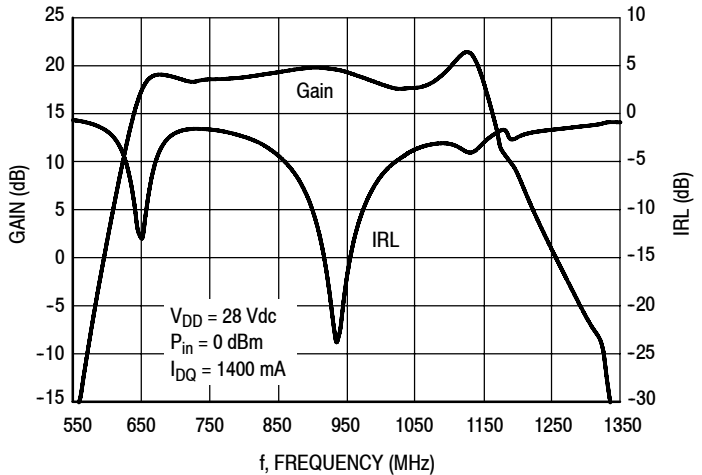


Figure 6. Broadband Frequency Response

W-CDMA TEST SIGNAL

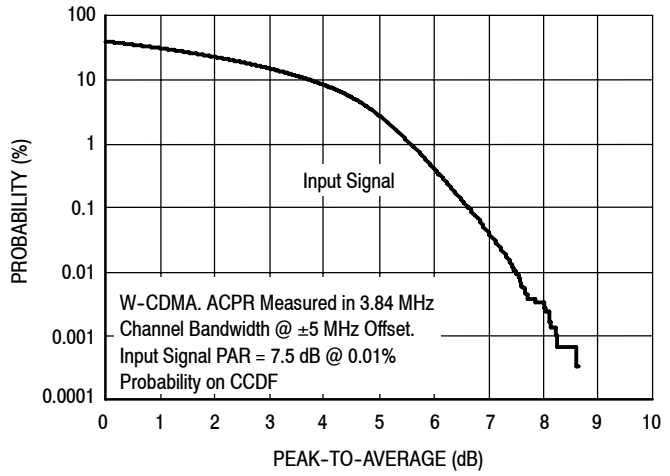


Figure 7. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

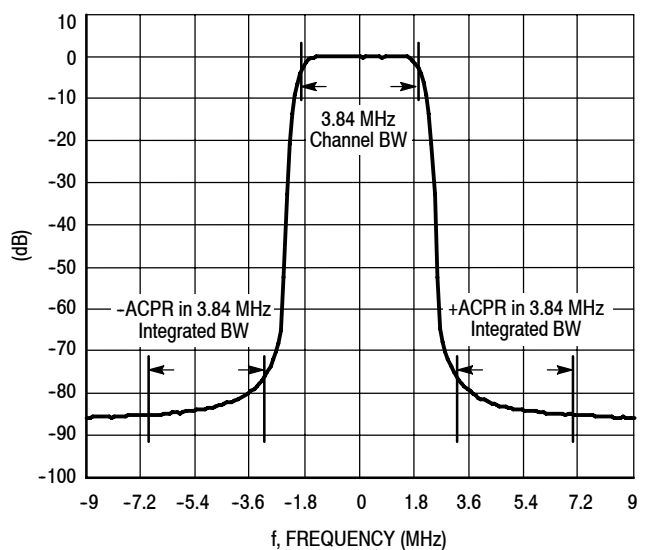


Figure 8. Single-Carrier W-CDMA Spectrum

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 1400 \text{ mA}$, $P_{out} = 58 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
820	1.16 - j2.85	2.29 - j2.08
840	1.09 - j2.63	2.11 - j1.95
860	1.04 - j2.45	1.94 - j1.81
880	0.98 - j2.27	1.76 - j1.68
900	0.93 - j2.08	1.59 - j1.51
920	0.88 - j1.90	1.42 - j1.33
940	0.83 - j1.72	1.28 - j1.13
960	0.79 - j1.55	1.14 - j0.93
980	0.76 - j1.39	1.02 - j0.73

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

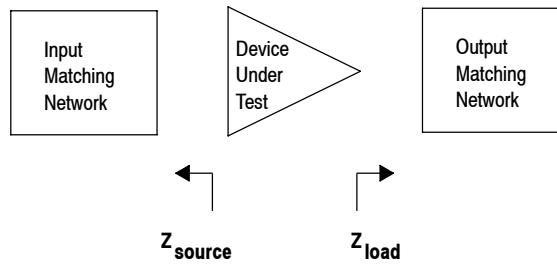
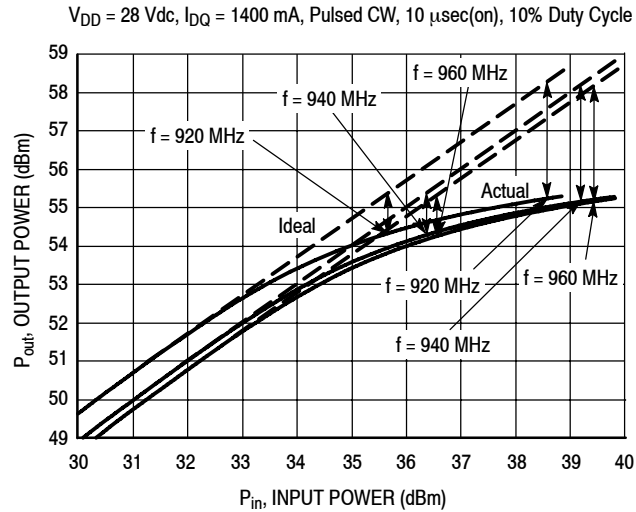


Figure 9. Series Equivalent Source and Load Impedance

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

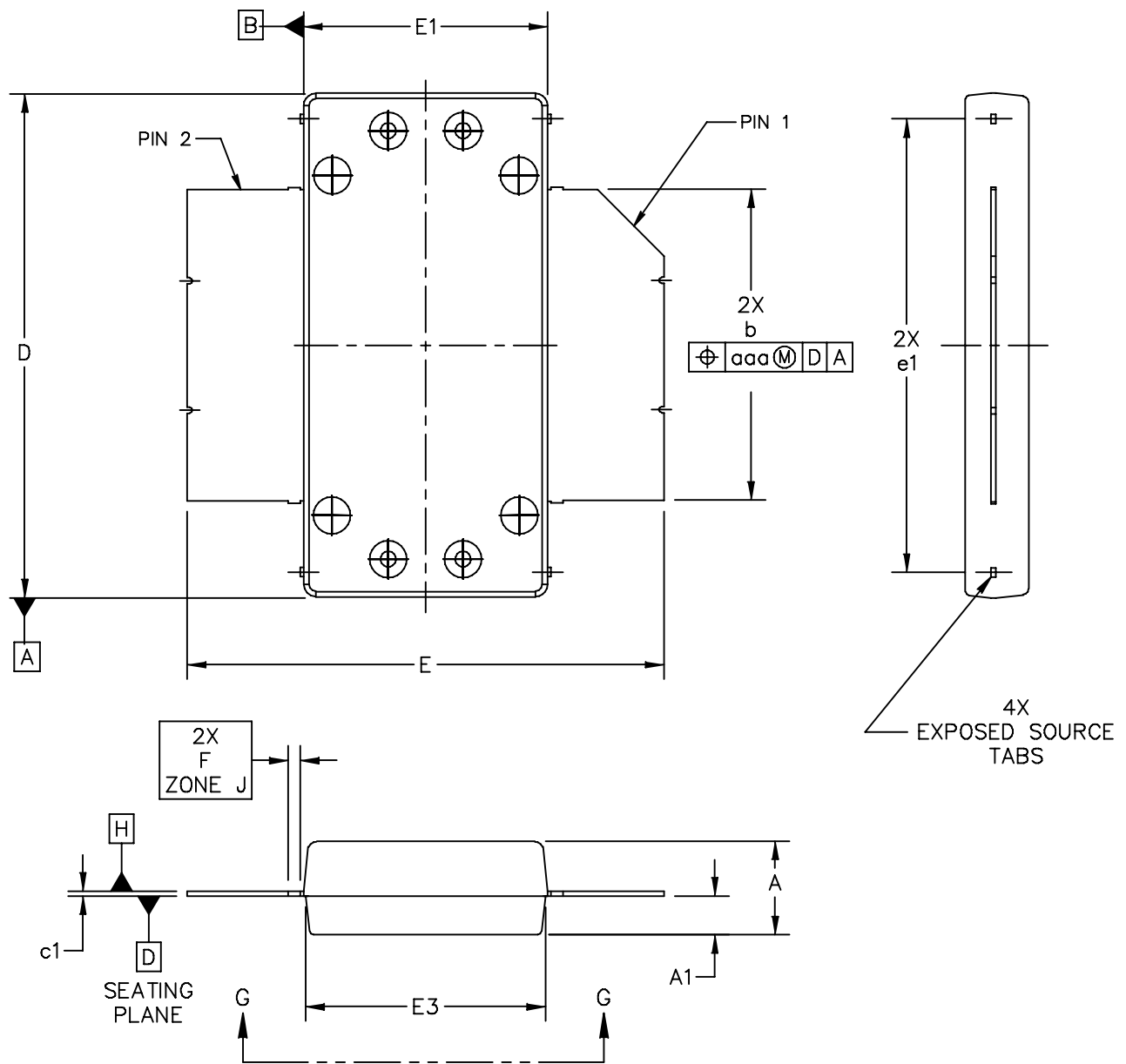
f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
920	267	54.3	332	55.2
940	263	54.2	327	55.1
960	261	54.2	327	55.2

Test Impedances per Compression Level

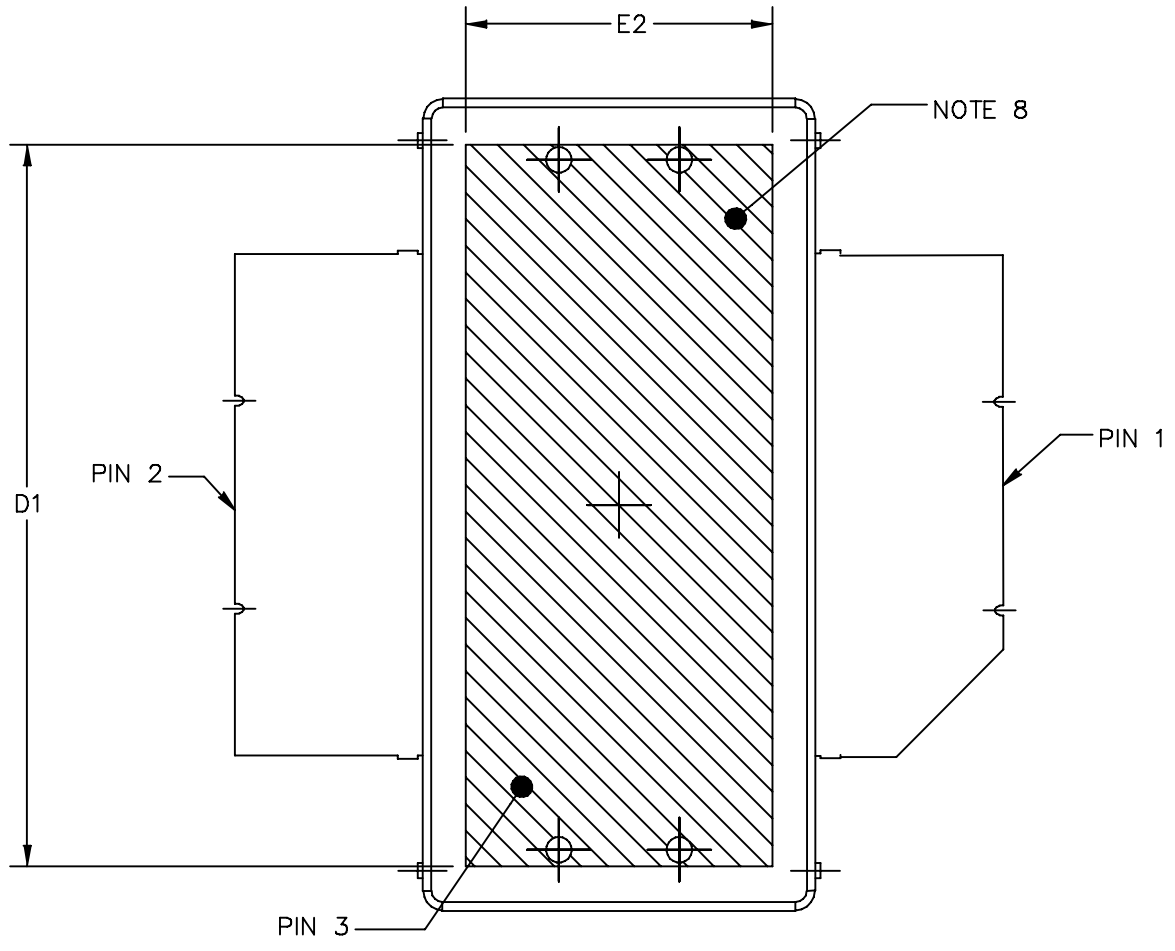
f (MHz)		Z_{source} Ω	Z_{load} Ω
920	P1dB	0.70 - j1.66	0.82 - j1.52
940	P1dB	0.68 - j1.85	0.73 - j1.60
960	P1dB	0.87 - j1.99	0.76 - j1.70

Figure 10. Pulsed CW Output Power versus Input Power @ 28 V

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: OM780-2 STRAIGHT LEAD		DOCUMENT NO: 98ASA10831D		REV: B	
		CASE NUMBER: 2021-03		22 OCT 2009	
		STANDARD: NON-JEDEC			



BOTTOM VIEW
VIEW G-G

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: OM780-2 STRAIGHT LEAD	DOCUMENT NO: 98ASA10831D	REV: B	
	CASE NUMBER: 2021-03	22 OCT 2009	
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:
 PIN 1 - DRAIN
 PIN 2 - GATE
 PIN 3 - SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	0.148	.152	3.76	3.86	b	.497	.503	12.62	12.78
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e1	.721	.729	18.31	18.52
D1	.720	----	18.29	----					
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83					
F	.025 BSC		0.635 BSC						

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: OM780-2 STRAIGHT LEAD		DOCUMENT NO: 98ASA10831D	REV: B
		CASE NUMBER: 2021-03	22 OCT 2009
		STANDARD: NON-JEDEC	

PRODUCT DOCUMENTATION, TOOLS AND SOFTWARE

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Aug. 2009	<ul style="list-style-type: none"> • Initial Release of Data Sheet
1	May 2010	<ul style="list-style-type: none"> • Revised VSWR statement to correct output power from 200 Watts CW to 300 Watts CW, p. 1 • Replaced Case Outline 2021-01, Issue O, with 2021-03, Issue B, p. 1, 9-11. Changed “Drain Lead” to “Pin 1” and “Gate Lead” to “Pin 2” on Sheet 1. Corrected “A2” to “A1” in Note 7, and changed dimension A1 from 0.061”–0.063” (1.55–1.60 mm) to 0.059”–0.065” (1.50–1.65 mm) on Sheet 3. Added 4 exposed source tabs at dimension e1 on Sheets 1 and 2. Added dimension e1 0.721”–0.729” (18.31–18.52 mm) in the table, revised D1 minimum dimension from 0.730” (18.54 mm) to 0.720” (18.29 mm), revised dimension E2 from 0.312” (7.92 mm) to 0.306” (7.77 mm), and revised wording of Note 8 on Sheet 3. • Changed Human Body Model ESD rating from Class 1C to Class 2 to reflect recent ESD test results of the device, p. 2

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2009-2010. All rights reserved.